gmB135 Data Sheet

(Bridge 135)

DAT0019C

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Genesis Microchip Inc.

165 Commerce Valley Dr. West, Thornhill, ON Canada L3T 7V8 Tel: (905) 889-5400 Fax: (905) 889-0035

1871 Landings Drive, Mountain View, CA, USA 94043 Tel: (650) 428-4277 Fax (650) 428-4288

www.genesis-microchip.com / info@genesis-microchip.on.ca

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- January, 1999 (First publication)
- March, 1999 (Update information)
- June, 1999 (New Format, Pin Diagram Orientation, Pin Assignment Corrections)
- July, 1999 (Added Related Documents)
- October, 1999 (Updated pin diagram on page 7 to match the pin descriptions)

Related Documents

- DSR-0019 (gmB135 Register Specification)
- SED-0694 (gmB135 Evaluation Board)
- MSD-0061 (gmB135 Stepping Infomation)

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1. General Description

1.1 Summary

Based on the B120 architecture, the gmB135 continues to simplify TFT LCD monitor design while providing "CRT-like" ease of use and uncompromising image quality. The gmB135's revolutionary scaling engine, capable of expanding any source resolution to a highly uniform and sharp image, combined with the critically proven integrated 8 bit triple-ADC and patented Rapid-Lock digital clock recovery system, create a uniquely cost effective solution. This rich feature set yields an extremely suitable match between the gmB135 and high end XGA and SXGA applications as illustrated in the figure on the next page.

1.2 Features

Integrated 135 Mhz Triple ADC

- No additional components are needed for the three differential input ADCs which are capable of converting analog RGB data rates up to 135 Mhz.
- Flexible resolution support without frame buffer, from low resolution VGA and NEC98 modes up to 1280 x 1024 at 75 Hz. All color depths up to 24 bits per pixel are supported.

Best of Class Scaling Engine

- The gmB135 scaling engine algorithm is optimized to match TFT LCDs optical display response to provide uniform intensity across the entire image.
- Text font clarity and sharpness is enhanced by gmB135's $(\sin\theta)/\theta$ re-scaling convolver.

Multiple Video Format Input Support

gmB135 interfaces to various video transmission formats to provide universal connectivity.

Serial Digital Receivers

- Serial digital receivers such as TMDS, LVDS or GVIF configured in either 1 pixel per clock or 2 pixels per clock connect directly to gmB135 to create a DFP, Plug and Display or DISM compatible monitor

Two Analog Connector Inputs

- Two separate sets of analog RGB inputs are internally multiplexed in gmB135. This allows the monitor to select RGB analog signals from two PCs.

Digital TV

- CCIR601 input from a digital TV decoder. Using the gmB135 internal YUV-to-RGB conversion circuit and expansion circuit, the de-interlaced image is displayed on a progressive-scan TFT LCD.

Integrated High Speed Digital Clock Recovery

- Solid and completely stable locking to the source pixel clock is achieved in worst case test patterns.
- All clocks required for the gmB135 are generated from a single 50 Mhz reference oscillator.

Integrated RAM based OSD Controller

Customer defined fonts as well as standard fonts are supported in a fully featured integrated OSD controller. Complete "look and feel" and a familiar user interface can be maintained.

Automatic ADC Sampling Phase Optimization

Performs measurements so that firmware can automatically optimize the ADC sampling phase.

Optimized Panel Clock

- Panel clock frequency is optimized to support each mode at the lowest possible frequency. 1280 x 1024 x 75Hz is supported without driving the panel clock at 135 Mhz.
- Panel clock pad drive strength and clock to data skew are programmable to reduce EMI in the panel interface cable.

TFT LCD Panel Support

- All panel resolutions and sizes are supported up to SXGA
- Panel interface supports one or two pixel per clock, Sync only, DE only and Sync/DE composite.

Four Wire Interface to Microcontroller

Simple 4 wire serial interface connects directly to monitor microcontroller. Can be expanded to 7 wires by increasing data width from 1 to 4.

Standard 292 Pin BGA Package

256 signal/power/ground pins plus 36 (6 x 6) middle ground pins.

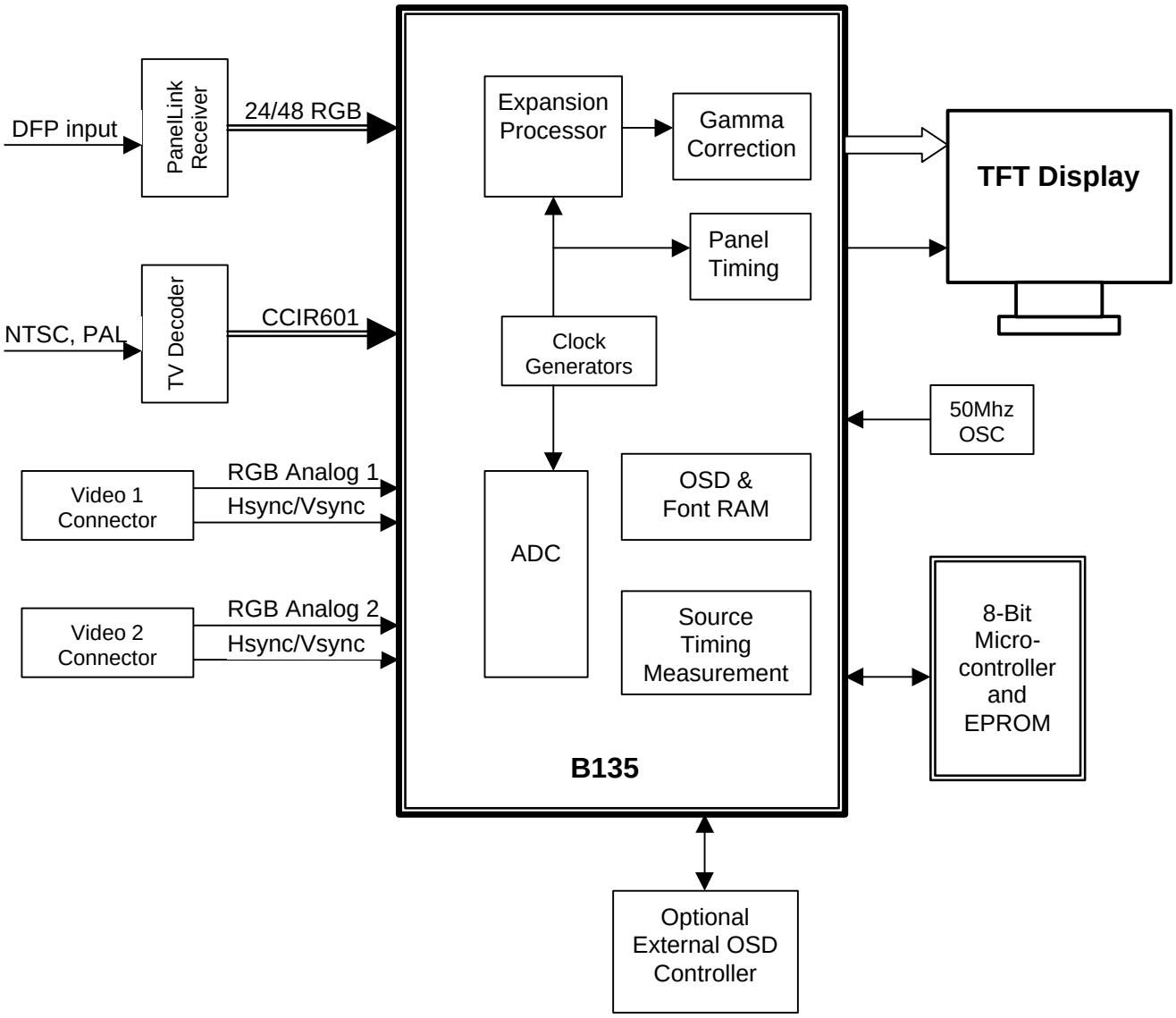
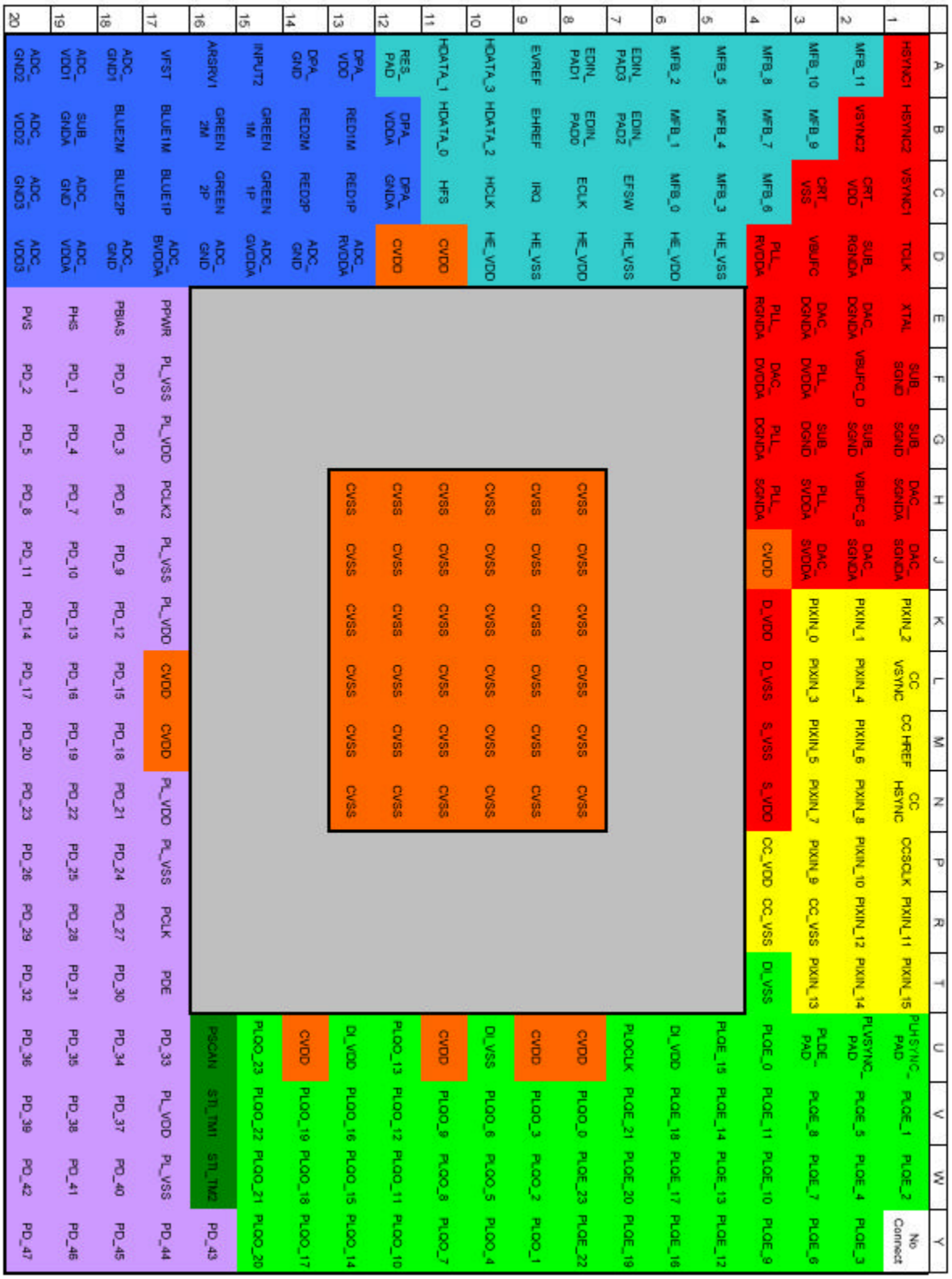


Figure 1.1.1 Single-Chip Solution for a Feature-Rich, Low-Cost Flat Panel Monitor

1.3 Pin Diagram

Bottom View of 292-pin BGA (including 6x6 middle pins).



1.4 Pin Description

Unless otherwise mentioned in the pin-description, tie unused input pins to ground and leave unused output pins open.For information about power distribution and ground plane isolation on a print circuit board, refer to gmB135-AN1: gmB135 Evaluation Board Application Note (to be published).

Table 1.4.1. Analog-to-Digital Converter

Pin No.	Name	In / Out	5-V Tolerant Input?	Description
A19	ADC_VDD1			Digital power for ADC clocking circuit. Must be bypassed with 0.1 uF capacitor to ACD_GND1.
A18	ADC_GND1			Digital GND for ADC clocking circuit. Must be directly connected to the digital system ground plane.
B20	ADC_VDD2			Digital power for ADC encoding logic. Must be bypassed with 0.1 uF capacitor to ADC_GND2.
A20	ADC_GND2			Digital GND for ADC encoding logic. Must be directly connected to the digital system ground plane.
D20	ADC_VDD3			Digital power for ADC encoding logic. Must be bypassed with 0.1 uF capacitor to ADC_GND3.
C20	ADC_GND3			Digital GND for ADC encoding logic. Must be directly connected to the digital system ground plane.
B19	SUB_GNDA			Dedicated pin for substrate guard ring that protects the ADC reference system. Must be directly connected to the analog system ground plane.
D19	ADC_VDDA			Analog power for ADC analog blocks that are shared by all three channels. Includes bandgap reference, master biasing and full scale adjust. Must be bypassed with 0.1 uF capacitor to ADC_GND (C19).
D17	ADC_BVDDA			Analog power for the blue channel. Must be bypassed with 0.1 uF capacitor to ADC_GND (D18).
D15	ADC_GVDDA			Analog power for the green channel. Must be bypassed with 0.1 uF capacitor to ADC_GND (D16).
D13	ADC_RVDDA			Analog power for the red channel. Must be bypassed with 0.1 uF capacitor to ADC_GND (D14).
D14, D16, D18, C19	ADC_GND			Analog ground for ADC. Must be directly connected to the analog system ground plane.
A15	INPUT2	In	Yes (5V-tolerant)	Reserved. For internal testing purposes.
C13	RED1P	In	No (up to 3.3V)	Positive analog input for Red channel 1. Enabled when analog port 1 is selected.
B13	RED1M	In	No (up to 3.3V)	Negative analog input for Red channel 1. Enabled when analog port 1 is selected.
C15	GREEN1P	In	No (up to 3.3V)	Positive analog input for Green channel 1. Enabled when analog port 1 is selected.
B15	GREEN1M	In	No (up to 3.3V)	Negative analog input for Green channel 1. Enabled when analog port 1 is selected.
C17	BLUE1P	In	No (up to 3.3V)	Positive analog input for Blue channel 1. Enabled when analog port 1 is selected.
B17	BLUE1M	In	No (up to 3.3V)	Negative analog input for Blue channel 1. Enabled when analog port 1 is selected.
C14	RED2P	In	No (up to 3.3V)	Positive analog input for Red channel 2. Enabled when analog port 2 is selected.
B14	RED2M	In	No (up to 3.3V)	Negative analog input for Red channel 2. Enabled when analog port 2 is selected.
C16	GREEN2P	In	No (up to 3.3V)	Positive analog input for Green channel 2. Enabled when analog port 2 is selected.
B16	GREEN2M	In	No (up to 3.3V)	Negative analog input for Green channel 2. Enabled when analog port 2 is selected.
C18	BLUE2P	In	No (up to 3.3V)	Positive analog input for Blue channel 2. Enabled when analog port 2 is selected.
B18	BLUE2M	In	No (up to 3.3V)	Negative analog input for Blue channel 2. Enabled when analog port 2 is selected.
B12	DPA_VDDA			Internal test pin.

Table 1.4.1. Analog-to-Digital Converter

Pin No.	Name	In / Out	5-V Tolerant Input?	Description
C12	DPA_GNDA			Internal test pin.
A13	DPA_VDD			Internal test pin.
A14	DPA_GND			Internal test pin.
A16	ARSRV1			Internal test pin.
A17	VFST			Internal test pin.

Table 1.4.2. Host Interface (HIF), External On-Screen Display (EOSD), and Multi-Function Bus (MFB).

Pin	Name	In / Out	5-V Tolerant Input /Output Drive Current @10pF	Description
A12	RES_PAD	In	5-V tolerant	Resets the gmB135 chip when low for at least 100 ns. Active low.
C9	IRQ	Out	4 mA	Interrupt request output
C10	HCLK	In	5-V tolerant	Host interface clock signal input.
C11	HFS	In	5-V tolerant	Active-high Host Frame Sync. Marks the beginning of the host interface data packet. This pin has an internal pull-down resistor.
A10	HDATA_3	In/Out	5-V tolerant / 8mA	Bit 3 of 4-bit host interface data HDATA[3:0].
B10	HDATA_2	In/Out	5-V tolerant / 8mA	Bit 2 of 4-bit host interface data HDATA[3:0].
A11	HDATA_1	In/Out	5-V tolerant / 8mA	Bit 1 of 4-bit host interface data HDATA[3:0].
B11	HDATA_0	In/Out	5-V tolerant / 8mA	Bit 0 of 4-bit host interface data HDATA[3:0].
A9	EVREF	Out	4 mA	VREF output for external OSD controller.
B9	EHREF	Out	4 mA	HREF output for external OSD controller.
C8	ECLK	Out	4 mA	Clock output for external OSD controller.
C7	EFSW	In	5-V tolerant	External OSD window display enable. Displays data from external OSD controller when high.
A7	EDIN_PAD3	In	5-V tolerant	Data input 3 from an external OSD controller.
B7	EDIN_PAD2	In	5-V tolerant	Data input 2 from an external OSD controller.
A8	EDIN_PAD1	In	5-V tolerant	Data input 1 from an external OSD controller.
B8	EDIN_PAD0	In	5-V tolerant	Data input 0 from an external OSD controller.
A2	MFB_11	In/Out	5-V tolerant / 8mA	Bit 11 of 12-bit Multi-Function Bus MFB[11:0], which may be used as general purpose I/O (GPIO).
A3	MFB_10	In/Out	5-V tolerant / 8mA	Bit 10 of 12-bit Multi-Function Bus MFB[11:0]. May be used as GPIO.
B3	MFB_9	In/Out	5-V tolerant / 8mA	Bit 9 of 12-bit Multi-Function Bus MFB[11:0]. May be used as GPIO.
A4	MFB_8	In/Out	5-V tolerant / 8mA	Bit 8 of 12-bit Multi-Function Bus MFB[11:0]. May be used as GPIO.
B4	MFB_7	In/Out	5-V tolerant / 8mA	Bit 7 of 12-bit Multi-Function Bus MFB[11:0]. May be used as GPIO. Do not connect external pull-up resistors to this pin.
C4	MFB_6	In/Out	5-V tolerant / 8mA	Bit 6 of 12-bit Multi-Function Bus MFB[11:0]. May be used as GPIO. If an external pull-up resistor is connected to this pin, gmB135 is configured for 1-bit host interface. The default host interface configuration is 4-bit.
A5	MFB_5	In/Out	5-V tolerant / 8mA	Bit 5 of 12-bit Multi-Function Bus MFB[11:0]. May be used as GPIO.
B5	MFB_4	In/Out	5-V tolerant / 8mA	Bit 4 of 12-bit Multi-Function Bus MFB[11:0]. May be used as GPIO.
C5	MFB_3	In/Out	5-V tolerant / 8mA	Bit 3 of 12-bit Multi-Function Bus MFB[11:0]. May be used as GPIO.
A6	MFB_2	In/Out	5-V tolerant / 8mA	Bit 2 of 12-bit Multi-Function Bus MFB[11:0]. May be used as GPIO.
B6	MFB_1	In/Out	5-V tolerant / 8mA	Bit 1 of 12-bit Multi-Function Bus MFB[11:0]. May be used as GPIO.
C6	MFB_0	In/Out	5-V tolerant / 8mA	Bit 0 of 12-bit Multi-Function Bus MFB[11:0]. May be used as GPIO.

Table 1.4.3. Clock Recovery and Time Base Conversion

Pin	Name	In / Out	5-V Tolerant Input?	Description
C2	CRT_VDD			Digital power for the Hsync/Vsync input pads.
C3	CRT_VSS			Digital ground for the Hsync/Vsync input pads.
J3	DAC_SVDDA			Analog power for the Source DDS DAC. Must be bypassed with a 0.1 uF capacitor to pin J2 (DAC_SGNDA)
H1, J1, J2	DAC_SGNDA			Analog ground for the Source DDS DAC. Must be directly connected to the analog ground plane.
F4	DAC_DVDDA			Analog power for Destination DDS DAC. Must be bypassed with a 0.1 uF capacitor to pin E3 (DAC_DGNDA)
E2, E3	DAC_DGNDA			Analog ground for Destination DDS DAC. Must be directly connected to the analog ground plane.
D4	PLL_RVDDA			Analog power for the Reference DDS PLL. Must be bypassed with a 0.1 uF capacitor to pin E4 (PLL_RGNDA)
E4	PLL_RGNDA			Analog ground for the Reference DDS PLL. Must be directly connected to the analog ground plane.
H3	PLL_SVDDA			Analog power for the Source DDS PLL. Must be bypassed with a 0.1 uF capacitor to pin H4 (PLL_SGNDA)
H4	PLL_SGNDA			Analog ground for the Source DDS PLL. Must be directly connected to the analog ground plane.
F3	PLL_DVDDA			Analog power for the Destination DDS PLL. Must be bypassed with a 0.1 uF capacitor to pin G4 (PLL_DGNDA)
G4	PLL_DGNDA			Analog ground for the Destination DDS PLL. Must be directly connected to the analog ground plane.
D2	SUB_RGNDA			Dedicated pin for the substrate guard ring that protects the Reference DDS. Must be directly connected to the analog ground plane.
G3	SUB_DGND			Dedicated pin for the substrate guard ring that protects the Destination DDS. Must be directly connected to the analog ground plane.
F1, G1, G2	SUB_SGND			Dedicated pin for the substrate guard ring that protects the Source DDS. Must be directly connected to the analog system ground plane.
D1	TCLK	In	5-V Tolerant	Reference clock (TCLK) input from the 50 Mhz crystal oscillator.
E1	XTAL	Out		Crystal oscillator output.
C1	VSYNC1	In	5-V Tolerant	CRT Vsync input 1. Enabled when analog port 1 is selected. TTL Schmitt trigger input.
A1	HSYNC1	In	5-V Tolerant	CRT Hsync or composite sync input 1. Enabled when analog port 1 is selected. TTL Schmitt trigger input.
B2	VSYNC2	In	5-V Tolerant	CRT Vsync input 2. Enabled when analog port 2 is selected. TTL Schmitt trigger input.
B1	HSYNC2	In	5-V Tolerant	CRT Hsync or composite sync input 2. Enabled when analog port 2 is selected. TTL Schmitt trigger input.
D3	VBUFC	Out		Used for testing only. Do not connect.
F2	VBUFC_D	Out		Used for testing only. Do not connect.
H2	VBUFC_S	Out		Used for testing only. Do not connect.

Table 1.4.4. TFT Panel Interface

NOTE: Drive current of the panel output pins are programmable									
Pin	**Name**	**In / Out**	**Output Drive Current @10pF**	**Description**	**TFT (one pixel/clock)**			**TFT (two pixel/clock)**	
					8 bit	**6 bit**	**4 bit**	**8 bit**	**6 bit**
Y20	PD_47	Out	2 mA ~ 20 mA	Panel data output 47				OB1	
Y19	PD_46	Out	2 mA ~ 20 mA	Panel data output 46				OB0	
Y18	PD_45	Out	2 mA ~ 20 mA	Panel data output 45				OG1	
Y17	PD_44	Out	2 mA ~ 20 mA	Panel data output 44				OG0	
Y16	PD_43	Out	2 mA ~ 20 mA	Panel data output 43				OR1	
W20	PD_42	Out	2 mA ~ 20 mA	Panel data output 42				OR0	
W19	PD_41	Out	2 mA ~ 20 mA	Panel data output 41	B1			EB1	
W18	PD_40	Out	2 mA ~ 20 mA	Panel data output 40	B0			EB0	
V20	PD_39	Out	2 mA ~ 20 mA	Panel data output 39	G1			EG1	
V19	PD_38	Out	2 mA ~ 20 mA	Panel data output 38	G0			EG0	
V18	PD_37	Out	2 mA ~ 20 mA	Panel data output 37	R1			ER1	
U20	PD_36	Out	2 mA ~ 20 mA	Panel data output 36	R0			ER0	
U19	PD_35	Out	2 mA ~ 20 mA	Panel data output 35				OB7	OB5
U18	PD_34	Out	2 mA ~ 20 mA	Panel data output 34				OB6	OB4
U17	PD_33	Out	2 mA ~ 20 mA	Panel data output 33				OB5	OB3
T20	PD_32	Out	2 mA ~ 20 mA	Panel data output 32				OB4	OB2
T19	PD_31	Out	2 mA ~ 20 mA	Panel data output 31				OB3	OB1
T18	PD_30	Out	2 mA ~ 20 mA	Panel data output 30				OB2	OB0
R20	PD_29	Out	2 mA ~ 20 mA	Panel data output 29				OG7	OG5
R19	PD_28	Out	2 mA ~ 20 mA	Panel data output 28				OG6	OG4
R18	PD_27	Out	2 mA ~ 20 mA	Panel data output 27				OG5	OG3
P20	PD_26	Out	2 mA ~ 20 mA	Panel data output 26				OG4	OG2
P19	PD_25	Out	2 mA ~ 20 mA	Panel data output 25				OG3	OG1
P18	PD_24	Out	2 mA ~ 20 mA	Panel data output 24				OG2	OG0
N20	PD_23	Out	2 mA ~ 20 mA	Panel data output 23				OR7	OR5
N19	PD_22	Out	2 mA ~ 20 mA	Panel data output 22				OR6	OR4
N18	PD_21	Out	2 mA ~ 20 mA	Panel data output 21				OR5	OR3
M20	PD_20	Out	2 mA ~ 20 mA	Panel data output 20				OR4	OR2
M19	PD_19	Out	2 mA ~ 20 mA	Panel data output 19				OR3	OR1
M18	PD_18	Out	2 mA ~ 20 mA	Panel data output 18				OR2	OR0
L20	PD_17	Out	2 mA ~ 20 mA	Panel data output 17	B7	B5	B3	EB7	EB5
L19	PD_16	Out	2 mA ~ 20 mA	Panel data output 16	B6	B4	B2	EB6	EB4
L18	PD_15	Out	2 mA ~ 20 mA	Panel data output 15	B5	B3	B1	EB5	EB3
K20	PD_14	Out	2 mA ~ 20 mA	Panel data output 14	B4	B2	B0	EB4	EB2
K19	PD_13	Out	2 mA ~ 20 mA	Panel data output 13	B3	B1		EB3	EB1
K18	PD_12	Out	2 mA ~ 20 mA	Panel data output 12	B2	B0		EB2	EB0
J20	PD_11	Out	2 mA ~ 20 mA	Panel data output 11	G7	G5	G3	EG7	EG5
J19	PD_10	Out	2 mA ~ 20 mA	Panel data output 10	G6	G4	G2	EG6	EG4
J18	PD_9	Out	2 mA ~ 20 mA	Panel data output 9	G5	G3	G1	EG5	EG3

Table 1.4.4. TFT Panel Interface

H20	PD_8	Out	2 mA ~ 20 mA	Panel data output 8	G4	G2	G0	EG4	EG2
H19	PD_7	Out	2 mA ~ 20 mA	Panel data output 7	G3	G1		EG3	EG1
H18	PD_6	Out	2 mA ~ 20 mA	Panel data output 6	G2	G0		EG2	EG0
G20	PD_5	Out	2 mA ~ 20 mA	Panel data output 5	R7	R5	R3	ER7	ER5
G19	PD_4	Out	2 mA ~ 20 mA	Panel data output 4	R6	R4	R2	ER6	ER4
G18	PD_3	Out	2 mA ~ 20 mA	Panel data output 3	R5	R3	R1	ER5	ER3
F20	PD_2	Out	2 mA ~ 20 mA	Panel data output 2	R4	R2	R0	ER4	ER2
F19	PD_1	Out	2 mA ~ 20 mA	Panel data output 1	R3	R1		ER3	ER1
F18	PD_0	Out	2 mA ~ 20 mA	Panel data output 0	R2	R0		ER2	ER0
T17	PDE	Out	2 mA ~ 20 mA	Panel Display Enable signal, active when flat panel data is valid.					
E19	PHS	Out	2 mA ~ 20 mA	This output provides the panel line clock signal.					
E20	PVS	Out	2 mA ~ 20 mA	This output provides the panel frame start signal.					
R17	PCLK	Out	2 mA ~ 20 mA	This output drives the flat panel shift clock.					
H17	PCLK2	Out	2 mA ~ 20 mA	This output drives the second panel shift clock. The polarity and phase of this signal is independently programmable.					
E17	PPwr	Out	8 mA	This output controls the power to a flat panel.					
E18	PBias	Out	8 mA	This output turns on/off the panel bias power or controls panel backlight.					

Table 1.4.5. Pin-Scan Test Pins

Pin#	Name	In/ Out	5-V Tolerant Input?	Description
U16	PSCAN	In	5-V tolerant	Automatic PCB assembly test enable. When this input is pulled high, the chip enters automatic PCB assembly test mode. An internal pull-down resistor drives this input low for normal operation. Do not connect for normal operation. For further details please refer to Appendix A: gmB135 Para-Scan.
V16	STI_TM1	In	5-V tolerant	Internal test pin.
W16	STI_TM2	In	5-V tolerant	Internal test pin.

Table 1.4.6. CCIR-601 Input Port

Pin#	Name	In/ Out	5-V Tolerant Input?	Description	
				8-bit (2x-clock) Configuration	16-bit (1x-clock) Configuration
T1	PIXIN_15	In	5-V Tolerant		U[7]/V[7]
T2	PIXIN_14	In	5-V Tolerant		U[6]/V[6]
T3	PIXIN_13	In	5-V Tolerant		U[5]/V[5]
R2	PIXIN_12	In	5-V Tolerant		U[4]/V[4]
R1	PIXIN_11	In	5-V Tolerant		U[3]/V[3]
P2	PIXIN_10	In	5-V Tolerant		U[2]/V[2]
P3	PIXIN_9	In	5-V Tolerant		U[1]/V[1]
N2	PIXIN_8	In	5-V Tolerant		U[0]/V[0]
N3	PIXIN_7	In	5-V Tolerant	Y[7]/U[7]/V[7]	Y[7]
M2	PIXIN_6	In	5-V Tolerant	Y[6]/U[6]/V[6]	Y[6]
M3	PIXIN_5	In	5-V Tolerant	Y[5]/U[5]/V[5]	Y[5]
L2	PIXIN_4	In	5-V Tolerant	Y[4]/U[4]/V[4]	Y[4]
L3	PIXIN_3	In	5-V Tolerant	Y[3]/U[3]/V[3]	Y[3]
K1	PIXIN_2	In	5-V Tolerant	Y[2]/U[2]/V[2]	Y[2]
K2	PIXIN_1	In	5-V Tolerant	Y[1]/U[1]/V[1]	Y[1]
K3	PIXIN_0	In	5-V Tolerant	Y[0]/U[0]/V[0]	Y[0]
L1	CCVSYNC	In	5-V Tolerant	Video Vsync	
N1	CCHSYNC	In	5-V Tolerant	Video Hsync	
M1	CCHREF	In	5-V Tolerant	Horizontal Display Reference. Valid when the data is valid.	
P1	CCSCLK	In	5-V Tolerant	2x Video Clock	1x Video Clock

Table 1.4.7. Digital Input Port

Pin#	Name	In / Out	5V Tolerant Input?	Description	One pixel/clock			Two pixels/clock	
					8 bit	6 bit	4 bit	8 bit	6 bit
U15	PLQO_23	In	No (up to 3.3V)	Digital odd data 23				OR7	OR5
V15	PLQO_22	In	No (up to 3.3V)	Digital odd data 22				OR6	OR4
W15	PLQO_21	In	No (up to 3.3V)	Digital odd data 21				OR5	OR3
Y15	PLQO_20	In	No (up to 3.3V)	Digital odd data 20				OR4	OR2
V14	PLQO_19	In	No (up to 3.3V)	Digital odd data 19				OR3	OR1
W14	PLQO_18	In	No (up to 3.3V)	Digital odd data 18				OR2	OR0
Y14	PLQO_17	In	No (up to 3.3V)	Digital odd data 17				OR1	
V13	PLQO_16	In	No (up to 3.3V)	Digital odd data 16				OR0	
W13	PLQO_15	In	No (up to 3.3V)	Digital odd data 15				OG7	OG5
Y13	PLQO_14	In	No (up to 3.3V)	Digital odd data 14				OG6	OG4
U12	PLQO_13	In	No (up to 3.3V)	Digital odd data 13				OG5	OG3
V12	PLQO_12	In	No (up to 3.3V)	Digital odd data 12				OG4	OG2
W12	PLQO_11	In	No (up to 3.3V)	Digital odd data 11				OG3	OG1
Y12	PLQO_10	In	No (up to 3.3V)	Digital odd data 10				OG2	OG0
V11	PLQO_9	In	No (up to 3.3V)	Digital odd data 9				OG1	
W11	PLQO_8	In	No (up to 3.3V)	Digital odd data 8				OG0	
Y11	PLQO_7	In	No (up to 3.3V)	Digital odd data 7				OB7	OB5
V10	PLQO_6	In	No (up to 3.3V)	Digital odd data 6				OB6	OB4
W10	PLQO_5	In	No (up to 3.3V)	Digital odd data 5				OB5	OB3
Y10	PLQO_4	In	No (up to 3.3V)	Digital odd data 4				OB4	OB2
V9	PLQO_3	In	No (up to 3.3V)	Digital odd data 3				OB3	OB1
W9	PLQO_2	In	No (up to 3.3V)	Digital odd data 2				OB2	OB0
Y9	PLQO_1	In	No (up to 3.3V)	Digital odd data 1				OB1	
V8	PLQO_0	In	No (up to 3.3V)	Digital odd data 0				OB0	
W8	PLQE_23	In	No (up to 3.3V)	Digital even data 23	R7	R5	R3	ER7	ER5
Y8	PLQE_22	In	No (up to 3.3V)	Digital even data 22	R6	R4	R2	ER6	ER4
V7	PLQE_21	In	No (up to 3.3V)	Digital even data 21	R5	R3	R1	ER5	ER3
W7	PLQE_20	In	No (up to 3.3V)	Digital even data 20	R4	R2	R0	ER4	ER2
Y7	PLQE_19	In	No (up to 3.3V)	Digital even data 19	R3	R1		ER3	ER1
V6	PLQE_18	In	No (up to 3.3V)	Digital even data 18	R2	R0		ER2	ER0
W6	PLQE_17	In	No (up to 3.3V)	Digital even data 17	R1			ER1	
Y6	PLQE_16	In	No (up to 3.3V)	Digital even data 16	R0			ER0	
U5	PLQE_15	In	No (up to 3.3V)	Digital even data 15	G7	G5	G3	EG7	EG5
V5	PLQE_14	In	No (up to 3.3V)	Digital even data 14	G6	G4	G2	EG6	EG4
W5	PLQE_13	In	No (up to 3.3V)	Digital even data 13	G5	G3	G1	EG5	EG3
Y5	PLQE_12	In	No (up to 3.3V)	Digital even data 12	G4	G2	G0	EG4	EG2
V4	PLQE_11	In	No (up to 3.3V)	Digital even data 11	G3	G1		EG3	EG1
W4	PLQE_10	In	No (up to 3.3V)	Digital even data 10	G2	G0		EG2	EG0
Y4	PLQE_9	In	No (up to 3.3V)	Digital even data 9	G1			EG1	
V3	PLQE_8	In	No (up to 3.3V)	Digital even data 8	G0			EG0	
W3	PLQE_7	In	No (up to 3.3V)	Digital even data 7	B7	B5	B3	EB7	EB5

Table 1.4.7. Digital Input Port

Y3	PLQE_6	In	No (up to 3.3V)	Digital even data 6	B6	B4	B2	EB6	EB4
V2	PLQE_5	In	No (up to 3.3V)	Digital even data 5	B5	B3	B1	EB5	EB3
W2	PLQE_4	In	No (up to 3.3V)	Digital even data 4	B4	B2	B0	EB4	EB2
Y2	PLQE_3	In	No (up to 3.3V)	Digital even data 3	B3	B1		EB3	EB1
W1	PLQE_2	In	No (up to 3.3V)	Digital even data 2	B2	B0		EB2	EB0
V1	PLQE_1	In	No (up to 3.3V)	Digital even data 1	B1			EB1	
U4	PLQE_0	In	No (up to 3.3V)	Digital even data 0	B0			EB0	
U1	PLHsync_ PAD	In	No (up to 3.3V)	PL Hsync input					
U2	PLVsync_ PAD	In	No (up to 3.3V)	PL Vsync input					
U3	PLDE_ PAD	In	No (up to 3.3V)	PL Display Enable input					
U7	PLOCLK	In	No (up to 3.3V)	PL Clock input					

Table 1.4.8. Digital VDD/VSS for the Core Circuitry, Host Interface, digital and CCIR-601 input ports, source and destination DDSs, and Panel Output Interface (All the VDDs including analog VDDs must be in the range of +3.3V +/-5%.)

Pins	Name	Description
D11, D12, J4, U8, U9, U11, U14, L17, M17	CVDD	Core circuitry VDD. Tie to PVDD on a print circuit board.
H8 ~ H13, J8 ~ J13, K8 ~ K13, L8 ~ L13, M8 ~ M13, N8 ~ N13 (middle 6x6 pins)	CVSS	Digital grounds for core circuitry and panel output interface.
G17, K17, N17, V17	PL_VDD	VDD for panel output interface. Tie to CVDD on a print circuit board.
F17, J17, P17, W17	PL_VSS	Ground for panel output interface.
D6, D8, D10	HE_VDD	VDD for host interface and external OSD interface.
D5, D7, D9	HE_VSS	Ground for host interface and external OSD interface.
K4	D_VDD	VDD for destination DDS.
L4	D_VSS	VSS for destination DDS.
N4	S_VDD	VDD for source DDS.
M4	S_VSS	VSS for source DDS.
P4	CC_VDD	CCIR-601 input port VDD.
R3, R4	CC_VSS	CCIR-601 input port ground.
U6, U13	DI_VDD	Digital input port VDD.
T4, U10	DI_VSS	Digital input port ground.

1.5 System-Level Implementation

Figure 1.5.1. Typical Configuration with 1-bit Host Interface, 1 pixel/clock XGA Panel, 2-Channel Analog RGB input and 1 pixel/clock TMDS Receiver.

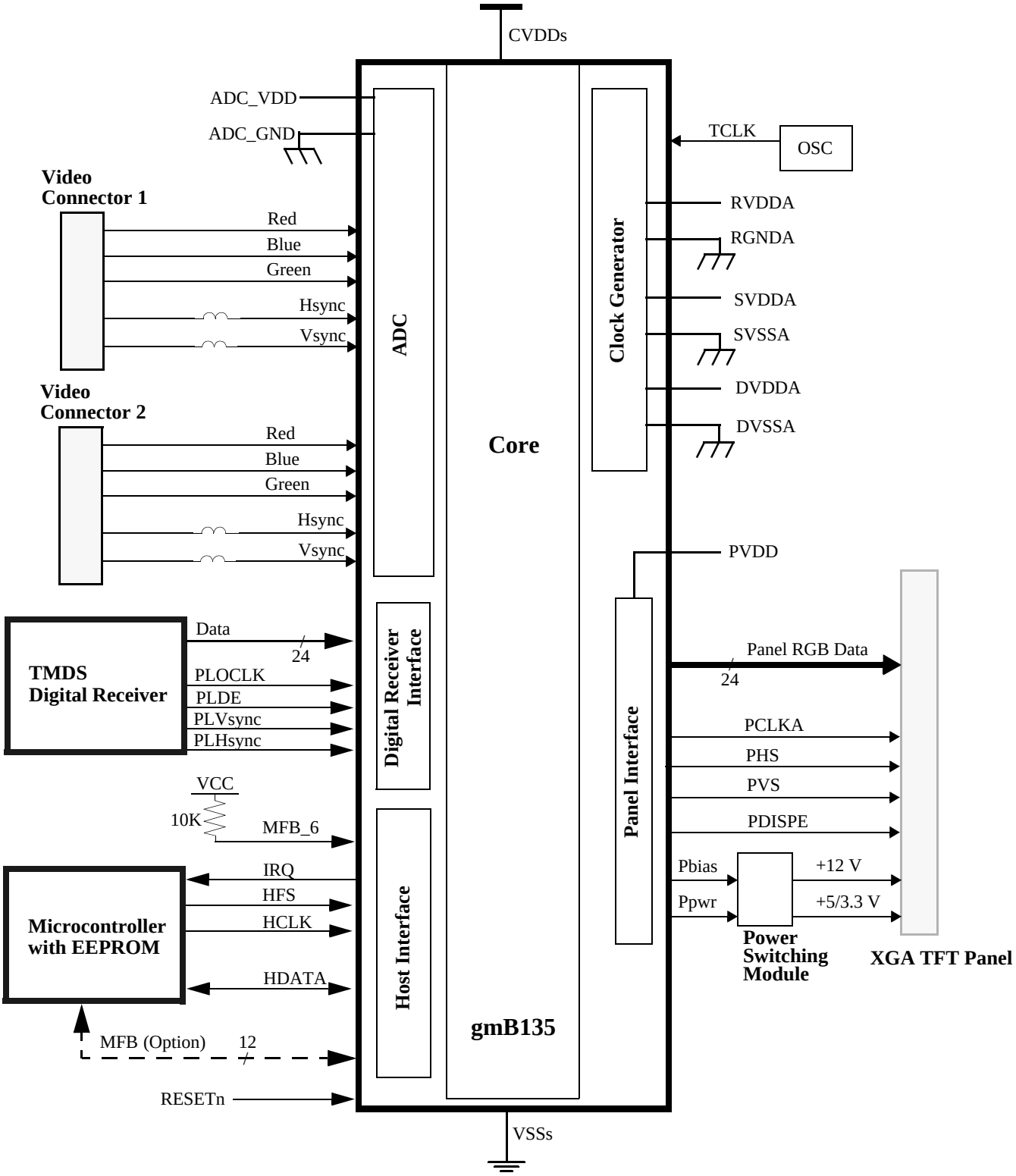
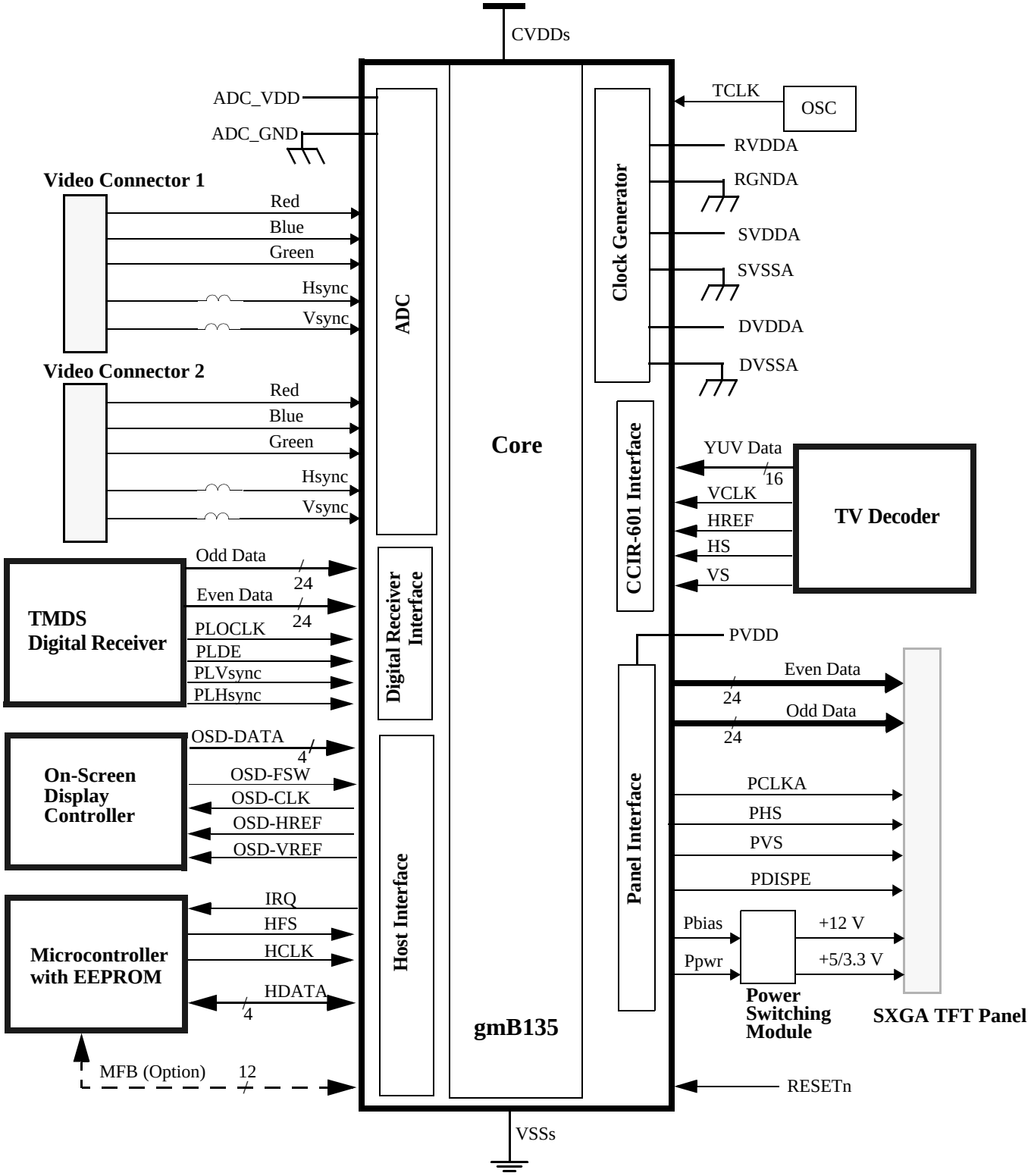


Figure 1.5.2. Typical Configuration with 4-bit Host Interface, 2 pixels/clock SXGA panel, 2-channel analog RGB input, 2 pixel/clock TMDS Receiver, digital TV decoder and external OSD controller



1.6 Operating Modes gmB135

This section describes the operating modes of the gmB135. To explain the types of operating modes, the Source Clock (also called as SCLK in this document), the Panel Clock are defined as follows:

- The Source Clock is the sample clock, either regenerated from the input Hsync timing (called clock recovery) by SCLK DDS (direct digital synthesis)/ PLL for analog inputs, or from the input digital clock for digital inputs.
- The Panel Clock is the timing clock for panel data at the one pixel per clock rate. The actual PCLK to the panel may be one-half that frequency for double-pixel panel data format. When its frequency is different from that of source clock, the panel clock is generated by Destination Clock (or DCLK) DDS/PLL.

There are six display modes: Native, Slow DCLK, Expansion, Downscaling, Destination Stand Alone, Source Stand Alone.

Each mode is unique in terms of:

- input video resolution vs. panel resolution,
- Source Clock frequency / Panel Clock frequency ratio,
- Source Hsync frequency / Panel Hsync frequency ratio,
- data source (video input, panel background color, on-chip pattern generator).

1.6.1 Native

Panel clock frequency = Source clock frequency
Panel Hsync frequency = Input Hsync frequency
Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is the same as the panel resolution and the input data clock frequency is within the panel clock frequency specification of a panel being used.

1.6.2 Slow DCLK

Panel clock frequency < Source clock frequency
Panel Hsync frequency = Input Hsync frequency
Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is the same as the panel resolution, but the input data clock frequency exceeds the panel clock frequency specification of a panel being used. The panel clock is scaled to the Source clock, and the internal data buffers are used to spread out the timing of the input data by making use of the large CRT blanking time to extend the panel horizontal display time.

1.6.3 Expansion

Panel clock frequency > Source clock frequency
Panel Hsync frequency > Input Hsync frequency
Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is less than the panel resolution. The input data clock is then locked to the panel clock, which is at a higher frequency. The input data is expanded.

1.6.4 Downscaling

Panel clock frequency > Source clock frequency
Panel Hsync frequency < Input Hsync frequency
Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is greater than the panel resolution, and is used to provide enough of a display to enable the user to recover to a supported resolution. The input clock is operated at a frequency less than that of the input pixel rate (under-sampled horizontally) and the expander function is used to drop input lines. Expansion interpolation is not provided and must be off.

1.6.5 Destination Stand Alone

Panel clock = DCLK in open loop (not locked)
Panel Hsync frequency = DCLK frequency / (Destination Htotal register value)
Panel Vsync frequency = DCLK frequency / (Destination Htotal register value * Destination Vtotal register value)

This mode is used when the input is changing or not available. The OSD may still be used as in all other display modes, and stable panel timing signals are produced. This mode may be automatically set when the gmB135 detect input timing changes that could cause out-of-spec operation of the panel.

1.6.6 Source Stand Alone

Panel clock = SCLK in open loop (not locked to input Hsync)
Panel Hsync frequency = SCLK frequency / (Source Htotal register value)
Panel Vsync frequency = SCLK frequency / (Source Htotal register value * Source Vtotal register value)

This mode is used to display the Pattern Generator Data. This mode may be useful for testing an LCD panel on the manufacturing line (color temperature calibration, etc.).

1.7 Input Video Mode Support

The gmB135 can support various standard VGA/VESA/Macintosh display modes depending on the LCD panel specifications. By default, all data input is expanded to full-panel-screen resolution. An Excel 97 spreadsheet (`Mode Support.XLS`) showing the relationship between panel specifications and supported modes is provided separately. Note that in the spreadsheet, the user needs to supply the panel parameters that are marked in blue. The spreadsheet will automatically determine whether the listed modes can be supported based on the user-supplied panel parameters.

2. Functional Block Description.

Figure 2.1 shows the high-level block diagram of gmB135 chip. Each block is described in detail in this chapter.

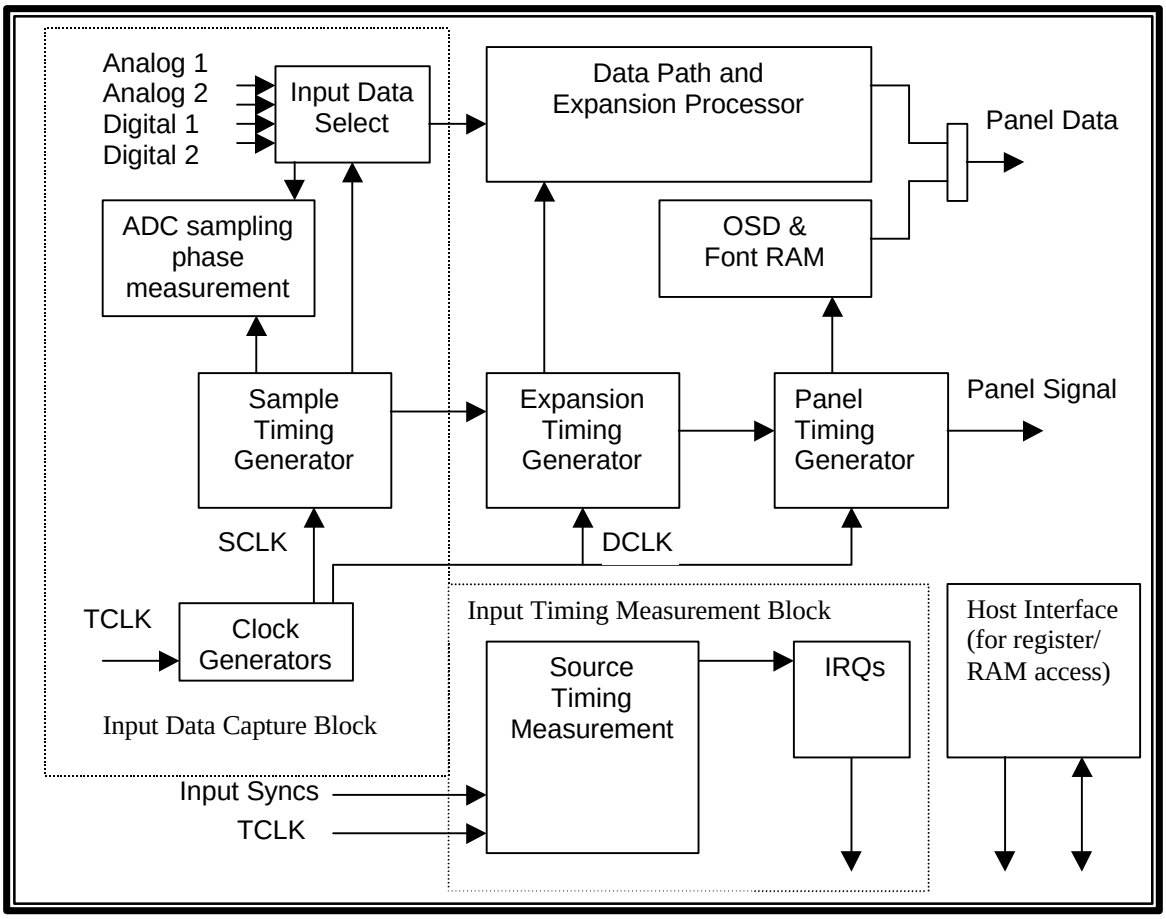


Figure 2.1 Functional Block Diagram of gmB135

2.1 Input Data Capture Block

Input data capture block consists of two major function blocks: (1)data source block and (2)source timing generator block.

The data source block consists of input ports, analog-to-digital converter (ADC), and clock-recovery circuit. There are four input ports: two analog and two digital. This block receives video data input and digitizes it if the video data is analog or perform YUV-to-RGB conversion if the video data is CCIR601 compatible.

Sitting right after the data source block, the source timing generator (STG) block sets a “capture window.” The data within this window gets sent to the data path block.

2.1.1 Input ports

gmB135 has four video inputs:

- Analog input port 1,
- Analog input port 2,
- Digital input port 1,
- Digital input port 2 (for CCIR601-compatible, YUV format data).

Only one input is selected at a time via a register programming.

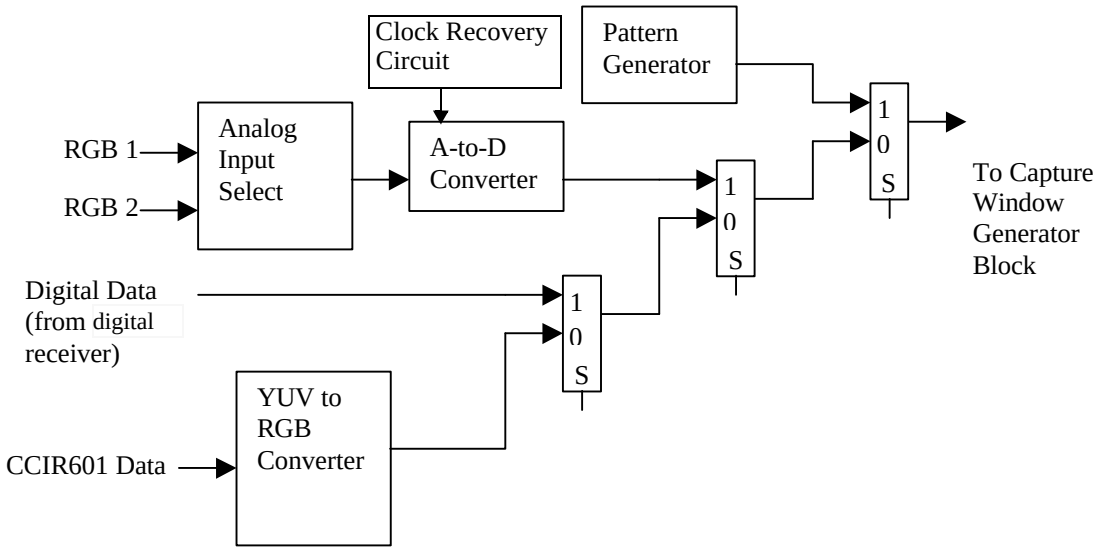


Figure 2.1.1 Data Source Block Diagram

2.1.1.a Analog input ports

Two analog input ports are connected to the same 3-channel ADCs and clock recovery circuit through an analog multiplexer inside the gmB135 chip.

Table 2.1.1 Pin Out of Analog Port 1 and Analog Port 2

Pin No.	Pin Name	
Analog Port 1		
TBD	RED1+	Positive analog input for the Red channel 1.
TBD	RED1-	Negative analog input for the Red channel 1.
TBD	GREEN1+	Positive analog input for the Green channel 1.
TBD	GREEN1-	Negative analog input for the Green channel 1.
TBD	BLUE1+	Positive analog input for the Blue channel 1.
TBD	BLUE1-	Negative analog input for the Blue channel 1.
C1	VSYNC1	CRT Vsync input 1. Enabled when analog port 1 is selected. TTL Schmitt trigger input.
A1	HSYNC1/ CSYNC1	CRT Hsync or composite sync input 1. Enabled when analog port 1 is selected. TTL Schmitt trigger input.
Analog Port 2		
TBD	RED2+	Positive analog input for the Red channel 2.
TBD	RED2-	Negative analog input for the Red channel 2.
TBD	GREEN2+	Positive analog input for the Green channel 2.
TBD	GREEN2-	Negative analog input for the Green channel 2.
TBD	BLUE2+	Positive analog input for the Blue channel 2.
TBD	BLUE2-	Negative analog input for the Blue channel 2.
B2	VSYNC2	CRT Vsync input 2. Enabled when analog port 2 is selected.TTL Schmitt trigger input.
B1	HSYNC2/ CSYNC2	CRT Hsync or composite sync input 2. Enabled when analog port 2 is selected.TTL Schmitt trigger input.

2.1.1.b Digital input port 1

The digital input port 1 can be configured either for 1 pixel/clock or for 2 pixels/clock. For data mapping information, refer to Table 1.4.7. on page 15. Panel output interface can be set to either 1 pixel/clock or 2 pixels/clock independent of the digital input port configuration.

This input port is to be connected to the output port of a digital receiver chip such as TMDS receiver. The minimum setup/hold time of this port is 1.5 ns. If the output of a receiver cannot meet this setup/hold time requirement, the clock input should be delayed inside gmB135. The delay value can be programmed in the range of 2- ~ 45 ns.

2.1.1.c CCIR601 input port

This input port is for the YUV video data. It is to be connected to a digital TV decoder chip that generates CCIR601-compatible video data.

Both 8 and 16 bit wide data are supported. For 8-bit data the input order is: U, Y0, V, Y1 … For the 16-bit data the D7:0 input order is: Y0, Y1, Y2, Y3 … . The D15:8 input order is: U0, V0, U2, V2, …

For data mapping information, refer to Table 1.4.6. on page 14. In 8-bit configuration, 2x video clock must be provided.

The U and V color component is the color for the first luminance sample of each pair of Y data. When this input data is reformatted for color conversion the “missing” U and V data for the other luminance data is merely the replicated U and V data.

For CCIR601 data the input Gamma Table will be used to provide both the proper gamma correction for the TV input and to re-scale the YUV-RGB converted data to the full 00h to FFh range.

The YUV to RGB conversion equations used are:

$R = Y + 1.375 (V - 128)$

$G = Y - 0.34375 (U - 128) - 0.6875 (V - 128)$

$B = Y + 1.75 (U - 128)$

The other inputs for the CCIR601 interface are: Hsync, Vsync, Href (which indicates valid data) and Clock.

2.1.2 Analog-to-digital converter

Table 2.1.2 summarizes the characteristics of the 3-channel analog-to-digital converters (ADCs) integrated in gmB135.

Table 2.1.2 ADC Characteristics

	MIN	TYP	MAX	NOTE
RGB Track & Hold Amplifiers				
Band Width		160 MHz		
Settling Time to 1/2%		8.5 ns		Full Scale Input = 0.75V, BW=160MHz
Full Scale Adjust Range @ R,G,B Inputs	0.55 V		0.9V	9 bits for adjustment per channel.
Full Scale Adjust Sensitivity		+/- 1 LSB		Measured @ ADC Output
Zero Scale Adjust Range for External Video Input		+/-50 mV		For a larger external DC offset, enable AC-coupling mode of Bridge135.
Zero Scale Adjust Sensitivity		+/- 1 LSB		Measured @ ADC Output
ADC + RGB Track & Hold Amplifiers				
Sampling Frequency (fs)	10 MHz		135 MHz	
DNL		+/- 0.5 LSB		fs = 135 MHz
INL		+/- 2.0 LSB		fs = 135 MHz
Channel to Channel Matching		+/- 1.0 LSB		fs = 135 MHz
Effective Number of Bits (ENOB)		7 Bits		fin = 1 MHz, fs = 80 MHz Vin= -1 db below full scale = 0.75V
Power Dissipation		TBD		fs = 135 MHz, Vdd = 3.3V
Shut Down Current			100uA	

The full scale and the zero scale of the three ADC channels can be independently adjusted. For adjustment, the overflow/ underflow status bits may be checked.

The overflow/underflow detection may take place throughout a frame or within a capture window as defined by the source timing generator registers.

2.1.3 Clock recovery circuit

The clock recovery circuit generates SCLK to sample analog RGB data. This circuit is locked to the HSYNC of the incoming video signal. The RCLK generated from the TCLK input is used as a reference clock of the clock recovery circuit.

The SCLK period is equal to the input horizontal period divided by the horizontal total value programmed in the gmB135 register. To sample analog data correctly, horizontal total register value must be the same as that of the video input.

The SCLK frequency (1/SCLK period) can be set to the range of 10- to 135-MHz. Using the DDS (direct digital synthesis) technology, this clock recovery circuit can generate any SCLK clock frequency within this range.

The DCLK, which is used to drive a panel when the panel clock is different from SCLK (or SCLK/2), is locked to the SCLK in a similar manner. DCLK frequency divided by N is locked to SCLK frequency divided by M. The value M and N are calculated and programmed in the register by firmware for each video input. The value M is to be close to the Source Htotal value.

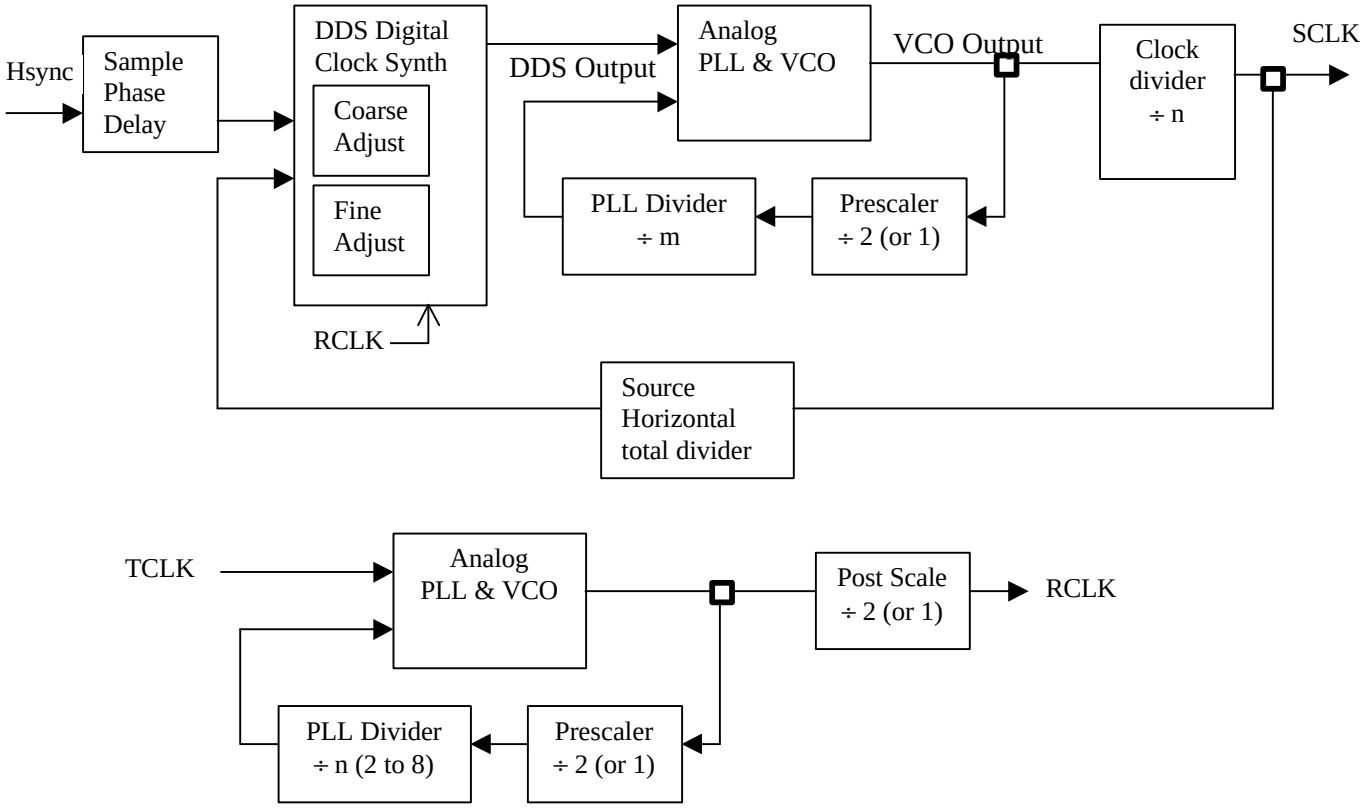


Figure 2.1.2 Clock Recovery Circuit

The table below summarizes the characteristics of the clock recovery circuit.

Table 2.1.3 Clock Recovery Circuit Characteristics

	MIN	TYP	MAX
SCLK Frequency	**10 MHz**		**135 MHz**
Sampling Phase Adjustment		**0.5 ns/step, 64 steps**	

2.1.3.a Sampling phase adjustment

The HSYNC input to the clock generator may be delayed. The delay value can be adjusted in 64 steps to adjust the ADC sampling phase. The accuracy of the sampling phase is checked by gmB135 and the “score” can be read in a register. This feature will enable accurate auto-adjustment of the ADC sampling phase.

2.1.3.b Composite-sync support

gmB135 can support a composite sync as long as VSYNC pulse is provided by an external sync separator chip.

With composite sync input, composite sync (CSYNC) pulses are either missing or different in polarity during the vertical blanking period. To generate a stable sampling clock with such an input, locking to HSYNC can be disabled for those lines during the vertical blanking period.

Note again that VSYNC pulse must be provided by an external sync separator for this feature to work.

2.1.4 Source Timing Generator Block

The input data is sent from the data source block to the source timing generator(STG) block. STG block defines a capture window. The data within this window is sent to the data path block.

2.1.4.a Capture window definition

The figure below shows how the window is defined. For horizontal direction, it is defined in SCLK count (equivalent to a pixel count) and for vertical direction, in line count.

All the parameters in the figure that start with “Source” are programmed into the gmB135 registers. Note that the vertical total is solely determined by the video input.

The reference point is as follows:

- The first pixel of a line: the pixel whose SCLK rising edge sees the transition of the HSYNC polarity from low to high.
- The first line of a frame: the line whose HSYNC rising edge sees the transition of the VSYNC polarity from low to high.

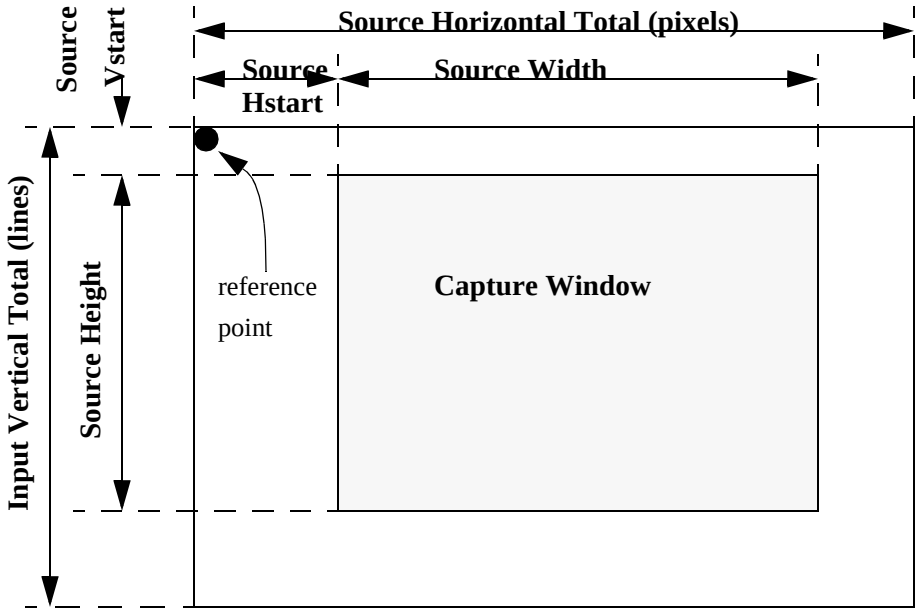


Figure 2.1.3 Capture Window

2.1.4.b Interlaced input support

When the input video is interlaced, the video image is expanded by 2 for each field. To improve the display quality, the gmB135 chip can be programmed so that one-line offset is added to the even field over the odd field (bobbing feature).

2.2 Input Timing Measurement Block

The input timing measurement block consists of the source timing measurement (STM) block and interrupt request (IRQ) controller.

Input timing parameters are measured by the STM block and stored in the registers. Some input conditions will generate IRQ to an external microcontroller. The IRQ-generating conditions are programmable.

2.2.1 Source timing measurement block

The table below lists all the parameters that can be read in the source timing measurement (STM) registers of gmB135.

Table 2.2.1 Input Timing Parameters Measured by the STM Block

Parameter	Unit	Updated at:
HSYNC/VSYNC Missing	**N/A**	**HSYNC: Every 4096 TCLKs** **VSYNC: Every 80 ms**
HSYNC/VSYNC Timing Change	**N/A**	**When the horizontal period delta or the vertical period delta to the previous line/frame exceeds the threshold value (programmable).**
HSYNC/VSYNC Polarity	**Positive/Negative**	**HSYNC: After register read** **VSYNC: Every frame**
Horizontal Period Min/Max	**TCLKs and SCLKs**	**After register read**
HSYNC High Period Min/Max	**TCLKs**	**After register read**
Vertical Period	**Lines**	**Every frame**
VSYNC High Period	**Lines**	**Every frame**
Horizontal Display Start	**SCLKs**	**Every frame**
Horizontal Display End	**SCLKs**	**Every frame**
Vertical Display Start	**Lines**	**Every frame**
Vertical Display End	**Lines**	**Every frame**
Interlaced Input Detect	**N/A**	**Every frame**
CRC Data/Line Data	**N/A**	**Every frame**

The definition of display start/end values is different depending on whether the input is analog or digital:

- For analog video input, the display start/end registers store the first and the last pixels/lines of the last frame that have RGB data above threshold. The threshold value is programmable.
- For digital video input, those registers store the first and the last pixels/lines of the Display Enable input signal.

The reference point of the STM block is same as that of the source timing generator (STG) block:

- The first pixel: the pixel whose SCLK rising edge sees the transition of the HSYNC polarity from low to high.
- The first line: the line whose HSYNC rising edge sees the transition of the VSYNC polarity from low to high.

The CRC data and the line data are used to detect a test pattern image sent to the gmB135 input ports.

2.2.2 IRQ controller

Some input timing condition can cause the gmB135 chip to generate IRQ. The IRQ-generation conditions are programmable as follows:

Table 2.2.2 IRQ-Generation Condition

IRQ Event	Remark
Timing event	**One of the three events:** **1. Leading edge of Vsync input,** **2. Panel line count (the line count is programmable),** **3. Every 10 ms** **(Only one event may be selected at a time.)**
Timing change	**Any of the following timing changes:** **1. Sync loss,** **2. Digital clock loss,** **3. DDS tracking error beyond threshold,** **4. Horizontal/vertical timing change beyond threshold.** **(Threshold values are programmable.)**

Reading the IRQ status flags will not affect the STM registers.

Note that if a new IRQ event occurs while the IRQ status register is being read, the IRQ signal will become inactive for a minimum of one TCLK period and get re-activated. The polarity of the IRQ signal is programmable.

2.3 Data Path Block

This section describes the data path block of gmB135 as shown in the following figure.

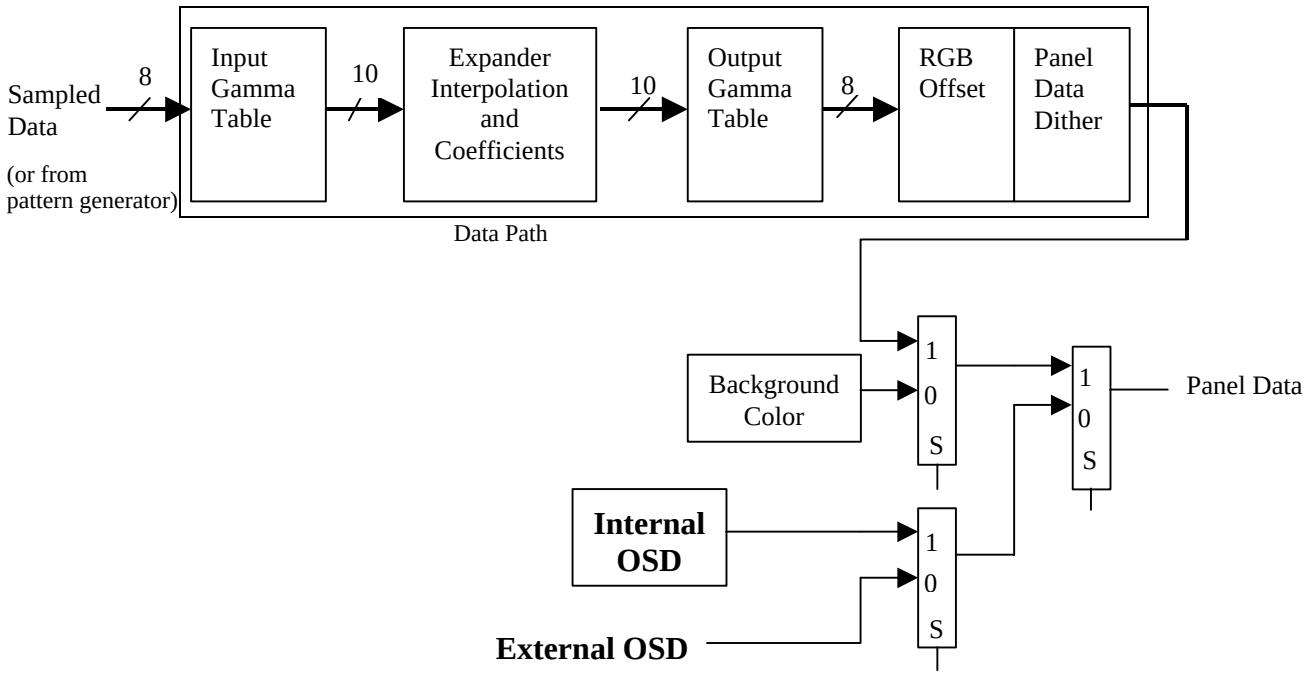


Figure 2.3.1 Data Path

2.3.1 Input Gamma Table

This lookup table takes the 8-bit R,G B data from the selected source and produces a 10-bit output. This feature is used to remove the gamma already present in the input data and produce an output that represents linear brightness (rather than the linear amplitude in the digital input). This is effectively an inverse gamma function, and provides the best representation of the input data to the expansion interpolation processor. When the digital YUV input is used, this lookup function is also used to provide the re-scaling of the converted RGB to a full range signal.

2.3.2 Expander Interpolator and Coefficients

For the best display quality when the source resolution is less than the panel resolution, the gmB135 provides an advanced data interpolator. A two dimensional matrix of input data is used to calculate the best output value for the horizontally and vertically expanded output data. A programmable 1024 byte table of 8 bit interpolator coefficients is used for this feature. The expander block takes in the 10-bit output from the input gamma table, and produces a 10-bit output. The vertical and horizontal expansion amounts are independently programmable.

2.3.3 Output Gamma Table

The output gamma is used to adjust the RGB data (from both expansion interpolation results and direct Native input) for the individual display characteristics of the TFT panel. The overall gamma of the display may be set, as well as separate corrections for each of the three display channels. In addition, the output gamma may be used for contrast, brightness, and white balance (temperature) adjustments. This lookup table has a 10-bit input (1024 different RGB entries) and produces an 8-bit output.

2.3.4 RGB Offset

The RGB offsets provide a simple shift (positive or negative) for each of the three color channels. This may be used as a simple brightness adjustment within a limited range. The data is clamped to zero for negative offsets, and clamped to FFh for positive offsets. This adjustment is much faster than recalculating the gamma table, and could be used with the OSD user controls to provide a quick brightness adjust. An offset range of plus 127 to minus 127 is available.

2.3.5 Panel Data Dither

For TFT panels that have fewer than eight bits for each R, G, B input, the gmB135 provides a dither pattern to more smoothly shade colors on 4 and 6 bit panels.

2.3.6 Panel Background Color

This simply provides a solid background color for a border around any partial expansion display data, or for the Destination Stand Alone Mode. The background color is most often set to black.

2.4 Panel Interface

The gmB135 chip interfaces directly with all of today's commonly used TFT LCD flat panels with 640x480, 800x600, 1024x768 and 1280x1024 resolutions. The resolution and the aspect ratio are NOT limited to specific values.

All aspects of the gmB135 panel interface are programmable. For horizontal parameters, Horizontal Display Enable Start, Horizontal Display Enable End, Horizontal Sync Start and Horizontal Sync End are programmable. Vertical Display Enable Start, Vertical Display Enable End, Vertical Sync Start and Vertical Sync Start are also fully programmable.

In order to maximize panel data setup and hold time, the panel clock (PCLKA, PCLKB) output skew is programmable. In addition, the current drive strength of the panel interface pins are programmable.

The following sections describe these functions in detail.

2.4.1 TFT Panel Interface Timing Specification

The TFT panel interface timing parameters of the gmB135 chip are listed in the table below. Refer to three timing diagrams of Figure 2.4.1 and Figure 2.4.2 for the timing parameter definition.

Table 2.4.2gmB135 TFT Panel Interface Timing ([ ] are for two pixels/clock mode)

Signal Name			min	typical	max	unit *1
PVS	period	t1	0		2048	lines
				16.67	-	ms
	frequency			60	-	Hz
	front porch	t2	0		2048	lines
	back porch	t3	0		2048	lines
	pulse width	t4	0		2048	lines
	PDispE	t5	0	panel height	2048	lines
	Disp. start from VS	t6	0		2048	lines
	PVS set up to PHS	t18	1		2048	pclk
	PVS hold from PHS	t19	1		2048	pclk
PHS	period	t7	0		2048 [1024]	pclk
	front porch	t8	0		2048	pclk
	back porch	t9	0		2048	pclk
	pulse width	t10	0		2048	pclk
	PDispE	t11	0	panel width	2048 [1024]	pclk
	Disp. start from HS	t12	0		2048	pclk
PclkA, PclkB*4	Frequency	t13			135 [67.5]	MHz
	Clock (H) *2	t14	DCLK/2 - 3 [DCLK - 3]		DCLK/2 - 2 [DCLK - 2]	ns
	Clock (L) *2	t15	DCLK/2 - 3 [DCLK - 3]		DCLK/2 - 2 [DCLK - 2]	ns
	type		-	one pels/clock [two pels/clock[	-	
Data	set up *3	t16	DCLK/2 - 5 [(DCLK - 5]		DCLK/2 - 2 [DCLK - 2]	ns
	hold *3	t17	DCLK/2 - 5 [(DCLK - 5]		DCLK/2 - 2 [DCLK - 2]	ns
	width		3 bits	18bits [36 bits]	24bits [48bits]	bits/pixel

NOTES

*1:The pclk is the panel shift clock.

*2: The DCLK stands for Destination Clock (DCLK) period. is equal to:

- pclk period in one pixel/clock mode,

- twice the pclk period in two pixels/clock mode. 40

The drive current of the panel interface signals is programmable as shown in Table 2.4.4 on page 40. The drive current is to be programmed through the API upon the chip initialization. Output current is programmable from 2 mA to 20 mA in increments of 2 mA. Drive strength should be programmed to match the load presented by the cable and input of the panel.

*3: The same setup/hold time specification to the pclk also applies to the PHS and the PDispE signals. The setup time (t16) and the hold time (t17) listed in this table are for the case in which no clock-to-data skew is added: The PVS/PHS/PDispE/ PData signals are asserted on the rising edge of the Pclk.

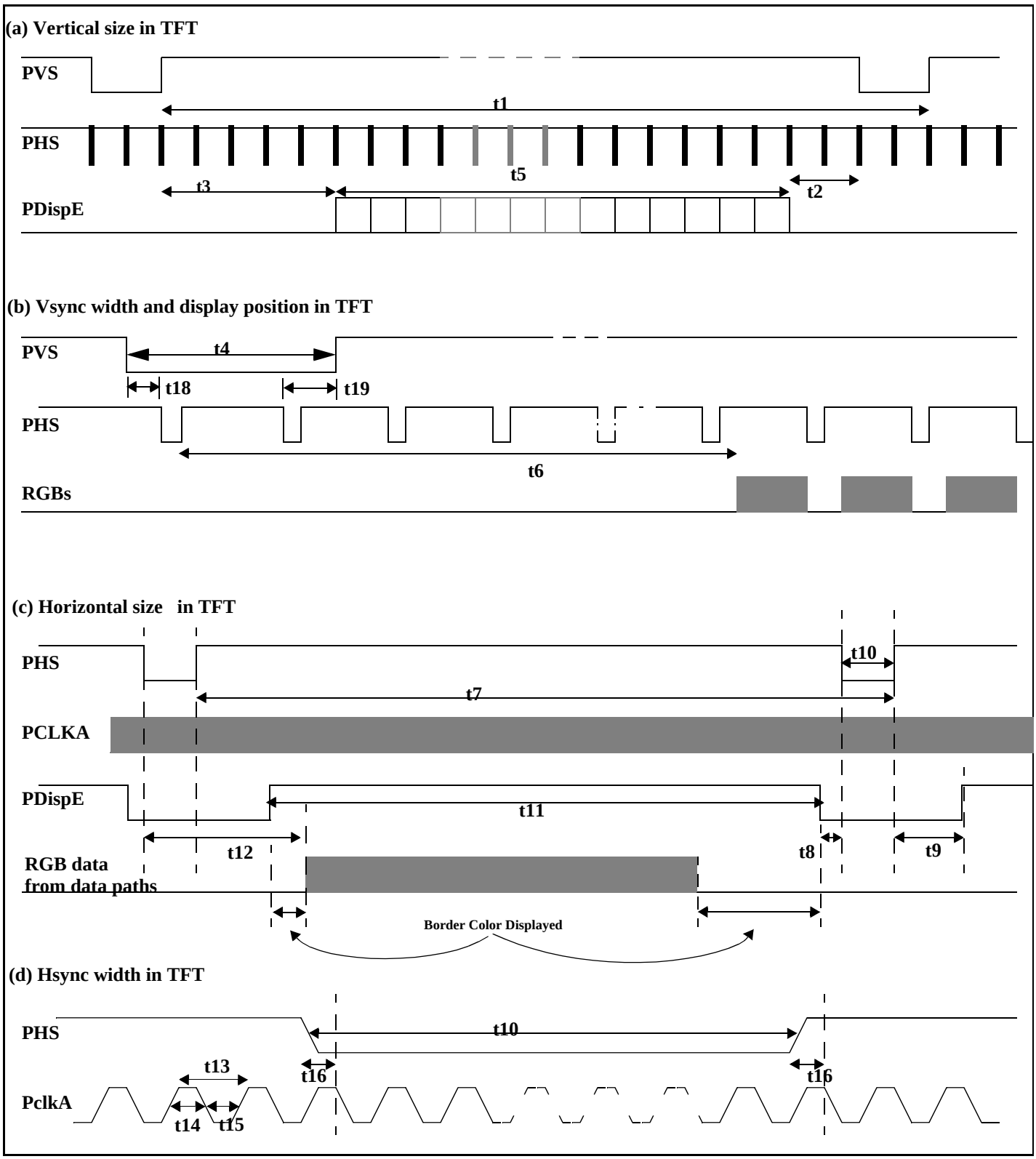
Note that the polarity of the Pclk and its skew are programmable. Clock to Data skew can be adjusted in sixteen 800-ps increments. In combination with the Pclk polarity inversion, the clock-to-data phase can be adjusted in total of 31 steps.

*4: The polarity of the PclkA and the PclkB are independently programmable.

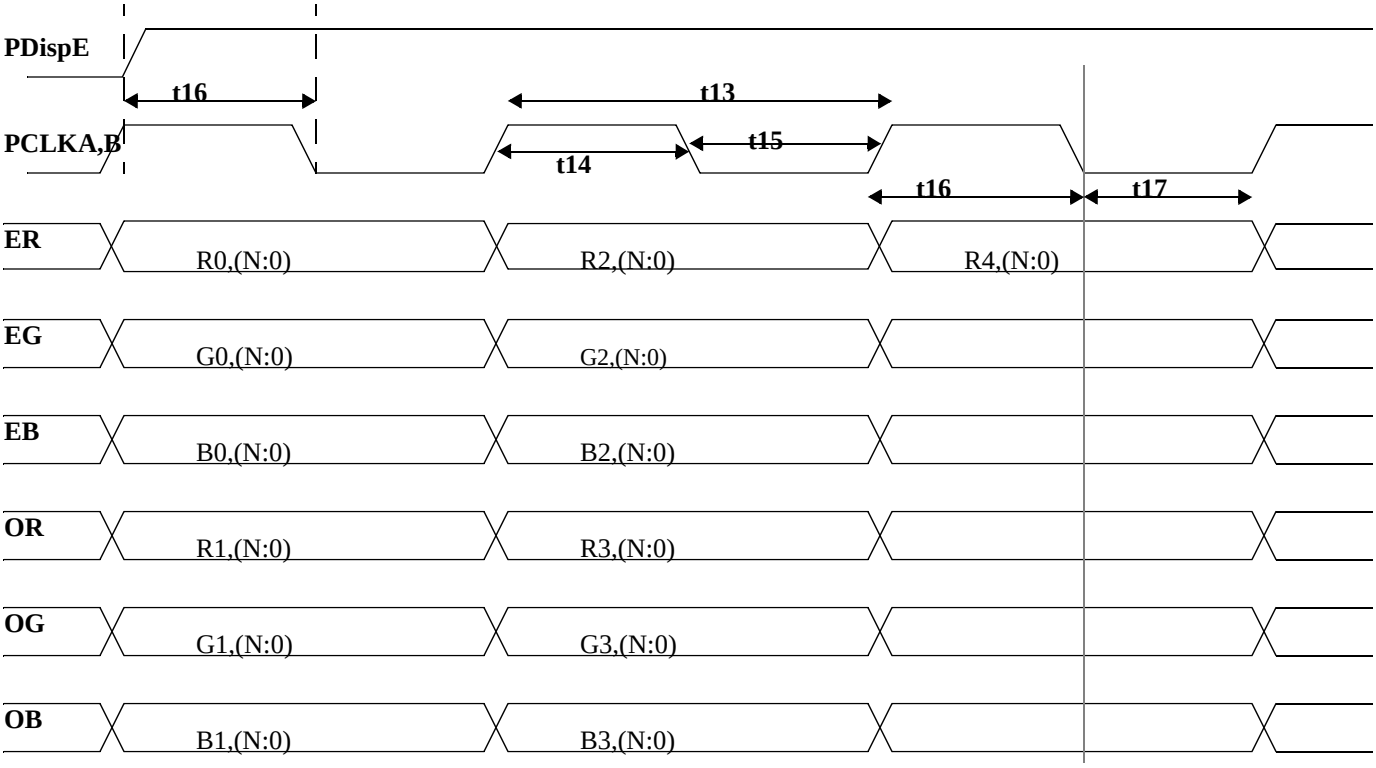
*5: The microcontroller must have all the timing parameters of the panel used for the monitor. The parameters are to be stored in a non-volatile memory. As can be seen from this table, the wide range of timing programmability of the gmB135 panel interface makes it possible to support various kinds of panels known today:

One pixel/clock and two pixels/clock; DE-only type, Sync-only type, and composite type; up to 8 bits/color.

Figure 2.4.1 Timing Diagrams of the TFT Panel Interface (one pixel per clock)



(a) Two pixel per clock mode in TFT



(b) One pixel per clock mode in TFT

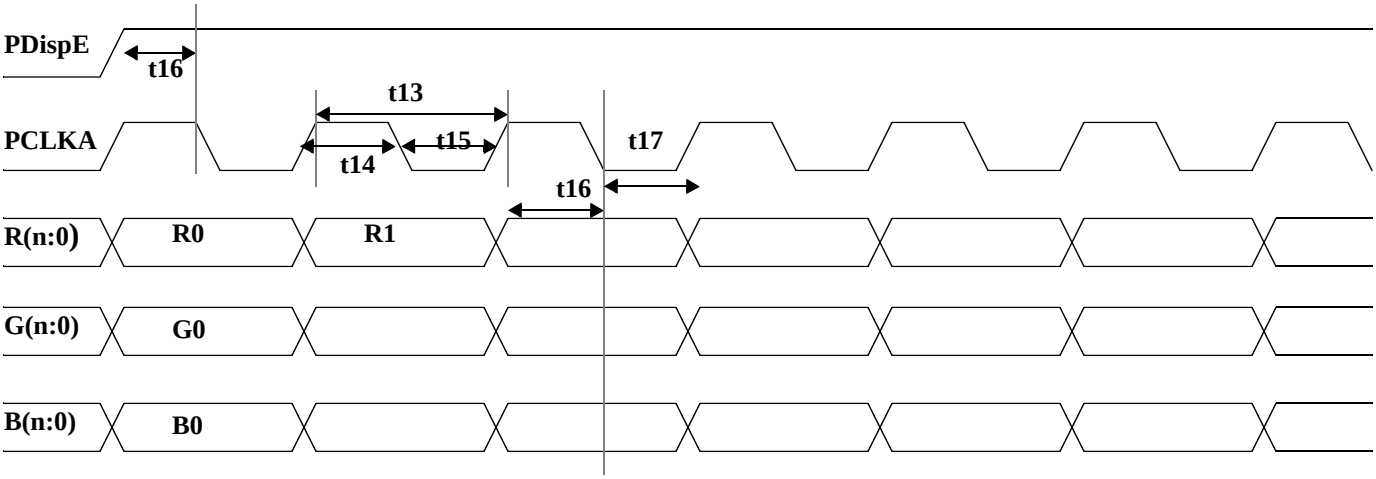


Figure 2.4.2 Data latch timing of the TFT Panel Interface

2.4.2 TFT LCD Power Manager/Sequencer

LCD panels require logic power, panel bias power, and control signals to be sequenced in a specific order. Otherwise, a severe damage may occur and disable the panel permanently.The gmB135 has a built-in power sequencer, the Power Manager that prevents this kind of damage.

The Power Manager controls the power up/down sequences for LCD panels within the four states described below. Also see the timing diagram, Figure 2.4.3.

State 0 (Power Off)

The Pbias signal and the Ppower signal are low (inactive). The panel controls and data are forced low. This state is both the beginning and final state in power sequence.

State 1 (Power On)

Intermediate step 1. The Ppower is high (active), the Pbias is low (inactive), and the panel interface is forced low (inactive).

State 2 (Panel Drive Enabled)

Intermediate step 2. The Ppower is high (active), the Pbias is low (inactive), and the panel control and data signals are active.

State 3 (Panel Fully Active)

Final step in power up sequence with Ppower and Pbias high (active), and the panel interface active. gmB135 power manager is kept in this state until the internal TFT_Enable signal is disabled and State 2 is entered.

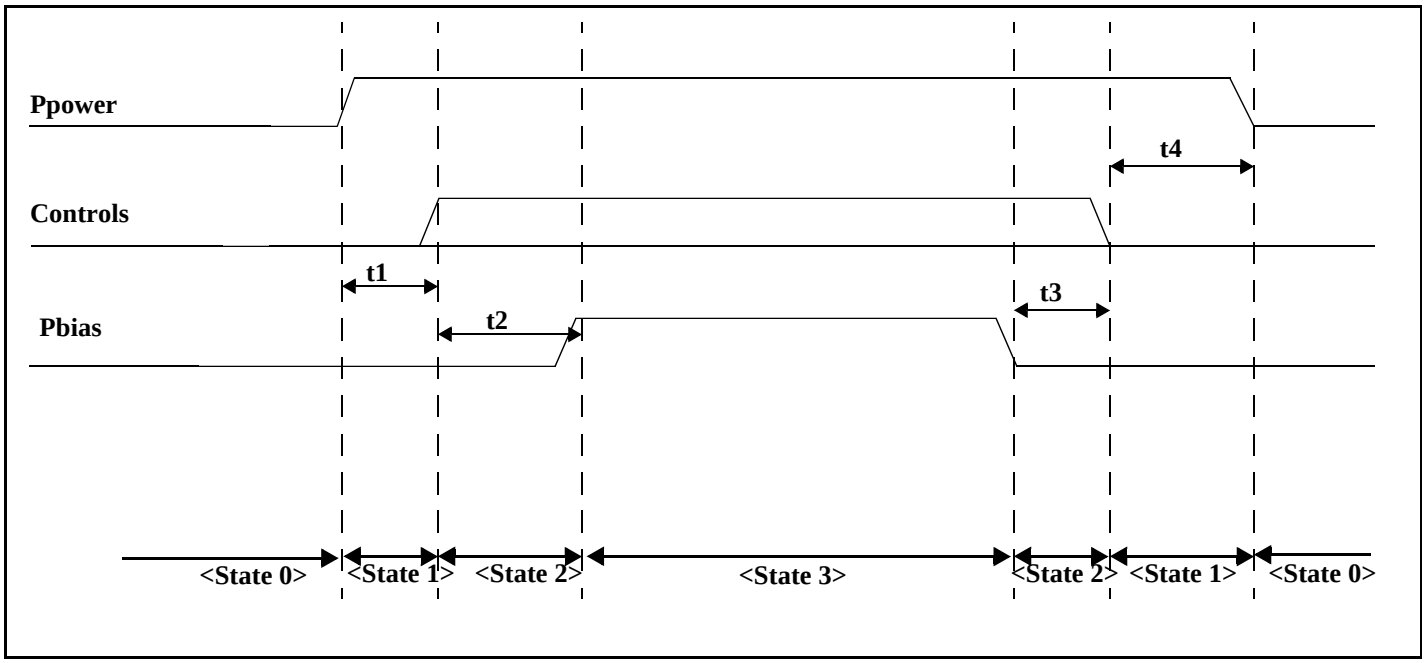


Figure 2.4.3 Panel Power Sequence

The power sequence state can be read in a status register of gmB135.

All of the four timing parameters (t1 ~ t4) in Figure 2.4.3 are independently programmable from one step to eight steps in length.

One-step length is TCLK * 2^{19} or about 10 ms when TCLK is 50 Mhz.

Table 2.4.3 Panel Power Sequence Timing Definition

Timing Symbol	Description
t1	Ppower active to all control signals active
t2	All control signals active to Pbias active
t3	From Pbias inactive to control signals inactive
t4	From control signals inactive to Ppower inactive.

2.4.3 Panel Interface Drive Strength

As mentioned previously, the gmB135 has programmable output pads for the TFT panel interface. Three groups of panel interface pads (panel clock, data, and control) are independently controlled by register programming.

Table 2.4.4 Panel Interface Pad Drive Strength

Value (4 bits)	Drive Strength in mA
0	Outputs are in tri-state condition
1	2 mA
2	4 mA
3, 4	6 mA
5, 8	8 mA
6, 9	10 mA
7, 10	12 mA
11, 12	14 mA
13	16 mA
14	18 mA
15	20 mA

2.5 Host Interface

The host microcontroller interface of the gmB135 has two modes of operation: B120 compatible mode and a 4 bit serial interface mode.

- B120 compatible mode - Four signals consisting of 1 data bit, a frame synchronization signal, a clock signal and a Interrupt Request signal (IRQ). This mode is entered when a pull down resistor is not connected to pin C8 (External OSD Clock).
- 4 bit serial interface mode - Same as B120 compatible mode with the addition of 3 data bits so that 4 data bits are transferred on each clock edge. This mode is entered when a pull down resistor is connected to pin C8 (External OSD Clock).

In both modes, a reset pin sets the chip to a known state when the pin is pulled low.

2.5.1 Host interface pin connection

Table 2.5.1 gmB135 Host Interface

Signal Name (Pin Number)	Description
HFS (C11)	**Host Frame Sync. that enables the serial communication when driven high by the microcontroller. The mgB135 chip has an internal pull-down resistor on chip. Thus, the default state of this signal is low.**
HCLK (C10)	**Serial clock driven by the microcontroller in the write operation. May be connected to an external pull-up resistor.**
HDATA[0](B11) **HDATA[3:0](A10, B10, A11, B11)**	**If 10k pull-down resistor is not connected to pin C8, the bus width is 1 bit.** **If 10k pull-down resistor is connected to pin C8, the bus width is 4 bits.** **Data is driven:** **- by the microcontroller in the write operation,** **- by the gmB135 in the read operation.**
IRQ (C9)	**IRQ pin driven by the gmB135 chip. The polarity is programmable.**
RESETn (A12)	**Sets the chip to a known state when pulled low.**

The gmB135 chip has an on-chip pull-down resistor in the HFS input pad. The signal stays low until driven high by the microcontroller.

As for the RESETn, this signal must be low for at least 100 ns after the CVDD has become stable (between +3.15V and +3.45V) to reset the chip to a known state.

2.5.2 gmB135 Serial Communication Protocol

In the serial communication between the microcontroller and the gmB135, the microcontroller always acts as an initiator while the gmB135 is always the target. The following timing diagram describes the protocol of the serial channel of the gmB135 chip in B120 compatible mode. In 4 bit serial interface mode, 3 clocks instead of 12 clocks are needed to transfer the instruction and data.

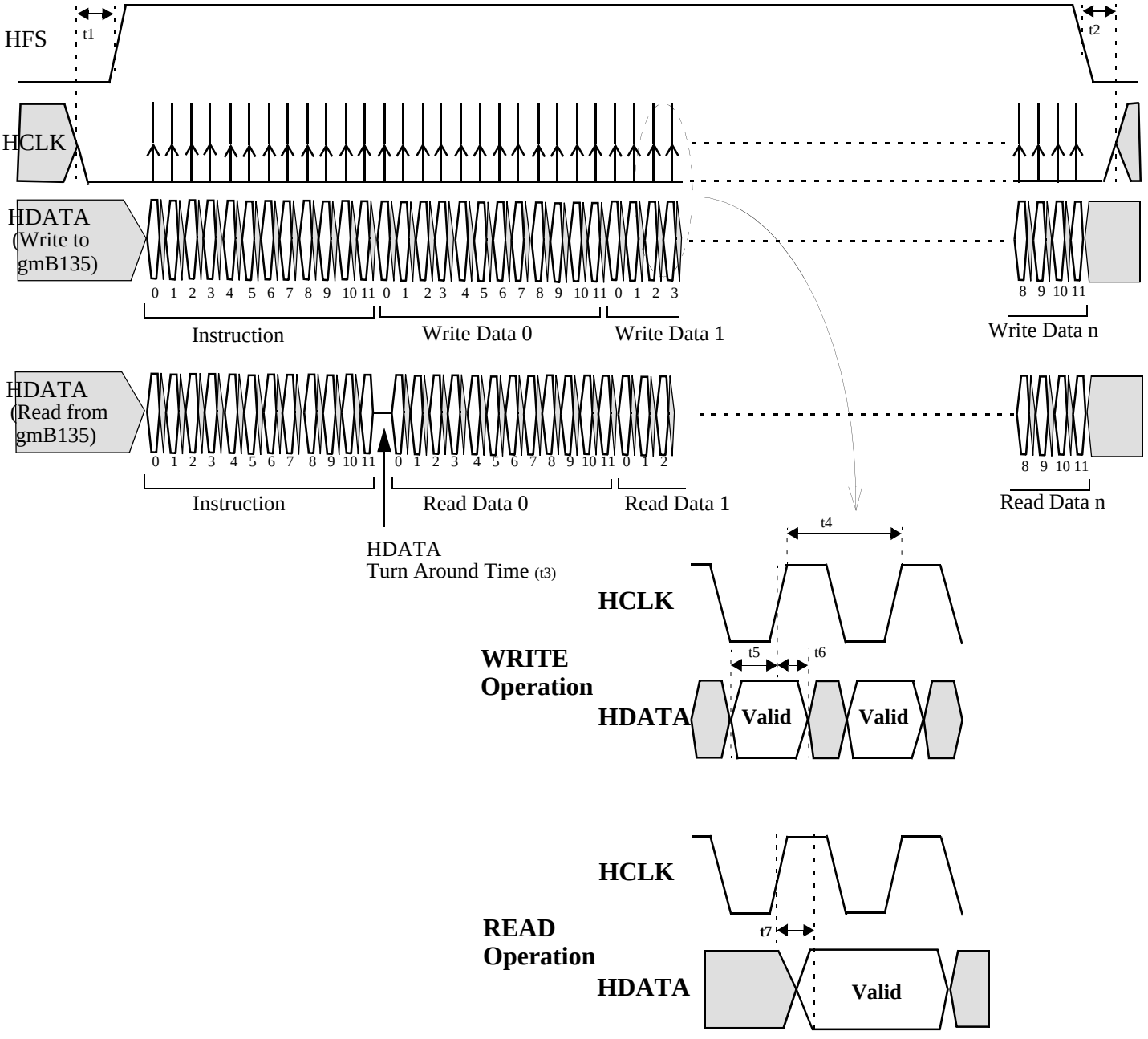


Figure 2.5.1 Timing Diagram of the gmB135 Serial Communication

Table 2.5.2 summarizes the serial channel specification of the gmB135. Refer to Figure 2.5.1 for the timing parameter definition.

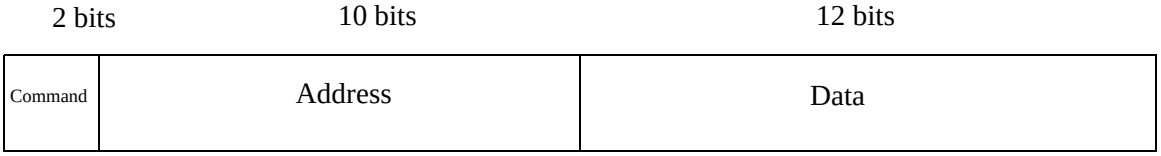
Table 2.5.2 gmB135 Serial Channel Specification

Parameter	min.	typ.	max.
Word Size (Instruction and Data)	---	12 bits	---
HCLK low to HFS high (t1)	100 ns		
HFS low to HCLK inactive (t2)	100 ns		
HDATA Write to Read Turnaround Time (t3)	1 HCLK cycle		1 HCLK cycle
HCLK cycle (t4)	100 ns		
Data in setup time (t5)	25 ns		
Data in hold time (t6)	25 ns		
Data out valid (t7)	5 ns		10

In the B120 compatible mode, during a read operation the microcontroller (Initiator) issues an instruction lasting 12 HCLKs. After the last bit of the command is transferred to the gmB135 on the 12th clock (3rd clock for 4 bit serial mode), the microcontroller must stop driving data before the next rising edge of HCLK at which point the gmB135 will start driving data. At the 13th (4th for 4 bit serial mode) rising edge of HCLK, the gmB135 will begin driving data.

In B120 compatible mode, the data order for address, read data or write data is
- D11 on the first clock
- D0 on the twelfth clock

In 4 bit serial interface mode, the data order for address, read data or write data is
- D[3:0] on the first clock
- D[7:4] on the second clock
- D[11:8] on the third clock



Command: 01 = Write
00 = Read
1x = Reserved

Figure 2.5.2 Serial Host Interface Data Transfer Format

2.6 OSD (On-Screen Display) Control

The gmB135 chip has a built-in OSD (On-Screen Display) controller with an integrated block of font SRAM. The chip also supports an external OSD controller as an option for monitor vendors to maintain a familiar user interface.

2.6.1 On-Chip OSD

Features of the gmB135's on-chip OSD controller include: download-able font SRAM, character blinking, OSD window shadowing, OSD window bordering and background transparency. In addition, the OSD window can be independently pixel or line doubled. There are no built in ROM fonts.

The gmB135's on-chip OSD controller is a download-able font-based graphics controller. All fonts are downloaded from the host microcontroller into the beginning of a 2048 x 12 bit internal SRAM and each font is 12 pixels x 16 lines. This SRAM is also used to store the 12 bit character codes displayed on the screen. The partition is flexible so the character codes can start at any location following the last location font data has been written. As an example, if 104 fonts are down-loaded from the microcontroller, the first 104 x 16 locations of SRAM would be used for font data. That would leave the remaining 384 locations for the character codes.

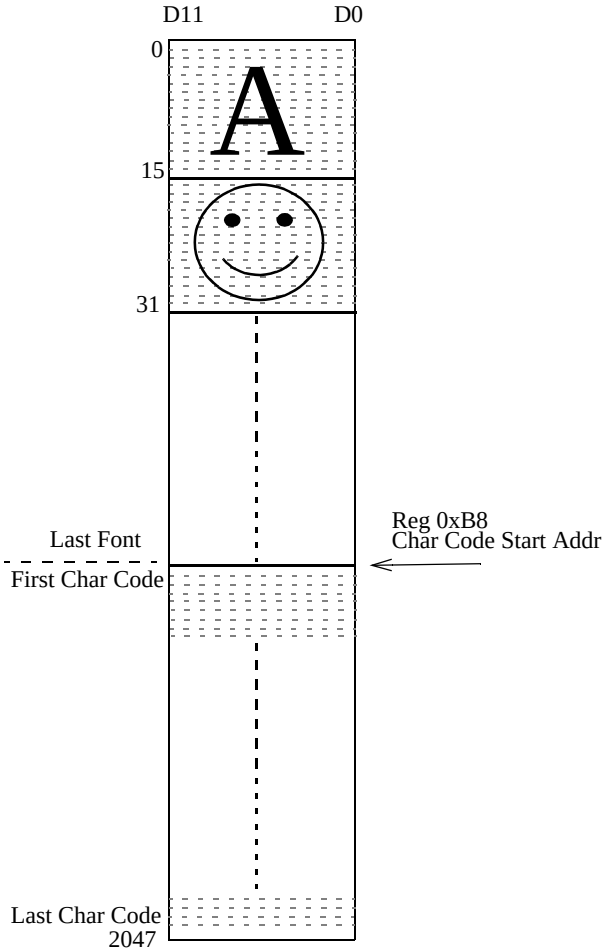


Figure 2.6.1 On-Chip OSD SRAM Map

The on-chip OSD SRAM is contiguously accessed through the 0x100-0x1ff register range of the gmB135. Three bits in the OSD SRAM Segment Select and Character Code Start Address register (0xb8) selects one of 8 segments accessed through the 0x100-0x1ff window. Eight bits in the same register also defines the starting address of the character codes in the OSD SRAM

Table 2.6.1 On-chip Character Code

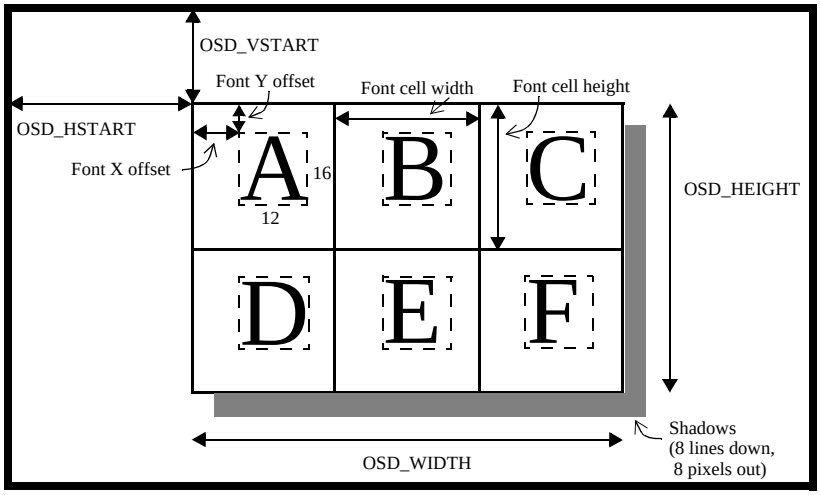
Blink Enable	Foreground Color	Background Color	Font Select
Bit 11 1 = blink 0 = no blink	Bit 10 - Bit 9 00 = fcolor 0 01 = fcolor 1 10 = fcolor 2 11 = fcolor 3	Bit 8 - Bit 7 00 = bcolor 0 01 = bcolor 1 10 = bcolor 2 11 = transparent	Bit 6 - Bit 0 Upper 7 bits of address used to point to font map

The blink rate is based on either a 32 or 64 frame cycle and the duty cycle may be selected as 25/75, 50/50 or 75/25.

The on-chip OSD colors are controlled by the foreground or background color selected. The foreground and background colors are stored in a separate color SRAM but share the same address range 0x100 - 0x110 as the on-chip OSD font SRAM. The color SRAM is selected by setting bit 11 of the OSD SRAM Segment Select and Character Code Start Address register (0xb8) and each location contains 12 bits that define the upper 4 bits of each 8 bit Red, Green and Blue color component. If any of the upper 4 RGB bits are set to 1, then the corresponding lower four RGB bits are all set to 1, otherwise the lower four RGB bits are set to 0.

Table 2.6.2 On-chip OSD Color Control

Offset from 0x100 when 0xb8[11] = 1	Color Selected	Selected by Char code bits
Offset 0x00	Foreground 0 <R7:4><G7:4><B7:4>	Bit 10 - Bit 9
Offset 0x01	Foreground 1 <R7:4><G7:4><B7:4>	Bit 10 - Bit 9
Offset 0x02	Foreground 2 <R7:4><G7:4><B7:4>	Bit 10 - Bit 9
Offset 0x03	Foreground 3 <R7:4><G7:4><B7:4>	Bit 10 - Bit 9
Offset 0x04	Background 0 <R7:4><G7:4><B7:4>	Bit 8 - Bit 7
Offset 0x05	Background 1 <R7:4><G7:4><B7:4>	Bit 8 - Bit 7
Offset 0x06	Background 2 <R7:4><G7:4><B7:4>	Bit 8 - Bit 7
Offset 0x07	Window Border Color <R7:4><G7:4><B7:4>	When OSD border is enabled
Offset 0x8 - 0xf	No function for on-chip OSD. External OSD colors 8-15	



OSD_HSTART: Starting pixel number 0-2047

OSD_VSTART: Starting line number 0-2047

Font X offset: Location of left pixel of font inside char cell 0-63

Font Y offset: Location of top line of font inside char cell 0-63

Font Cell Width: Cell width in pixels 3-66

Font Cell Height: Cell height in lines 2-65

OSD_Width: OSD Window Width in char cells 1-64

OSD_Height: OSD Window Height in char cells 1-64

Figure 2.6.2 On-Chip OSD Window Location

The reference point for the OSD starting position is Panel Display Enable in both the horizontal and vertical directions.

When the OSD window shadow is enabled, a shadow region the same size as the OSD but shifted down and to the right by 8 pixels/lines is shown. The data on the panel will be half intensity in the shadow region. OSD foreground and background colors will always appear on top of the shadow region but the transparent background color will be 'lost' in the shadow since it is also half intensity.

When the OSD window border is enabled, a 1, 2, 4 or 8 pixel/line wide border is drawn around the OSD window. In this case, the OSD vertical and horizontal start positions include the thickness of the border and the actual start of the character display is offset from the start position by the thickness of the border. If the OSD window border is enabled, the OSD window shadow must be disabled. Only one may be selected at a time.

If the Cell Height or Cell Width is larger than the 12 x 16 font, the extra pixels and lines in each cell will display as the background color of that cell's character code. If the Cell Height or Cell Width is smaller than the 12 x 16 font, the cell will clip the right most pixels and the bottom lines of the font.

2.6.2 External OSD Support

The gmB135 supports an external OSD controller for monitor vendors who wish to maintain a specific user interface, or the look and feel. Only those OSD controllers that are developed for a flat-panel monitor application and have a pixel-clock input pin are supported. As is the case with an on-chip OSD, the OSD window size is not affected by the expansion operation.

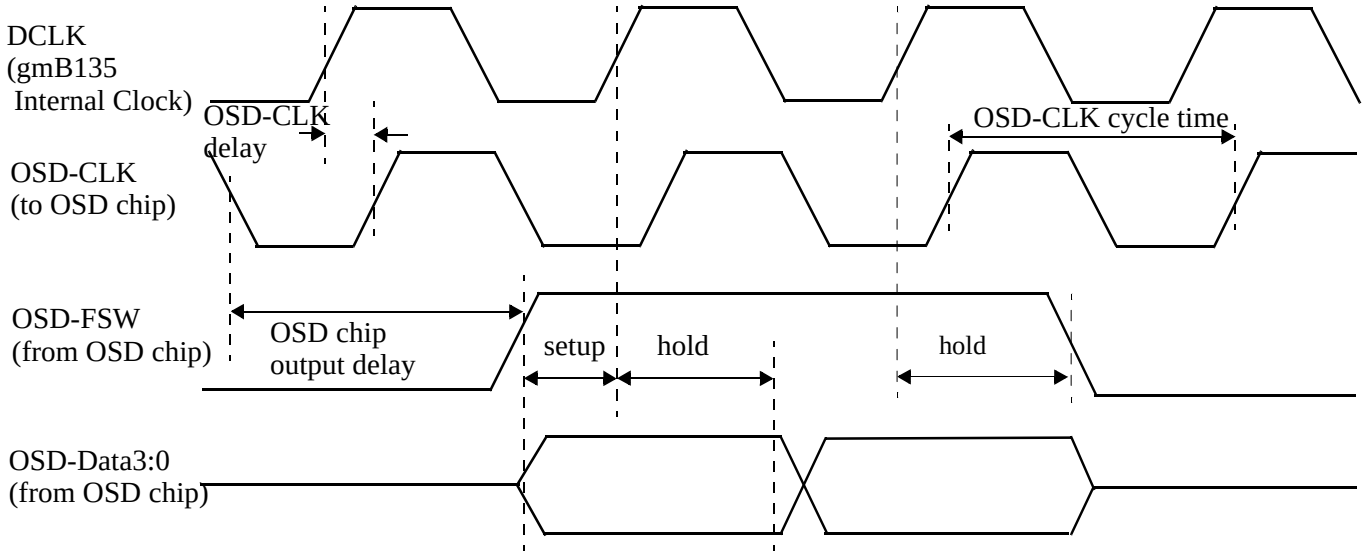
An external OSD controller is connected to the gmB135 chip as shown in Table 2.6.3.

Table 2.6.3 Pin Connection Between the gmB135 and an External OSD controller

gmB135 Pin Name (Pin#, in/out)	External OSD Controller Pin (in/out)	Polarity	Position
OSD-HREF (B9, output)	HSync (input)	Programmable	Relative to left edge of panel. Leading edge of PDispE.
OSD-VREF (A9, output)	VSync (input)	Programmable	Relative to top edge of panel. Leading edge of first PDispE after vertical blanking period.
OSD-CLK (C8, output)	Pixel Clock (input)		
OSD-FSW (C7, input)	OSD Window Indicator (output)	Programmable	Horizontal: M OSD-CLK cycles after the HREF for N pixels. Vertical: M' HREF pulses after the VREF for N' lines (M, N, M',N' programmed to external OSD chip)
OSD-DATA[3:0] (#118~#121, inputs)	Intensity, R, G, and B (outputs)		

The four-bit data from an external OSD controller becomes one of the 16 entries to the OSD look-up table (LUT), which is 12 bits wide and contains the upper four bits (D7:4) of each color component. The lower four bits are determined as follows to make a full 8 bit color value:

D[7:4]	D[3:0]
0000b	0000b
If any bit =1	1111b



OSD-CLK delay = 3 ns default. Additional 0 ~ 8 ns delay can be added.

OSD-FSW/OSD-DATA setup/hold time = 1.5 ns min.

OSD-CLK cycle time = DCLK cycle time = 135 MHz max.

Figure 2.6.4 External OSD Interface Data Latch Timing

When the external OSD controller interface is enabled, the data from the OSD LUT is displayed on a TFT panel instead of captured input data whenever the OSD-FSW signal is active.

The OSD-CLK output to an external OSD controller chip is derived from the DCLK (destination clock) whose clock frequency is the same as the panel clock in frequency (or twice the panel clock frequency on a two-pixels-per-clock panel). The maximum frequency is 135 MHz. The OSD-CLK can be divided down by a factor of 2 or 4 from DCLK which will double or quadruple each OSD pixel on the display.

Both the OSD Data and OSD-FSW signals are latched by gmB135on the rising edge of the DCLK. To maximize the setup/hold time for the OSD-Data and OSD-FSW signal, an internal programmable delay of up to 12 ns in sixteen 800 ps increments is available.

To maximize OSD-HREF setup/hold time to the external OSD controller chip, an internal programmable delay is available to delay OSD-HREF up to 12 ns in sixteen 800 ps increments.

Table 2.6.4 External OSD Interface Timing Parameters

Parameter	minimum	typical	maximum
OSD-CLK Frequency			**135 MHz**
OSD-FSW/OSD-DATA setup time	**1.5 ns**		
OSD-FSW/OSD-DATA hold time	**1.5 ns**		
OSD-CLK delay from DCLK		**0 ~ 12 ns, programmable in 16 800-ps increment**	
OSD-HREF delay from DCLK		**0 ~ 12 ns, programmable in 800-ps increments**	
OSD-CLK/DCLK ratio		**1/4x, 1/2x, 1x, programmable**	

The external-OSD window position is referenced to the edge of the OSD-HREF and OSD-VREF. The horizontal start position is defined in terms of OSD-CLK pulse counts. The vertical position is defined in terms of OSD-HREF pulse counts. These values are programmed into an external OSD controller chip.

2.7 TCLK Input

The source timing is measured by using the TCLK input as a reference. Also, the reference clock to the on-chip PLL's are derived from the TCLK. Thus, it is crucial to have a jitter-free clock as TCLK.

Table 2.7.1 shows the requirements for the TCLK signal.

Table 2.7.1 TCLK Specification

Frequency	**20 MHz ~ 50 MHz**
Jitter	**250 ps maximum**
Rise Time (10% to 90%)	**5 ns**
Duty Cycle	**40-60**

2.8 Power Down Mode

Each functional block of gmB135 can be independently disabled for power saving mode as shown in the following table.

Table 2.8.1 Disabling Functional Blocks of gmB135

Functional Block	Disabled:
Analog input port1	**By a register bit.**
Analog input port2	**By a register bit.**
Digital input port	**By a register bit.**
CCIR601 port	**By a register bit.**
ADC	**By a register bit.**
Sampling Phase Measurement	**By a register bit.**
SCLK DDS	**By a register bit. Disable after ADC is disabled.**
SCLK PLL	**By a register bit.**
DCLK DDS	**By a register bit.**
DCLK PLL	**By a register bit.**
RCLK PLL	**By a register bit. Disable after SCLK and DCLK are disabled.**
Input Gamma LUT	**By a register bit.**
Expansion Engine	**By a register bit.**
Interpolation Engine	**By a register bit.**
Output Gamma LUT	**By a register bit.**
Dithering Engine	**By a register bit.**
Internal OSD	**By a register bit.**
External OSD Interface	**By a register bit.**
Panel Interface	**By a register bit.**
Pattern Generator	**When SCLK is disabled.**
Source Timing Generator	**When SCLK is disabled.**
Host interface	**When TCLK is stopped.**
Source Timing Measurement	**When TCLK is stopped.**
Interrupt Request Controller	**When TCLK is stopped.**

3. Electrical Characteristics

3.1 Absolute Ratings and other Electrical Characteristics

Table 3.1.1. Absolute Ratings

Parameter	Minimum	Typical	Maximum	Note
PVDD			5.6 V	
CVDD			5.6 V	
V_{IN}	V_{SS} - 0.5 V		V_{CC} + 0.5 V	
Operating temperature	0 degreeC		70 degreeC	
Storage temperature	-65 degreeC		150 degreeC	
Maximum power consumption			TBD	

Table 3.1.2. Electrical Characteristics

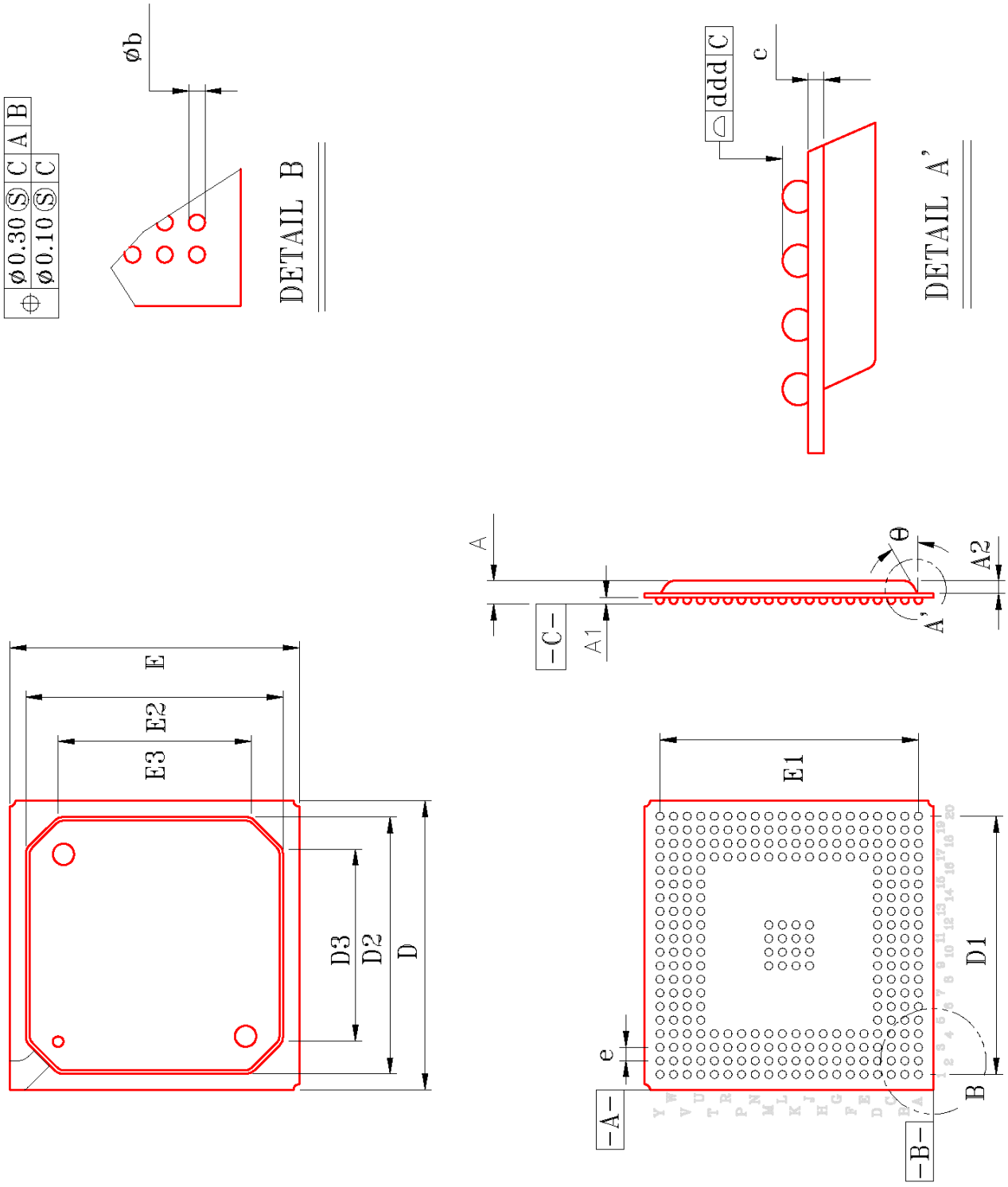
Parameter	Minimum	Typical	Maximum	Note
PVDD	3.15 V	3.3 V	3.47 V	
CVDD	3.15 V	3.3 V	3.47 V	
V_{IL} (CMOS inputs) V_{IL} (TTL inputs)			0.3 * CVDD 0.8 V	
V_{IH} (CMOS inputs) V_{IH} (TTL inputs)	0.7 * CVDD 2.0 V		1.1 * CVDD 5.0 + 0.5 V	(1)
V_{OH}	2.4 V		CVDD	
V_{OL}		0.2 V	0.4 V	
Input current	-10 uA		10 uA	
PVDD operating supply current	0 mA		20 mA/pad @ 10pF	(2)
CVDD operating supply current	0 mA		TBD	(3)

NOTE 1: All input pads except for digital interface pads are 5V-tolerant TTL inputs. For the digital interface, 3.3V input must be fed.

NOTE 2: When the panel interface is disabled, the supply current is 0 mA. The drive current of each pad can be programmed in the range of 2 mA to 20 mA (@capacitive loading of 10 pF).

NOTE 3: When all circuits are powered down and TCLK is stopped, the CVDD supply current becomes 0 mA.

4. Package Dimension



Package Dimension *(Continued)*

Symbol	dimension in mm			dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.20	2.33	2.50	0.087	0.092	0.098
A1	—	0.60	—	—	0.024	—
A2	1.12	1.17	1.22	0.044	0.046	0.048
b	—	0.75	—	—	0.030	—
c	0.51	0.56	0.61	0.020	0.022	0.024
D	26.80	27.00	27.20	1.055	1.063	1.071
D1	—	24.13	—	—	0.950	—
D2	23.80	24.00	24.20	0.937	0.945	0.953
D3	17.95	18.00	18.05	0.707	0.709	0.711
E	26.80	27.00	27.20	1.055	1.063	1.071
E1	—	24.13	—	—	0.950	—
E2	23.80	24.00	24.20	0.937	0.945	0.953
E3	17.95	18.00	18.05	0.707	0.709	0.711
e	—	1.27	—	—	0.050	—
ddd	—	—	0.15	—	—	0.006
θ	30° TYP			30° TYP		