DRAM MODULE

256K x 36 DRAM

FEATURES

- Industry standard pin-out in a 72-pin single-in-line package
- High performance CMOS silicon gate process.
- Single 5V±10% power supply
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- Low power, 100mW standby; 2000mW active, typical
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$, and HIDDEN
- 512 cycle refresh distributed across 8ms
- Optional Page Mode

OPTIONS	MARKING
• Timing	
80ns access	- 8
100ns access	-10
120ns access	-12
• Lead dress	
Tin/Lead	None
Gold (SIMM only)	G
• Packages:	
Leadless 72-pin SIMM	M
Leaded 72-pin ZIP	ZN

GENERAL DESCRIPTION

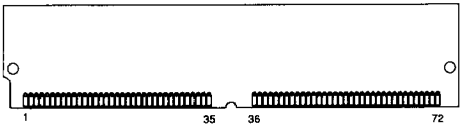
The MT8C36256 is a randomly accessed solid-state memory containing 262,144 words organized in a x36 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. $\overline{\text{RAS}}$ is used to latch the first 9 bits and $\overline{\text{CAS}}$ the latter 9 bits. A READ or WRITE cycle is selected with the $\overline{\text{WE}}$ input. A logic high on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. If $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{\text{CAS}}$ cycle. If $\overline{\text{WE}}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{\text{CAS}}$ remains LOW (regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This late $\overline{\text{WE}}$ pulse results in a READ-WRITE cycle.

Returning $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{\text{RAS}}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{\text{RAS}}$ cycle (READ, WRITE, $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$, or HIDDEN refresh) so that all 512 combinations of $\overline{\text{RAS}}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

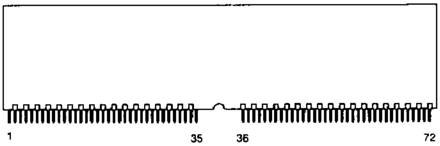
PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The PAGE MODE cycle is always initiated with a row address strobed in by $\overline{\text{RAS}}$ followed by a column address strobed in by $\overline{\text{CAS}}$. By holding $\overline{\text{RAS}}$ LOW, $\overline{\text{CAS}}$ may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{\text{RAS}}$ HIGH terminates the PAGE MODE operation.

PIN ASSIGNMENT (Top View)

72 PIN SIMM (MN)

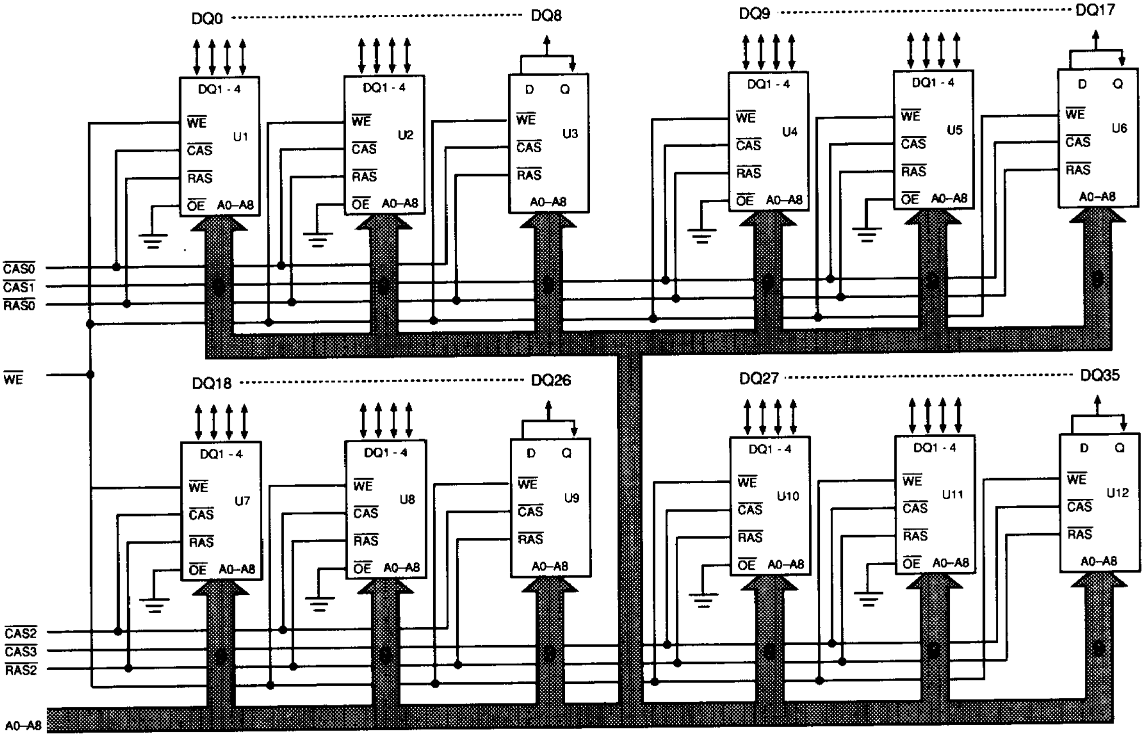


72 PIN ZIP (MP)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	19	NC	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	Vss	57	DQ13
4	DQ1	22	DQ5	40	$\overline{\text{CAS0}}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{\text{CAS2}}$	59	Vcc
6	DQ2	24	DQ6	42	$\overline{\text{CAS3}}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{\text{CAS1}}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{\text{RAS0}}$	62	DQ33
9	DQ21	27	DQ25	45	NC	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{\text{WE}}$	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PRD1
14	A2	32	NC	50	DQ27	68	PRD2
15	A3	33	NC	51	DQ10	69	PRD3
16	A4	34	$\overline{\text{RAS2}}$	52	DQ28	70	PRD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	Vss

FUNCTIONAL BLOCK DIAGRAM



U1, U2, U4, U5, U7, U8, U10, U11 = MT4C4256DJ
U3, U6, U9, U12 = MT1259EJ

TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Addresses			NOTES
				tR	tC		
Standby	H	H	H	X	X	High Impedance	
READ	L	L	H	ROW	COL	Data Out	
WRITE (EARLY-WRITE)	L	L	L	ROW	COL	Data In	
PAGE-MODE READ	L	H→L→H, H→L→H	H	ROW	COL	Valid Data Out, Valid Data Out	
PAGE-MODE WRITE	L	H→L→H, H→L→H	L	ROW	COL	Valid Data In, Valid Data In	
$\overline{RAS}$ ONLY REFRESH	L	H	H	ROW	n/a	High Impedance	
HIDDEN REFRESH	L→H→L	L	H	ROW	COL	Valid Data Out	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH	H→L	L	H	X	X	High Impedance	

PRESENCE DETECT

SYMBOL	-8	-10	-12
PRD1	GND	GND	GND
PRD2	NC	NC	NC
PRD3	GND	GND	NC
PRD4	NC	GND	NC

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss	-1.0V to +7.0V
Operating Temperature, TA(Ambient)	0°C to +70°C
Storage Temperature (Plastic)	-55°C to +150°C
Power Dissipation	12 Watt
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT (any input (0V ≤ V_{IN} ≤ V_{CC}), all other pins not under test = 0 volts) (For each package input)	I_I	-120	120	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ V_{CC}) (For each package input)	I_{OZ}	-120	120	µA	
OUTPUT LEVELS Output High voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	1
Output Low voltage (I_{OUT} = 5mA)	V_{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT ($\overline{RAS}$ and $\overline{CAS}$ = Cycling: t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		720	mA	2
OPERATING CURRENT: PAGE MODE ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = Cycling: t_{PC} = $t_{PC(MIN)}$)	I_{CC2}		720	mA	2
STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} after 8 $\overline{RAS}$ cycles min.)	I_{CC3}		36	mA	
STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V after 8 $\overline{RAS}$ cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V)	I_{CC4}		14	mA	
REFRESH CURRENT: $\overline{RAS}$ ONLY ($\overline{RAS}$ = Cycling: $\overline{CAS}$ = V_{IH})	I_{CC5}		840	mA	2
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ ($\overline{RAS}$ and $\overline{CAS}$ = Cycling)	I_{CC6}		840	mA	2

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		60	pF	18
Input Capacitance: $\overline{WE}$	C_{I2}		84	pF	18
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		42	pF	18
Input Capacitance: $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$	C_{I4}		21	pF	18
Input/Output Capacitance: DQ0 - DQ35	C_{IO}		17	pF	18

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

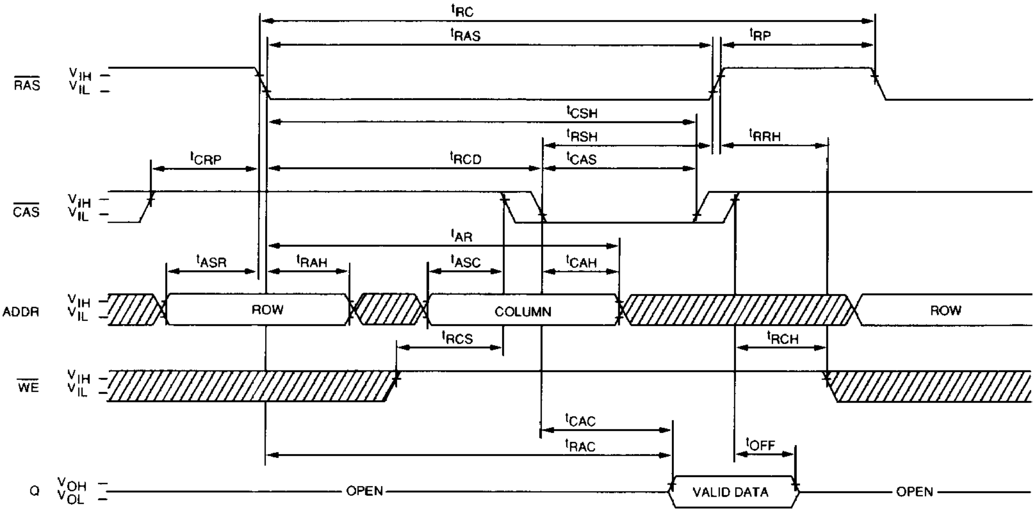
(Notes: 3, 4, 5, 10, 11, 17, 18) (0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ±10%)

A.C. CHARACTERISTICS		-8		-10		-12		-15			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Random READ or WRITE cycle time	^{t}RC	150		190		220		260		ns	6, 7
READ-MODIFY-WRITE cycle time	^{t}RWC	180		220		255		295		ns	
PAGE-MODE cycle time	^{t}PC	75		90		100		120		ns	6, 7
Access time from $\overline{\text{RAS}}$	^{t}RAC		80		100		120		150	ns	7, 8
Access time from $\overline{\text{CAS}}$	^{t}CAC		40		50		60		75	ns	7, 9
$\overline{\text{RAS}}$ pulse width	^{t}RAS	80	10,000	100	10,000	120	10,000	150	10,000	ns	
$\overline{\text{RAS}}$ hold time	^{t}RSH	40		50		60		75		ns	
$\overline{\text{RAS}}$ precharge time	^{t}RP	60		80		90		100		ns	
$\overline{\text{CAS}}$ pulse width	^{t}CAS	40	10,000	50	10,000	60	10,000	75	10,000	ns	
$\overline{\text{CAS}}$ hold time	^{t}CSH	80		100		120		150		ns	
$\overline{\text{CAS}}$ precharge time	^{t}CPN	20		25		25		30		ns	19
$\overline{\text{CAS}}$ precharge time (PAGE-MODE)	^{t}CP	25		30		30		35		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	^{t}RCD	20	40	25	50	25	60	25	75	ns	13
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ set-up time	^{t}CRP	10		15		20		20		ns	
Row address set-up time	^{t}ASR	0		0		0		0		ns	
Row address hold time	^{t}RAH	15		15		15		15		ns	
Column address set-up time	^{t}ASC	0		0		0		0		ns	
Column address hold time	^{t}CAH	15		20		20		25		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	^{t}AR	50		70		80		100		ns	
READ command set-up time	^{t}RCS	0		0		0		0		ns	
READ command hold time referenced to $\overline{\text{CAS}}$	^{t}RCH	0		0		0		0		ns	14
READ command hold time referenced to $\overline{\text{RAS}}$	^{t}RRH	0		0		0		0		ns	
Output buffer turn-off delay	^{t}OFF	0	25	0	30	0	30	0	35	ns	12
$\overline{\text{WE}}$ command set-up time	^{t}WCS	0		0		0		0		ns	16
WRITE command hold time	^{t}WCH	15		35		40		45		ns	
WRITE command hold time referenced to $\overline{\text{RAS}}$	^{t}WCR	35		85		100		120		ns	
WRITE command pulse width	^{t}WP	15		35		40		45		ns	
WRITE command to $\overline{\text{RAS}}$ lead time	^{t}RWL	35		35		40		45		ns	
WRITE command to $\overline{\text{CAS}}$ lead time	^{t}CWL	35		35		40		45		ns	
Data-in set-up time	^{t}DS	0		0		0		0		ns	15
Data-in hold time	^{t}DH	15		35		40		45		ns	15
Data-in hold time referenced to $\overline{\text{RAS}}$	^{t}DHR	35		85		100		120		ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay	^{t}CWD	30		40		50		60		ns	16
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay	^{t}RWD	70		90		110		135		ns	16
Transition time (rise or fall)	^{t}T	3	100	3	100	3	100	3	100	ns	5, 17
Refresh Period (256 cycles)	^{t}REF		4		4		4		4	ms	21
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh)	^{t}CHR	15		20		25		30		ns	20
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$) refresh	^{t}CSR	10		15		20		20		ns	20
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	^{t}RPC	0		0		0		0		ns	20

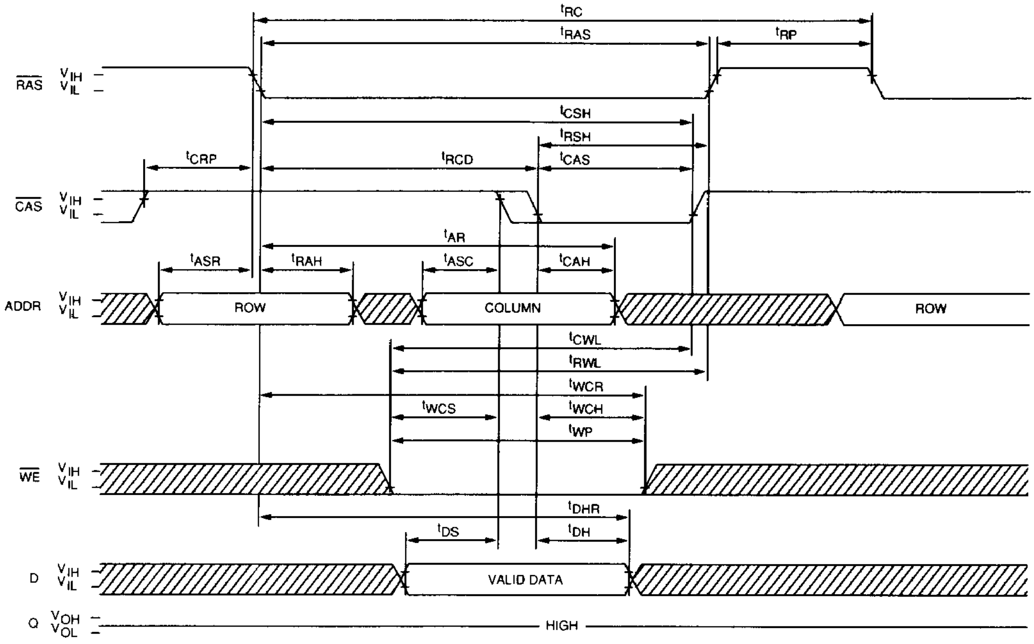
NOTES

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of 100µs is required after power-up followed by any 8 $\overline{\text{RAS}}$ cycles before proper device operation is assured. The 8 $\overline{\text{RAS}}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 5ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. Measured with a load equivalent to 2 TTL gates and 100pF.
8. Assumes that ^{t}RCD < ^{t}RCD (max). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
9. Assumes that ^{t}RCD ≥ ^{t}RCD (max).
10. If $\overline{\text{CAS}}$ = V_{IH}, data output is high impedance.
11. If $\overline{\text{CAS}}$ = V_{IL}, data output may contain data from the last valid READ cycle.
12. ^{t}OFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
13. Operation within the ^{t}RCD (max) limit ensures that ^{t}RAC (max) can be met. ^{t}RCD (max) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (max) limit, then access time is controlled exclusively by ^{t}CAC.
14. ^{t}RCH is referenced to the first rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$.
15. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early WRITE cycles and to the $\overline{\text{WE}}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.
16. ^{t}WCS, ^{t}CWD and ^{t}RWD are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If ^{t}WCS ≥ ^{t}WCS (min), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}CWD ≥ ^{t}CWD (min) and ^{t}RWD ≥ ^{t}RWD (min), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until $\overline{\text{CAS}}$ goes back to V_{IH}) is indeterminate.
17. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
18. Capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3V and V_{CC} = 5V. This parameter is sampled.
19. If $\overline{\text{CAS}}$ is LOW at the falling edge of $\overline{\text{RAS}}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{\text{CAS}}$ must be pulsed HIGH for ^{t}CP. Note 8 applies to determine valid data out.
20. On-chip refresh and address counters are enabled.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{\text{WE}}$ = LOW.

READ CYCLE



EARLY-WRITE CYCLE

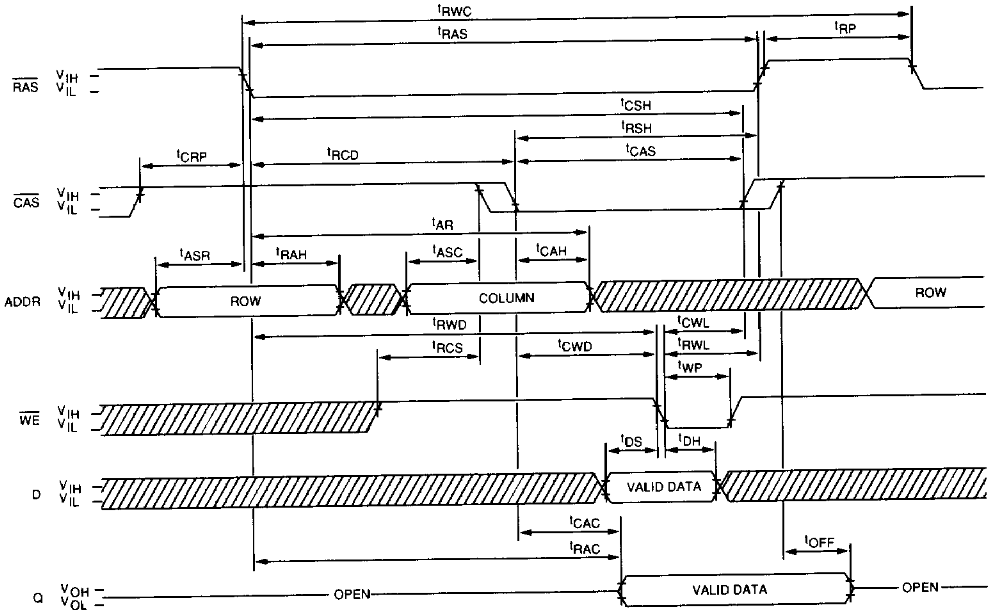


▨ DON'T CARE

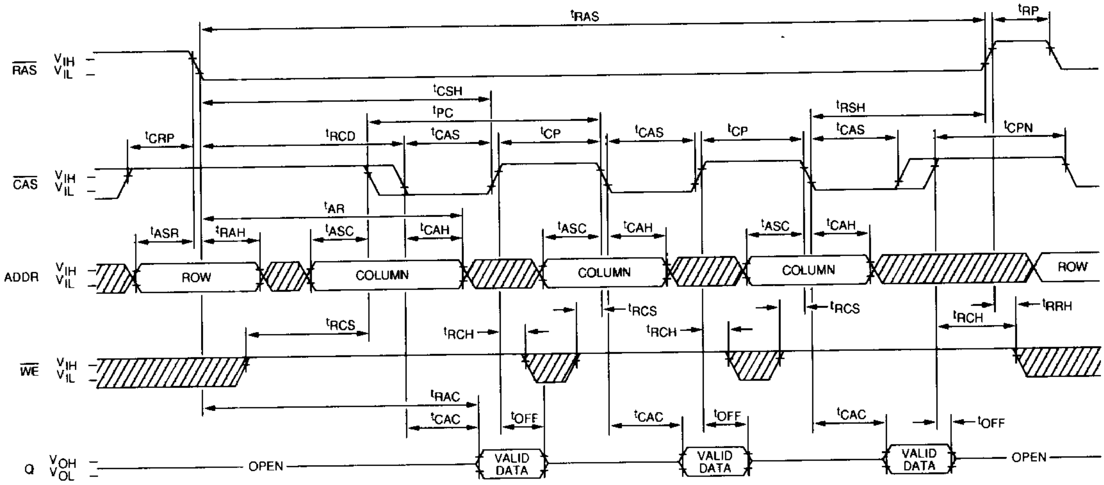
▩ UNDEFINED

READ-WRITE CYCLE

(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



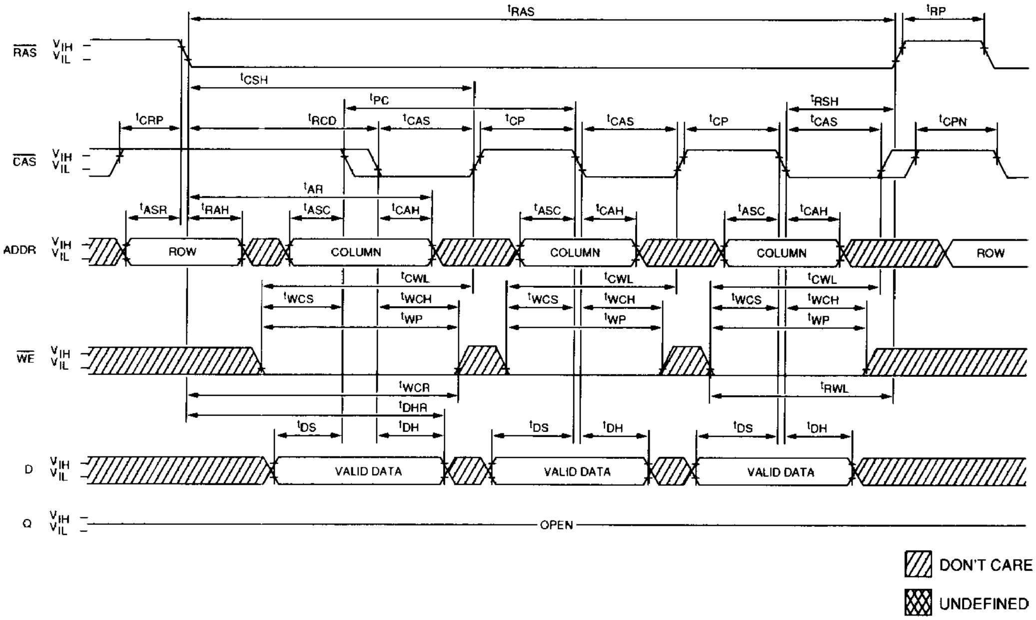
PAGE-MODE READ CYCLE



▨ DON'T CARE

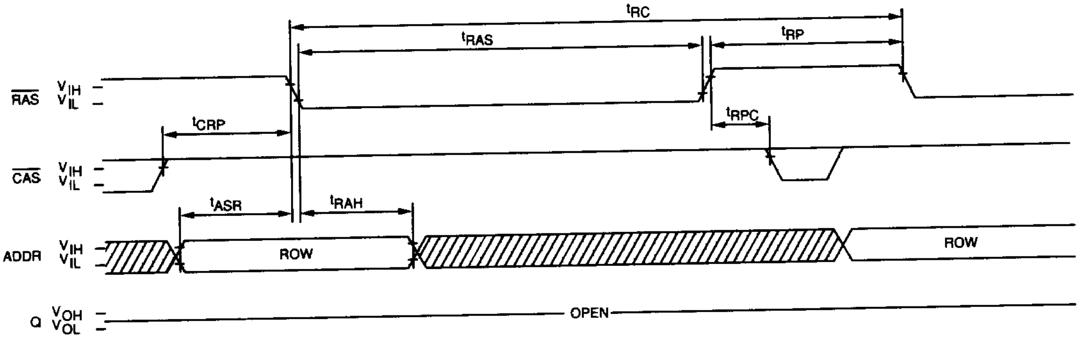
▩ UNDEFINED

PAGE-MODE EARLY-WRITE CYCLE



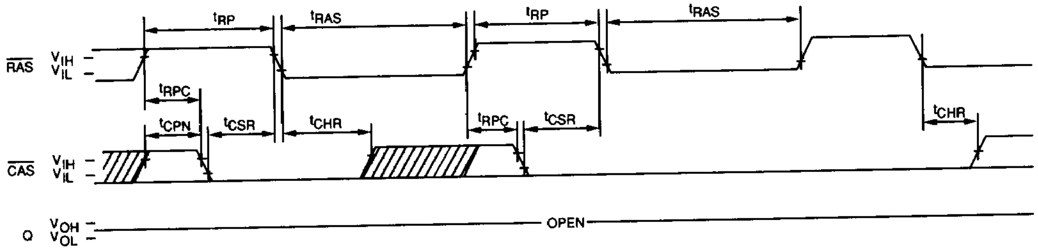
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

(ADDR = A_0 - A_7; A_8 and $\overline{\text{WE}}$ = DON'T CARE.)



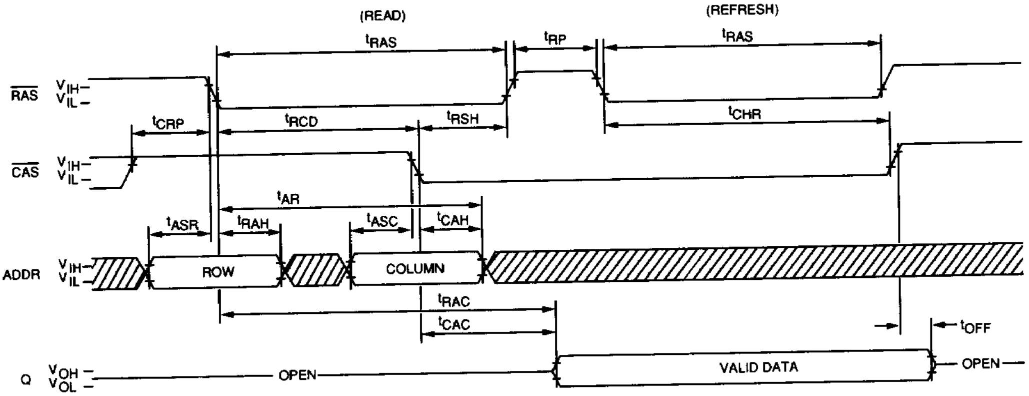
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE

(A_0 - A_8 and $\overline{\text{WE}}$ = DON'T CARE.)



HIDDEN REFRESH CYCLE

($\overline{\text{WE}}$ = HIGH)[21]



▨ DON'T CARE

▩ UNDEFINED