

9240LP Block Diagram

FEATURES:

- RAD-PAK® radiation-hardened against natural space radiation
- Low power dissipation: 285 mW
- Single 5 V supply
- Integral nonlinearity error: 2.5 LSB
- Differential nonlinearity error: 0.6 LSB
- Input referred noise: 0.36 LSB
- Complete: On-chip sample-and-hold amplifier and voltage reference
- Signal-to-noise and distortion ratio: 77.5 dB
- Spurious-free dynamic range: 90 dB
- Out-of-range indicator
- Straight binary output data
- Total dose hardened to 100 krad (Si), dependent on orbit and mission duration
- Single Event Latchup (SEL) protected

DESCRIPTION:

DDC's 9240LP is a 14-bit analog to digital converter that operates at a 10 MSPS rate. Manufactured with a high speed CMOS process, this A/D, with latch-up protection, contains an on-chip, high performance, low noise, sample-and-hold amplifier and a programmable voltage reference.

The 9240LP offers single supply operation and dissipates only 480 mW with a 5 volt supply. This device provides no missing codes and excellent temperature drift performance over the full operating temperature range.

The 9240LP utilizes DDC's LPT™ Latchup Protection Circuit.

DDC's patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK® provides protection to 100 krad (Si) radiation dose tolerance. This product is available with screening up to DDC's self-defined Class K flow.



DQS Inc.
DATA DEVICE CORPORATION
REGISTERED TO:
AS9100:2016, ISO9001:2015
FILE NO. 10001296

TABLE 1. 9240LP PIN DESCRIPTION

PIN NUMBER	NAME	DESCRIPTION
1	DVSS	Digital Ground
2, 29	AVSS	Analog Ground
3	DVDD	5V Digital Supply
4, 28	AVDD	5V Analog Supply
5	NC	No Connect
6	DVDD	5V Digital Supply
7	CLK	Clock Input Pin
8	LPTSTATUS	A 0 to 5V square-wave is output during the decision time and protect time. Normally low.
9	LPTBIT	The LPT circuit will crowbar the power supplies to the 9240 for as long as a logic high is applied. Used to verify operation of the LPT. Normally a logical low or ground is applied to this input.
10	NC	No Connect
11	BIT 14	Least Significant Data Bit (LSB)
12-23	BIT 13-BIT 2	Data Output Bits
24	BIT 1	Most Significant Data Bits (MSB)
25	OTR	Out of Range
26, 27, 30	NC	No Connect
31	SENSE	Reference Select
32	VREF	Reference I/O
33	REFCOM	Reference Common
34, 38	DNC	Do Not Connect
35	BIAS ¹	Power/Speed Programming
36	CAPB	Noise Reduction Pin
37	CAPT	Noise Reduction Pin
39	CML	Common-Mod Level (Midsupply)
40	LPTVREF	Protected Reference I/O
41	VINA	Analog Input Pin (+)
42	VINB	Analog Input Pin (-)
43	LPTDVDD	Protected 5V Digital Supply
44	LPTAVDD	Protected 5V Analog Supply

1. See Speed/Power programmability section.

TABLE 2. 9240LP ABSOLUTE MAXIMUM RATINGS ¹

PARAMETER	SYMBOL	WITH RESPECT TO	MIN	TYP	MAX	UNIT
AVDD		AVSS	-0.3		6.5	V
DVDD		DVSS	-0.3		6.5	V
AVSS		DVSS	-0.3		0.3	V
AVDD		DVDD	-6.5		6.5	V
DRVSS		AVSS	-0.3		0.3	V
REFCOM		AVSS	-0.3		0.3	V
CLK		AVSS	0		AVDD -0.5	V
Digital Outputs		DRVSS	-0.3		DVDD + 0.3	V
VINA, VINB		AVSS	-0.3		AVDD + 0.3	V
VREF		AVSS	-0.3		AVDD + 0.3	V
SENSE		AVSS	-0.3		AVDD + 0.3	V
CAPB, CAPT		AVSS	-0.3		AVDD + 0.3	V
BIAS		AVSS	-0.3		AVDD + -.3	V
Junction Temperature	T _J		--		150	°C
Operating Temperature	T _A		-55		125	°C
Package Weight			--	10.5	--	Grams
Thermal Resistance	T _{JC}		--	9.6	--	°C/W
Storage Temperature	T _{STG}		-65		150	°C
Lead Temperature (10 sec)	T _L		--		300	°C

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

TABLE 3. DELTA PARAMETERS

PARAMETERS	VARIATION
IDVDD	+/- 10 %
IADVD	+/- 10%

1. Parameters are measured and recorded as Deltas per MIL-STD-883 for Class K devices. Specified in Table 4.

TABLE 4. 9240LP DC SPECIFICATIONS

(AVDD = 5V, DVDD = 5V, R_{BIAS} = 2k Ω , V_{REF} = 2.5V,
 V_{IN}A=V_{IN}B = \pm 2.5V DIFFERENTIAL INPUT CENTERED ON V_{REF}(1.25V TO 3.75V ABSOLUTE)
 T_A = -55 TO +125°C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SUBGROUPS	MIN	TYP ¹	MAX	UNIT
RESOLUTION	1	14	--	--	Bits min
MAX CONVERSION RATE	9, 10, 11	10	--	--	MHz min
MAX REFERRED NOISE ¹					LSB rms
V _{REF} = 1 V		--	0.9	--	
V _{REF} = 2.5V		--	0.36	--	
ACCURACY ²					
Integral Nonlinearity (INL)	1, 2, 3	-3	\pm 2.5	3	LSB
Differential Nonlinearity (DNL)	1, 2, 3	-1	\pm 0.6	1.0	LSB
INL ³		--	\pm 2.5	--	LSB
DNL ³		--	\pm 0.7	--	LSB
No Missing Codes	1	--	--	14	Bits Guaranteed
Zero Error (@ 25 °C)	1	-0.3	--	0.3	% FSR
Gain Error (@ 25 °C) ^{1,4}		-1.5	--	1.5	% FSR
Gain Error (@ 25 °C) ⁵	1	-0.75	--	0.75	% FSR
TEMPERATURE DRIFT	1, 2, 3				
Zero Error		--	3.0	--	ppm/°C
Gain Error ⁴		--	20.0	--	ppm/°C
Gain Error ⁵		--	5.0	--	ppm/°C
POWER SUPPLY REJECTION	1, 2, 3	--	--	0.1	% FSR
ANALOG INPUT ¹					
Input Span (with V _{REF} = 1.0 V)		2	--	--	V p-p
(with V _{REF} = 2.5 V)	1, 2, 3	--	--	5	V p-p
Input (V _{IN} A OR V _{IN} B) Range		0	--	AVDD + .25	V
Input Capacitance		--	16	--	pF
INTERNAL VOLTAGE REFERENCE ¹					
Output Voltage (1V mode)		--	1	--	V
Output Voltage Tolerance (1 V Mode)		--	--	\pm 14	mV
Output Voltage (2.5 V Mode)		--	2.5	--	V
Output Voltage Tolerance (2.5 V Mode)		--	--	\pm 35	mV
Load Regulation V _{REF}		--	10	--	mV
Load Regulation LPTV _{REF} ^{6,7}		--	--	10.0	mV

TABLE 4. 9240LP DC SPECIFICATIONS

(AVDD = 5V, DVDD = 5V, R_{BIAS} = 2k Ω , V_{REF} = 2.5V,
 V_{IN A}=V_{IN B} = $\pm 2.5V$ DIFFERENTIAL INPUT CENTERED ON V_{REF}(1.25V TO 3.75V ABSOLUTE)
 T_A = -55 TO +125°C, UNLESS OTHERWISE SPECIFIED) (continued)

PARAMETER	SUBGROUPS	MIN	TYP ¹	MAX	UNIT
LPT ASIC	1, 2, 3				
INPUT RESISTANCE (RDS ON)					
- V _{REF}			8	15	Ω
- AVDD			8		Ω
- DVDD			8		Ω
- V _{IN A}			105		Ω
- V _{IN B}			105		Ω
LATCHUP PROTECTION					
- Decision Time			10		μs
- Protect Time			70		μs
- AVDD Trip Current			85		mA
- AVDD Trip Current Tolerance			± 15		mA
- DVDD Trip Current			28		mA
- DVDD Trip Current Tolerance			± 5		mA
POWER SUPPLIES					
Supply Voltages					
- AVDD		--	5	5	V ($\pm 5\%$ AVDD Operating)
- DVDD		--	5	5	V ($\pm 5\%$ DVDD Operating)
Supply Current		--			
- I _{AVDD}	1, 2, 3	--	43	55	mA
- I _{DVDD}	1, 2, 3	--	3	19	mA
POWER CONSUMPTION ⁸			295	355	mW

1. Guaranteed by design
2. Tested using external V_{REF} with servo control
3. V_{REF} = 1V
4. Including internal reference
5. Excluding internal reference
6. Load regulation with 1 mA load current
7. LPTV_{REF} should not be capacitively loaded above 0.1 μF
8. Calculated from I_{DD}

TABLE 5. 9240LP AC SPECIFICATIONS

(AVDD = 5V, DVDD = 5V, f_{SAMPLE} = 10MSPS, BIAS = 2kΩ, V_{REF} = 2.5V,
V_{INA} = -0.5dBFS, AC COUPLED/DIFFERENTIAL INPUT, T_A = -55 TO +125°C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SUBGROUPS	MIN	TYP ¹	MAX	UNIT
SIGNAL-TO-NOISE AND DISTORTION RATIO (S/N+D)					
f _{INPUT} = 500 kHz		--	76.0	--	dB
f _{INPUT} = 1.0 MHz		--	76.0	--	dB
f _{INPUT} = 5.0 MHz		--	75.5	--	dB
EFFECTIVE NUMBER OF BITS (ENOB) ²					
f _{INPUT} = 500 kHz		12	--	--	Bits
f _{INPUT} = 1.0 MHz		--	12.3	--	Bits
f _{INPUT} = 5.0 MHz		--	11.9	--	Bits
SIGNAL-TO-NOISE RATION (SNR) ²	4, 5, 6				
f _{INPUT} = 500 kHz		74.5	77	--	dB
f _{INPUT} = 1.0 MHz		--	77	--	dB
f _{INPUT} = 5.0 MHz		--	77	--	dB
TOTAL HARMONIC DISTORTION (THD)					
f _{INPUT} = 500 kHz		--	-76.0	--	dB
f _{INPUT} = 1.0 MHz		--	-83.0	--	dB
f _{INPUT} = 5.0 MHz		--	-75.0	--	dB
SPURIOUS FREE DYNAMIC RANGE	4, 5, 6				
f _{INPUT} = 500 kHz		--	90.0	--	dB
f _{INPUT} = 1.0 MHz		--	90.0	--	dB
f _{INPUT} = 5.0 MHz		--	80.0	--	dB
DYNAMIC PERFORMANCE ¹					
Full Power Bandwidth		--	70	--	MHz
Small Signal Bandwidth		--	70	--	MHz
Aperture Delay		--	1	--	ns
Aperture Jitter		--	4	--	ps rms
Acquisition to Full-Scale Step (0.0025%)		--	45	--	ns
Overvoltage Recovery Time		--	167	--	ns

1. Guaranteed by design

2. Not tested

TABLE 6. 9240LP DIGITAL SPECIFICATIONS

(AVDD = 5V, DVDD = 5V, T_A = -55 TO +125°C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SUBGROUPS	SYMBOL	MIN	TYP	MAX	UNIT
CLOCK INPUT ¹	1, 2, 3					
High Level Input Voltage ²		V _{IH}	3.5		--	V
Low Level Input Voltage		V _{IL}	--		1.0	V
High Level Input Current (V _{IN} = DVDD)		I _{IH}	--		±10	μA
Low Level Input Current (V _{IN} = 0V)		I _{IL}	--		±10	μA
Input Capacitance		C _{IN}	--	5	--	pF

TABLE 6. 9240LP DIGITAL SPECIFICATIONS
(AVDD = 5V, DVDD = 5V, T_A = -55 TO +125°C, UNLESS OTHERWISE SPECIFIED)

PARAMETER	SUBGROUPS	SYMBOL	MIN	TYP	MAX	UNIT
LOGIC OUTPUTS (with DRVDD = 5V)	1, 2, 3					
High Level Output Voltage (I _{OH} = 50 μA)		V _{OH}			4.5	V min
High Level Output Voltage (I _{OH} = 0.5 mA)		V _{OH}			2.4	V min
Low Level Output Voltage (I _{OL} = 1.6 mA)		V _{OL}			0.4	V max
Low Level Output Voltage (I _{OL} = 50 μA)		V _{OL}			0.1	V max
Output Capacitance		C _{OUT}			5	pF typ

1. Due to the voltage drop across the LPT circuitry the CLOCK signal must be no greater than AVDD - 0.5V
2. Guaranteed by design

TABLE 7. 9240LP SWITCHING CHARACTERISTICS¹
(T_A = -55 TO +125°C WITH AVDD = 5V, DVDD = 5V, R_{BIAS} = 2 kW, C_L = 20 pF)

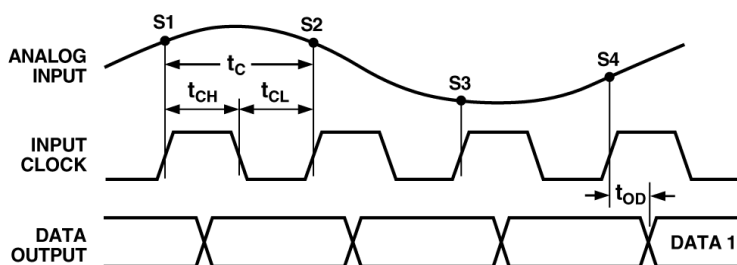
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Clock Period	t _C	100	--	--	ns
CLOCK Pulse width High	t _{CH}	45	--	--	ns
CLOCK Pulse width Low	t _{CL}	45	--	--	ns
Output Delay	t _{OD}	8	--	--	ns
		--	13	--	ns
		--	--	19	ns
Pipeline Delay (Latency)		--	--	--	Clock Cycles

1. Guaranteed by design

TYPICAL DIFFERENTIAL CHARACTERIZATION CURVES/PLOTS

(AVDD = 5V, DVDD = 5V, DRVDD = 5V, f_{SAMPLE} = 10 MSPS, R_{BIAS} = 2 kW, T_A = 25 °C, DIFFERENTIAL INPUT)

FIGURE 1. TIMING DIAGRAM



RECOMMENDED EXTERNAL REFERENCE

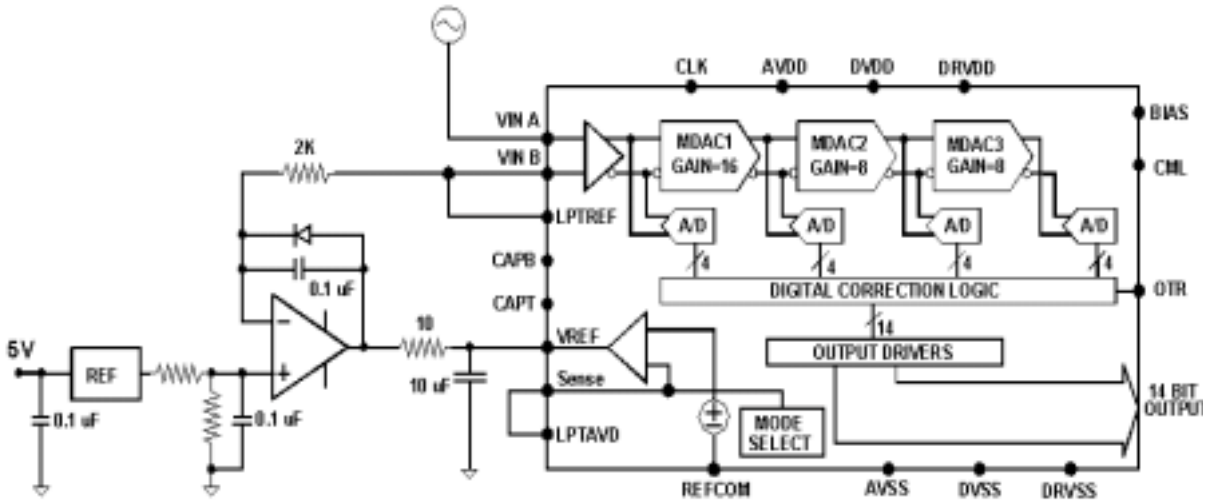


FIGURE 2. SINAD vs. INPUT FREQUENCY (INPUT SPACE = 2V, VCM = 2.5V)

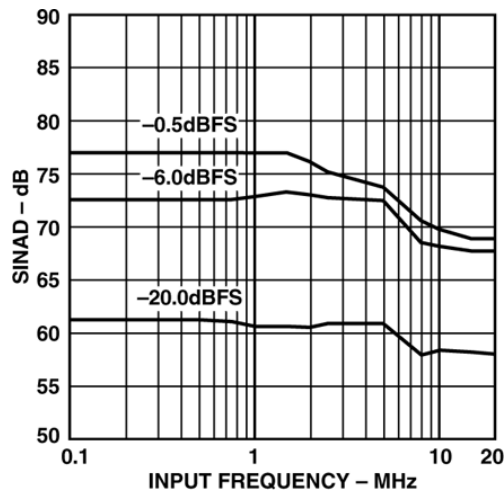


FIGURE 3. THD vs. INPUT FREQUENCY (INPUT SPAN = 5V, VCM = 2.5V)

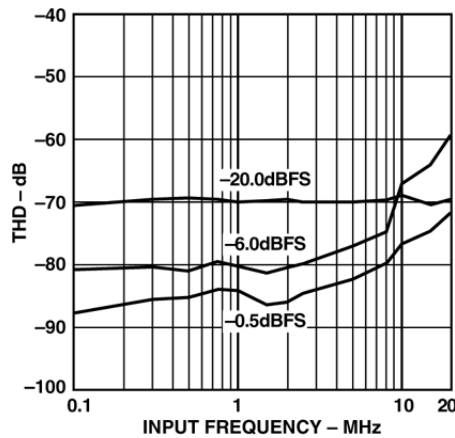


FIGURE 4. TYPICAL FFT, $f_{IN} = 1.0 \text{ MHz}$ (INPUT SPACE = 5V, $V_{CM} = 2.5V$)

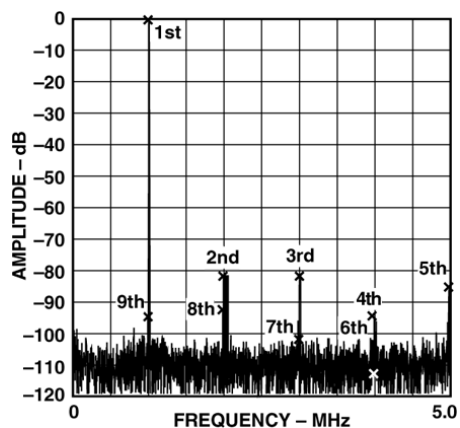


FIGURE 5. SINAD VS. INPUT FREQUENCY (INPUT SPAN = 2V, $V_{CM} = 2.5V$)

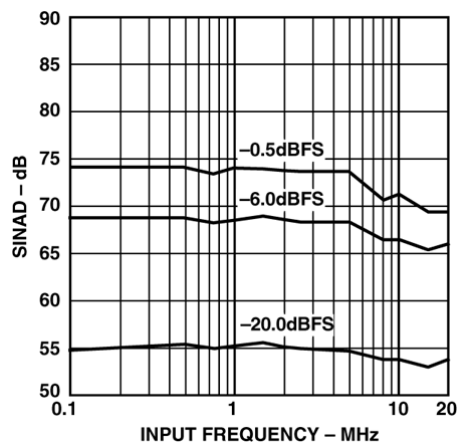


FIGURE 6. THD VS. INPUT FREQUENCY (INPUT SPAN = 2V, $V_{CM} = 2.5V$)

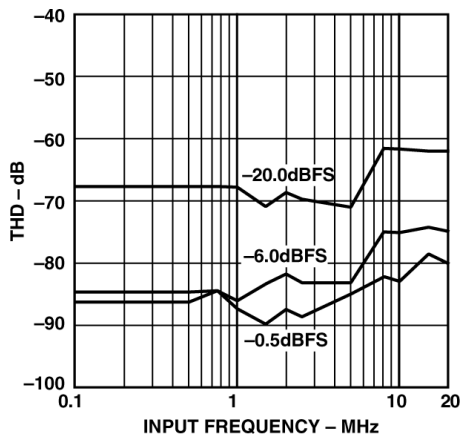


FIGURE 7. TYPICAL FFT, $f_{IN} = 5.0$ MHz (INPUT SPAN = 2 V, $V_{CM} = 2.5$ V)

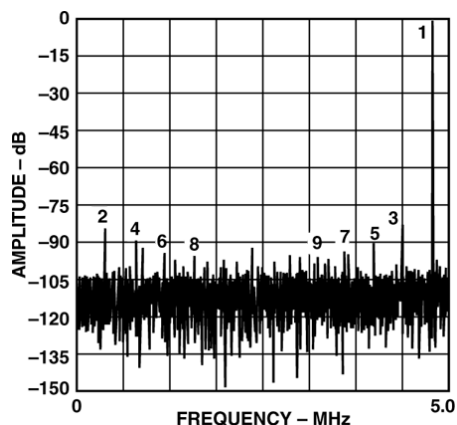


FIGURE 8. THD VS. SAMPLE RATE ($f_{IN} = 5.0$ MHz, $A_{IN} = -0.5$ dBFS, $V_{CM} = 2.5$ V)

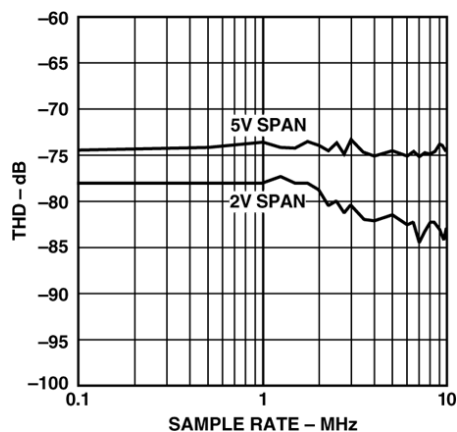


FIGURE 9. SINGLE TONE SFDR ($f_{IN} = 5.0$ MHz, $V_{CM} = 2.5$ V)

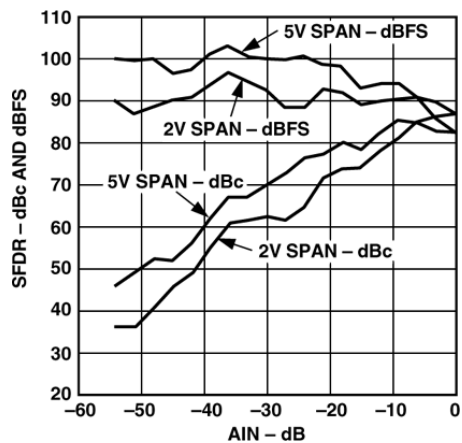


FIGURE 10. DUAL TONE SFDR ($F_1 = 0.95 \text{ MHz}$, $F_2 = 1.04 \text{ MHz}$, $V_{CM} = 2.5 \text{ V}$)

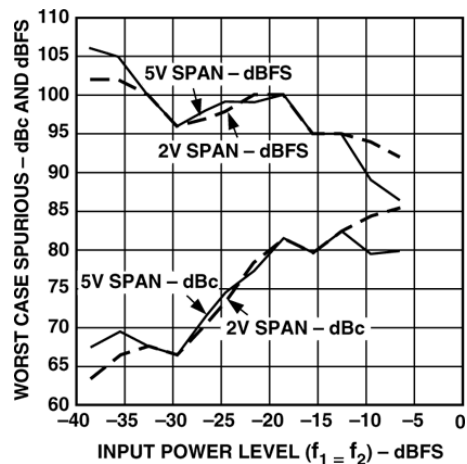


FIGURE 11. TYPICAL INL (INPUT SPAN = 5 V)

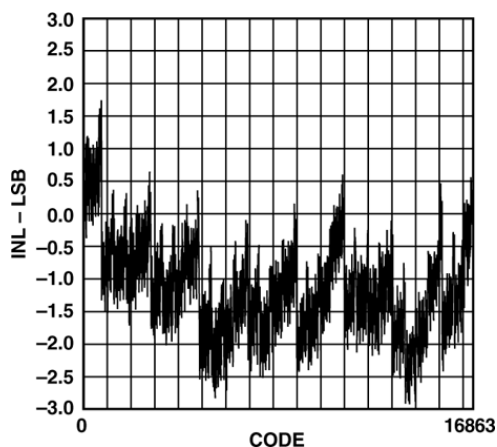


FIGURE 12. TYPICAL DNL (INPUT SPAN = 5 V)

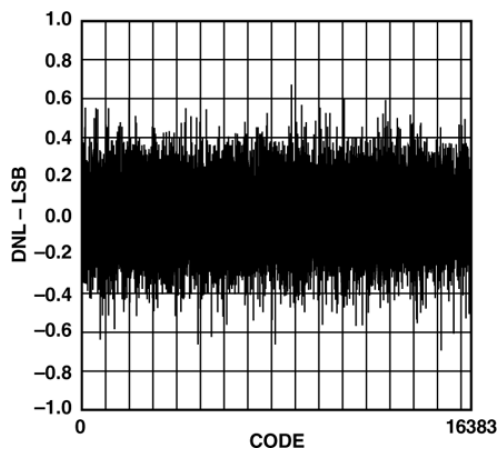


FIGURE 13. "GROUNDED-INPUT" HISTOGRAM (INPUT SPAN = 5 V)

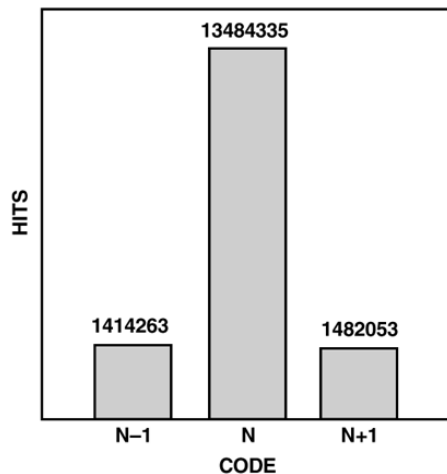


FIGURE 14. SINAD VS. INPUT FREQUENCY (INPUT SPAN = 2 V, $V_{CM} = 2.5V$)

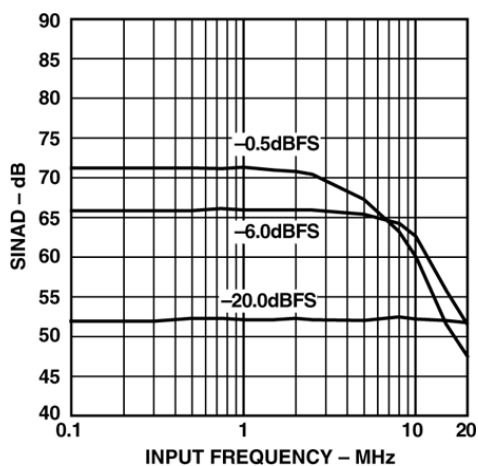


FIGURE 15. THD vs. INPUT FREQUENCY (INPUT SPAN = 5 V, $V_{CM} = 2.5$ V)

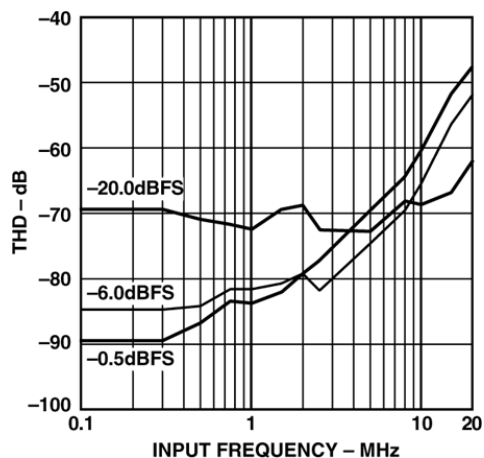


FIGURE 16. CMR vs. INPUT FREQUENCY (INPUT SPAN = 2 V, $V_{CM} = 2.5$ V)

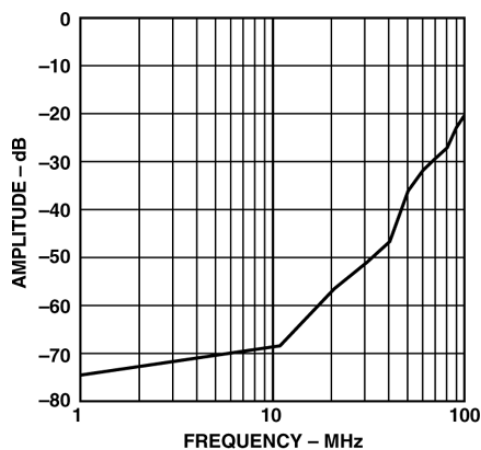


FIGURE 17. SINAD VS. INPUT FREQUENCY (INPUT SPAN = 5 V, $V_{CM} = 2.5$ V)

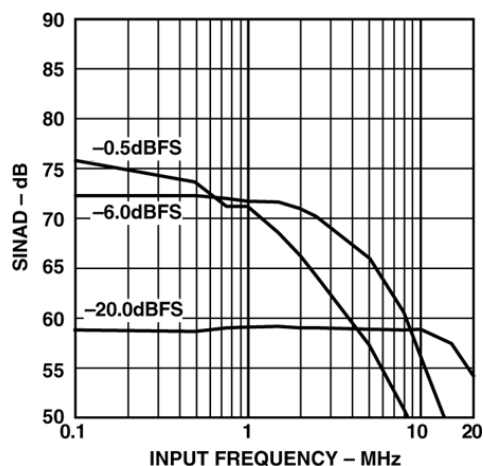


FIGURE 18. THD VS. INPUT FREQUENCY (INPUT SPAN = 5 V, $V_{CM} = 2.5$ V)

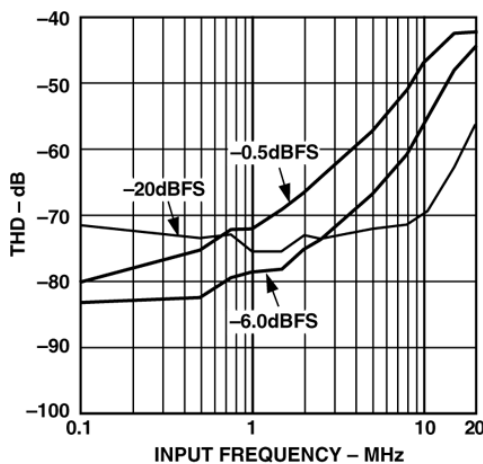
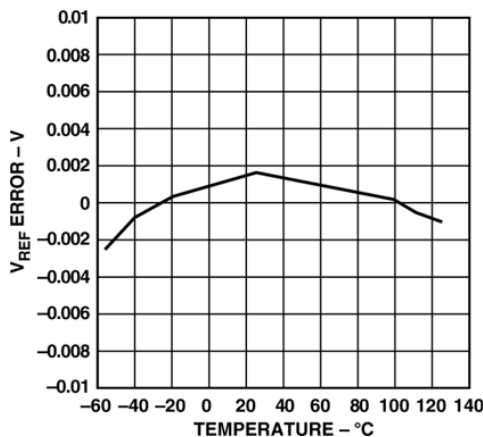
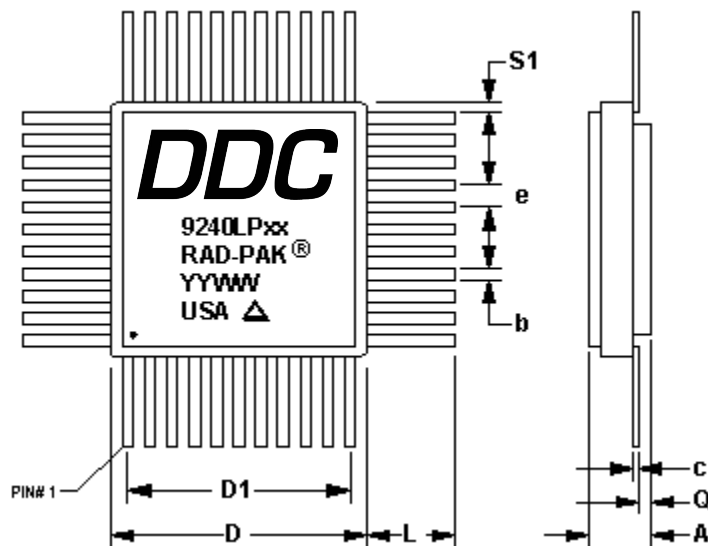


FIGURE 19. TYPICAL VOLTAGE REFERENCE ERROR VS. TEMPERATURE





44 PIN RAD-PAK® QUAD FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.185	0.205	0.225
b	0.015	0.017	0.019
c	0.008	0.010	0.012
D	0.643	0.650	0.657
D1	0.50 BSC		
e	0.050 BSC		
S1	0.005	0.067	--
L	0.260	0.270	0.280
Q	0.020	0.025	0.030
N	44		

Note: All dimensions in inches

Important Notice:

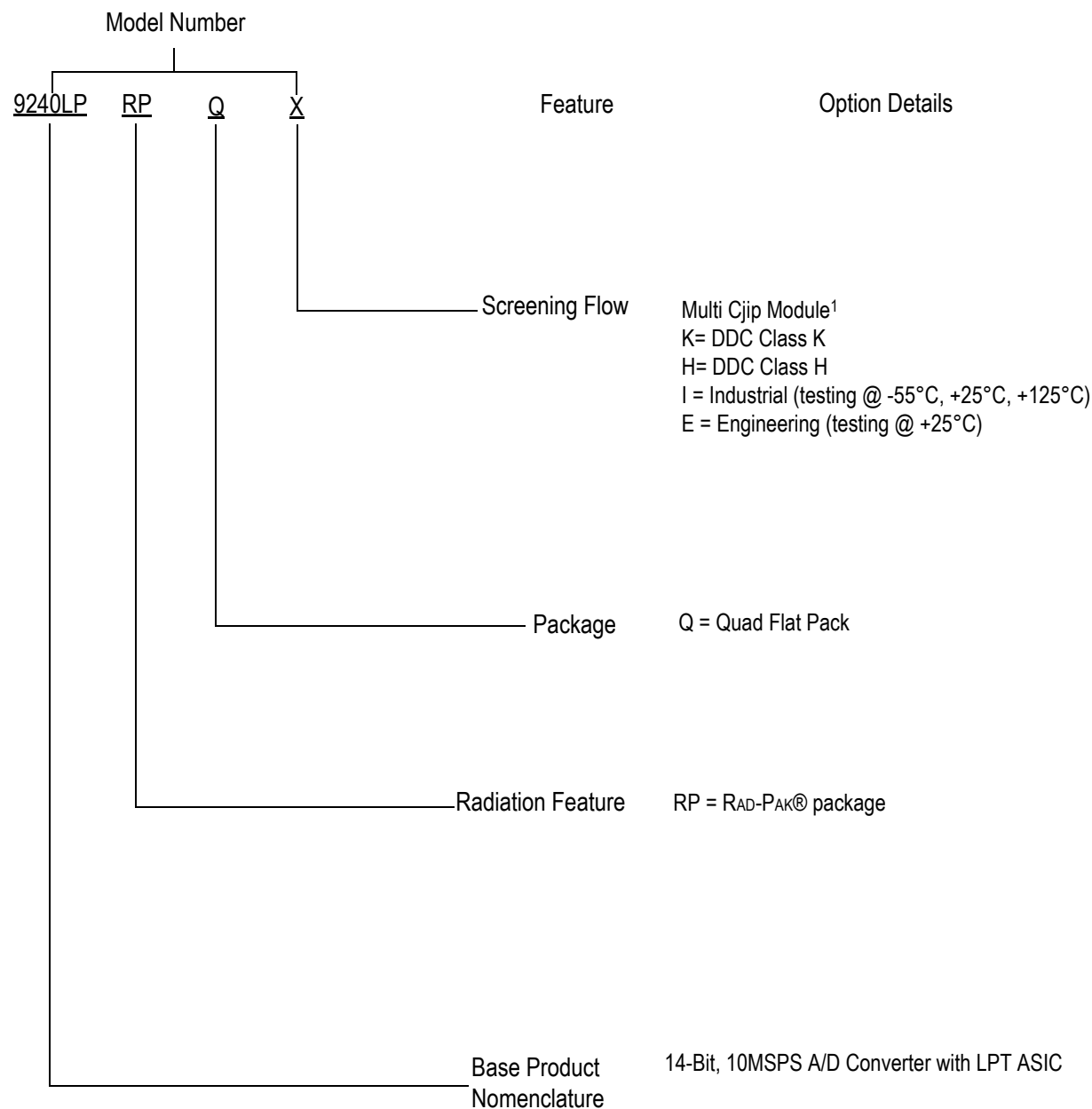
These data sheets are created using the chip manufacturers published specifications. DDC verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and DDC assumes no responsibility for the use of this information.

DDC's products are not authorized for use as critical components in life support devices or systems without express written approval from DDC.

Any claim against DDC must be made within 90 days from the date of shipment from DDC. DDC's liability shall be limited to replacement of defective parts.

Product Ordering Options



1) Products are manufactured and screened to DDC's self-defined CLASS H and CLASS K flows.