

**LC89610****Mini-Disk Decoder LSI****Preliminary****Overview**

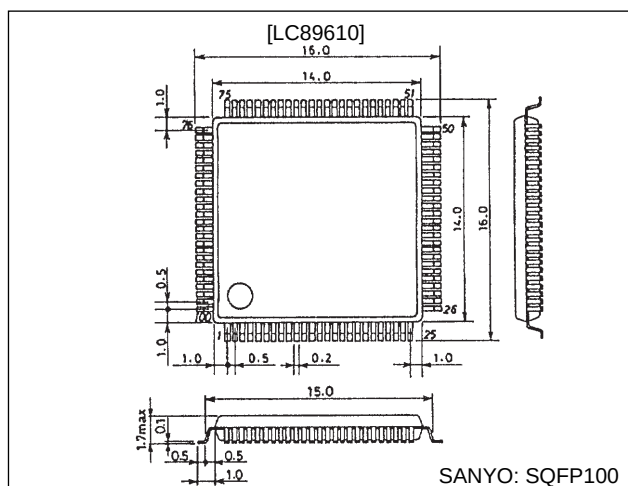
The LC89610 is a playback signal processing CMOS LSI that supports the mini-disk data format. Data that has been decoded by a CD decoder, an ACIRC decoder, or a CD-ROM decoder circuit is passed to a DRAM controller circuit and the LC89610 uses external DRAM to process shock proof. The shock proof processed data is passed to an audio data decoding LSI, the LC89602.

Features

- EFM decoder and PLL clock generator
- Detection, protection, and interpolation of the EFM frame synchronization signal
- Servo command control
- On-chip ACIRC decoder and ACIRC RAM
- ± 8 frame jitter margin
- Powerful error detection and correction (C1: dual errors, C2: quadruple errors)
- CLV control using EFM and ADIP signals
- Subcode Q decoding and CRC error checking
- Shock proof memory using 1, 4, 16, or 64 Mbits of external DRAM
- Buffering control and management for TOC and UTOC data
- Buffering control and management for subdata
- ADIP decoding and CRC error checking
- Low-power design using a 0.8 μm rule CMOS process
- Support for low-voltage operation ($V_{DD} = 3.0$ to 5.5 V)
- CCB based CPU interface

Package Dimensions

unit: mm

3181A-SQFP100

Specifications

Absolute Maximum Ratings at $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$	$T_a = 25^\circ\text{C}$	$-0.3\text{ to }+7.0$	V
Input and output voltages	V_I, V_O	$T_a = 25^\circ\text{C}$	$-0.3\text{ to }V_{DD} + 0.3$	V
Operating temperature	T_{opr}		$-30\text{ to }+70$	$^\circ\text{C}$
Storage temperature	T_{stg}		$-55\text{ to }+125$	$^\circ\text{C}$
Soldering conditions		10 seconds (pins only)	260	$^\circ\text{C}$

Allowable Operating Ranges at $T_a = -30\text{ to }+70^\circ\text{C}$, $V_{SS} = 0\text{ V}$

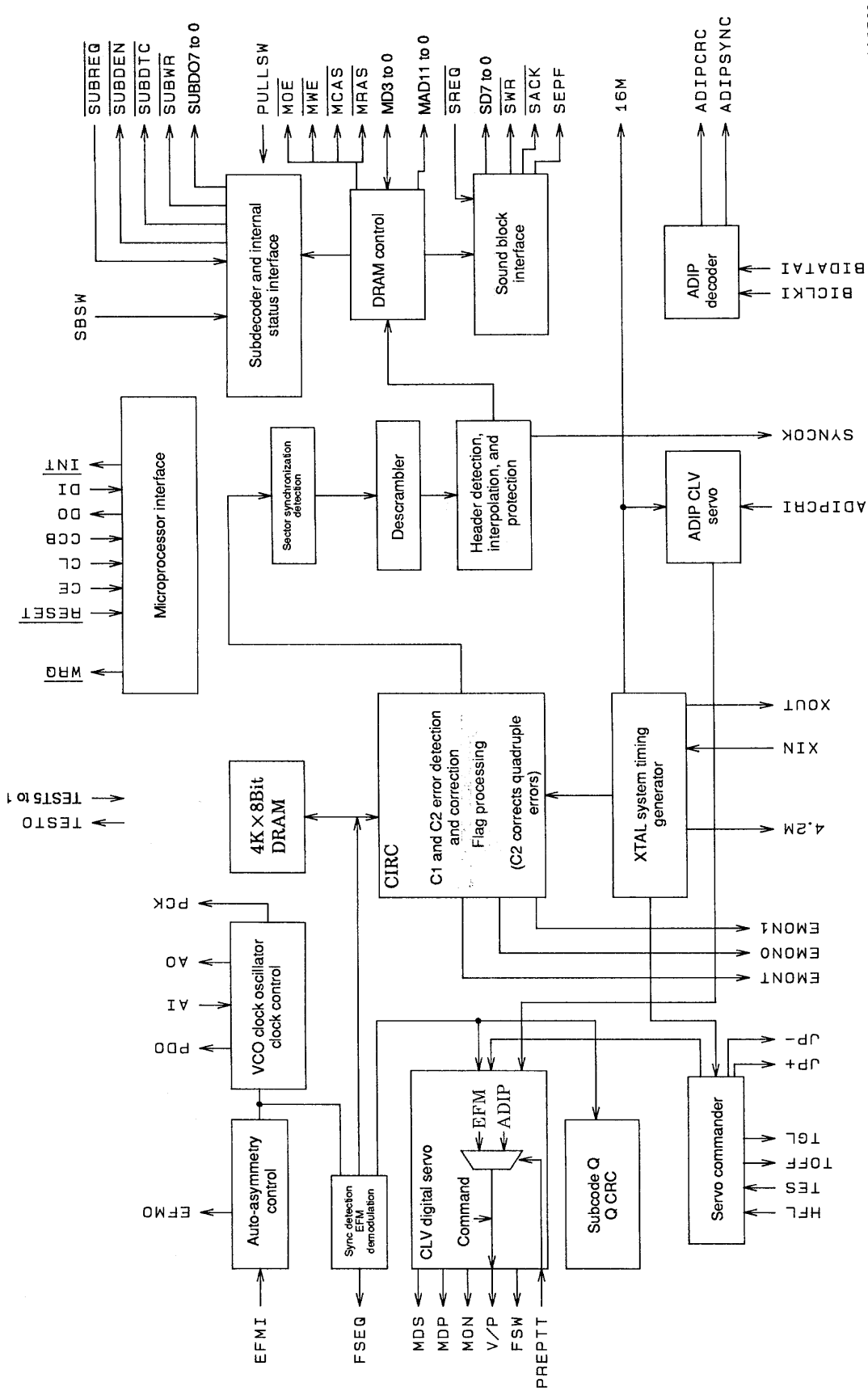
Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		3.0		5.5	V
Input voltage	V_{IN}		0		V_{DD}	V

DC Characteristics at $T_a = -30\text{ to }+70^\circ\text{C}$, $V_{SS} = 0\text{ V}$, $V_{DD} = 4.5\text{ to }5.5\text{ V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high level voltage	V_{IH}	*1	$0.8 V_{DD}$			V
Input low level voltage	V_{IL}	*1			$0.2 V_{DD}$	V
Input high level voltage	V_{IH}	*2	$0.7 V_{DD}$			V
Input low level voltage	V_{IL}	*2			$0.3 V_{DD}$	V
Input high level voltage	V_{IH}	*3	$0.6 V_{DD}$			V
Input low level voltage	V_{IL}	*3			$0.4 V_{DD}$	V
Output high level voltage	V_{OH}	$I_{OH} = -1\text{ mA}$, *4	$V_{DD} - 0.1$			V
Output low level voltage	V_{OL}	$I_{OL} = 1\text{ mA}$, *4			0.1	V
Output high level voltage	V_{OH}	$I_{OH} = -1\text{ mA}$, *5	$V_{DD} - 1.0$			V
Output low level voltage	V_{OL}	$I_{OL} = 1\text{ mA}$, *5			1.0	V
Output high level voltage	V_{OH}	$I_{OH} = -3\text{ mA}$, *6	$V_{DD} - 2.1$			V
Output low level voltage	V_{OL}	$I_{OL} = 3\text{ mA}$, *7			0.4	V
Input leakage current	I_L	$V_I = V_{SS}, V_{DD}$	-10		+10	μA
Output leakage current	I_{OZ}	For high-impedance state outputs	-10		+10	μA
Pull-up resistance	R_{UP}	*8	10	20	40	$\text{k}\Omega$
Quiescent current	I_{DD}	*9		0.1	200	μA
Quiescent current	I_{DD}	*10		250	475	μA

Note: 1. HFL, TES, CE, CL, $\overline{\text{SUBREQ}}$, $\overline{\text{SREQ}}$, $\overline{\text{RESET}}$, ADIPCRI, BIDATAI, BICKI
 2. Inputs other than *1, 2, and 4 XIN.
 3. EFMIN
 4. PDO
 5. EFMO
 6. Outputs other than *5 and *6 XOUT, AO, and DO (open-drain output).
 7. Outputs other than *5 and *6 XOUT, and AO.
 8. For MD0 to MD3, TEST1 to TEST5. However, note that the pull-up resistors are not connected when the PULLSW pin is low.
 9. When the PULLSW pin is low, outputs are open, and $V_I = V_{SS}$ or V_{DD} .
 10. When the PULLSW pin is high, outputs are open, and $V_I = V_{SS}$ or V_{DD} .

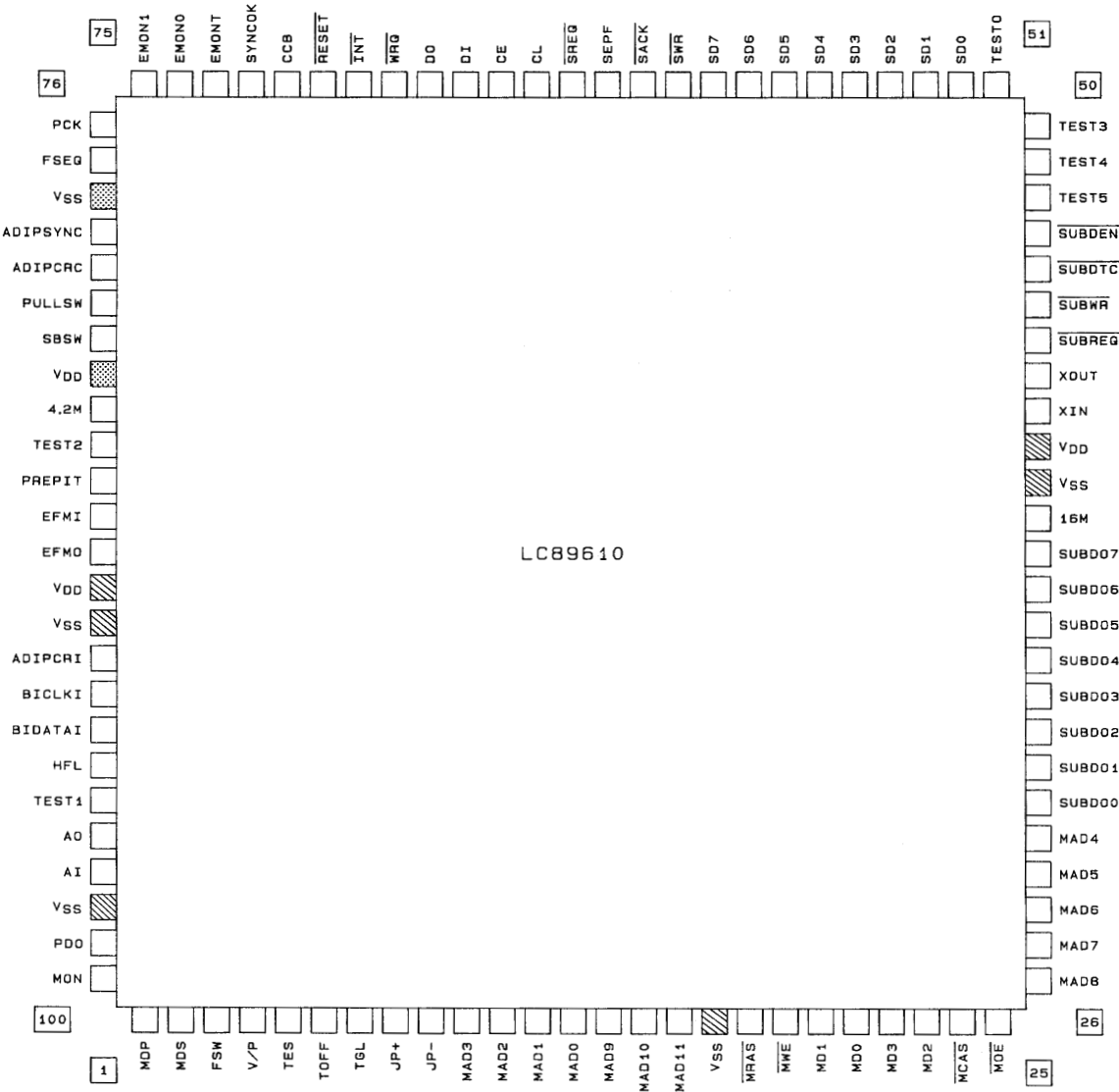
Block Diagram



A03790

LC89610

Pin Assignment



■ DRAM (8 bits × 4K words) dedicated power supply
■ Power supply for circuits other than DRAM

Top view

A03791

Pin Functions

Pin No.	Symbol	I/O	Function
1	MDP	O	CLV servo signal output
2	MDS	O	CLV servo signal output
3	FSW	O	CLV servo signal output
4	V/P	O	CLV servo signal output
5	TES	I	Track jump signal input
6	TOFF	O	Track jump signal output
7	TGL	O	Track jump signal output
8	JP +	O	Track jump signal output
9	JP –	O	Track jump signal output
10	MAD3	O	DRAM address output
11	MAD2	O	DRAM address output
12	MAD1	O	DRAM address output
13	MAD0	O	DRAM address output
14	MAD9	O	DRAM address output
15	MAD10	O	DRAM address output
16	MAD11	O	DRAM address output
17	V _{SS}	—	Ground
18	$\overline{\text{MRAS}}$	O	DRAM $\overline{\text{RAS}}$ signal output
19	$\overline{\text{MWE}}$	O	DRAM $\overline{\text{WE}}$ signal output
20	MD1	I/O	DRAM data I/O
21	MD0	I/O	DRAM data I/O
22	MD3	I/O	DRAM data I/O
23	MD2	I/O	DRAM data I/O
24	$\overline{\text{MCAS}}$	O	DRAM $\overline{\text{CAS}}$ signal output
25	$\overline{\text{MOE}}$	O	DRAM $\overline{\text{OE}}$ signal output
26	MAD8	O	DRAM address output
27	MAD7	O	DRAM address output
28	MAD6	O	DRAM address output
29	MAD5	O	DRAM address output
30	MAD4	O	DRAM address output
31	SUBDO0	O	Subdata and internal status output
32	SUBDO1	O	Subdata and internal status output
33	SUBDO2	O	Subdata and internal status output
34	SUBDO3	O	Subdata and internal status output
35	SUBDO4	O	Subdata and internal status output
36	SUBDO5	O	Subdata and internal status output
37	SUBDO6	O	Subdata and internal status output
38	SUBDO7	O	Subdata and internal status output
39	16M	O	16.9344 MHz clock output
40	V _{SS}	—	V _{SS} ground
41	V _{DD}	—	Power supply
42	XIN	I	16.9344 oscillator input
43	XOUT	O	16.9344 oscillator output
44	$\overline{\text{SUBREQ}}$	I	Subdata request signal input
45	$\overline{\text{SUBWR}}$	O	Subdata transfer clock output
46	$\overline{\text{SUBDTC}}$	O	Subdata transfer complete signal output
47	$\overline{\text{SUBDEN}}$	O	Subdata enable output
48	TEST5	I	Test input (normally tied to V _{DD})
49	TEST4	I	Test input (normally tied to V _{DD})
50	TEST3	I	Test input (normally tied to V _{DD})
51	TESTO	I	Test output
52	SD0	O	Sound block data output
53	SD1	O	Sound block data output
54	SD2	O	Sound block data output
55	SD3	O	Sound block data output

Continued on next page.

LC89610

Continued from preceding page.

Pin No.	Symbol	I/O	Function
56	SD4	O	Sound block data output
57	SD5	O	Sound block data output
58	SD6	O	Sound block data output
59	SD7	O	Sound block data output
60	$\overline{\text{SWR}}$	O	Sound block data transfer clock output
61	$\overline{\text{SACK}}$	O	Sound block data acknowledge signal output
62	SEPF	O	Sound block data empty signal output
63	$\overline{\text{SREQ}}$	I	Sound block data request signal input
64	CL	I	CPU interface data transfer clock input
65	CE	I	CPU interface chip enable signal input
66	DI	I	CPU interface data input
67	DO	O	CPU interface data output
68	$\overline{\text{WRQ}}$	O	CPU interface interrupt signal output
69	$\overline{\text{INT}}$	O	CPU interface interrupt signal output
70	$\overline{\text{RESET}}$	I	System reset
71	CCB	I	CPU interface type switching input
72	SYNCK	O	Sector synchronization detection signal output
73	EMONT	O	Error detection monitor signal output
74	EMON0	O	Error detection monitor signal output
75	EMON1	O	Error detection monitor signal output
76	PCK	O	4.3218 MHz monitor signal output
77	FSEQ	O	Frame synchronization detection signal output
78	V_{SS}	—	Ground (for the on-chip DRAM only)
79	ADIPSYN	O	ADIP synchronization timing signal output
80	ADIPCRC	O	ADIP data CRC flag output
81	PULLSW	I	Internal pull-up resistor switching signal input
82	SBSW	I	Subdata/internal status switching signal input
83	V_{DD}	—	Power supply (for the on-chip DRAM only)
84	4.2M	I	Test input (normally tied to V_{DD})
85	TEST2	I	Test input (normally tied to V_{DD})
86	PREPIT	I	CLV servo output signal switching input
87	EFMI	I	HF signal input
88	EFMO	O	EFM signal output
89	V_{DD}	—	Power supply
90	V_{SS}	—	Ground
91	ADIPCRI	I	ADIP carrier signal input
92	BICLK	I	Bi-phase data transfer clock input
93	BIDATA	I	Bi-phase data input
94	HFL	I	Track detection signal input
95	TEST1	O	4.2336 MHz output
96	AO	O	VCO control signal output
97	AI	I	VCO control signal input
98	V_{SS}	O	VCO control signal output
99	PDO	—	Ground
100	MON	O	CLV servo signal output

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of August, 1995. Specifications and information herein are subject to change without notice.