HD81501A

ISDN I-Interface LSI

I-INTERFACE LSI is a full-duplex transceiver for an ISDN basic user-network interface specified by ITU-T I-Series Recommendations.
This LSI contains all layer 1 and 2 control functions following I.430 and I.441 at S/T reference points, and also includes layer3 interface, which is selectable data transfer mode (DMA/Programmed I/O), for direct connection to 3 types of microprocessors, and moreover, Master/Slave operations modes for various kind of Terminal equipments (TE) and network termination (NT2).

Features

- Layer1 Control Following ITU-T Recommendation I.430
  - 192kb/s Transmission Rate
  - B+B+D Channel Structure
  - Synchronization Control (Timing Recover, Frame Alignment)
  - D Channel Collision Control by E-bit with Retransmission Function
  - Multiframing Control by Q-bit
  - Master/Slave Mode Operations
  - Selectable B Channel Use
    Individual Use of B1 and B2 (64kb/s)
    Bulk Use of B1+B2 (128kb/s)
  - B Channel Data Input/Output Clock Selectable (Internal or External Clock)
- Layer2 Control Following ITU-T Recommendation I.441
  - HDLC Frame Control (Flag Control, FCS Addition/Check, 0 Insertion/Deletion)
  - LAPD Status Control for TE Mode (Error Control, Flow Control, DLCI Control)*
  - Internal Timer for Time-out Check

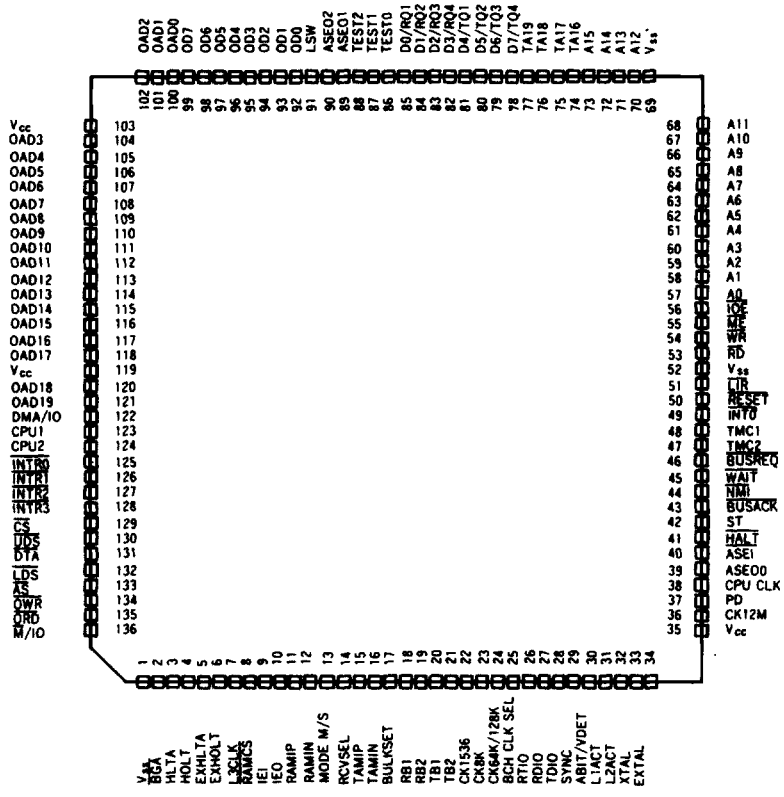
  *This LSI contains LAPD firmware for TE (Slave) mode.
- Layer3 Interface Function
  - Direct Connection to 3 Types of Microprocessor Bus . . . . 8086 Type, 68000 Type, 6809 Type
  - Selectable Data Transfer Mode . . . . . DMA/Programmed I/O
  - Logical Interface by Interface Primitives
- Built-in 8 bit Microprocessor (64180 Core) for LAPD Sequence
- Contains 16kB ROM and 1kB RAM for LAPD Software
- Implanted LAPD Firmware in on Chip-ROM for Slave Application
- Adaptation to Circuit Switching (without Ext. RAM) or Packet Switching (with Ext. RAM) by Contained LAPD
- Memory Area Extension Capability for Master Mode and X.25 Packetization (User Program Available)
- Individual Operation Modes of Layer1 and Layer2 Functions
- Power Down Mode for Low Power Operation
- Oscillation Circuit Provided
- 1.3μm CMOS Double Metal Technology
- TTL/CMOS Compatible Input/Output
- Single Power Supply 5V±5%
- 136 pin Quad Flat Package

Main Operation Mode

- Operation Layer Selectable
  - All Layer Operation
  - Layer1 Individual Operation
  - Layer2 Individual Operation
- Master/Slave Mode Selectable
- Receive Timing Selectable at Master Mode
  - Transmit Synchronized Mode for Short Passive Bus
  - Receive Synchronized Mode for Point to Point Bus and Extended Bus
- B Channel Data Input/Output Clock Selectable (8kHz, 64kHz/128kHz)
  - Internal Clock Mode
  - External Clock Mode
- B Channel Use Selectable
  - Nomal Use . . . . B1 and B2 (64kb/s) 2Channels
  - Bulk Use . . . . B1 + B2 (128kB/s) 1Channel
- Layer3 Interface Bus Selectable
  - 8086, Z80 Type
  - 6800, 6809 Type
  - 68000 Type
- Data Transfer Mode to Layer3 Bus Selectable
  - Programmed I/O Transfer Mode
  - DMA Transfer Mode
- Internal Microprocessor Clock Rate Selectable
  - Nomal Mode . . . . . Layer2 Microprocessor Operation Clock; 6.144MHz
  - Power Down Mode . . Layer 2 Microprocessor Operation Clock; 3.072MHz for Low Power mode
- Internal/External Memory Area Selectable
  - 4 Types of Memory Space Area

- Circuit Switching/Packet Switching Mode Selectable
  Internal LAPD firmware for terminal equipment is automatically operated as follows
  - Circuit Switching Mode . . . . without external RAM. SAPI=0 only
  - Packet Switching Mode . . with external RAM (8kB). both SAPI=0 and 16
    (SAPI=0: Circuit Switching Service SAPI=16: Packet Switching Service)

Pin Arrangement

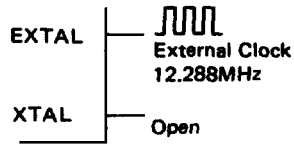


(Top View)

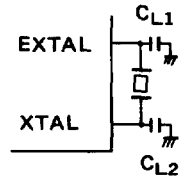
Pin Descriptions

1. Common Part

Pin No.	Symbol	I/O	Function
35 103 119	V_{CC}	I	Power Supply; 5V±5%
1 52 69	V_{SS}	I	Ground
33	XTAL	O	Oscillator Output: X'tal connect
34	EXTAL	I	Oscillator Input: X'tal connect or External Clock Input



(A) External Input Mode



(B) X'tal Mode

- X'tal; AT Cut Type
- Frequency; 12.288MHz
- Co<7pF
- Rs<60Ω
- C_{L1}, C_{L2}; 10–22pF±10%

38	CPU CLK	O	System Clock: 6.144MHz Output at PD="L" 3.072MHz Output at PD="H"
36	CK12M	O	12.288MHz Clock Output:
37	PD	I	Power Down Set: Internal CPU System Clock Select PD="L" ..... 6.144MHz PD="H" 3.072MHz
50	$\overline{\text{RESET}}$	I	RESET: LSI is RESET if this pin remains low level for over 6 cycles.
86	TEST0		Mode Set: LSI is set as follows by these pins.
87	TEST1	I	
88	TEST2		

T2	T1	T0	Mode
0	0	0	Normal Operation Using Internal LAPD
0	0	1	Internal CPU Inactive for ASE.
0	1	1	Internal RAM Inactive
1	0	1	Internal ROM Inactive
1	1	0	Internal ROM/RAM Inactive

At memory inactive mode, memory address space is switched from internal area to external, and external memory is available. Even if LSI is set to Normal Operation, external RAM may be connected. In this case, LSI should be adapted to not only circuit but also packet switching.

2. Internal CPU Part

Pin No.	Symbol	I/O	Function
49	$\overline{INTO}$	I/O (Open Drain)	INTERRUPT 0: This input is request pin for maskable interrupt level 0. At this LSI, operation mode 2 (IM2; VECTOR method) must be set. This pin is connected to internal interrupt factors of layer1, 2 and layer3 interface, and each interrupt factors are controlled by daisy chain system. This pin must be connected to V_{CC} through resister (10k–100kΩ).
44	$\overline{NMI}$	I	NON MASKABLE INTERRUPT: This pin is request pin for nonmaskable request. Normally, this pin is connected to V_{CC}.
9	IEI	I	IEI INPUT FOR DAISY CHAIN: This is interrupt permission signal for internal factors. Normally, connect to V_{CC}.
10	IEO	O	IEO OUTPUT FOR DAISY CHAIN: This is output of internal daisy chain.
48 47	TMC1 TMC2	I	CPU TEST PIN: These pins must be connected to "HIGH" level.
39 89 90	ASEO0 ASEO1 ASEO2	O	CPU TEST MONITOR: These pins are monitor outputs under test mode.
40	$\overline{ASEI}$	I	CPU TEST MONITOR SET: This pin is for test, and connected to V_{CC} at normal mode.
53	$\overline{RD}$	I/O (3-state)	READ: indicates read cycle of layer2 microprocessor.
54	$\overline{WR}$		WRITE: indicates write cycle of layer2 microprocessor.
55	$\overline{ME}$		MEMORY ENABLE: indicates memory read/write cycle of layer2 microprocessor.
56	$\overline{IOE}$		I/O ENABLE: indicates I/O read/write cycle of layer2 microprocessor.
46	$\overline{BUSREQ}$	I	BUS REQUEST: This pin is used for bus release request to layer2 microprocessor. When this pin goes "LOW" level, microprocessor suspends execution cycle, and makes CPU buses high impedance. At bus release state, internal logic parts can not be accessed by external BUS MASTER.
43	$\overline{BUSACK}$	O	BUS ACKNOWLEDGE: This output indicates that this microprocessor is at bus release state caused by BUS REQUEST. "LOW" is active level.
41	$\overline{HALT}$	O	HALT: When microprocessor executes HALT or SLP operands, this output turns to "LOW" which means HALT/SLEEP/SYSTEM STOP mode.
45	$\overline{WAIT}$	I	WAIT: This pin is used for wait cycle insertion when low speed memory or I/O devices are connected. "LOW" is active level. Normally, connect to V_{CC}.
51	$\overline{LIR}$	I/O	LOAD INSTRUCTION REGISTER: This output indicates that execution cycle is Op-code fetch cycle. However, if LIRE bit in the operation mode control register is set to "0", this pin turn to "LOW" only during RETI instruction cycle or $\overline{INT0}$ acknowledge cycle.
42	ST	O	STATUS: This signal indicates operation status as follows.

ST	$\overline{HALT}$	$\overline{LIR}$	Operation
0	1	0	CPU Operation (1st Opcode cycle)
1	1	0	CPU Operation (2nd, 3rd Opcode cycle)
1	1	1	CPU Operation (except for Opcode cycle)
0	0	0	Halt Mode
1	0	1	Sleep/System Stop Mode

78 | 85	D7 | D0	I/O (3-state)	DATA Bus: These are bi-directional 8 bits data buses of layer2 microprocessor. At L1MODE, these pins turn to 0-bit input/output pins.
57 | 73	A0 | A15	I/O (3-state)	ADDRESS BUS: These are address pins for 16 bits memory space (64kB). These go high impedance at reset status and bus release status.
74 | 77	TA16 | TA19	I/O (3-state)	TEST ADDRESS BUS: These are address buses for test.
8	$\overline{RAMCS}$	O	RAM CHIP SELECT: This pin outputs "LOW" level when address space are between E000H–FFFFH and $\overline{ME}$ goes "LOW" level at memory access cycle. This pin may be used for external RAM select. In case of packet switching application, this pin should be connected to $\overline{CS}$ of additional external RAM.

3. Layer1 and Layer2 Control Parts

Pin No.	Symbol	I/O	Function
11	RAMIP	I	RECEIVE AMI POSITIVE: At receiving AMI positive pulse which means "0", "HIGH" level may be input to this pin at 192kb/s.
12	RAMIN	I	RECEIVE AMI NEGATIVE: At receiving AMI negative pulse which means "0", "HIGH" level may be input to this pin at 192kb/s.
15	TAMIP	O	TRANSMIT AMI POSITIVE: This is output pin for positive pulse when transmit AMI signal goes "0". Output is synchronized by 192kHz divided external standard clock 1.536MHz at master mode, and 192kHz extracted from receive AMI signal at slave mode, respectively.
16	TAMIN	O	TRANSMIT AMI NEGATIVE: This is output pin for negative pulse when transmit AMI signal goes "0". Output timing is the same as TAMIP.
13	MODE M/S	I	MASTER/SLAVE MODE SELECT: • Slave Mode at "LOW" Level Input • Master Mode at "HIGH" Level Input
31	L1ACT	I	LAYER1 ACTIVE:
32	L2ACT	I	LAYER2 ACTIVE: Operation layer can be selected as follows by these pins.

L1ACT	L2ACT	Mode	Function
1	0	L1MODE	LAYER1 INDIVIDUAL
0	1	L2MODE	LAYER2 INDIVIDUAL
1	1	NORMAL	ALL LAYERs OPERATION

14	RCVSEL	I	RECEIVE TIMING SELECT: Receive timing select pin at master mode. At slave mode, "LOW" level should be input. • "LOW" level input ..... Receive synchronized mode. Receive side operates by clock synchronized to receive AMI. • "HIGH" level input ..... Transmit synchronized mode. Receive side operates by timing extracted from external 1.536MHz clock.
25	BCH CLK SEL	I	Bch CLOCK SELECT: Select pin for Bch data input/output clock. This pin also switches input/output mode of CK8K pin and CK64K/128K pin.

INPUT	SYNCHRONIZED CLOCK	CK8K	CK64K/128K
0	INTERNAL CLOCK	OUTPUT	OUTPUT
1	EXTERNAL CLOCK	INPUT	INPUT

23	CK8K	I/O	Bch FRAME TIMING: Input/output pin for frame timing of RB1, RB2 and TB1, TB2.
24	CK64K/128K	I/O	Bch BIT TIMING: Input/output pin for bit timing of RB1, RB2 and TB1, TB2.
17	BULKSET	I	BULK MODE SET: Select pin for Bch BULK mode.

	BULKSET="LOW"	BULKSET="HIGH"
RB1	RECEIVE B1 OUTPUT	RECEIVE B1+B2 OUTPUT
RB2	RECEIVE B2 OUTPUT	DON'T USE
TB1	TRANSMIT B1 INPUT	TRANSMIT B1+B2 INPUT
TB2	TRANSMIT B2 INPUT	CONNECT to V_{CC} or GND
CK64K/128K	64kHz clock	128kHz clock
BIT RATE	64kb/s	128kb/s

18	RB1	O	RECEIVE B1ch DATA:
19	RB2	O	RECEIVE B2ch DATA:

(to be continued)

Pin No.	Symbol	I/O	Function
20	TB1	I	TRANSMIT B1ch DATA:
21	TB2	I	TRANSMIT B2ch DATA:
26	RTIO	I/O	Dch DATA RECEIVE/TRANSMIT TIMING CLOCK: Input/output pin for 16kHz clock. Duty isn't 50%.
27	RDIO	I/O	RECEIVE Dch DATA: Input/output pin for receive Dch data (HDLC format). Data input/output is synchronized to RTIO timing.
28	TDIO	I/O	TRANSMIT Dch DATA: Input/output pin for transmit Dch data (HDLC format). Data input/output is synchronized to RTIO timing. Input/output of above pins are controlled as follows.
22	CK1536	I/O	1.536MHz CLOCK: • At MASTER MODE, input pin for transmit basis clock 1.536MHz. • At SLAVE MODE, output pin of 1.536MHz clock in DPLL.
30	ABIT/VDET	I	ABITSET/VDET: • At MASTER MODE, input pin for activation of layer1. Only at L1MODE, this pin may be used. If this goes "HIGH" level, A-bit in the transmit frame turn to "1". At normal mode, this pin must be connected to V_{SS}. At SLAVE MODE, input pin for power feed detection. Power feed detection is noticed to LSI by "HIGH" level input. If power is removed, layer1 transmits info0 signal and TE is deactivated.
29	SYNC	I	SYNCHRONIZATION: This pin indicates establishment of receive frame synchronization. • At MASTER MODE, this pin outputs "HIGH" level when frame alignment is established according to CCITT I.430. • At SLAVE MODE, this pin outputs "HIGH" level when 3 consecutive "1" s of A-bit are detected after frame alignment.
91	LSW	I/O	LAYER1 ACTIVATION SWITCH: Input/output pin for layer1 activation signal. • At L1MODE, a "HIGH" input on this pin enables layer1 part to activate. • At other mode, this is an output of layer2 microprocessor indication for layer1 activation.
78 | 81	TQ1 | TQ4	I	TRANSMIT Q-BIT: At L1MODE, these are used to set Q-bit in the SLAVE transmit frame for SLAVE MODE. For MASTER, these should be input "LOW" level.
82 | 85	RQ1 | RQ4	O	RECEIVE Q-BIT: At L1MODE, these are used to output Q-bit in the MASTER receive frame.

	L1MODE	L2MODE	NOMAL MODE
RTIO	OUTPUT	INPUT	OUTPUT
RDIO	OUTPUT	INPUT	OUTPUT
TDIO	INPUT	OUTPUT	OUTPUT

4. Layer3 Interface Part

Pin No.	Symbol	I/O	Function
122	DMA/IO	I	DMA/IO MODE SELECT: This pin sets transfer mode to layer3 buses as follows. DMA/IO = 0: Programmed I/O Transfer Mode DMA/IO = 1: DMA Transfer Mode
123 124	CPU1 CPU2	I I	CPU TYPE SELECT: These pins determine layer3 microprocessor types as follows. CPU1 = 0, CPU2 = 0: 80 Type ... 8086, Z80 etc CPU1 = 1, CPU2 = 0: 68 Type ... 6809, 6800 etc CPU1 = 0, CPU2 = 1: 60 Type ... 68000 etc
129	$\overline{CS}$	I	CHIP SELECT: This is used by layer3 microprocessor to select this LSI when this signal is active "LOW". This pin is available during programmed transfer input/output at programmed I/O transfer mode or DMA transfer mode. During DMA transfer at DMA transfer mode, this pin must be remained "HIGH" level.
92 | 99	OD0 | OD7	I/O (3-state)	DATA BUS FOR LAYER3: These are bi-directional 8 bits buses for layer3 interface.
100	OAD0	I/O (3-state)	ADDRESS BUS FOR LAYER3: During programmed transfer, I/O DATA REGISTER and EXTERNAL MASK REGISTER are selected by this pin. During DMA transfer, this is output of DMA address.
101 | 120	OAD1 | OAD18	O (3-state)	ADDRESS BUS FOR LAYER3: These are outputs of DMA addresses during DMA transfer.
121	OAD19	I/O (3-state)	ADDRESS BUS FOR LAYER3: This is an output of DMA address except for 80Type selection. In case of selecting 80Type, this is used as READY input. READY signal is active "LOW".
125 126 127 128	$\overline{INTR0}$ $\overline{INTR1}$ $\overline{INTR2}$ $\overline{INTR3}$	O	INTERRUPT FOR LAYER3 microprocessor: $\overline{INTR0}$ is for read request, and $\overline{INTR1}$ is for write request. $\overline{INTR2}$ and $\overline{INTR3}$ indicate DMA READ END and DMA WRITE END, respectively. These pins are "LOW" active. At programmed I/O transfer mode, $\overline{INTR0}$ and $\overline{INTR1}$ are available, and at DMA transfer mode, $\overline{INTR1}$–$\overline{INTR3}$ are available.

Note 1. Programmed transfer means that I/O transfer sequence is executed by layer3 microprocessor program at programmed I/O transfer mode or DMA transfer mode for address set.
DMA transfer means that DMA transfer sequence is executed by internal DMAC at DMA transfer mode.

Pin No.	Symbol	I/O	Function
7	L3CLK	I	LAYER3 MICROPROCESSOR SYSTEM CLOCK: System clock input of layer3 microprocessor.
134	$\overline{OWR}$	I/O (3-state)	WRITE FOR LAYER3: This pin corresponds to $\overline{WR}$ of 8086 and R/$\overline{W}$ of 6809 and 68000. This is "LOW" active.
135	$\overline{ORD}$	I/O (3-state)	READ FOR LAYER3: This pin corresponds to $\overline{RD}$ of 8086. This is "LOW" active.
4	HOLT	O	HOLD REQUEST TO LAYER3 MICROPROCESSOR: This pin is output of bus request signal which corresponds to HOLD (high active) of 8086, $\overline{DMA}$/$\overline{BREQ}$ (low active)of 6809 and $\overline{BR}$ (low active) of 68000.
3	HLTA	I	HOLD ACKNOWLEDGEMENT FROM LAYER3 MICROPROCESSOR: Bus release signal from layer3 microprocessor is provided to this pin. This signal corresponds to HLDA of 8086, BA of 6809 (high active) and $\overline{BG}$ of 68000 (low active).
136	$\overline{M}$/IO	O (3-state)	MEMORY REQUEST TO 8086 BUS: This goes "LOW" level during DMA transfer at 80Type, which corresponds to inverted signal of M/$\overline{IO}$.
133	$\overline{AS}$	I/O (3-state)	ADDRESS STROBE: This corresponds to $\overline{AS}$ of 68000. "LOW" is active level.
130	$\overline{UDS}$	O (3-state)	UPPER DATA STROBE: This is used only at DMA transfer mode. On 8086 bus, this goes "LOW" during DMA transfer and corresponds to A0 signal and inverted signal of $\overline{BHE}$. Lower byte (even address) will become active by this. On 68000 bus, this goes "HIGH" during DMA transfer and corresponds to $\overline{UDS}$. Upper byte (D8—D15) will be inhibited by this pin.
132	$\overline{LDS}$	I/O (3-state)	LOWER DATA STROBE: This corresponds to $\overline{LDS}$ of 68000. "LOW" is active level. During DMA transfer, this pin goes "LOW" and selects lower byte of data buses.
131	$\overline{DTA}$	I/O (3-state)	DATA TRANSFER ACKNOWLEDGE: This pin will be connected to $\overline{DTACK}$ of 68000. "LOW" is active.
2	$\overline{BGA}$	I/O (3-state)	BUS GRANT ACKNOWLEDGE: This pin will be connected to $\overline{BGACK}$ of 68000.
6	EXHOLT	I	EXTERNAL BUS MASTER HOLD: This is connected to bus request signal from external DMAC. If there is bus request of external DMAC, this LSI will execute bus arbitration between internal and external DMACs. When unused, this pin must be set as follows. This pin is valid only at DMA transfer mode. • 80 Type ... Pull Down • 68 Type, 68000 Type ... Pull Up
5	EXHLTA	O	HLTA TO EXTERNAL BUS MASTER: This is HOLD acknowledge signal to external DMAC. This pin is valid only at DMA transfer mode.

Note 1. Above I/O pins are set to inputs during programmed transfer and outputs during DMA transfer except $\overline{DTA}$. $\overline{DTA}$ is set conversely.

Description for Function

Block diagram of ISDN I-INTERFACE LSI is shown in figure 1. The descriptions for function in each block are as follows.

1. Layer1 Control Function Part

Layer1 part controls basic access interface layer1 of which channel structure is 2B+D specified on ITU-T Recommendation I.430.

This LSI satisfies with all layer1 specifications shown in table. 1 by connecting to specified Driver/Receiver Module, and fully corresponds to transmission frame structure at S/T reference points. Frame format is shown in figure 2. In this figure, 2 bits offset means delayed time between input and output of Driver/Receiver Module at the point of interface cable side of TE. At input/output points of LSI, it is adjusted to 1.5 bits offset.

Multiframe function specified in '86 Recommendations can be also provided in this LSI. (This function isn't supported on internal firmware.) At slave mode, Q-bit insertion frame is detected by M-bit and FA-bit transmitted from NT, and Q-bit information, which is set by layer2 microprocessor, is transmitted to NT every 20 frames. Multiframe structure is shown in table 2.

Collision control part supports D-channel collision detection, empty detection and retransmission of suspended D-channel frame. In case of mismatching send D-bit and received E-bit, T.E instantly stops frame transmission and supervises empty of lines. When Empty is detected, buffered suspended D-channel frame is retransmitted without resetting by layer2 and layer3 microprocessors. This part is also supports priority control (class1/class2). TEs are assigned two priority classes with two priority levels for each class. Signalling is highest priority class.

2. B Channel Buffer

B channel receive buffer is FIFO configuration. This part derives B-channel (B1, B2) from receive frame, and output two B channel informations (64kb/s) at normal mode or one information as 128kb/s channel at BULK mode.

B channel transmit buffer is also FIFO structure, and sends 64kb/s two informations (B1 and B2) at normal mode, or, 128kb/s information (B1+B2) at BULK mode.

B channel Input/output clock is selectable out of internal clock mode and external clock mode by switching BCH CLK SEL pin. Phase between transmit frame timing and B channel input/output timing is free by FIFO structure.

B channel data input/output timing is shown in figure 3.

When layer1 is at operation status (state number F7 for TE, G3 for NT), B channel data is transparent, therefore, in case of unassignment on B channel, TB1 and TB2 must be inactivated by "HIGH" level input. RB1 and RB2 will output receive data irrespective of assignment or not.

When layer1 is at asynchronized state (SYNC= "0"), outputs of RB1 and RB2 go "HIGH" level.

Table. 1 Basic Interface Layer1 Specifications

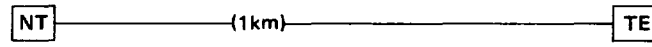
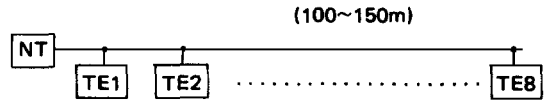
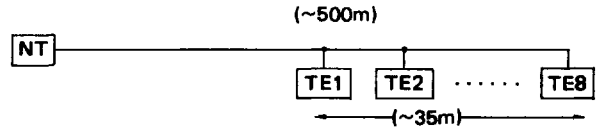
Items	Content
Channel Structure	2B+D; B=64kb/s ... User-to-User Information Transfer ; D=16kb/s ... Signalling Information Packetized Data Management Protocol
Interface	4 Signal Lines for Balanced Transmit and Receive
Physical Configuration	(1) Point to Point  (2) Short Passive Bus  (3) Extended Passive Bus 
Transmission Rate	192kb/s
Line Encoding	Pseudo Ternary Code
Frame Structure	48 Bits/Frame Every 250μs 20 Frames/Multiframe
Power Supply	Phantom Power Supply
D-Channel Contension	Echo-Bit Check

Table 2 Detection of Q-Bit Position and Multiframe Configuration

Frame Number	NT→TE FA Bit Position	TE→NT FA Bit Position	M Bit
1	ONE	Q1	ONE
2	ZERO	ZERO	ZERO
3	ZERO	ZERO	ZERO
4	ZERO	ZERO	ZERO
5	ZERO	ZERO	ZERO
6	ONE	Q2	ZERO
7	ZERO	ZERO	ZERO
8	ZERO	ZERO	ZERO
9	ZERO	ZERO	ZERO
10	ZERO	ZERO	ZERO
11	ONE	Q3	ZERO
12	ZERO	ZERO	ZERO
13	ZERO	ZERO	ZERO
14	ZERO	ZERO	ZERO
15	ZERO	ZERO	ZERO
16	ONE	Q4	ZERO
17	ZERO	ZERO	ZERO
18	ZERO	ZERO	ZERO
19	ZERO	ZERO	ZERO
20	ZERO	ZERO	ZERO
1	ONE	Q1	ONE
2	ZERO	ZERO	ZERO

Note 1. Q-bit must be set to binary "1" if Q-bit is not utilized.

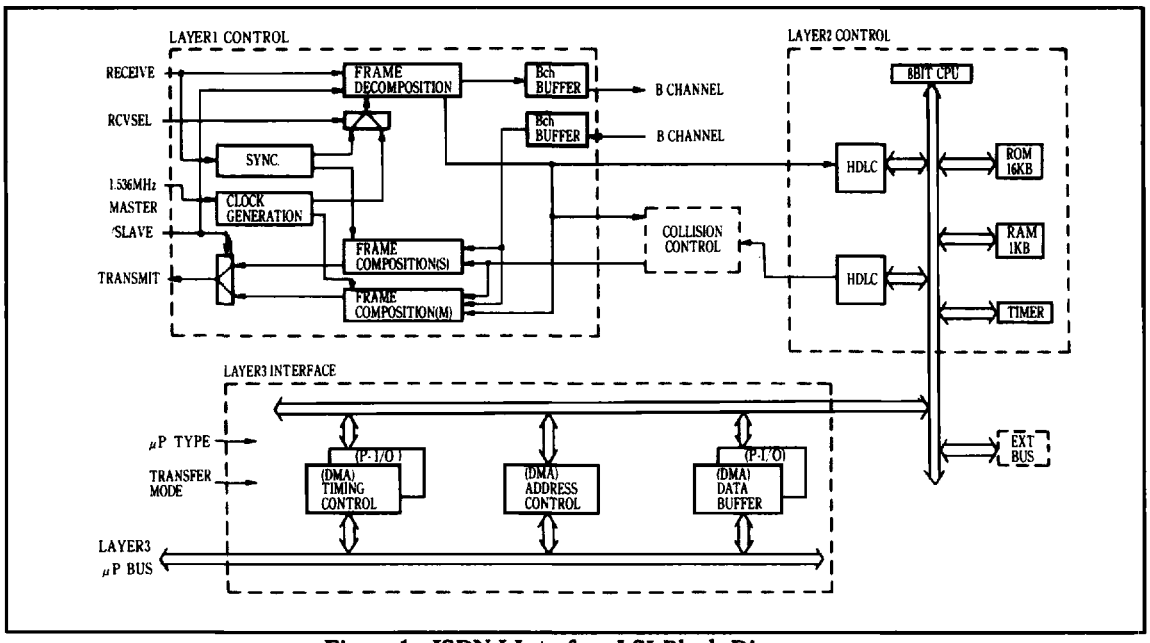
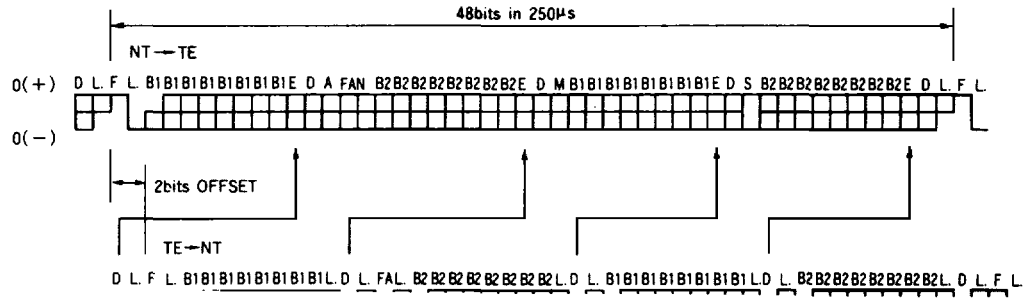


Figure 1. ISDN I-Interface LSI Block Diagram



F = Framing Bit
L. = DC Balancing Bit
D = D-Channel Bit
E = D-Echo-Channel Bit
FA = Auxiliary Framing Bit
N = Bit Set to a Binary Value N=Not (FA)
B1 = Bit within B-Channel 1
B2 = Bit within B-Channel 2
A = Bit used for Activation
S = Reserved for Future Standardization
M = Multiframing Bit

Notes 1. Dots(.) demarcate those parts of the frame that are independently DC-balanced.
2. FA bit (TE→NT) is used as Qbit every 5 frame at multiframing.
3. Nominal 2 bits offset is applied at TE output point. The offset at NT point might become large by the interface cable delay or connection configuration. The offset at LSI point is adjusted to 1.5 bits offset.

Figure 2 Frame Structure at Reference Point S and T

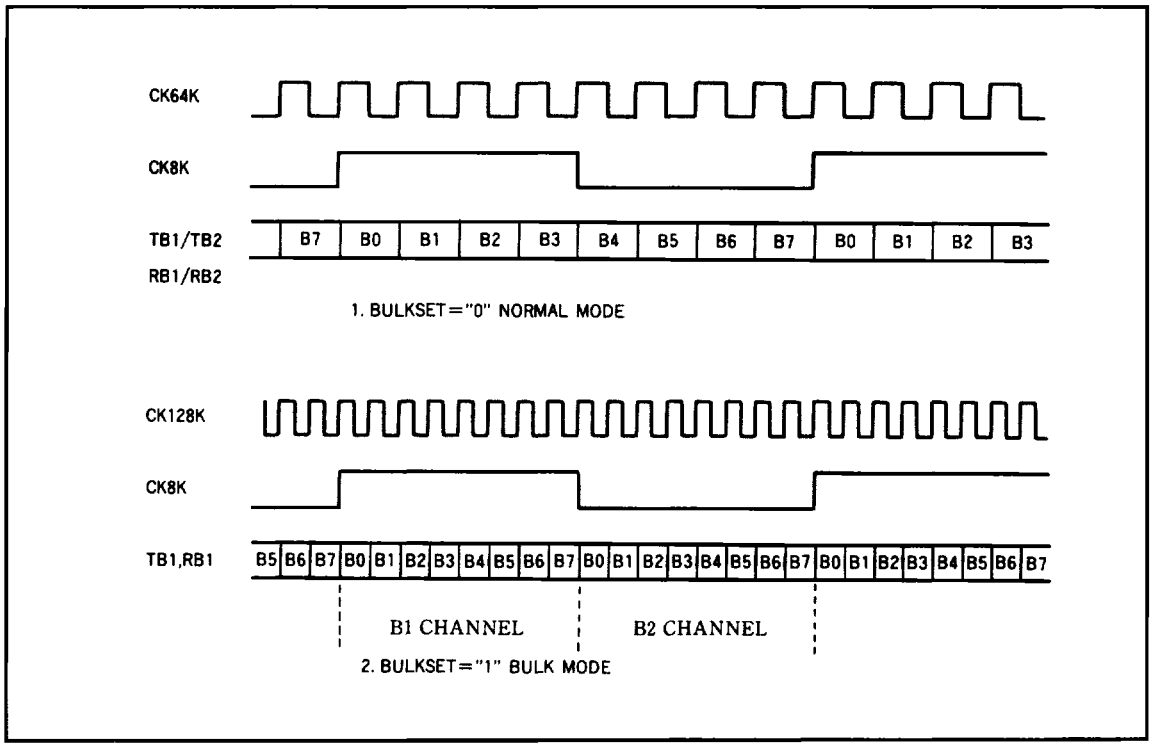


Figure 3 B-Channel Input/Output Timing

3. HDLC Part

HDLC part performs specification about HDLC (High level Data Link Control) format in layer2 protocol, LAPD (Link Access Protocol on the D channel) following ITU-T Recommendation I. 441.

That is, this part functions contain the following; formatting/deformatting of layer2 frame which is composed of opening flag, address field, control field, information field, FCS (Frame Check Sequence) and closing flag, 0 insertion/deletion for transparency, FCS generation/check, detection of invalid frame and generation/check of abort/idle signals. This part is also controls retransmission sequence.

HDLC part is composed of transmit part and receive part.

4. Layer2 State Control Microprocessor Part

This part performs status control of LAPD and interface control to layer3 interface part and HDLC control part. Status control is as follows: flow control, error control and DLCI (SAPI, TEI) control.

Layer2 microprocessor is composed of two parts. One is internal memory part with 16kB ROM and 1kB RAM, and the other is CPU core compatible with 64180Z. 16kB ROM is implanted LAPD software for terminal equipment (slave mode). Internal LAPD firmware is automatically operated as follows.

(1) Circuit switching mode ... Not connected to external RAM. Only SAPI=0 available.
(2) Packet switching mode ... Connected to external RAM (8kB). SAPI=0 and 16 available.

And also, program made by user can be executed on the external ROM/RAM by switching memory space area from internal to external. Memory and I/O maps are shown in Figure 4.

5. Layer3 Interface Part

This block performs interface function to connect to layer3 microprocessor which realizes function following ITU-T Recommendation I. 451.

General 16Bit and 8Bit microprocessors are available. That is, microprocessor type can be selectable out of 80 series (8086, Z80, 64180), 68 series (6800, 6809) and 68000 series.

Transfer mode can be also selectable out of DMA transfer mode and programmed I/O transfer mode.

This LSI contains BUS ARBITER for other DMAC to perform bus arbitration between external and internal DMACs, so this can be applied for various kinds of system configurations.

Logical interface between layer2 and layer3 is performed by primitive specified ITU-T Recommendation I. 441.

5.1 Layer3 Control Microprocessor Interface Function

(1) Selection of Layer3 Microprocessor

Layer3 microprocessor type can be selected by using CPU1 and CPU2 pins.

This can be connected to three types of 16bit and 8bit microprocessors, but data transfer width is limited to 8bits.

(2) Selection of Transfer Mode

Transfer mode is changeable by setting DMA/IO pin.

At DMA transfer mode, layer3 processor must inform start address of this LSI. Transfer word numbers is set by length information in primitive format. Function of built-in DMAC is shown in table 3.

(3) Control Primitives

This LSI can be connected to layer3 buses by interface primitives of which format is designed based on CCITT Recommendation primitives.

5.2 Hardware Interface between Layer2 and Layer3

(1) Connection to Layer3 Microprocessor

Connection to layer3 microprocessor is shown in table 4. Data bus width is limited to 8bits. Therefore, in case of connection to 16bit CPU at DMA transfer mode, a few external circuits may be required. For example, at 8086 type, $\overline{UDS}$ may control ADDR0 and $\overline{BHE}$ with additional circuit for access to either odd address or even address. At 8086 type, OAD19 pin is changed to $\overline{READY}$ input pin to control slow speed memory. At 6809 type, memory access is inhibited during the DEAD-CYCLE.

(2) Accessible Register from Layer3 Processor

DATA Register and MASK Register are available for data transfer to/from layer3 processor, as shown in table 5. These registers can be accessed by OAD0 and $\overline{CS}$ pins.

DATA Register is used for input/output of primitive at I/O transfer mode. At DMA transfer mode, this is used as control register for notice of DMA direction and setting address of transfer memory buffer. To set address, layer3 processor must transmit 3bytes addresses continuously (low byte; A0-A7, middle byte: A8-A15, high byte: A16-A19).

MASK Register is used for mask set to $\overline{INTR0}$ and $\overline{INTR1}$, and clear for $\overline{INTR2}$ and $\overline{INTR3}$.

(3) Interrupt Outputs to Layer 3 Processor

Interrupt outputs ($\overline{INTR0}$–$\overline{INTR3}$) are low-active, and connected to INTERRUPT CONTROLLER of layer3 system.

At I/O transfer mode, only $\overline{INTR0}$ and $\overline{INTR1}$ are available, and at DMA transfer mode, $\overline{INTR1}$–$\overline{INTR3}$ are used. Interrupt function is shown in table 6.

Table 3 Built-In DMA

Item	Content
Priority to Ext. DMAC	Contains
DMA Channels	2: Receive/Transmit
Address Bus Width	20 Bit
Data Bus Width	8 Bit
Number of Transfer Words	267Bytes: Maximum
Address Increment	+1
Notice for DMA End	Interrupt x 2; ($\overline{INTR2}$, $\overline{INTR3}$)
Vector Generation	No

NOTE . . . Operation condition at DMA mode
Transmit/Receive . . . set start address (layer3 microprocessor)
indicate DMA activation (layer3 microprocessor)
notice DMA End (layer2 microprocessor)

Table 4 Connection to Layer3 Processor Interface

Pin Name	80 Series (8086)		68 Series (6809)		60 Series (68000)	
	P-I/O Mode	DMA Mode	P-I/O Mode	DMA Mode	P-I/O Mode	DMA Mode
CPU1	0	0	1	1	0	0
CPU2	0	0	0	0	1	1
DMA/IO	0	1	0	1	0	1
$\overline{CS}$	Input	Input at Address Set	Input	Input at Address Set	Input	Input at Address Set
$\overline{INTR0}$	Read Request	Open	Read Request	Open	Read Request	Open
$\overline{INTR1}$	Write Request	Write Request	Write Request	Write Request	Write Request	Write Request
$\overline{INTR2}$	Open	DMA Read End	Open	DMA Read End	Open	DMA Read End
$\overline{INTR3}$	Open	DMA Write End	Open	DMA Write End	Open	DMA Write End
OD0–OD7	D0–D7	D0–D7	D0–D7	D0–D7	D0–D7	D0–D7
OAD0	ADDR1	ADDR1	A0	A0	A1	A1
OAD1–OAD18	Open	ADDR2–ADDR19	Open	A1–A15	Open	A2–A19
OAD19	Pull Up	Input Inverted Ready Signal (If Unused, Pull Up)	Pull Up	Pull Up	Pull Up	A20 etc.
L3CLK	CPU CLK		E CLK		CPU CLK	
HOLT	Open	Hold "H" Active	Open	$\overline{DMA}/\overline{BREQ}$ "L" Active	Open	$\overline{BR}$ "L" Active
HLTA	Pull Down	HLDA "H" Active	Pull Down	BA "H" Active	Pull Up	$\overline{BG}$ "L" Active
OWR	$\overline{WR}$		R/$\overline{W}$		R/$\overline{W}$	
ORD	$\overline{RD}$		Pull Up		Pull Up	
M/$\overline{IO}$	Open	Inverted to M/$\overline{IO}$	Open		Open	
$\overline{AS}$	Pull Up		Pull Up		$\overline{AS}$	
$\overline{UDS}$	Open	Inverted to $\overline{BHE}$ Non-inverted to ADDR0	Open		Open	$\overline{UDS}$
$\overline{LDS}$	Pull Up		Pull Up		$\overline{LDS}$	
$\overline{DTA}$	Pull Up		Pull Up		$\overline{DTACK}$	
$\overline{BGA}$	Pull Up		Pull Up		$\overline{BGACK}$	
EXHOLT	Pull Down	External DMAC If Unused, Pull Down.	Pull Up	External DMAC If Unused, Pull Up.	Pull Up	External DMAC If Unused, Pull Up.
EXHLTA	Open	External DMAC or Open.	Open	External DMAC or Open.	Open	External DMAC or Open.

Table 5 Accessible Registers from Layer3 Microprocessor

Address	Name	Read	Write	Notes
OAD0		DB DB DB DB DB DB DB DB DB DB DB DB DB DB DB DB		
		7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	
0	I/O Data Register	D7 D6 D5 D4 D3 D2 D1 D0	D7 D6 D5 D4 D3 D2 D1 D0	Read/Write at P-I/O Write only at DMA
1	Ext. Mask Register	D. C	OMSK1 OMSK0 D. C	CLWED CLRED OMSK1 OMSK0

OMSK0, OMSK1: "1" at Mask. "1" at Initial Reset
CLRED: "1" for Clear of $\overline{INTR2}$ CLWED: "1" for Clear of $\overline{INTR3}$
CLWED and CLRED are automatically reset after $\overline{INTR2}$ and $\overline{INTR3}$ Clear.
$\overline{INTR2}$ and $\overline{INTR3}$ are non maskable.

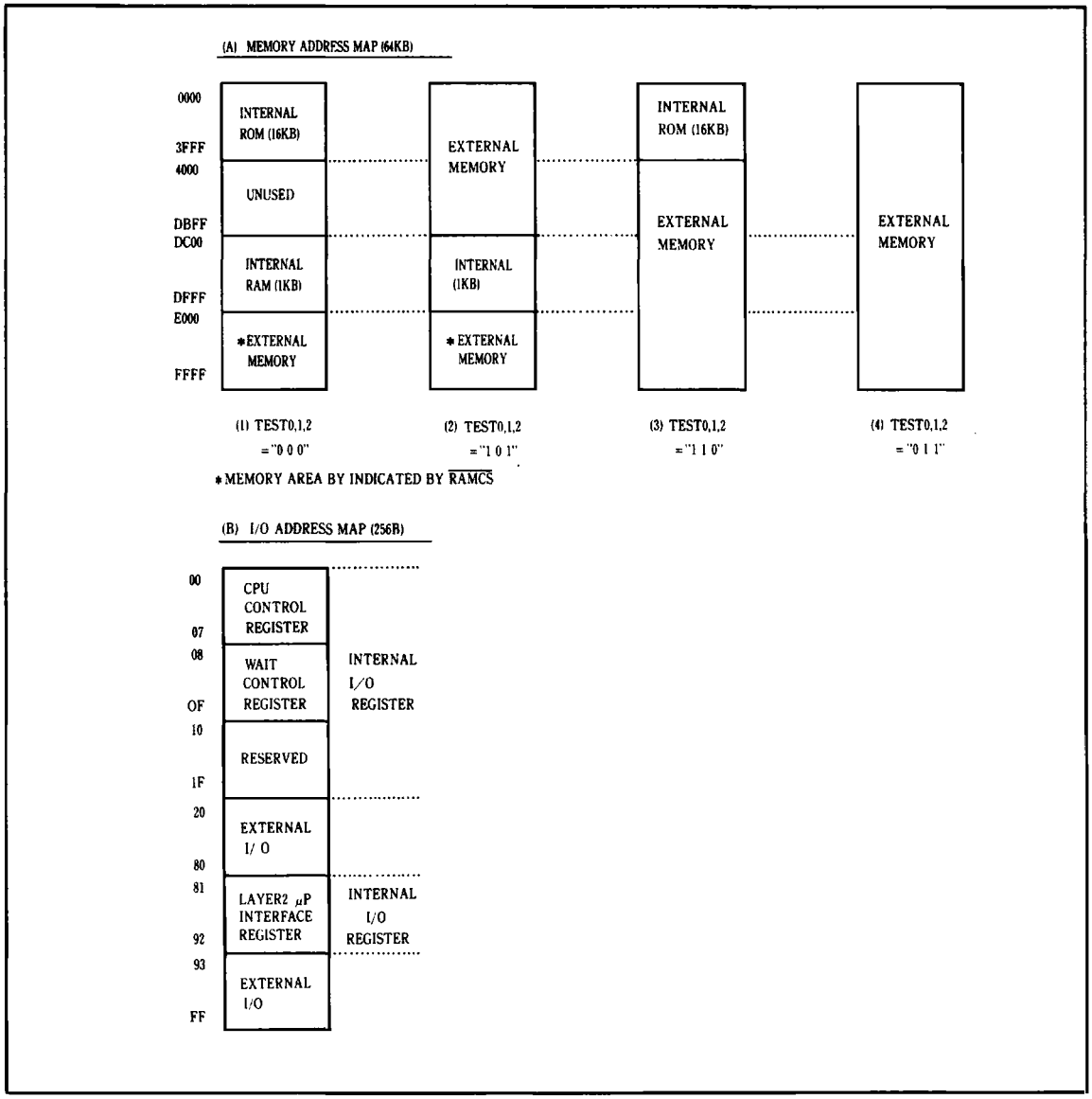


Figure 4 Memory and I/O Address Map

5.3 Primitive Interface between Layer2 and Layer3

Interface primitive between layer2 and 3 corresponds to primitive based on ITU-T Recommendation I. 441.

(1) Available Interface Primitive

Available interface primitive of this LSI is shown in table 7.

(2) Interface Primitive Format

Interface primitive format is shown in figure 5. and content of individual part is shown in table 7. Common part expresses the attribute of interface primitives and individual part expresses parameters or data corresponding to each interface primitive.

(3) DMA Transfer Mode

a) DMA Read Sequence

After setting primitives on the layer3 RAMs, layer3 microprocessor must indicate start addresses to LSI. At first, layer3 microprocessor may output address discrimination ("53H") to I/O data register. After that, it must output 3 bytes address data continuously, that is, high byte (OAD19-OAD16), middle byte (OAD15-OAD8) and low byte (OAD7-OAD0), Upper 4bits (5bits at 8086 type) in high byte are invalid. Every write cycle of programmed transfer may be controlled by $\overline{\text{INTR1}}$ indicating write request. After setting addresses by programmed transfer, DMA sequence will be automatically start to read primitives on layer3 RAMs. At the end of reading primitives, $\overline{\text{INTR2}}$ will be activated. Layer3 microprocessor must set bit2 (CLRED) in mask register to "1" after detecting $\overline{\text{INTR2}}$. At this time, other bits must not be changed.

b) DMA Write Sequence

Addresses setting at DMA write sequence is the same as at DMA read sequence, except for address discrimination ("52H"). At the end of writing primitive on layer3 RAMs, $\overline{\text{INTR3}}$ will be activated to indicate DMA write end. Layer3 microprocessor must set bit3 (CLWED) in mask register to "1" after receiving $\overline{\text{INTR3}}$, and then new addresses of receive buffer must be indicated again to LSI by layer3 microprocessor. CLWED and CLRED will be automatically reset after acknowledgement by layer2 microprocessor. Number of transfer words is indicated by 6th and 7th octets in primitive format.

(4) I/O Transfer Mode

Layer3 microprocessor may write and read primitives every 1 byte according to $\overline{\text{INTR0}}$ or $\overline{\text{INTR1}}$. At both DMA and programmed I/O transfer modes, $\overline{\text{INTR0}}$ and $\overline{\text{INTR1}}$ are maskable. But, $\overline{\text{INTR0}}$ is not used at DMA transfer mode.

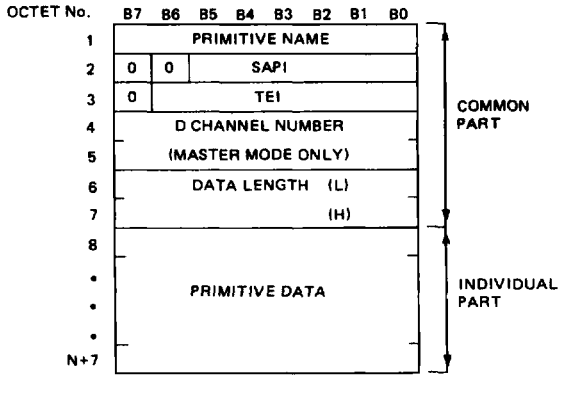
Table 6 Interrupt Pins Function

Pin	Function	Set Condition ("Low" Active)	Reset Condition	Note
$\overline{\text{INTR0}}$	Read Request from Data Register	When output data is set in data register.	When Layer3 microprocessor completes reading output data from data register.	Only Programmed I/O Transfer Mode
$\overline{\text{INTR1}}$	Write Request to Data Register	When data register goes empty and turns into "Write Enable".	When input data is set in data register by Layer3 microprocessor.	Programmed I/O Transfer Mode. DMA Transfer Mode for Address Setting.
$\overline{\text{INTR2}}$	Notice of DMA Transfer End (Layer3→Layer2)	When 1 primitive is transfered to Layer2 microprocessor.	When Bit2 (CLRED) in mask register is set to "1".	DMA Transfer Mode
$\overline{\text{INTR3}}$	Notice of DMA Transfer End (Layer2→Layer3)	When 1 primitive is transfered to Layer3 Bus.	When Bit3 (CLWED) in mask register is set to "1".	DMA Transfer Mode

Table 7 Interface Primitive

L-Name	G-Name	Type	Direction	Individual Part
DL	Establish	Request	L3→L2	B7 B6 B5 B4 B3 B2 B1 B0 / D.C / 1
		Indication	L3←L2	
		Confirm	L3←L2	
	Release	Request	L3→L2	B7 B6 B5 B4 B3 B2 B1 B0 / ERRID / V / D.C / 1
		Indication	L3←L2	
		Confirm	L3←L2	
	Data	Request	L3→L2	B7 B6 B5 B4 B3 B2 B1 B0 / 1 / N
		Indication	L3←L2	
	Unit Data	Indication	L3←L2	N=Data Length

Notes 1. ERRID: Valid at DL-Release-Indication
00: Normal End 01: Link Establish N.G 10: Link Release N.G
11: Information Retransmission N.G
2. V: Valid at DL-Release-Indication
0 = Voltage Detection On, 1 = Voltage Detection Off



Notes 1. PRIMITIVE NAME

LNAME: LAYER NAME 01; layer2-layer3 (DL)
OTHERS; UNDEFINED
GNAME: ATTRIBUTE 0000; LINK ESTABLISH
0001; LINK RELEASE
0010; DATA TRANSFER
0011; UNIT DATA TRANSFER
OTHERS; UNDEFINED
TYPE: 00; REQUEST
01; INDICATION
10; UNDEFINED
11; CONFIRM

2. SAPI 000000: SIGNAL
010000: PACKET
OTHERS; UNDEFINED

3. TEI 1111111: GLOBAL TEI
1000000:
| AUTO-ASSIGNED TEI
1111110:

4. Primitive attribute is expressed in common part.
5. Parameters and data of each primitive is expressed in individual part.
6. At slave mode, "0" should be set in octet No. 4 and 5.

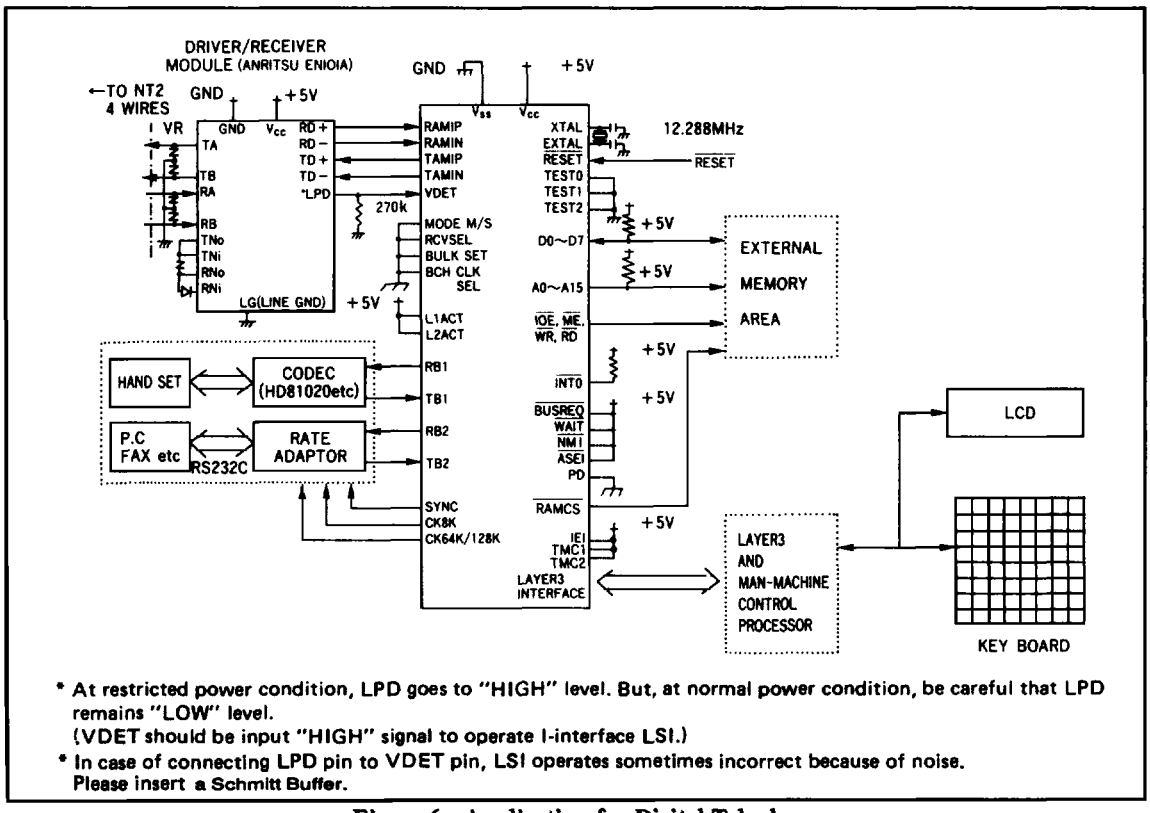
Figure 5 Interface Primitive Format

Application

The ISDN I-INTERFACE LSI is applied for digital telephones and NT2 systems. This LSI can control all functions required for layer1 and layer2 of ISDN system equipments. Therefore, the digital telephone system requires only the additions of the microprocessor for layer3 and man-machine interface, codecs and driver/receiver module for line interface.

NT2 has two interfaces. The LSI connecting to S point is used as master. The LSI connecting to T point is used as slave. This LSI is used as both controller, and the B channels can be directly connected with each other.

Digital telephone set system using this LSI is shown in figure 6. Layer3 bus interface examples are shown in figure 7 and figure 8.



* At restricted power condition, LPD goes to "HIGH" level. But, at normal power condition, be careful that LPD remains "LOW" level.
(VDET should be input "HIGH" signal to operate I-interface LSI.)
* In case of connecting LPD pin to VDET pin, LSI operates sometimes incorrect because of noise. Please insert a Schmitt Buffer.

Figure 6 Application for Digital Telephone

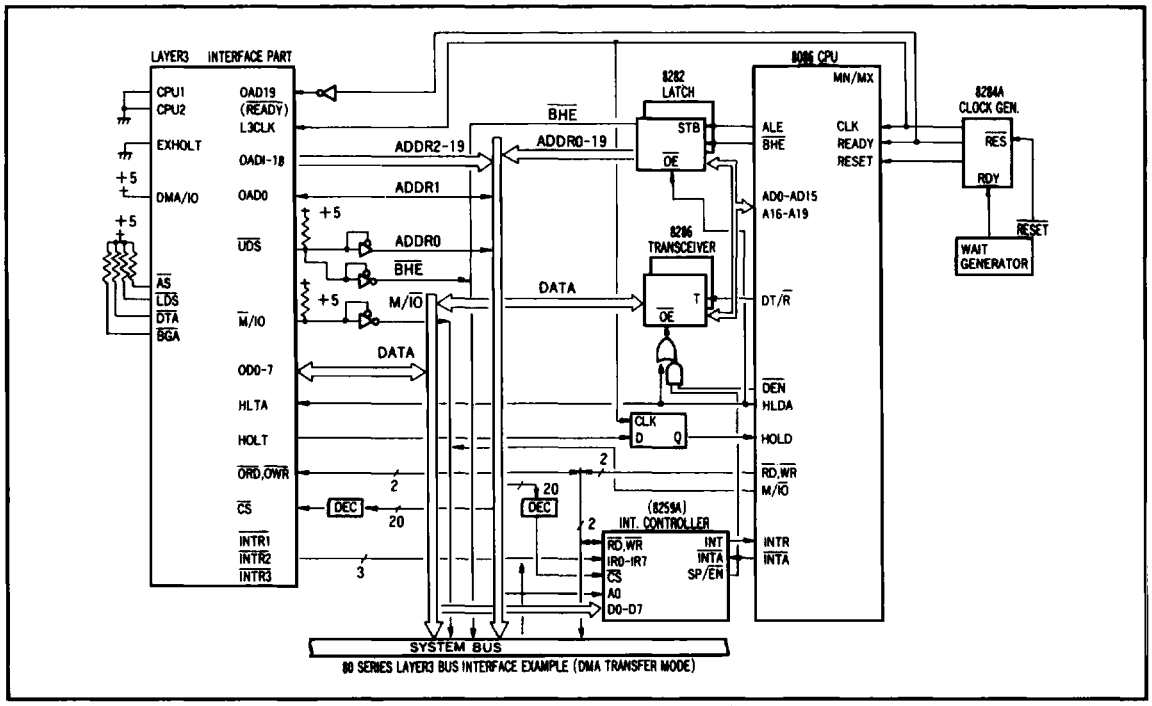


Figure 7 80 Series Layer3 Bus Interface Example (DMA Transfer Mode)

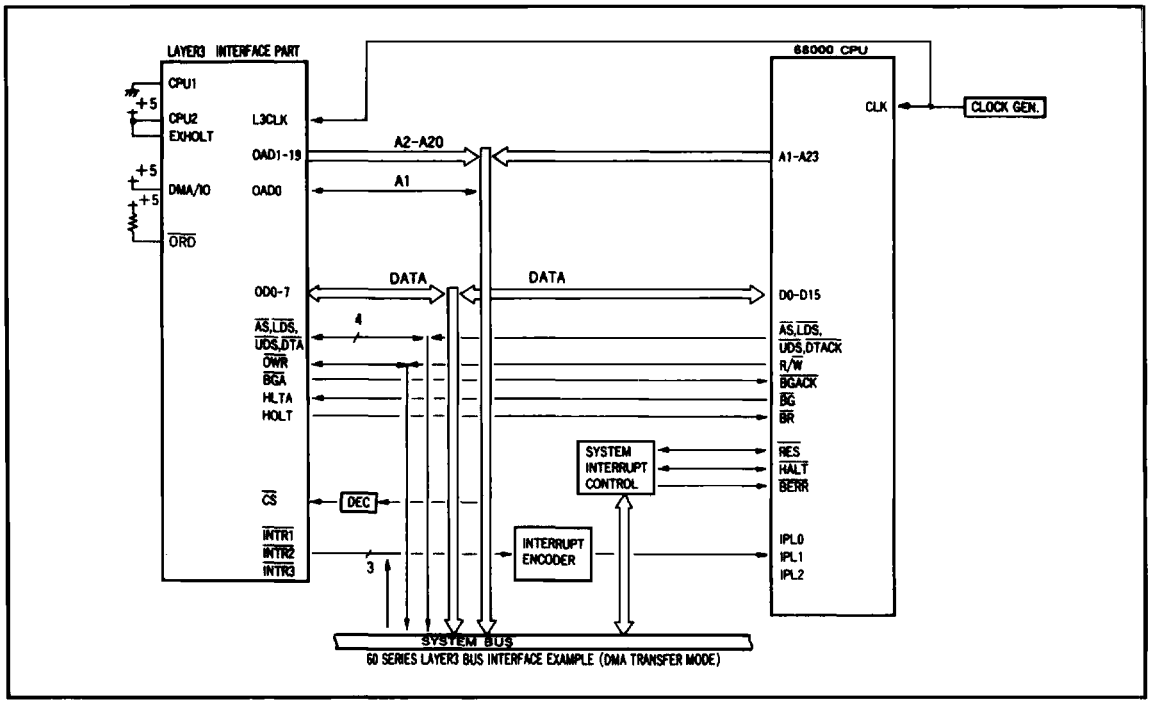


Figure 8 60 Series Layer3 Bus Interface Example (DMA Transfer Mode)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to V_{CC} +0.3	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

Notes 1. This product has protection circuits in input terminals against high electrostatic voltage or high electric fields. Not withstanding, be careful not to apply any voltage higher than the absolute maximum rating to these high input impedance circuits.
To assure normal operation, we recommend V_{in}, V_{out}; $V_{ss} \leqq (V_{in}$ or $V_{out}) \leqq V_{CC}$.

2. The flat package with absorbed moisture might be cracked under reflow processing. To prevent crack, we recommend you should bake packages at 125°C for about 24 hours before reflow process.
Package tray is heat-proof and the tray can be baked with packages.
After baking, the relative humidity and temperature should be under 60% and 30°C, respectively, and also, reflow process should be executed within 168 hours.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.00	5.25	V
Operating Temperature	T_{opr}	0	25	70	°C
Input Voltage	V_{in}	−0.3	–	V_{CC}+0.3	V

Electrical Characteristics (V_{CC}=5V±5%, V_{SS}=0V, Ta=0 to +70°C, Unless otherwise noted)

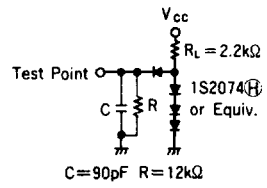
DC Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Input "HIGH" Voltage $\overline{RESET}$, EXTAL, $\overline{NMI}$	V_{IH1}	V_{CC}−0.6	–	V_{CC}+0.3	V	
Input "HIGH" Voltage OTHER INPUTS	V_{IH2}	2.2	–	V_{CC}+0.3	V	
Input "LOW" Voltage $\overline{RESET}$, EXTAL, $\overline{NMI}$	V_{IL1}	−0.3	–	0.6	V	
Input "LOW" Voltage OTHER INPUTS	V_{IL2}	−0.3	–	0.8	V	
Output "HIGH" Voltage ALL OUTPUTS	V_{OH}	2.4	–	–	V	I_{OH} = −200μA
		V_{CC}−1.2	–	–	V	I_{OH} = −20μA
Output "LOW" Voltage ALL OUTPUTS	V_{OL}	–	–	0.45	V	I_{OL} = 2.2mA
Input Leakage Current INPUTS except XTAL, EXTAL	$\|I_{IL}\|$	–	–	10	μA	V_{in} = 0.5V to V_{CC}−0.5V
Three-State Current	$\|I_{TL}\|$	–	–	10	μA	V_{in} = 0.5V to V_{CC}−0.5V
Power dissipation (Normal Operation)	I_{CC}	–	22	34	mA	No Load, CPU f = 6.144MHz*1
		–	14	20	mA	No Load, CPU f = 3.072MHz*2
Pin Capacitance	C_P	–	–	15	pF	

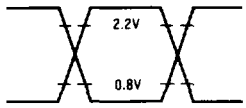
Notes 1. PD = 'LOW' 2. PD = 'HIGH'

AC Characteristics

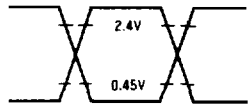
• Bus Timing Test Loads, Reference Level



Test Loads (TTL Loads)
(C=40pF for CPUCLK, CK12M)



Input Reference Level



Output Reference Level

· Line Interface

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Delay between RCV. Data and TX. Data	Rtd	–	1.5*1	–	Bit	Slave Mode (TE only) Fig. 9-1
X'tal Frequency Deviation	D_{XTL}	−100	–	100	p.p.m	I.430 8.1.2
Timing Extraction Jitter	J	−7	–	7	%	I.430 8.2.2 (TE only) (Short Passive Bus)
Total Phase Deviation	TPD	−7	–	15	%	I.430 8.2.3 (TE only) (Short Passive Bus)
Tolerance Round Trip Delay *2	Drt	12	–	16	μs	I.430 A2.1.2 (NT only) (Short Passive Bus) Fig. 9-2

Notes 1. In case of connecting to Driver/Receiver Module, delay is adjusted to 2 bits offset.
2. This delay is defined as the time of RAMI inputs delay from TAMI outputs of LSI.

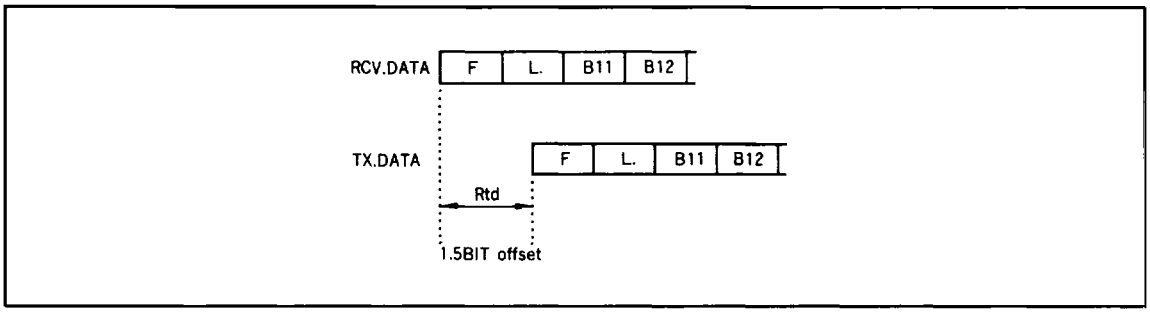


Figure 9-1 The offset from receive data to transmit data at slave mode

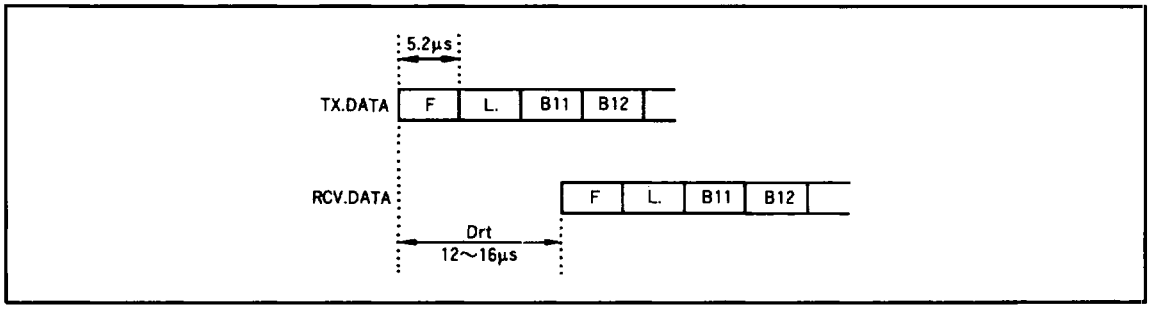


Figure 9-2 Torelance round trip delay in short passive bus at master mode

· B-Channel Interface

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Clock Period (Normal Use)	t_{BCYCN}	15.623	–	15.627	μs	Fig. 10-1 (f=64kHz)
Clock Period (Bulk Use)	t_{BCYCB}	7.811	–	7.814	μs	Fig. 10-2 (f=128kHz)
Clock Duty	Duty	45	50	55	%	Fig. 10-1, -2, $D=t_{CH}/t_{cyc}$
Clock Rise Time	t_{cr}	–	–	50	ns	Fig. 10-1, Fig. 10-2
Clock Fall Time	t_{cf}	–	–	50	ns	
Frame Clock deviation	t_{CD}	250	–	250	ns	
RCV. Data Output Delay	t_{BD}	–	–	1	μs	
TX. Data Set-up Time	t_{BS}	3	–	–	μs	
TX. Data Hold Time	t_{BH}	3	–	–	μs	

· D-Channel Interface

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Timing Clock Period	t_{RTCYC}	62.49	62.50	62.51	μs	Fig. 11 (RTIO)
Timing Clock Rise Time	t_{RTr}	–	–	50	ns	
Timing Clock Fall time	t_{RTf}	–	–	50	ns	
RCV. Dch Data Output Delay (Normal Mode)	t_{RD}	–	–	1.0	μs	Fig. 11 (RDIO)
TX. Dch Data Output Delay (Normal Mode)	t_{TD}	–	–	1.0	μs	Fig. 11 (TDIO)
RCV. Dch Data Input Timing (Layer 2 Mode)	t_{RD}	0	–	1.0	μs	Fig. 11 (RDIO)
TX. Dch Data Input Timing (Layer 1 Mode)	t_{TD}	0	–	1.0	μs	Fig. 11 (TDIO)

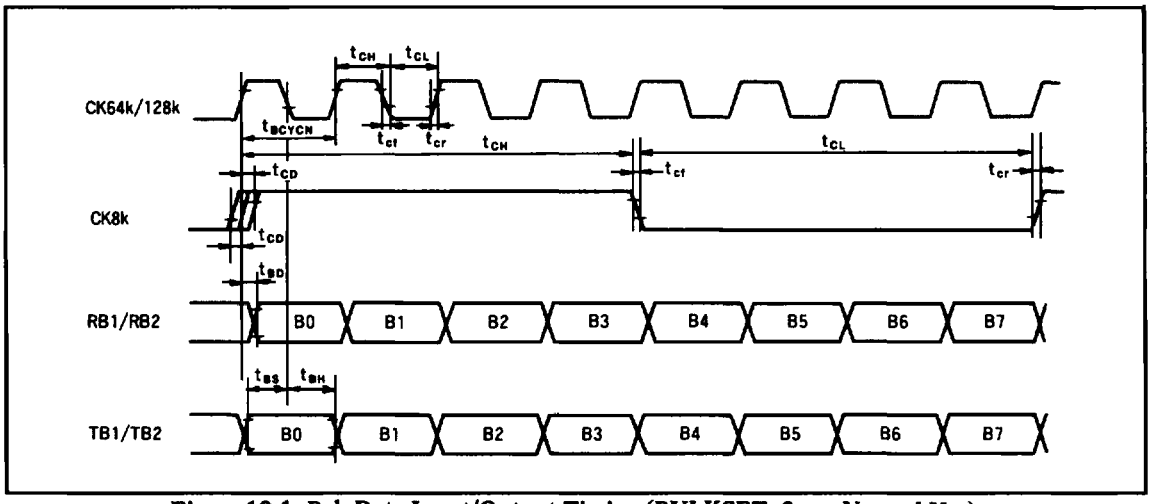


Figure 10-1 Bch Data Input/Output Timing (BULKSET=0 . . . Normal Use)

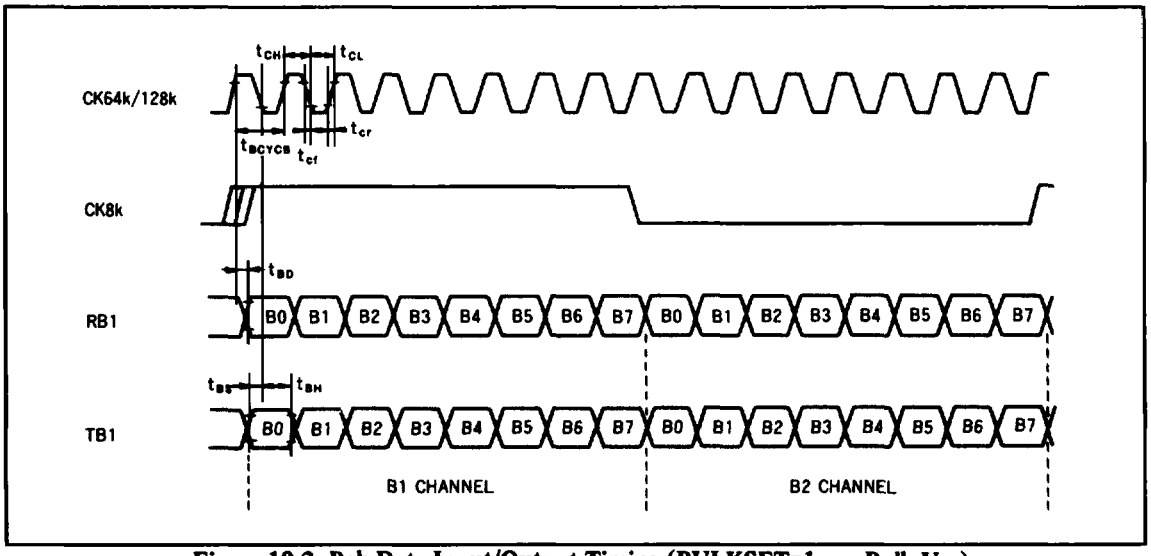


Figure 10-2 Bch Data Input/Output Timing (BULKSET=1 . . . Bulk Use)

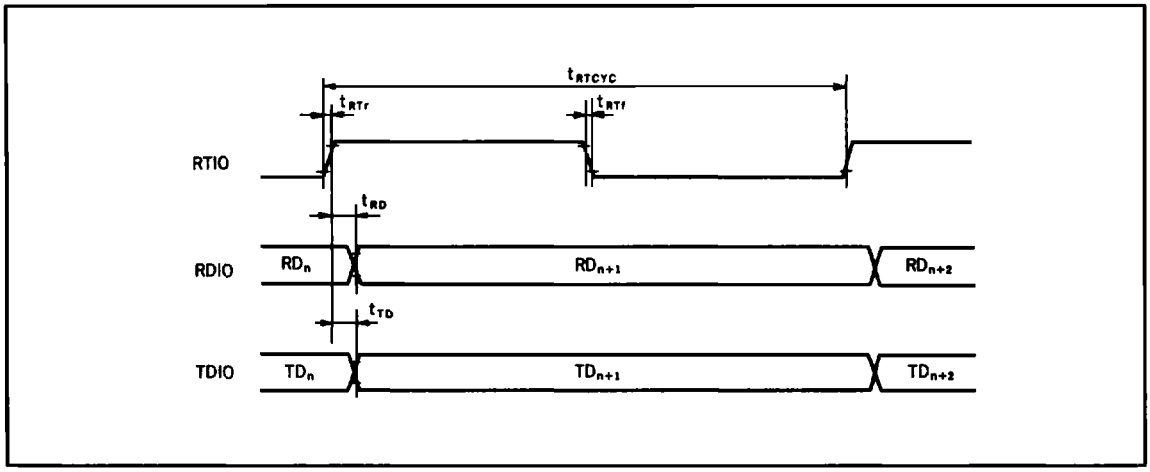


Figure 11 Dch Data Input/Output Timing

· Layer 2 CPU Interface

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Clock Period	t_{CYC}	162	–	333	ns	Fig. 14-1 (1)
Clock Pulse Width "HIGH"	t_{CHW}	57	–	–	ns	
Clock Pulse Width "LOW"	t_{CLW}	57	–	–	ns	
Clock Fall Time	t_{cf}	–	–	25	ns	
Clock Rise Time	t_{cr}	–	–	25	ns	
External Clock Rise Time	t_{EXr}	–	–	25	ns	Fig. 12
External Clock Fall Time	t_{EXf}	–	–	25	ns	
Address Delay Time	t_{AD}	–	–	90	ns	Fig. 14-1 (1)
Address Set-up Time (for $\overline{ME}$ or $\overline{IOE}\downarrow$)	t_{AS}	30	–	–	ns	
$\overline{ME}$ Delay Time 1	t_{MED_1}	–	–	60	ns	
$\overline{RD}$ Delay Time 1	t_{RDD_1}*1	–	–	65	ns	
$\overline{LIR}$ Delay TIme	t_{LD_1}	–	–	80	ns	
Address Hold Time (For $\overline{ME}$, $\overline{IOE}$, $\overline{RD}$ or $\overline{WR}\uparrow$)	t_{AH}	35	–	–	ns	
$\overline{ME}$ Delay Time 2	t_{MED_2}	–	–	60	ns	
$\overline{RD}$ Delay Time 2	t_{RDD_2}	–	–	60	ns	
$\overline{LIR}$ Delay Time 2	t_{LD_2}	–	–	80	ns	
Data Read Set-up time	t_{DRS}	50	–	–	ns	Fig. 14-1 (1), (2)
Data Read Hold Time	t_{DRH}	0	–	–	ns	
ST Delay Time 1	t_{STD_1}	–	–	90	ns	Fig. 14-1 (1)
ST Delay Time 2	t_{STD_2}	–	–	90	ns	
$\overline{WAIT}$ Set-up Time	t_{WS}	40	–	–	ns	
$\overline{WAIT}$ Hold Time	t_{WH}	40	–	–	ns	
Write Data Floating Delay Time	t_{WDZ}	–	–	95	ns	
$\overline{WR}$ Delay Time 1	t_{WRD_1}	–	–	65	ns	
Write Data Delay Time	t_{WDD}	–	–	90	ns	
Write Data Set-up Time (For $\overline{WR}\downarrow$)	t_{WDS}	35	–	–	ns	
$\overline{WR}$ Delay Time 2	t_{WRD_2}	–	–	80	ns	
$\overline{WR}$ Pulse Width	t_{WRP}	170	–	–	ns	
Write Data Hold Time (For $\overline{WR}\uparrow$)	t_{WDH}	40	–	–	ns	
$\overline{IOE}$ Delay Time 1	t_{IOD_1}*1	–	–	65	ns	
$\overline{IOE}$ Delay Time 2	t_{IOD_2}	–	–	60	ns	
$\overline{IOE}$ Delay Time 3 (For $\overline{LIR}\downarrow$)	t_{IOD_3}	340	–	–	ns	Fig. 14-1 (2)

Note 1. These values are specified from CPUCLK falling edge at $\overline{IOC}$="1", otherwise from CPUCLK rising edge at $\overline{IOC}$="0" (Z80 compatible mode).

Item	Symbol	Min	Typ	Max	Unit	Test Condition
$\overline{INT}$ Set-up Time (For CPUCLK↓)	t_{INTS}	40	–	–	ns	Fig. 14-1 (2)
$\overline{INT}$ Hold Time (For CPUCLK↓)	t_{INTH}	40	–	–	ns	
$\overline{NMI}$ Pulse width	t_{NMIW}	120	–	–	ns	
Bus Floating Delay time	t_{BZD}	–	–	125	ns	
$\overline{HALT}$ Delay Time 1	t_{HAD1}	–	–	90	ns	
$\overline{HALT}$ Delay Time 2	t_{HAD2}	–	–	90	ns	
$\overline{RESET}$ Set-up Time	t_{RES}	120	–	–	ns	Fig. 14-1 (1)
$\overline{RESET}$ Hold Time	t_{REH}	80	–	–	ns	
$\overline{RESET}$ Rise Time	t_{Rr}	–	–	50*1	ms	
$\overline{RESET}$ Fall time	t_{Rf}	–	–	50*1	ms	
Input Terminal Rise Time (Except $\overline{RESET}$)	t_{Ir}	–	–	100*1	ns	Fig. 13
Input Terminal Fall Time (Except $\overline{RESET}$)	t_{If}	–	–	100*1	ns	
Oscillation Start Time	t_{OSC}	–	–	20	ms	
Valid $\overline{RESET}$ Pulse Width	t_{RVALID}	6	–	–	cycle	

Note 1. Even if these specifications are satisfied, when other specifications are not, rise time and fall time should be set to be satisfied with such specifications.

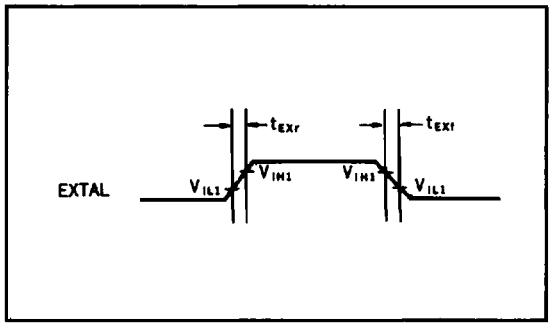


Figure 12 Rise/Fall Time of External Clock Input

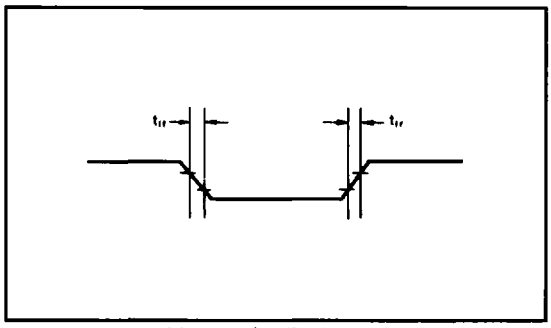
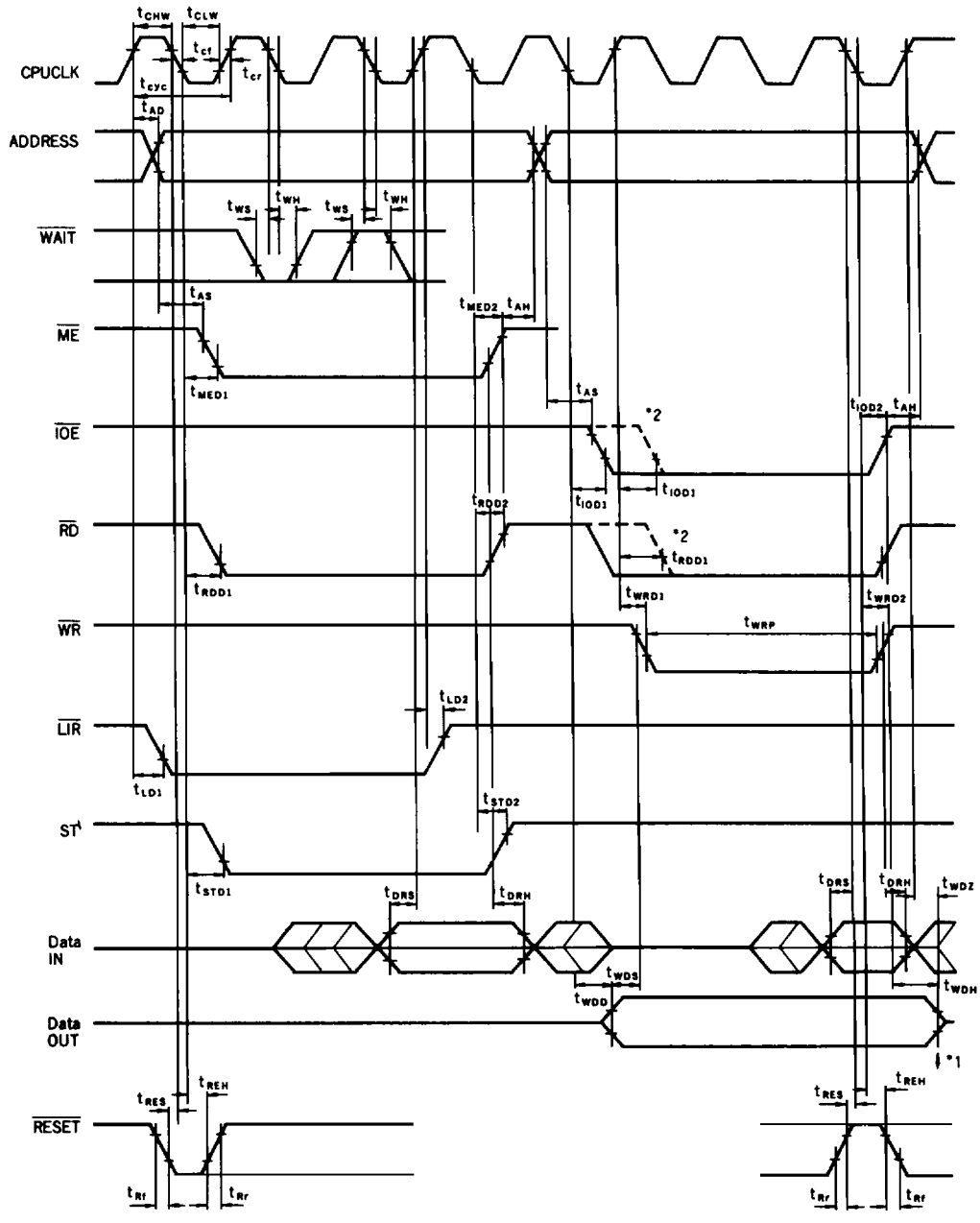
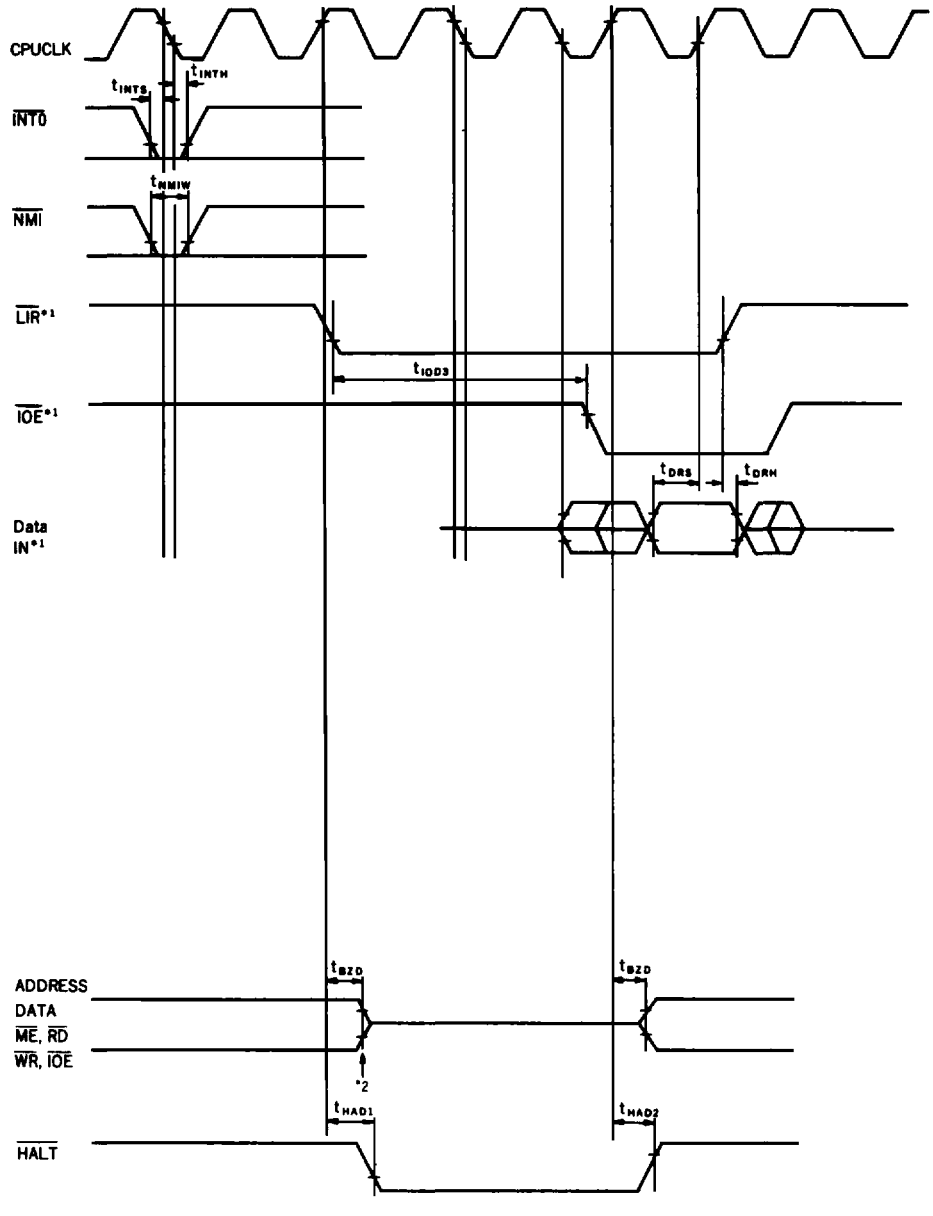


Figure 13 Rise/Fall Time of Inputs Except EXTAL, $\overline{RESET}$



Notes 1. At point of output buffer "OFF"
2. These Specifications are measured from CPUCLK falling edge at $\overline{IOC}$="1", otherwise from CPUCLK rising edge at $\overline{IOC}$="0" (Z80 compatible mode).

Figure 14-1 CPU Timing (1)



Notes 1. At point of INT0 Acknowledge Cycle
2. At point of output buffer "OFF"

Figure 14-2 CPU Timing (2)

· 80 Type Bus Interface

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Clock Period	t_{CLCL}	162	–	500	ns	Fig. 15-1, Fig. 15-2
Clock Pulse width "LOW"	t_{CLCH}	80	–	–	ns	
Clock Pulse width "HIGH"	t_{CHCL}	62	–	–	ns	
Clock Rise Time	t_{CH1CH2}	–	–	10	ns	
Clock Fall Time	t_{CL2CL1}	–	–	10	ns	
Address, $\overline{CS}$ Valid Delay	t_{CLAV}	10	–	80	ns	Fig. 15-1
$\overline{RD}$ Active Delay	t_{CLRL}	10	–	80	ns	
$\overline{RD}$ Inactive Delay	t_{CLRH}	10	–	80	ns	
Data Output Delay Time (Read Cycle)	t_{DVCL}	–	–	160	ns	
Data Hold Time (Read Cycle)	t_{CLDX}	10	–	–	ns	
$\overline{WR}$ Active Delay	t_{CVCTV}	10	–	80	ns	
$\overline{WR}$ Inactive Delay	t_{CVCTX}	10	–	80	ns	
Data Valid Delay	t_{CLDV}	–	–	110	ns	
Data Hold Time (Write Cycle)	t_{CHDX}	10	–	–	ns	
HLDA Valid Delay	t_{CLHAV}	10	–	100	ns	Fig. 15-2
Signal Active Delay (During DMA)	t_{DML}	–	–	160	ns	
Signal Inactive Delay (During DMA)	t_{DMH}	–	–	160	ns	
$\overline{READY}$ Set-up time (During DMA)	t_{RDYSET}	80	–	–	ns	
Data Hold time (During DMA)	t_{CLDXDM}	10	–	–	ns	
Data Set-up Time (During DMA)	t_{DVCLDM}	80	–	–	ns	
HOLT Inactive Delay	t_{DMLH}	–	–	200	ns	

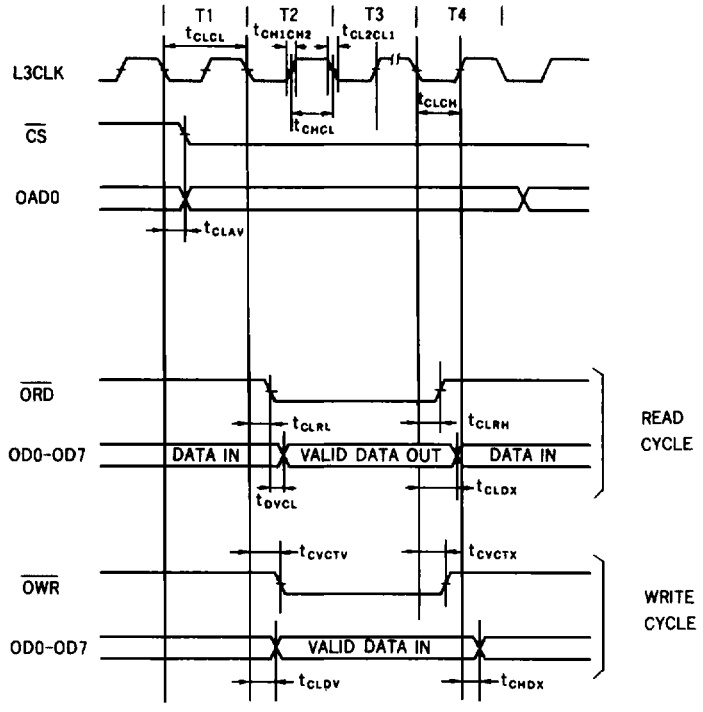
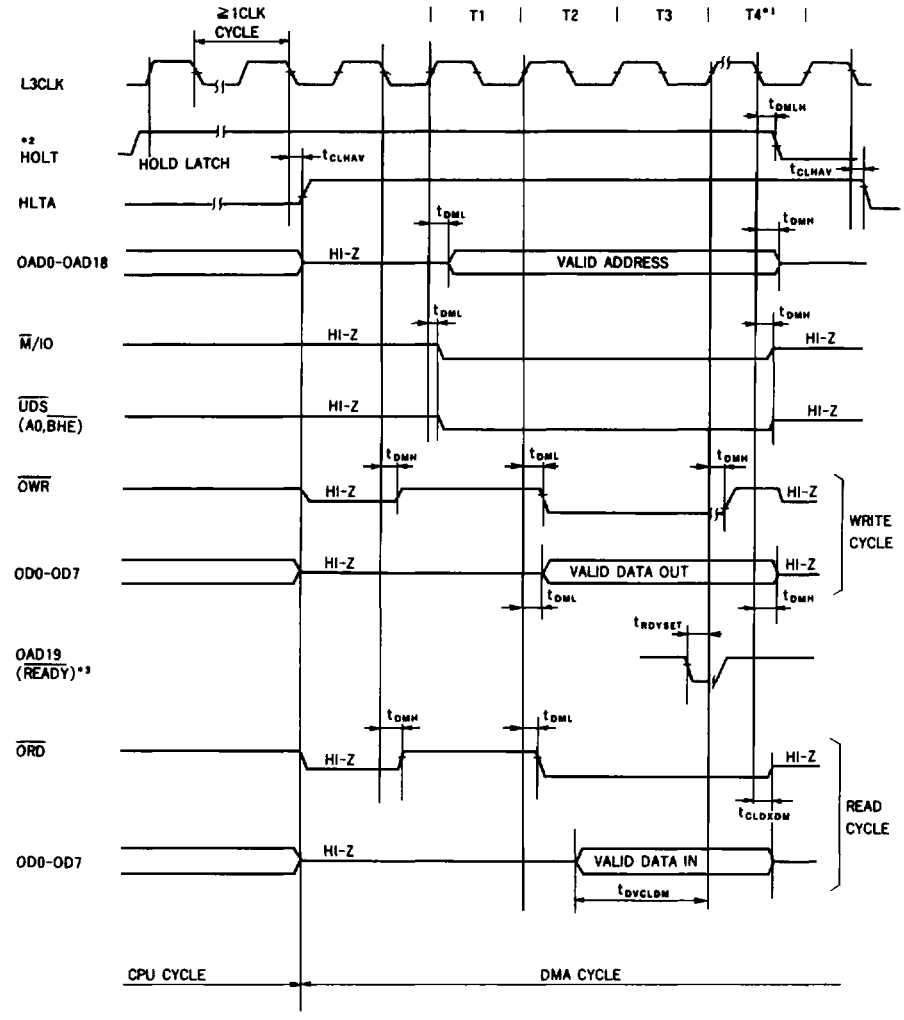


Figure 15-1 80 type I/O Mode Timing



Notes 1. During READY "LOW" cycle, each signal holds previous status and wait cycles are inserted.
2. HOLT isn't synchronized at L3 CLK rising edge. If synchronization is necessary, external circuit should make circuit should make synchronization to layer 3 clock.
3. OAD19 pin turns to READY input.

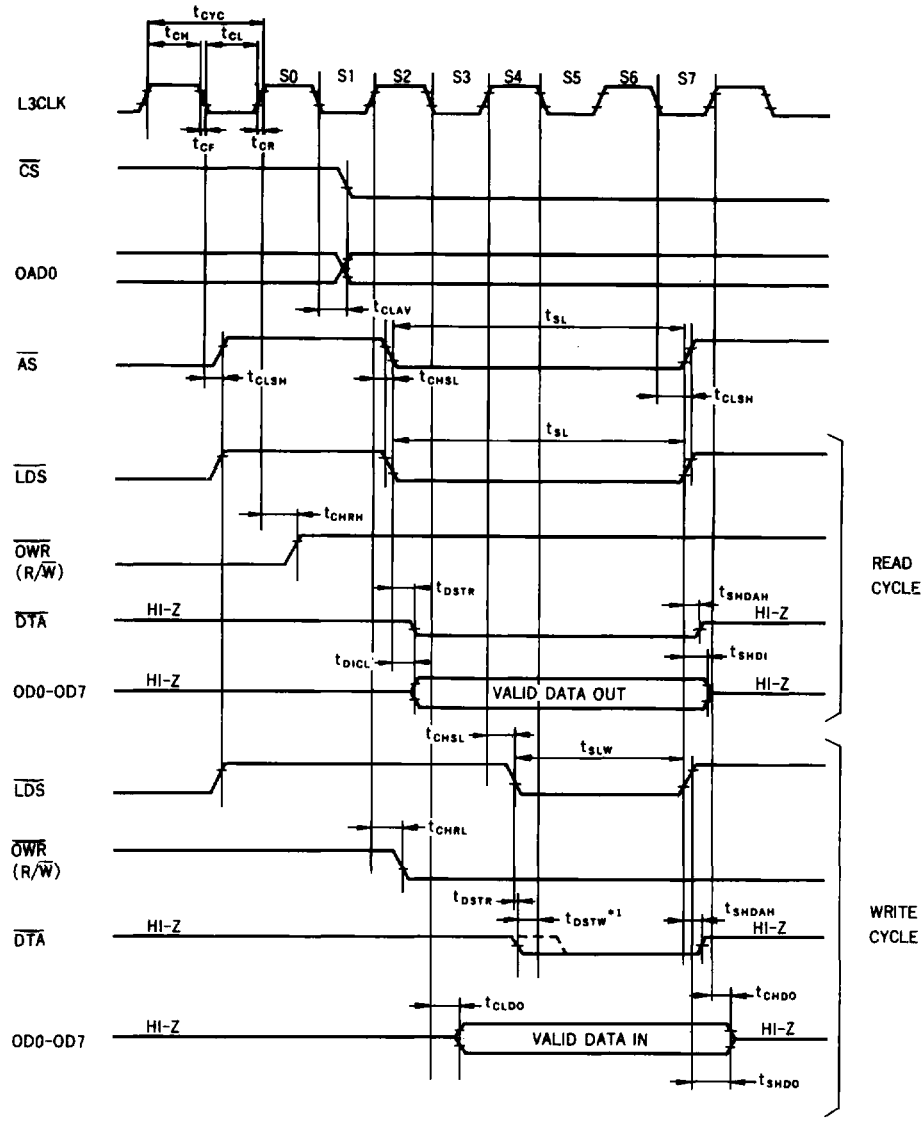
Figure 15-2 80 type DMA Mode Timing

• 60 Type Bus Interface

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Clock Period	t_{CYC}	162	–	500	ns	
Clock Pulse Width "LOW"	t_{CL}	75	–	250	ns	
Clock Pulse Width "HIGH"	t_{CH}	75	–	250	ns	Fig. 16-1, Fig. 16-2
Clock Fall Time	t_{CF}	–	–	10	ns	
Clock Rise Time	t_{CR}	–	–	10	ns	
Address Valid Delay	t_{CLAV}	–	–	80	ns	
$\overline{AS}$, $\overline{LDS}$ Active Delay	t_{CHSL}	0	–	70	ns	
$\overline{AS}$, $\overline{LDS}$ Inactive Delay	t_{CLSH}	–	–	80	ns	
$\overline{AS}$, $\overline{LDS}$ Pulse Width "LOW" (Read Cycle)	t_{SL}	337	–	–	ns	
R/$\overline{W}$="H" Active Delay	t_{CHRH}	10	–	80	ns	
$\overline{DTA}$ Active Delay (Read Cycle)	t_{DSTR}	0	–	140	ns	
$\overline{DTA}$ Hold Time	t_{SHDAH}	0	–	325	ns	
Data Output Delay Time (Read Cycle)	t_{DICL}	–	–	160	ns	Fig. 16-1
Data Hold Time (Read Cycle)	t_{SHDI}	0	–	–	ns	
$\overline{LDS}$ Pulse Width "LOW" (Write Cycle)	t_{SLW}	170	–	–	ns	
R/$\overline{W}$="H" Active Delay	t_{CHRL}	10	–	80	ns	
Data Valid Delay	t_{CLDO}	–	–	80	ns	
Data Hold Time (Write Cycle)	t_{CHDO}	0	–	–	ns	
$\overline{LDS}$→Data Invalid Time	t_{SHDO}	40	–	–	ns	

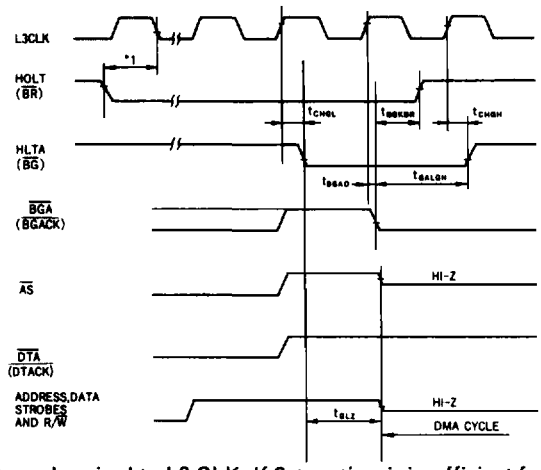
Note 1. In case of $t_{DSTW} \leqq 25$ns, wait state may be inserted between S4 and S5.

Item	Symbol	Min	Typ	Max	Unit	Test Condition
$\overline{BG}$ Valid Delay	t_{CHGL}	–	–	80	ns	
Strobe, R/$\overline{W}$ Float Delay	t_{GLZ}	–	–	160	ns	
$\overline{BGA}$"L"→$\overline{BG}$"H" Delay Time	t_{GALGH}	1.5	–	3.0	CLOCK	Fig. 16-2
$\overline{BG}$ Inactive Delay	t_{CHGH}	–	–	80	ns	
$\overline{BGA}$"L"→$\overline{BR}$"H" Delay time	t_{BGKBR}	20	–	–	ns	
$\overline{BGA}$ Valid Delay	t_{BGAD}	–	–	160	ns	
CLK"L"→Signal Delay Time	t_{CLAVD}	–	–	160	ns	
CLK"H"→Signal Delay Time	t_{CHAVD}	–	–	160	ns	
$\overline{DTA}$ Set-up Time	t_{DKST}	80	–	–	ns	Fig. 16-3
$\overline{DTA}$ Hold Time	t_{DKLH}	10	–	350	ns	
Data Set-up Time	t_{DICLD}	80	–	–	ns	
Data Hold Time	t_{SHDID}	20	–	–	ns	



Note 1. In case of $t_{DSTW} \leqq 25$ns under some load condition, Set-up time of $\overline{DTACK}$ may not be assured at S4 rising edge. Then, wait cycle is inserted for 1 clock period (2 wait status) between S4 and S5.

Figure 16-1 68000 type I/O Mode Timing



Note 1. HOLT isn't synchronized to L3 CLK. If Set-up time is insufficient for L3 CLK rising edge, HOLT is fetched by layer 3 CPU after 1 clock cycle.

Figure 16-2 68000 type Bus Arbitoration

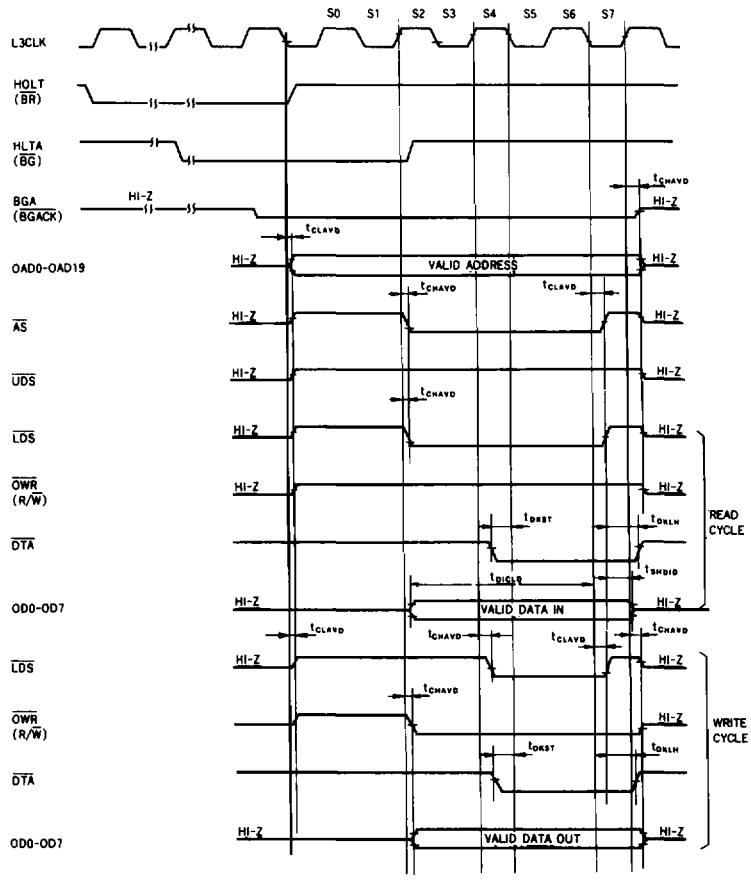


Figure 16-3 68000 type DMA Mode Timing

• 68 Type Bus Interface

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Clock Period	t_{CYC}	1.0	–	10.0	μs	Fig. 17-1, Fig. 17-2
Total Up Time	t_{UT}	975	–	–	ns	
Clock Pulse Width "HIGH"	t_{PWEH}	450	–	5500	ns	
Clock Pulse Width "LOW"	t_{PWEL}	430	–	5000	ns	
Clock Fall Time	t_{EF}	–	–	25	ns	
Clock Rise Time	t_{ER}	–	–	25	ns	
Address, R/$\overline{W}$ Valid Delay	t_{AD}	–	–	220	ns	
Address, R/$\overline{W}$ Hold Time	t_{AH}	20	–	–	ns	Fig. 17-1
Data Set-up Time (Read Cycle)	t_{DSR}	80	–	–	ns	Fig. 17-1, Fig. 17-2
Data Hold Time (Read Cycle)	t_{DHR}	20	–	–	ns	
Data Set-up Time (Write Cycle)	t_{DSW}	0	–	–	ns	Fig. 17-1
Data Hold Time (Write Cycle)	t_{DHW}	30	–	–	ns	
HOLT Delay Time	t_{PCSD}	–	–	350	ns	Fig. 17-2
Address Delay Time (DMA Cycle)	t_{ADDMA}	0.5	–	2.0	CYCLE OF CPU CLK	
Address Hold Time (DMA Cycle)	t_{ADH}	10	–	–	ns	

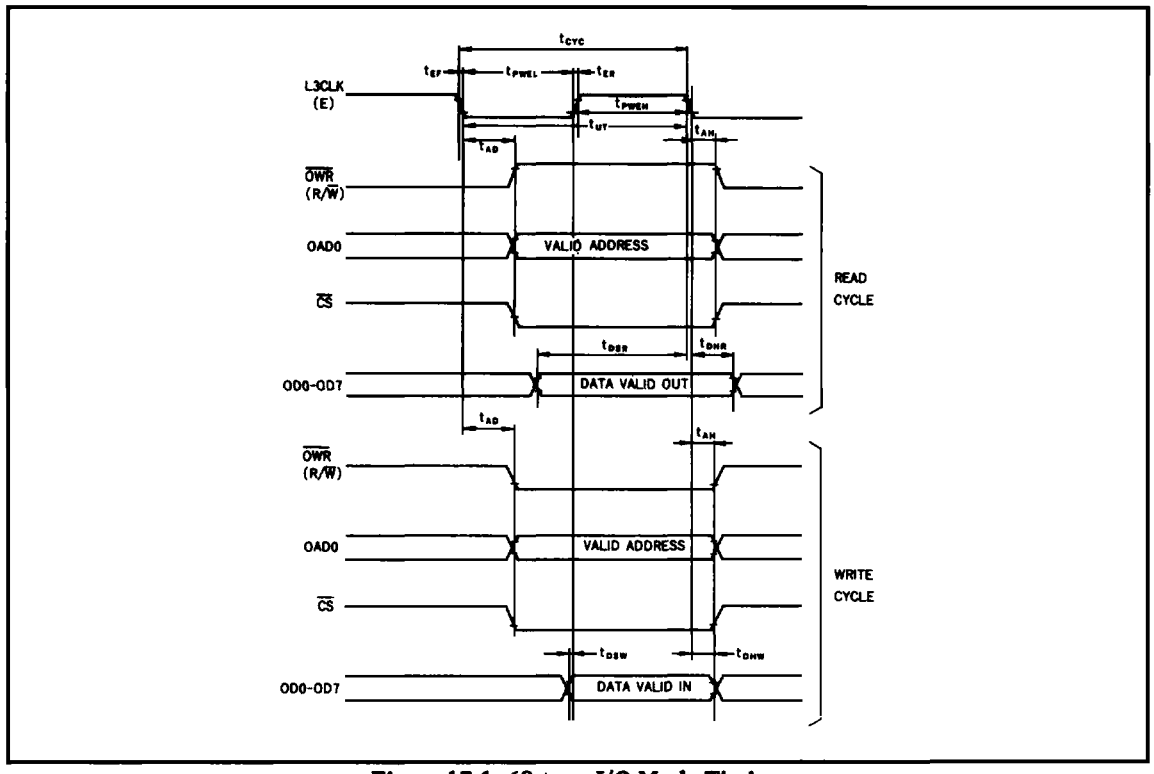
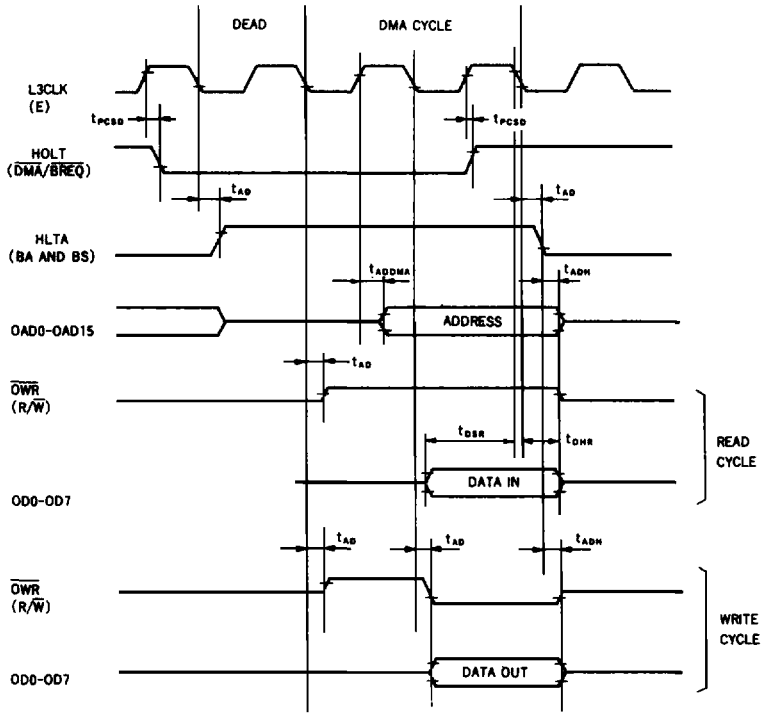


Figure 17-1 68 type I/O Mode Timing



Note 1. Memory access is inhibited during dead-cycle.

Figure 17-2 68 type DMA Mode Timing