

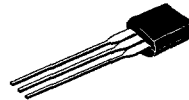
2N5484 SERIES N-Channel JFETs

The 2N5484 Series of n-channel JFETs is designed to provide high-performance amplification, especially at high-frequency. These parts feature low noise (4 dB max @ 400 MHz), high gain (5.5 mS typical @ 400 MHz) and provide wide bandwidth. Additionally, its low-cost TO-92 package is available with tape and reel to support automated assembly. (See Section 7.)

PART NUMBER	V _{GS(OFF)} MAX (V)	V _{(BR)GSS} MIN (V)	g _{fs} MIN (mS)	I _{DSS} MAX (mA)
2N5484	-3	-25	3	5
2N5485	-4	-25	3.5	10
2N5486	-6	-25	4	20

For additional design information please see performance curves NH.

TO-92 (TO-226AA)



BOTTOM VIEW



- 1 DRAIN
- 2 SOURCE
- 3 GATE

SIMILAR PRODUCTS

- SOT-23, See SST4416
- Chips, See NH Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V _{GD}	-25	V
Gate-Source Voltage	V _{GS}	-25	
Gate Current	I _G	10	mA
Drain Current	I _D	30	
Power Dissipation	P _D	360	mW
Power Derating		3.27	
Operating Junction Temperature Range	T _J	-65 to 135	°C
Storage Temperature Range	T _{stg}	-65 to 150	
Lead Temperature (1/16" from case for 10 sec.)	T _L	300	

2N5484 SERIES



SPECIFICATIONS ^a				LIMITS							
PARAMETER	SYMBOL	TEST CONDITIONS	TYP ^b	2N5484		2N5485		2N5486		UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX		
STATIC											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = -1 \mu A, V_{DS} = 0 V$	-35	-25		-25		-25		V	
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	$V_{DS} = 15 V, I_D = 10 nA$		-0.3	-3	-0.5	-4	-2	-6		
Saturation Drain Current ^c	I_{DSS}	$V_{DS} = 15 V, V_{GS} = 0 V$		1	5	4	10	8	20	mA	
Gate Reverse Current	I_{GSS}	$V_{GS} = -20 V, V_{DS} = 0 V$ $T_A = 100^\circ C$	-0.002		-1		-1		-1	nA	
			-0.2		-200		-200		-200		
Gate Operating Current ^d	I_G	$V_{DG} = 10 V, I_D = 1 mA$	-20							pA	
Gate-Source Forward Voltage ^d	$V_{GS(F)}$	$I_G = 10 mA, V_{DS} = 0 V$	0.8							V	
DYNAMIC											
Common-Source Forward Transconductance ^c	g_{fs}	$V_{DS} = 15 V, V_{GS} = 0 V$ $f = 1 kHz$		3	6	3.5	7	4	8	mS	
					50		60		75	μS	
Common-Source Output Conductance ^c	g_{os}				50		60		75	μS	
Common-Source Input Capacitance	C_{iss}	$V_{DS} = 15 V, V_{GS} = 0 V$ $f = 1 MHz$	2.2		5		5		5	pF	
Common-Source Reverse Transfer Capacitance	C_{rss}		0.7		1		1		1		
Common-Source Output Capacitance	C_{oss}		1		2		2		2		
Equivalent Input Noise Voltage ^d	\bar{e}_n	$V_{DS} = 15 V, V_{GS} = 0 V$ $f = 100 Hz$	10							nV/\sqrt{Hz}	
HIGH-FREQUENCY											
Common-Source Transconductance	Y_{fs}	$V_{DS} = 15 V$ $V_{GS} = 0 V$	$f = 100 MHz$	4.5	2.5					mS	
			$f = 400 MHz$	5.5			3		3.5		
Common-Source Output Conductance	Y_{os}		$f = 100 MHz$	30		75				μS	
			$f = 400 MHz$	50			100		100		
Common-Source Input Conductance	Y_{is}		$f = 100 MHz$			0.1				mS	
			$f = 400 MHz$				1		1		
Common-Source Power Gain	G_{ps}	$V_{DS} = 15 V, I_D = 1 mA$ $f = 100 MHz$	20	16	25					dB	
		$V_{DS} = 15 V$ $I_D = 4 mA$	$f = 100 MHz$	21			18	30	18		30
			$f = 400 MHz$	13			10	20	10		20
Noise Figure	NF	$V_{DS} = 15 V, V_{GS} = 0 V$ $R_G = 1 M\Omega, f = 1 kHz$	0.3		2.5		2.5		2.5	dB	
		$V_{DS} = 15 V, I_D = 1 mA$ $R_G = 1 M\Omega, f = 100 MHz$	2		3						
		$V_{DS} = 15 V$ $I_D = 4 mA$ $R_G = 1 M\Omega$	$f = 100 MHz$	1				2			2
			$f = 400 MHz$	2.5				4			4

NOTES:

- a. $T_A = 25^\circ C$ unless otherwise noted.
- b. For design aid only, not subject to production testing.
- c. Pulse test; $PW = 300 \mu S$, duty cycle $\leq 3\%$.
- d. This parameter not registered with JEDEC.