VITESSE

VSC834
Data Sheet

2.7 Gbps 17x17 Crosspoint Switch with Input Signal Activity (ISA) Monitoring

FEATURES

- 17 input by 17 output crosspoint switch
- 2.7 Gbps NRZ data bandwidth
- 46 Gbps aggregate bandwidth
- TTL-compatible µP interface
- Differential PECL data inputs
- On-chip 50 Ω input terminations
- 50 Ω source-terminated PECL output drivers
- Single 3.3 V power supply
- 9 W maximum power dissipation
- 256-pin BGA package

GENERAL DESCRIPTION

The VSC834 is a monolithic 17x17 asynchronous crosspoint switch designed to carry broadband data streams at up to 2.7 Gbps. The non-blocking switch core is programmed through a parallel microprocessor interface that allows random access programming of each output port. A high degree of signal integrity is maintained through the chip through fully differential signal paths.

The crosspoint function is based on a multiplexer tree architecture. Each data output is driven by a 17:1 multiplexer tree that can be programmed to one and only one of its 17 inputs, and each data input can be programmed to multiple outputs. The signal path is unregistered, so no clock is required for the data inputs. The signal path is asynchronous, so there are no restrictions on the phase, frequency, or signal pattern at each input. Each input channel has an activity monitor function that can be used to identify Loss of Activity (LOA). An interrupt pin is provided to signal LOA, after which an external controller can query the chip to determine the channel(s) on which the fault occurred.

Each output driver is a fully differential switched current driver with on-die back-terminations for maximum signal integrity. Data inputs are terminated on die through 50 Ω resistors connected to V_{TERM}.

The parallel interface uses TTL levels and provides address, data, and control pins that are compatible with a microprocessor-style interface. The control port provides access to all chip functions, including LOA and programming. Program buffering is provided to allow multiple program assignments to be queued and issued simultaneously via a single configure command.

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Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com

Block Diagrams

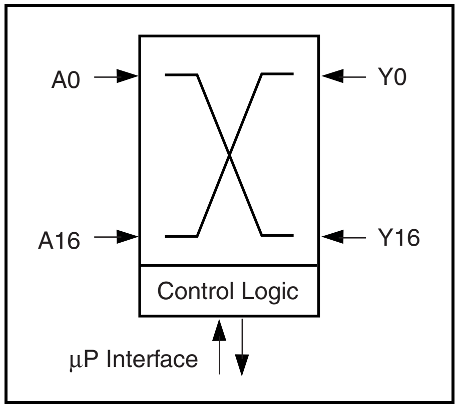


Figure 1. High-level Block Diagram

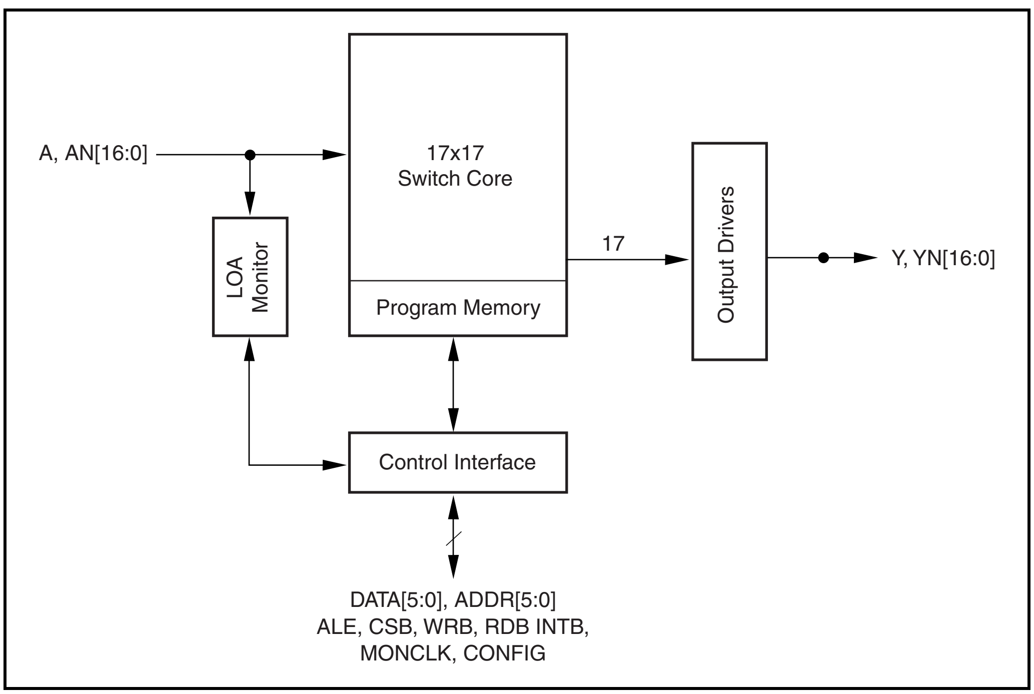


Figure 2. Function Block Diagram

Functional Description

Data Paths

All input data must be differential and biased to PECL levels. On-chip terminations are provided, with a nominal impedance of 50 Ω. All input termination resistors are tied to V_{TERM}.

Data outputs are provided through differential current switches with on-chip terminations that produce a PECL level output swing. The drive level of the output circuit is designed to produce standard PECL levels when terminated in 50 Ω to 2.0 V. Other termination voltages are possible, such as to V_{CC} or 1.3 V, however, the voltage level of the output swing will be shifted from its nominal value. The common-mode voltage of the output swing can be adjusted using the VCOM pin. The adjustment range is not calibrated but typically allows for about ±200 mV of adjustment in the output common-mode voltage.

Output channels can be powered off in pairs if fewer than 17 outputs are required. By connecting the VEE pin associated with a given pair of outputs to V_{CC}, the output pairs will pull to V_{CC} and chip power will be reduced by approximately 200 mW.

Skew between physically adjacent pins is typically less than 10 ps; maximum skew between any two pins is typically 300 ps.

Programming Interface

The switch core is programmed through a parallel interface circuit that allows random reads or writes to the program memory array. The program memory array is buffered to allow multiple programming instructions to be loaded simultaneously with the CONFIG pin. Parallel programming can be clocked up to a 50 MHz rate.

The program data is composed of two parts: output address and input address. The output address, denoted by ADDR[5:0], specifies which output channel is to be programmed. The input address, denoted by DATA[4:0], specifies to which input port the switch slice should be connected. The format of the program data is simple binary, where the binary value maps directly to the switch slice position and/or input port number. For example, ADDR[5:0] (000100) / DATA[5:0] (000110) would direct output channel Y4 to connect to input channel A6. The programming state may be verified (read back) by applying the address of the desired output and asserting RDB. The programming state is unknown at power-on. Additional address space is provided for access to the monitor registers (see Table 2 on page 5). The microprocessor interface consists of the signals listed in Table 1. Levels are TTL (see Table 8 on page 9).

Table 1. Programming Interface Signals

Pin	I/O	Description
D[5:0]	B	Bidirectional data bus to transfer data to/from internal program registers.
A[5:0]	I	Address bus to select internal program registers for read/write operations.
ALE	I	Address Latch Enable. For use with multiplexed address/data buses. Latches the address bus internally when LOW.
CSB	I	Chip Select (active LOW). Assert this pin whenever the part is being read or programmed.
WRB	I	Write (active LOW). Program data will be transferred to the first-level internal registers on the rising edge of this signal (when CSB is also LOW).

Table 1. Programming Interface Signals *(continued)*

Pin	I/O	Description
RDB	I	Read (active LOW). Program data from the internal program or monitor registers will be read out on the data bus when this signal goes LOW (with CSB also LOW).
INTB	O	Interrupt (active LOW). This signal is asserted when an LOA condition is found.
CONFIG	I	Configure (active HIGH). Assert this signal to transfer queued program information from the first-level internal registers to the second-level registers. This signal may be tied HIGH to leave the second-level registers transparent so all programming will take effect immediately. CSB must be active (LOW) when CONFIG is asserted. CONFIG may be tied to a high-order bit of the address bus.
MONCLK	I	Monitor states are transferred to monitor registers on the rising edge of this signal. MONCLK is not expected to exceed 3 MHz.

Loss of Activity (LOA) Monitoring

The LOA function consists of an activity monitor on each input channel and each output channel connected directly to the pads. The state of a monitor (whether or not it has been toggled by an input transition) can be observed by applying the address (see Table 2 on page 5) of the monitor register corresponding to the signal of interest and asserting RDB. Each monitor register is 4 bits in length, covering the state of four inputs or outputs. There is one extra 1-bit monitor for each of the 17^{th} input and 17^{th} output. The state of each monitor is transferred to the register periodically on the rising edge of MONCLK, whereupon the activity monitor is cleared until more activity is detected.

If any change in a monitor state occurs after sampling by MONCLK, an interrupt will be signaled by asserting INTB, and the user must identify the channel by reading the monitor states. The interrupt will be cleared when the corresponding activity monitor is read, however, the monitor state will not be changed. If multiple monitors have triggered the interrupt, it will continue until all the corresponding monitors have been read. See Figures 4 through 6.

To distinguish noise from live data, LOA requires at least two transitions of a minimum input signal level to recognize an input as active. The trigger threshold for activity detection is controlled by V_{HYS}. A bias network on-chip will set V_{HYS} to $V_{CC/2}$, which will set the input threshold to approximately 200 mV. By externally forcing V_{HYS} to other bias voltages, the trigger threshold can be adjusted as shown in Figure 1. Note that the trigger threshold adjustment is not tightly controlled, therefore, to assure that the trigger threshold does not exceed the minimum input swing specification, it is recommended that V_{HYS} be driven at V_{CC}.

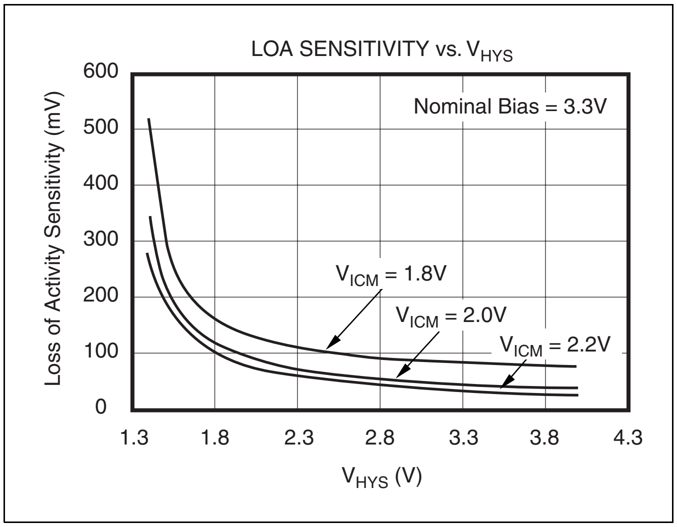


Figure 3. Loss of Activity (LOA) Sensitivity

Table 2. Memory Map

Address	Access	Description
00'h	R/W	Output Y0's programmed input channel (write and then assert CONFIG to program).
01'h	R/W	Output Y1's programmed input channel .
⋮	⋮	⋮
10'h	R/W	Output Y16's programmed input channel.
21'h	Read Only	Rx activity monitor for inputs A0, A1, A2, A3 (logic 1 = no activity).
22'h	Read Only	Rx activity monitor for inputs A4, A5, A6, A7.
23'h	Read Only	Rx activity monitor for inputs A8, A9, A10, A11.
24'h	Read Only	Rx activity monitor for inputs A12, A13, A14, A15.
25'h	Read Only	Rx activity monitor for input A16.

Electrical Specifications

Unless stated otherwise, all data is assumed to be over Recommended Operating Conditions.

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}, V_{CCP}	Power supply voltage	+3.135	+3.3	+3.465	V
V_{EE}	Power supply voltage		0		V
V_{TERM}	Termination voltage		V_{CC} – 1.3		V
T_C	Case operating temperature range	0		+85	°C

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{CC}	Power supply voltage, referenced to ground	–0.5	+4.0	V
	Input voltage applied (TTL, ECL)	–0.5	V_{CC} + 0.5	V
I_{OUT}	Output current	–50	+50	mA
I_{IN}	Input current	–50	+50	mA
I_{TERM}	V_{TERM} current	–800	+800	mA
T_C	Case temperature under bias	–55	+125	°C
T_S	Storage temperature range	–65	+150	°C
V_{ESD}	Electrostatic discharge voltage, human body model	–750	+750	V

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

AC Characteristics

Table 5. Data Path

Symbol	Parameter	Min	Typ	Max	Units	Condition
f_{RATE}	Data rate(1)			2.7	Gbps	
t_{ISKW}	Input channel delay skew(2)		300		ps	
t_{OSKW}	Output channel delay skew(3)		300		ps	
t_R, t_F	High-speed input rise and fall times(4)			150	ps	20% to 80%
t_R, t_F	High-speed output rise and fall times			150	ps	20% to 80%
$t_{Jp\text{-}p}$	Output data eye jitter, peak-to-peak(5)			100	ps	PRBS 2^{23}

1. *Guaranteed by characterization. Not tested.*
2. *Skew between any two input channels to a given output.*
3. *Skew between any two output channels from the same input channel.*
4. *Required for high-speed output rise and fall specifications at f_{RATE} = 2.7 Gbps. For lower rate signals, use 0.375/f_{RATE}.*
5. *Broadband jitter added to a jitter-free signal; jitter is primarily in the form of ISI for random data.*

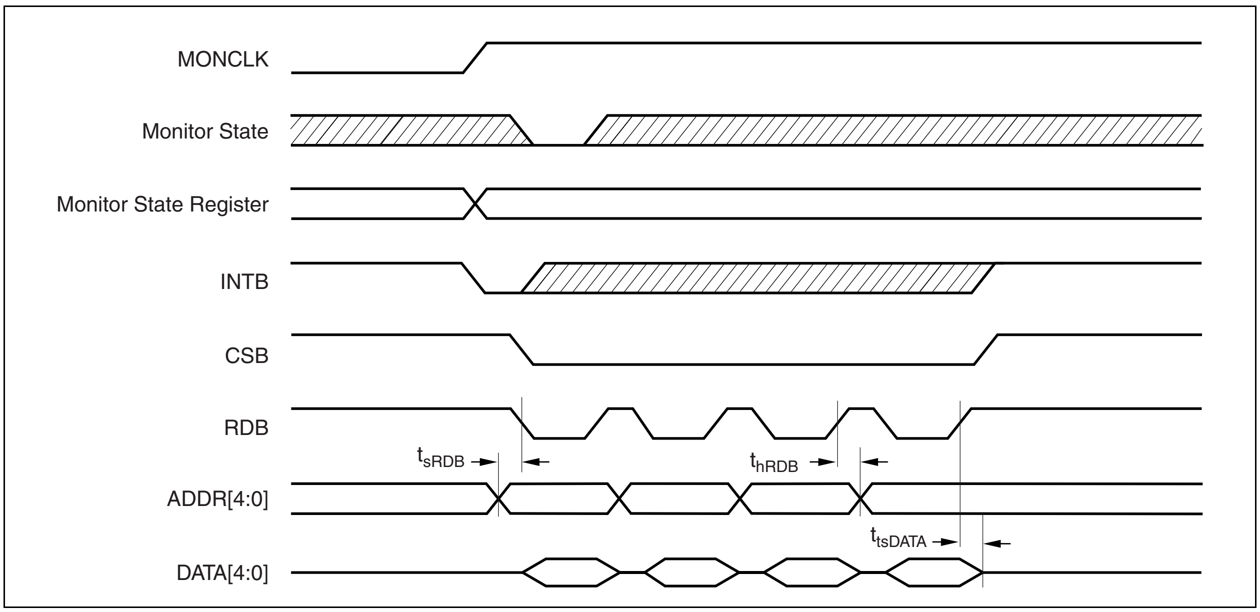


Figure 4. Interrupt Timing Diagram (Change in Monitor State Registers)

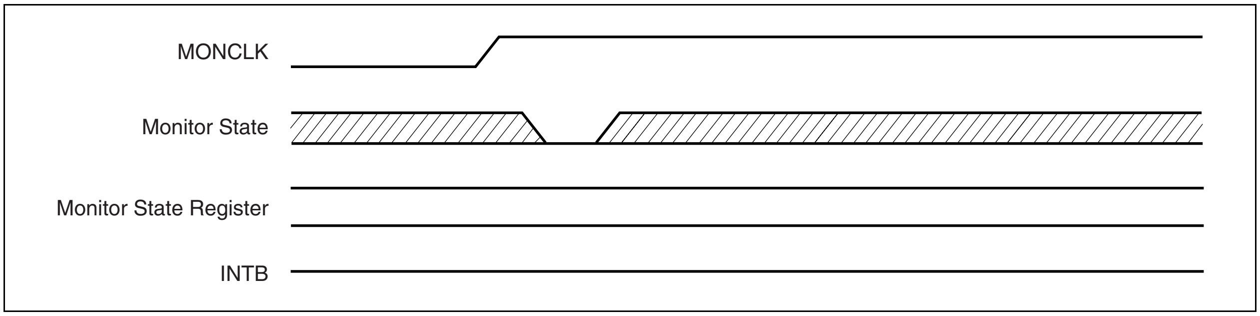


Figure 5. Interrupt Timing Diagram (No Change in Monitor State Registers)

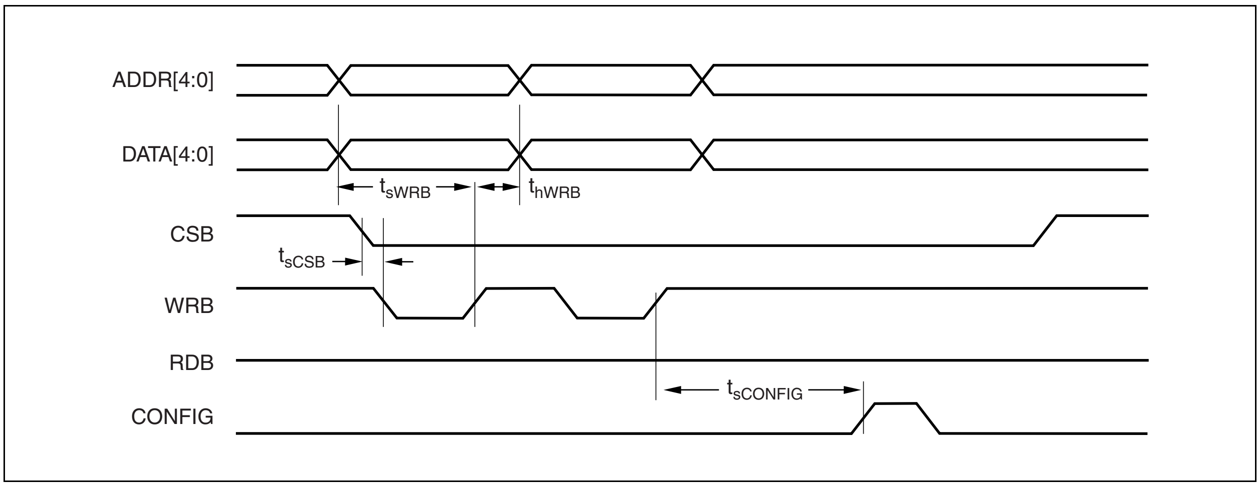


Figure 6. Programming Timing Diagram

Table 6. Programming Port Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{CONFIG}	Switch configuration delay			6	ns
t_{pdADDR}	Data read propagation delay from ADDR			30	ns
t_{pdRDB}	Data read propagation delay from RDB(1)			7	ns
t_{pdINTB}	Interrupt propagation delay from MONCLK(2)			50	ns
$t_{pdSTATE}$	MONCLK to internal state register change delay(2)			6	ns
t_{sRDB}	ADDR to RDB setup time	5			ns
t_{hRDB}	RDB to ADDR hold time	3			ns
t_{sWRB}	WRB setup time (for either ADDR or DATA)	5			ns
t_{hWRB}	WRB hold time (for either ADDR or DATA)	3			ns
$t_{sCONFIG}$	WRB to CONFIG setup time	1			ns
t_{sCSB}	CSB setup time (to either WRB or RDB)	0			ns
$t_{pwCONFIG}$	CONFIG pulse width (LOW)	10			ns

Table 6. Programming Port Interface Timing *(continued)*

Symbol	Parameter	Min	Typ	Max	Unit
t_{pwWRB}	WRB pulse width (LOW and HIGH)	10			ns
t_{pwRDB}	RDB pulse width (LOW and HIGH)	10			ns
t_{sDATA}	DATA tri-state delay (from either RDB or CSB)(2)			10	ns
t_{sALE}	ALE setup time (for multiplexed ADDR/DATA bus)	5			ns
t_{hALE}	ALE hold time (for multiplexed ADDR/DATA bus)	3			ns

1. *Measured from falling edge.*
2. *Measured from rising edge.*

DC Characteristics

Table 7. Power Supply Requirements

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{CC}	V_{CC} supply current(1)			2600	mA	
P_T	Total chip power			9	W	V_{CC} = 3.45V and +85°C case
I_{TERM-V}	V_{TERM} supply current			0	mA	$V_{TERM} = V_{CC} – 1.3V$
I_{TERM-E}	V_{TERM} supply current			–600	mA	$V_{TERM} = V_{CC} – 2.0V$

1. *I_{CC} specified with outputs terminated with 50Ω resistors to +2.0V and chip V_{TERM} = +2.0V.*

Table 8. Control Port Input Levels—TTL

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{COM}	VCOM bias voltage (L and R)	1.9	2.0	2.1	V	V_{CC} = 3.3V
V_{IH}	Input HIGH voltage	2.0		3.5	V	
V_{IL}	Input LOW voltage	0		0.8	V	
V_{OH}	Output HIGH voltage	2.4		3.0	V	I_{OH} = 2mA
V_{OL}	Output LOW voltage	0		0.4	V	I_{OL} = 1.5mA
I_{IH}	Input HIGH current			+500	µA	V_{IN} = 2.4V
I_{IL}	Input LOW current			–500	µA	V_{IN} = 0.5V
I_{OZ}	Tri-state output current	–100		+100	µA	V_{OUT} = 0.4V to 2.4V

Table 9. Data Input Levels—Differential PECL

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{ID}	Input differential voltage	200		1000	mV	
V_{ICM}	Input common-mode voltage	1.8		2.2	V	V_{CC} = 3.3V

Table 10. Data Output Levels—Differential PECL

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OD}	Output differential voltage(1)	600		1000	mV	
V_{OCM}	Output common-mode voltage(1)	1.8		2.2	V	

1. Nominal PECL mode, $V_{CC} = V_{CCP} = 3.3V$, $V_{EE} = 0$, terminated with 50Ω resistors to +2.0V.

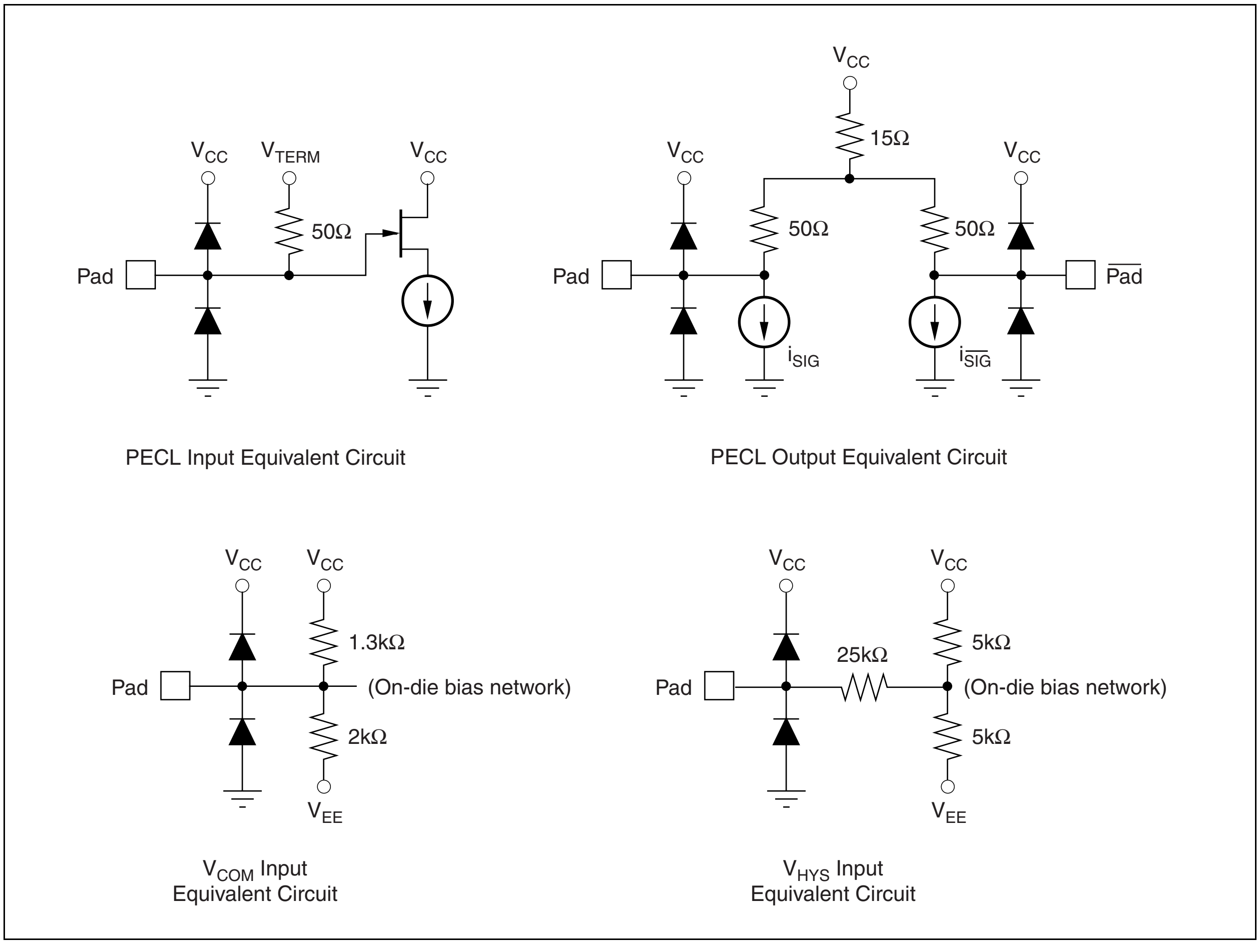


Figure 7. Input/Output Equivalent Circuits

Package Information

The VSC834 is packaged in a 27 mm x 27 mm 256-pin BGA. The 256-pin BGA package (UB) is thermally enhanced and carries the high-speed signals over controlled impedance lines from the solder ball to the circuit die.

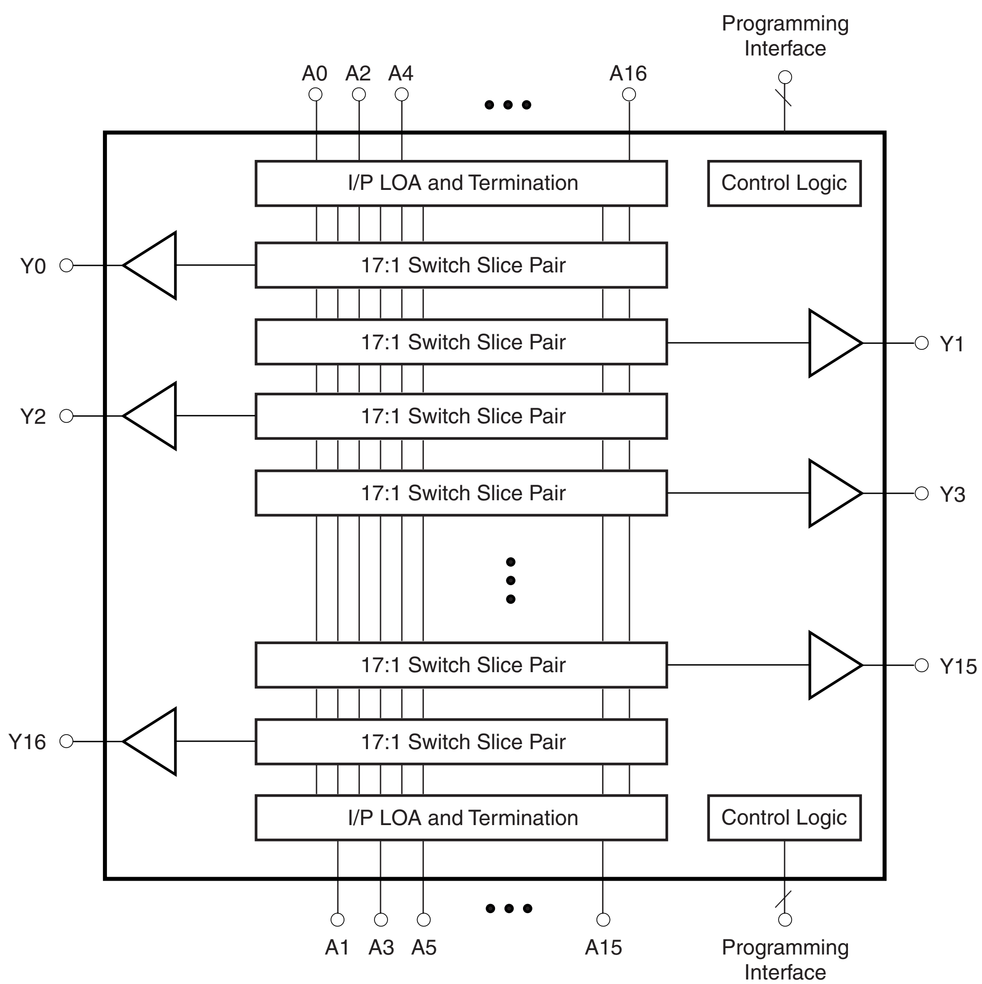


Figure 8. Functional Pinout Floorplan

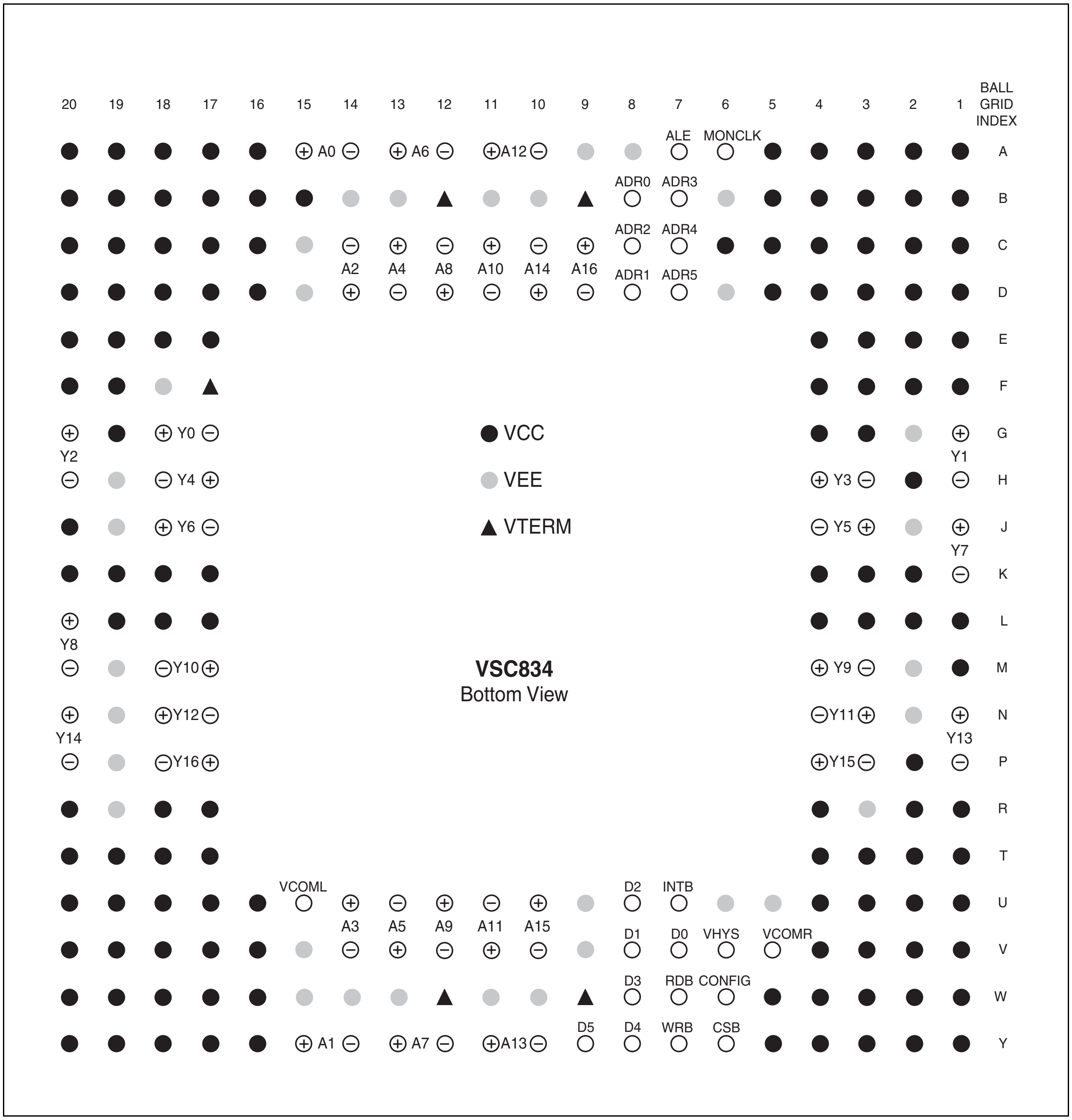


Figure 9. Pin Diagram for 256-Pin BGA (UB)

Table 11. Pin Identifications for 256-Pin BGA (UB)

Signal	Ball Site	I/O	Level	Description
High-Speed Data Inputs				
A0, NA0	A15, A14	I	PECL	Data Input Channel 0; True, Complement.
A1, NA1	Y15, Y14	I	PECL	Data Input Channel 1; True, Complement.
A2, NA2	D14, C14	I	PECL	Data Input Channel 2; True, Complement.
A3, NA3	U14, V14	I	PECL	Data Input Channel 3; True, Complement.

Table 11. Pin Identifications for 256-Pin BGA (UB) *(continued)*

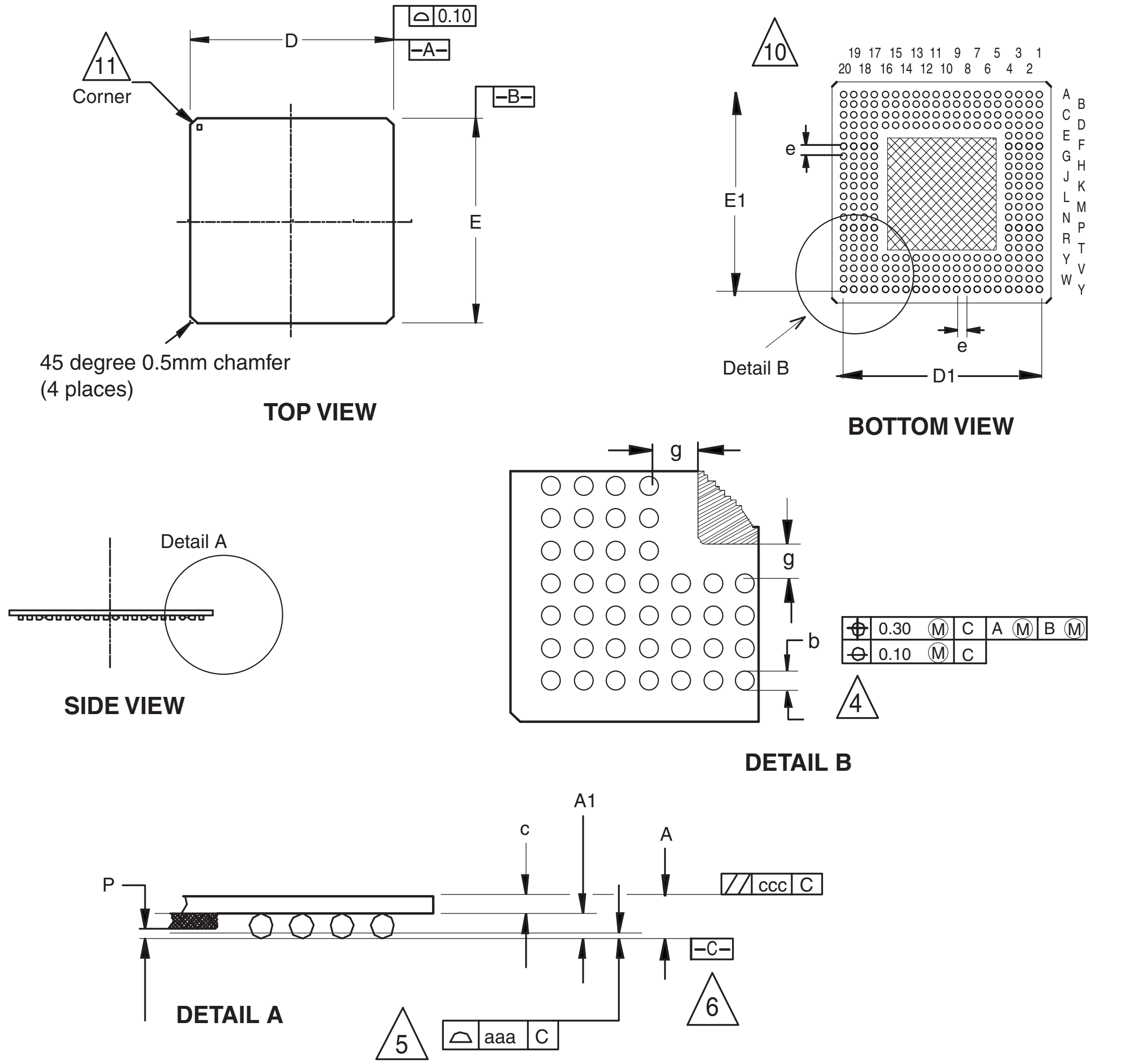
Signal	Ball Site	I/O	Level	Description
A4, NA4	C13, D13	I	PECL	Data Input Channel 4; True, Complement.
A5, NA5	V13, U13	I	PECL	Data Input Channel 5; True, Complement.
A6, NA6	A13, A12	I	PECL	Data Input Channel 6; True, Complement.
A7, NA7	Y13, Y12	I	PECL	Data Input Channel 7; True, Complement.
A8, NA8	D12, C12	I	PECL	Data Input Channel 8; True, Complement.
A9, NA9	U12, V12	I	PECL	Data Input Channel 9; True, Complement.
A10, NA10	C11, D11	I	PECL	Data Input Channel 10; True, Complement.
A11, NA11	V11, U11	I	PECL	Data Input Channel 11; True, Complement.
A12, NA12	A11, A10	I	PECL	Data Input Channel 12; True, Complement.
A13, NA13	Y11, Y10	I	PECL	Data Input Channel 13; True, Complement.
A14, NA14	D10, C10	I	PECL	Data Input Channel 14; True, Complement.
A15, NA15	U10, V10	I	PECL	Data Input Channel 15; True, Complement.
A16, NA16	C9, D9	I	PECL	Data Input Channel 16; True, Complement.
High-Speed Data Outputs				
Y0, YN0	G18, G17	O	PECL	Data Output Channel 0; True, Complement.
Y1, YN1	G1, H1	O	PECL	Data Output Channel 1; True, Complement.
Y2, YN2	G20, H20	O	PECL	Data Output Channel 2; True, Complement.
Y3, YN3	H4, H3	O	PECL	Data Output Channel 3; True, Complement.
Y4, YN4	H17, H18	O	PECL	Data Output Channel 4; True, Complement.
Y5, YN5	J3, J4	O	PECL	Data Output Channel 5; True, Complement.
Y6, YN6	J18, J17	O	PECL	Data Output Channel 6; True, Complement.
Y7, YN7	J1, K1	O	PECL	Data Output Channel 7; True, Complement.
Y8, YN8	L20, M20	O	PECL	Data Output Channel 8; True, Complement.
Y9, YN9	M4, M3	O	PECL	Data Output Channel 9; True, Complement.
Y10, YN10	M17, M18	O	PECL	Data Output Channel 10; True, Complement.
Y11, YN11	N3, N4	O	PECL	Data Output Channel 11; True, Complement.
Y12, YN12	N18, N17	O	PECL	Data Output Channel 12; True, Complement.
Y13, YN13	N1, P1	O	PECL	Data Output Channel 13; True, Complement.
Y14, YN14	N20, P20	O	PECL	Data Output Channel 14; True, Complement.
Y15, YN15	P4, P3	O	PECL	Data Output Channel 15; True, Complement.
Y16, YN16	P17, P18	O	PECL	Data Output Channel 16; True, Complement.
Programming Port				
ADR0	B8		TTL	Program Data Address Bit 0.
ADR1	D8		TTL	Program Data Address Bit 1.
ADR2	C8		TTL	Program Data Address Bit 2.
ADR3	B7		TTL	Program Data Address Bit 3.
ADR4	C7		TTL	Program Data Address Bit 4.
ADR5	D7		TTL	Program Data Address Bit 5.
D0	V7		TTL	Program Data Bit 0.
D1	V8		TTL	Program Data Bit 1.
D2	U8		TTL	Program Data Bit 2.

Table 11. Pin Identifications for 256-Pin BGA (UB) *(continued)*

Signal	Ball Site	I/O	Level	Description
D3	W8		TTL	Program Data Bit 3.
D4	Y8		TTL	Program Data Bit 4.
D5	Y9		TTL	Program Data Bit 5.
ALE	A7		TTL	Address Latch Enable (active HIGH).
INTB	U7		TTL	Interrupt (active LOW).
RDB	W7		TTL	Read Enable (active LOW).
WRB	Y7		TTL	Write Enable (active LOW).
CONFIG	W6		TTL	Configuration Strobe (active HIGH).
CSB	Y6		TTL	Chip Select (active LOW).
MONCLK	A6		TTL	Loss of Activity Monitor Clock (active HIGH).

Table 12. Power Supplies

Signal	Ball Site	Description
V_{CC}	A1, A2, A3, A4, A5, A16, A17, A18, A19, A20, B1, B2, B3, B4, B5, B15, B16, B17, B18, B19, B20, C1, C2, C3, C4, C5, C6, C16, C17, C18, C19, C20, D1, D2, D3, D4, D5, D16, D17, D18, D19, D20, E1, E2, E3, E4, E17, E18, E19, E20, F1, F2, F3, F4, F19, F20, G3, G4, G19, H2, J20, K2, K3, K4, K17, K18, K19, K20, L1, L2, L3, L4, L17, L18, L19, M1, P2, R1, R2, R4, R17, R18, R20, T1, T2, T3, T4, T17, T18, T19, T20, U1, U2, U3, U4, U16, U17, U18, U19, U20, V1, V2, V3, V4, V16, V17, V18, V19, V20, W1, W2, W3, W4, W5, W16, W17, W18, W19, W20, Y1, Y2, Y3, Y4, Y5, Y16, Y17, Y18, Y19, Y20	Power Supply, +3.3V.
V_{EE}	A8, A9, B6, B10, B11, B13, B14, C15, D6, D15, F18, M19, R3, U5, U6, U9, V9, V15, W10, W11, W13, W14, W15	Ground.
V_{EE}	A8, A9, B6, B10, B11, B13, B14, C15, D6, D15, F18, M19, R3, U5, U6, U9, V9, V15, W10, W11, W13, W14, W15	Ground.
V_{EE}	H19	Power for Output Channels 0, 2.
V_{EE}	G2	Power for Output Channels 1, 3.
V_{EE}	J19	Power for Output Channels 4, 6.
V_{EE}	J2	Power for Output Channels 5, 7.
V_{EE}	N19	Power for Output Channels 8, 10.
V_{EE}	M2	Power for Output Channels 9, 11.
V_{EE}	P19	Power for Output Channels 12, 14.
V_{EE}	N2	Power for Output Channels 13, 15.
V_{TERM}	B9, B12, F17, W9, W12	Termination Power Supply, +2.0V.
Miscellaneous		
V_{COML}	U15	Analog; Slicing Level for Y0 through YN16 (even).
V_{COMR}	V5	Analog; Slicing Level for Y1 through YN15 (odd).
V_{HYS}	V6	Analog; Loss of Activity Hysterisis Threshold.



DIMENSIONAL REFERENCES			
REF.	MIN.	TYP.	MAX.
A	1.55	1.75	1.95
A1	0.50	0.60	0.70
D	26.80	27.00	27.20
D1	24.13 (BSC.)		
E	26.80	27.00	27.20
E1	24.13 (BSC.)		
b	0.60	0.75	0.90
c	1.05	1.15	1.25
M	20		
N	256		
aaa			0.15
ccc			0.25
e	1.27 TYP.		
g	0.35		
P	0.15		

NOTES:

1. All dimensions are in millimeters.
2. “e” represents the basic solder ball grid pitch.
3. “M” represents the basic solder ball matrix size, and “N” is the maximum allowable number of balls after depopulating.
4. “b” is measured at the maximum solder ball diameter parallel to primary datum –C–.
5. “aaa” is measured parallel to primary datum –C–.
6. Primary datum –C– and seating plane are defined by the spherical crowns of the solder balls.
7. Package surface is black oxide.
8. Cavity depth varies with die thickness
9. Substrate material base is copper.
10. Bilateral tolerance zone is applied to each side of package body.
11. 45 degree 0.5mm chamfer corner and white dot for Pin 1 identification.

Figure 10. Package Drawing for 256-Pin BGA (UB)

Moisture Sensitivity

This device is rated moisture sensitivity level 3 or better as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

Ordering Information

VSC834 2.7 Gbps 17x17 Crosspoint Switch with Input Signal Activity (ISA) Monitoring

Part Number	Description
VSC834UB	256-Pin BGA, 27 mm x 27 mm x 1.5 mm body

CORPORATE HEADQUARTERS
Vitesse Semiconductor Corporation
741 Calle Plano
Camarillo, CA 93012
Tel: 1-800-VITESSE • FAX:1-(805) 987-5896

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