National Semiconductor

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DP83251/55 PLAYER™ Device (FDDI Physical Layer Controller)

General Description

The DP83251/DP83255 PLAYER device implements one Physical Layer (PHY) entity as defined by the Fiber Distributed Data Interface (FDDI) ANSI X3T9.5 Standard. The PLAYER device contains NRZ/NRZI and 4B/5B encoders and decoders, serializer/deserializer, framing logic, elasticity buffer, line state detector/generator, link error detector, repeat filter, smoother, and configuration switch.

Features

- Low power CMOS-BIPOLAR process
- Single 5V supply
- Full duplex operation
- Separate management interface (Control Bus)
- Parity on PHY-MAC Interface and Control Bus Interface
- On-chip configuration switch
- Internal and external loopback
- DP83251 for single attach stations
- DP83255 for dual attach stations

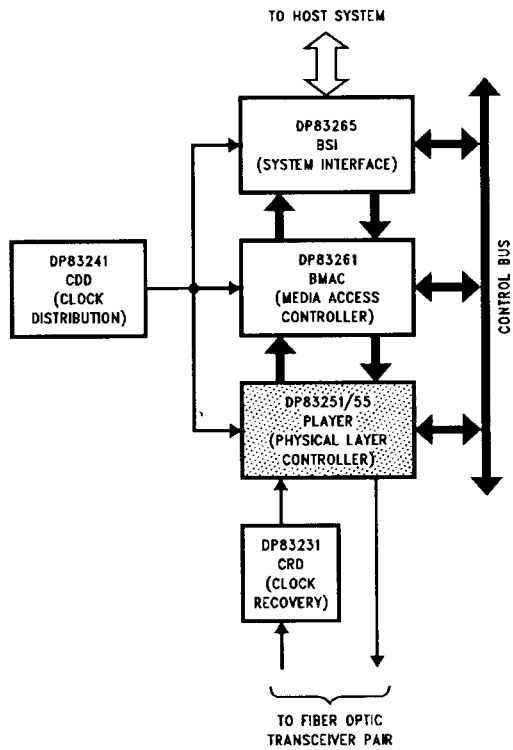

FIGURE 1-1. FDDI Chip Set Block Diagram

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1.0 FDDI Chip Set Overview

National Semiconductor's FDDI chip set consists of five components as shown in *Figure 1-1*. For more information on the other devices of the chip set, consult the appropriate datasheets and application notes.

DP83231 CRD™ Device Clock Recovery Device

The Clock Recovery Device extracts a 125 MHz clock from the incoming bit stream.

Features

- PHY Layer loopback test
- Crystal controlled
- Clock locks in less than 85 μs

DP83241 CDD™ Device Clock Distribution Device

From a 12.5 MHz reference, the Clock Distribution Device synthesizes the 125 MHz, 25 MHz, and 12.5 MHz clocks required by the BSI, BMAC and PLAYER devices.

DP83251/55 PLAYER™ Device Physical Layer Controller

The PLAYER device implements the Physical Layer (PHY) protocol as defined by the ANSI FDDI PHY X3T9.5 Standard.

Features

- 4B/5B encoders and decoders
- Framing logic
- Elasticity Buffer, Repeat Filter and Smoother
- Line state detector/generator
- Link error detector
- Configuration switch
- Full duplex operation
- Separate management port that is used to configure and control their operation

In addition, the DP83255 contains an additional PHY_Data.request and PHY_Data.indicate port required for concentrators and dual attach stations.

DP83261 BMAC™ Device Media Access Controller

The BMAC device implements the Timed Token Media Access Control protocol defined by the ANSI FDDI X3T9.5 MAC Standard.

Features

- All of the standard defined ring service options
- Full duplex operation with through parity
  Supports all FDDI Ring Scheduling Classes (Synchronous, Asynchronous, etc.)
- Supports Individual, Group, Short, Long, and External Addressing
- Generates Beacon, Claim, and Void frames internally
- Extensive ring and station statistic gathering
- Extensions for MAC level bridging
- Separate management port that is used to configure and control their operation
- Multi-frame streaming interface

DP83265 BSI™ Device System Interface

The BSI device implements the interface between the BMAC device and a host system.

Features

- 32-bit wide Address/Data path with byte parity
- Programmable transfer burst sizes of 4 or 8 32-bit words
- Interfaces to low cost DRAMs or directly to system bus
- Provides 2 Output and 3 Input Channels
- Supports Header/Info splitting
- Efficient data structures
- Programmable Big or Little Endian alignment
- Full duplex data path allows transmission to self
- Confirmation status batching services
- Receive frame filtering services
- Operates from 12.5 MHz to 25 MHz synchronously with the host system

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2.0 Architecture Description

2.1 OVERVIEW

The PLAYER device is comprised of four blocks: Receiver, Transmitter, Configuration Switch and Control Bus Interface as shown in *Figure 2-1.*

Receiver

During normal operation, the Receiver Block accepts serial data as inputs at the rate of 125 Mbps from the Clock Recovery Device (DP83231). During the Internal Loopback mode of operation, the Receiver Block accepts data from the Transmitter Block as inputs.

The Receiver Block performs the following operations:

- Converts the incoming data stream from NRZI to NRZ, if necessary
- Decodes the data from 5B to 4B coding
- Converts the serial bit stream into 10-bit bytes
- Compensates for the differences between the upstream and local clocks
- Decodes Line States
- Detects link errors

Finally, the Receiver Block presents data symbol pairs (bytes) to the Configuration Switch Block

Configuration Switch

An FDDI station may be in one of three configurations: Isolate, Wrap or Thru. The Configuration Switch supports these configurations by switching the transmitted and received data paths between the PLAYER and BMAC devices.

The configuration switching is performed internally, therefore no external logic is required for this function.

Transmitter

The Transmiter Block accepts 10-bit bytes from the Configuration Switch.

The Transmitter Block performs the following operations:

- Encodes the data from 4B to 5B coding.
- Filters out code violations from the data stream.
- Generates Idle, Master, Halt, Quiet or other user defined symbol pairs upon request.
- Converts the data stream from NRZ to NRZI format ready for transmission, if necessary.
- Provides smoothing function when necessary.

During normal operation, the Transmitter Block presents serial data to the fiber optic transmitter. While in the External Loopback mode, the Transmitter Block presents serial data to the Clock Recovery Device.

Control Bus Interface

The Control Bus Interface allows a user to:

- Program the Configuration Switch.
- Enable/disable functions within the Transmitter and Receiver Blocks (i.e., NRZ/NRZI Encoder, Smoother, PHY Request Data Parity, Line State Generation, Symbol Pair Injection, NRZ/NRZI Decoder, Cascade Mode, etc.).

The Control Bus Interface also performs the following functions:

- Monitors Line States received
- Monitors link errors detected by the Receiver Block
- Monitors other error conditions

2.2 INTERFACES

The PLAYER device connects to external components via 5 functional interfaces: Serial Interface, PHY Port Interface, Control Bus Interface, Clock Interface, and the Miscellaneous Interface.

Serial Interface

The Serial Interface connects the PLAYER device to a fiber optic transmitter (FOTX) and the Clock Recovery Device (DP83231).

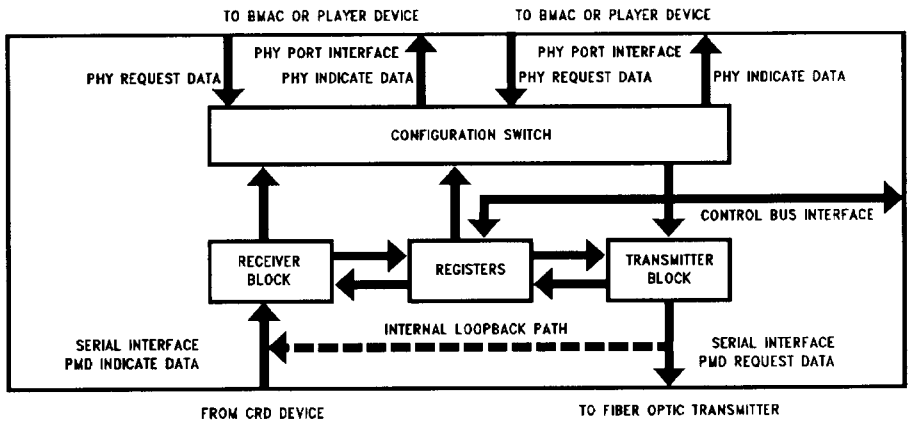

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FIGURE 2-1. PLAYER Device Block Diagram

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2.0 Architecture Description

(Continued)

PHY Port Interface

The PHY Port Interface connects the PLAYER device to one or more BMAC devices and/or PLAYER devices. Each PHY Port Interface consists of two byte-wide-interfaces, one for PHY Request data input to the PLAYER device and one for the PHY Indicate data output of the PLAYER device. Each byte-wide interface consists of a parity bit (odd parity), a control bit, and two 4-bit symbols.

The DP8355 PLAYER device has two PHY Port Interfaces and the DP83251 has only one PHY Port Interface.

Control Bus Interface

The Control Bus Interface connects the PLAYER device to a wide variety of microprocessors and microcontrollers. The Control Bus is an asynchronous interface which provides access to 32 8-bit registers.

Clock Interface

The Clock Interface consists of 12.5 MHz and 125 MHz clocks used by the PLAYER device.

The clocks are generated by either the Clock Distribution Device (CDD device) or the Clock Recovery Device (CRD device).

Miscellaneous Interface

The Miscellaneous Interface consists of:

- A reset signal
- User definable sense signals
- User definable enable signals
- Synchronization for cascaded PLAYER devices (a high-performance non-FDDI mode)
- CMOS power and ground, and ECL ground and power

3.0 Functional Description

The PLAYER Device is comprised of four blocks: Receiver, Transmitter, Configuration Switch and Control Bus Interface.

3.1 RECEIVER BLOCK

During normal operation, the Receiver Block accepts serial data as inputs at the rate of 125 Mbps from the Clock Recovery Device (DP83231). During the Internal Loopback mode of operation, the Receiver Block accepts data from the Transmitter Block as input.

The Receiver Block performs the following operations:

- Converts the incoming data stream from NRZI to NRZ, if necessary
- Decodes the data from 5B to 4B coding
- Converts the serial bit stream into National byte-wide code
- Compensates for the differences between the upstream and local clocks
- Decodes Line States
- Detects link errors

Finally, the Receiver Block presents data symbol pairs to the Configuration Switch Block.

The Receiver Block consists of the following functional blocks:

NRZI to NRZ Decoder
Shift Register
Framing Logic
Symbol Decoder
Line State Detector
Elasticity Buffer
Link Error Detector

See *Figure 3-1.*

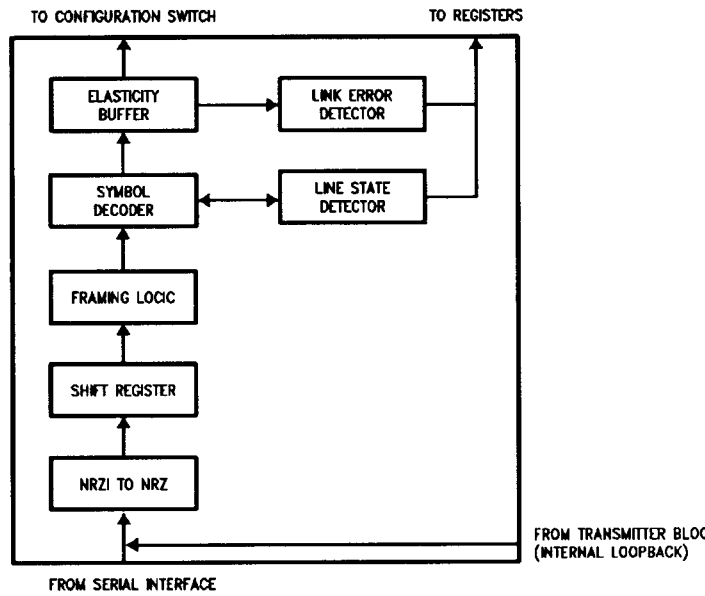

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FIGURE 3-1. Receiver Block Diagram

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3.0 Functional Description (Continued)

NRZI TO NRZ DECODER

The NRZI to NRZ Decoder converts Non-Return-To-Zero-Invert-On-Ones data to Non-Return-To-Zero data.

This function can be enabled and disabled through bit 7 (RNRZ) of the Mode Register (MR). When the bit is cleared, it converts the incoming bit stream from NRZI to NRZ. When the bit is set the incoming NRZ bit stream is passed unchanged.

SHIFT REGISTER

The Shift Register converts the serial bit stream into symbol-wide data for the 5B/4B Decoder.

The Shift Register also provides byte-wide data for the Framing Logic.

FRAMING LOGIC

The Framing Logic performs the Framing function by detecting the beginning of a frame or the Halt-Halt or Halt-Quiet symbol pair.

The J-K symbol pair (11000 10001) indicates the beginning of a frame during normal operation. The Halt-Halt (00100 00100) and Halt-Quiet (00100 00000) symbol pairs are detected during Connection Management (CMT).

Framing can be temporarily suspended (i.e. framing hold), in order to maintain data integrity. The Framing Hold rules are explained in Section 8.1.

SYMBOL DECODER

The Symbol Decoder is a two level system. The first level is a 5-bit to 4-bit converter, and the second level is a 4-bit symbol pair to the NSC byte-wide code converter.

The first level latches the received 5-bit symbols and decodes them into 4-bit symbols. Symbols are decoded into two types: data and control. The 4-bit symbols are sent to the Line State Detector and the second level of the Symbol Decoder. See Table 3-1 for the 5B/4B Symbol Decoding list.

The second level translates two 4-bit symbols from the 5B/4B converter and the line state information from the Line State Detector into the National byte-wide code. More details on the National byte-wide code can be found in Section 8.6.

LINE STATE DETECTOR

The FDDI Physical Layer (PHY) standard specifies eight Line States that the Physical Layer can transmit. These Line States are used in the Connection Management process. They are also used to indicate data within a frame during the normal operation.

The Line State Detector detects nine Line States, one more than the required Line States specified in the standard.

The Line States are reported through the Current Receive State Register (CRSR), Receive Condition Register A (RCRA), and Receive Condition Register B (RCRB).

Line States Description

Active Line State

The Line State Detector recognizes the incoming data to be in the Active Line State upon the reception of the Starting Delimiter (JK symbol pair).

The Line State Detector continues to indicate Active Line State while receiving data symbols, Ending Delimiter (T symbols), and Frame Status symbols (R and S) after the JK symbol pair.

Idle Line State

The Line State Detector recognizes the incoming data to be in the Idle Line State upon the reception of 2 Idle symbol pairs nominally (plus up to 9 bits of 1 in start up cases).

Idle Line State indicates the preamble of a frame or the lack for frame transmission during normal operation. Idle Line State is also used in the handshake sequence of the PHY Connection Management process.

TABLE 3-1. Symbol Decoding

Symbol	Incoming 5B	Decoded 4B
0	11110	0000
1	01001	0001
2	10100	0010
3	10101	0011
4	01010	0100
5	01011	0101
6	01110	0110
7	01111	0111
8	10010	1000
9	10011	1001
A	10110	1010
B	10111	1011
C	11010	1100
D	11011	1101
E	11100	1110
F	11101	1111
I (Idle)	11111	1010
H (Halt)	00100	0001
JK (Starting Delimiter)	11000 & 10001	1101
T (Ending Delimiter)	01101	0101
R (Reset)	00111	0110
S (Set)	11001	0111
Q (Quiet)	00000	0010
V (Violation)	00001	0010
V	00010	0010
V	00011	0010
V	00101	0010
V	00110	0010
V	01000	0010
V	01100	0010
V	10000	0010
V'		0011
I'		1011

Notes:

V' denotes PHY Invalid or an Elasticity Buffer stuff byte.

I' denotes Idle symbol in ILS or an Elasticity Buffer stuff byte.

Super Idle Line State

The Line State Detector recognizes the incoming data to be in the Super Idle Line State upon the reception of eight consecutive Idle symbol pairs nominally (plus 1 symbol pair).

The Super Idle Line State is used to insure synchronization.

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3.0 Functional Description (Continued)

No Signal Detect

The Line State Detector recognizes the incoming data to be in the No Signal Detect state upon the deassertion of the Signal Detect signal. No Signal Detect indicates that the incoming link is inactive.

Master Line State

The Line State Detector recognizes the incoming data to be in the Master Line State upon the reception of eight consecutive Halt-Quiet symbol pairs nominally (plus up to 2 symbol pairs in start up cases).

The Master Line State is used in the handshake sequence of the PHY Connection Management process.

Halt Line State

The Line State Detector recognizes the incoming data to be in the Halt Line State upon the reception of eight consecutive Halt symbol pairs nominally (plus up to 2 symbol pairs in start up cases).

The Halt Line State is used in the handshake sequence of the PHY Connection Management process.

Quiet Line State

The Line State Detector recognizes the incoming data to be in the Quiet Line State upon the reception of eight consecutive Quiet symbol pairs nominally (plus up to 9 bits of 0 in start up cases).

The Quiet Line State is used in the handshake sequence of the PHY Connection Management process.

Noise Line State

The Line State Detector recognizes the incoming data to be in the Noise Line State upon the reception of 16 noise symbol pairs.

The Noise Line State indicates that data is not received correctly. A detailed description of a noise event can be found in Section 8.2.

Line State Unknown

The Line State Detector recognizes the incoming data to be in the Line State Unknown state upon the reception of one inconsistent symbol pair (i.e. data that is not expected). This may be the beginning of a new line state.

Line State Unknown indicates that data is not received correctly. If the condition persists the noise line state may be entered.

ELASTICITY BUFFER

The Elasticity Buffer performs the function of a "variable depth" FIFO to compensate for clock skews between the Receive Clock (RXC±) and the Local Byte Clock (LBC).

Bit 5 (EBOU) of the Receive Condition Register B (RCRB) is set to 1 to indicate an error condition when the Elasticity Buffer cannot compensate for the clock skews.

The Elasticity Buffer will support maximum clock skews of ±50 ppm with a maximum packet length of 4500 bytes.

To make up for the accumulation of frequency disparity between the two clocks, the Elasticity Buffer will insert or delete Idle symbol pairs in the preamble. Data is written into the byte-wide registers of the Elasticity Buffer with the Receive Clock, while data is read from the registers with the Local Byte Clock.

The Elasticity Buffer will recenter (i.e. set the read and write pointers to a predetermined distance from each other) upon the detection of a JK or every four byte times during PHY Invalid (i.e. MLS, HLS, QLS, NLS, NSD) and Idle Line State. To resolve metastability problems, the Elasticity Buffer is designed such that a given register cannot be written and read simultaneously under normal operating conditions. In a symbol-wide station, a 5-bit off boundary JK following after a maximum size frame situation may be produced which may result in a small increase in the probability of an error caused by a metastability condition.

LINK ERROR DETECTOR

The Link Error Detector provides continuous monitoring of an active link (i.e. during Active and Idle Line States) to insure that it meets the minimum Bit Error Rate requirement as set by the standard or user to remain on the ring.

Upon detecting a link error, the internal 8-bit Link Error Monitor Counter is decremented. The start value for the Link Error Monitor Counter is programmed through the Link Error Threshold Register (LETR). When the Link Error Monitor Counter reaches zero, bit 4 (LEMT) of the Interrupt Condition Register (ICR) is set to 1. The current value of the Link Error Monitor Counter can be read through the Current Link Error Count Register (CLECR). For higher error rates the current value is an approximate count because the counter rolls over.

There are two ways to determine Link Error Rate: polling and interrupt.

Polling

The Link Error Monitor Counter is set to the value of FF. This start value is programmed through the Link Error Threshold Register (LETR).

Upon detecting a link error, the Current Link Error Counter is decremented.

The Host System reads the current value of the Link Error Monitor Counter via the Current Link Error Count Register (CLECR). The Counter is then reset to FF.

Interrupt

The Link Error Monitor Counter is set to the value of FF. This start value is programmed through the Link Error Threshold Register (LETR).

Upon detecting a link error, the Line Error Monitor Counter is decremented. When the counter reaches zero, bit 4 (LEMT) of the Interrupt Condition Register (ICR) is set to 1, and the interrupt signal goes low.

The Host System is interrupted when the Link Error Monitor Counter reaches 0.

A state table describing Link Errors in more detail can be found in Section 8.3.

Miscellaneous Items

When bit 0 (RUN) of the Mode Register (MR) is set to zero, or when the PLAYER device is reset through the Reset pin ($\overline{RST}$), the Signal Detect line (TTLSD) is internally forced to zero and the Line State Detector is set to Line State Unknown.

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3.0 Functional Description (Continued)

3.2 TRANSMITTER BLOCK

The Transmitter Block accepts 10-bit bytes from the Configuration Switch.

The Transmitter Block performs the following operations:

- Encodes the data from 4B to 5B coding
- Filters out code violations from the data stream
- Is capable of generating Idle, Master, Halt, Quiet, or other user defined symbol pairs
- Converts the data stream from NRZ to NRZI ready for transmission
- Serializes data

During normal operation, the Transmitter Block presents serial data to the fiber optic transmitter.

While in the External Loopback mode, the Transmitter Block presents serial data to the Clock Recovery Device.

The Transmitter Block consists of the following functional blocks:

Data Registers
Parity Checker
4B/5B Encoder
Repeat Filter
Smoother
Line State Generator
Injection Control Logic
Shift Register
NRZ to NRZI Encoder

See *Figure 3-2.*

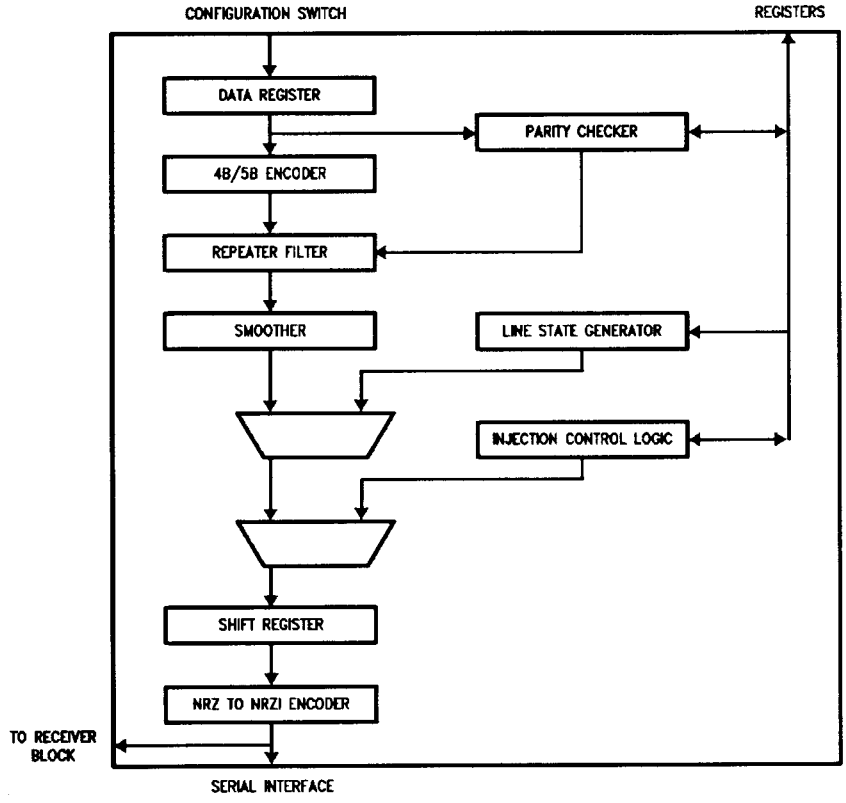

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FIGURE 3-2. Transmitter Block Diagram

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3.0 Functional Description (Continued)

DATA REGISTERS

Data from the Configuration Switch is stored in the Data Registers. The 10-bit byte-wide data consists of a parity bit, a control bit, and two 4-bit symbols as shown in *Figure 3-3*.

b9	b8	b7 b0
Parity Bit	Control Bit	Data Bits

FIGURE 3-3. Byte-Wide Data

PARITY CHECKER

The Parity Checker verifies that the parity bit in the Data Register represents odd parity (i.e. odd number of 1s).

The parity checking is enabled and disabled through bit 6 (PRDPE) of the Current Transmit State Register (CTSR).

If a parity error occurs, the Parity Checker will set bit 0 (DPE) in the Interrupt Condition Register (ICR) and report the error to the Repeat Filter.

4B/5B ENCODER

The 4B/5B Encoder converts the two 4-bit symbols from the Configuration Switch into their respective 5-bit codes.

See Table 3-2 for the Symbol Encoding list.

REPEAT FILTER

The Repeat Filter is used to prevent the propagation of code violations in data frames, to the downstream station.

Upon receiving violations in data frames, the Repeat Filter replaces them with two Halt symbol pairs followed by Idle symbols. Thus the code violations are isolated and recovered at each link and will not be propagated throughout the entire ring.

Details on Repeat Filter operation are described in Section 8.4.

SMOOTHER

The Smoother is used to keep the preamble length of a frame to a minimum of 6 Idle symbol pairs.

Idle symbols in the preamble of a frame may have been added or deleted by each station to compensate for the difference between the Receive Clock and its Local Clock. The preamble needs to be maintained at a minimum length to allow stations enough time to complete processing of one frame and prepare to receive another. Without the Smoother function, the minimum preamble length (6 Idle symbol pairs) may not be maintained as several stations may consecutively delete Idle symbols.

The Smoother attempts to keep the number of Idle symbol pairs in the preamble at 7 by:

- Deleting an Idle symbol pair in preambles which have more than 7 Idle symbol pairs

and/or

- Inserting an Idle symbol pair in preambles which have less than 7 idle symbol pairs (i.e. Extend State).

The Smoother Counter starts counting upon detecting an Idle symbol pair. It stops counting upon detecting a JK symbol pair.

More details on the operation of the Smoother can be found in Section 8.5.

LINE STATE GENERATOR

The Line State Generator allows the transmission of the PHY Request data and can also generate and transmit Idle, Master, Halt, or Quiet symbol pairs which can be used to implement the Connection Management procedures as specified in the FDDI Station Management (SMT) document.

The Line State Generator is programmed through Transmit bits 0 to 2 (TM<2:0>) of the Current Transmit State Register (CTSR).

Based on the setting of these bits, the Transmitter Block operates in the Transmit Modes where the Line State Generator overwrites the Repeat Filter and Smoother outputs.

See Table 3-3 for the listing of the Transmit Modes.

TABLE 3-2. 4B/5B Symbol Encoding

Symbol		4B Code	Outgoing 5B
0		0000	11110
1		0001	01001
2		0010	10100
3		0011	10101
4		0100	01010
5		0101	01011
6		0110	01110
7		0111	01111
8		1000	10010
9		1001	10011
A		1010	10110
B		1011	10111
C		1100	11010
D		1101	11011
E		1110	11100
F		1111	11101
N		0000	11110 or 11111
JK	(Starting Delimiter)	1101	11000 and 10001
T	(Ending Delimiter)	0100 or 0101	01101
R	(Reset)	0110	00111
S	(Set)	0111	11001

TABLE 3-3. Transmit Modes

Active Transmit Mode	Normal Transmission Mode
Off Transmit Mode	Transmit Quiet symbol pairs and disable the Fiber Optic Transmitter
Idle Transmit Mode	Transmit Idle symbol pairs
Master Transmit Mode	Transmit Halt-Quiet symbol pairs
Quiet Transmit Mode	Transmit Quiet symbol pairs
Reserved Transmit Mode	Reserved for future use. If selected, Quiet symbol pairs will be transmitted.
Halt Transmit Mode	Transmit Halt symbol pairs

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3.0 Functional Description (Continued)

INJECTION CONTROL LOGIC

The Injection Control Logic replaces the data stream with a programmable symbol pair. This function is used to transmit data other than the normal data frame or Line States.

The Injection Symbols overwrite the Line State Generator (Transmit Modes) and the Repeat Filter and Smoother outputs.

These programmable symbol pairs are stored in the Injection Symbol Register A (ISRA) and Injection Symbol Register B (ISRB). The Injection Threshold Register (IJTR) determines where the Injection Symbol pair will replace the data symbols.

The Injection Control Logic is programmed through the bits 0 and 1 (IC<1:0>) of the Current Transmit State Register (CTSR) to one of the following Injection Modes (see *Figure 3-4*):

1. No Injection (i.e. normal operation)
2. One Shot
3. Periodic
4. Continuous

In the No Injection mode, the data stream is transmitted unchanged.

In the One Shot mode, ISRA and ISRB are injected once on the nth byte after a JK, where n is the programmed value specified in the Injection Threshold Register.

In the Periodic mode, ISRA and ISRB are injected every nth symbol.

In the Continuous mode, all data symbols are replaced with the contents of ISRA and ISRB. This is the same as periodic mode with IJTR = 0.

SHIFT REGISTER

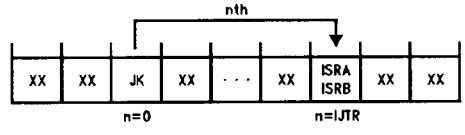
The Shift Regiser converts encoded parallel data to serial data. The parallel data is clocked into the Shift Register by the Transmit Byte Clock (TBC±), and clocked out by the Transmit Bit Clock (TXC±).

NRZ TO NRZI ENCODER

The NRZ to NRZI Encoder converts the serial Non-Return-To-Zero data to Non-Return-To-Zero-Invert-On-One data.

This function can be enabled and disabled through bit 6 (TNRZ) of the Mode Register (MR). When programmed to "0", it converts the bit stream from NRZ to NRZI. When programmed to "1", the bit stream is transmitted NRZ.

One Shot (Notes 1, 3)



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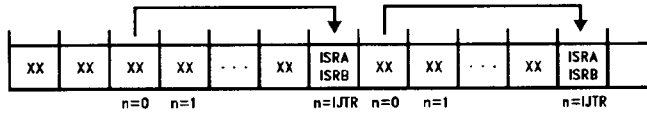
Periodic (Notes 2, 3)



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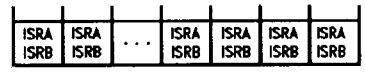
Continuous (Note 3)



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Where

ISRA: Injection Symbol Register A

ISRB: Injection Symbol Register B

IJTR: Injection Threshold Register

Note 1: In one shot when n + 0 the JK is replaced.

Note 2: In periodic when n = 0 all symbols are replaced.

Note 3: Max value on n = 255.

FIGURE 3-4. Injection Modes

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3.0 Functional Description (Continued)

3.3 CONFIGURATION SWITCH

The Configuration Switch consists of a set of multiplexors and latches which allow the PLAYER device to configure the data paths without the need of external logic. The Configuration Switch is controlled through the Configuration Register (CR).

The Configuration Switch has four internal buses, the A_Request bus, the B_Request bus, the Receive bus, and the PHY_Invalid bus. The two Request buses can be driven by external input data connected to the external PHY Port Interface. The Receive bus is internally connected to the Receive Block of the PLAYER device, while the PHY_Invalid bus has a fixed 10-bit LSU pattern, useful during the connection process. The configuration switch also has three internal multiplexors, each can select any of the four buses to connect to its respective data path. The first two are PHY Port Interface output data paths, A_Indicate and B_Indicate, that can drive output data paths of the external PHY Port Interface. The third output data path is connected internally to the Transmit Block.

The Configuration Switch is the same on both the DP83251 device and the DP83255 device. However, the DP83255 has two PHY Port interfaces connected to the Configuration Switch, whereas the DP83251 has one PHY Port Interface. The DP83255 uses the A_Request and A_Indicate paths as one PHY Port Interface and the B_Request and B_Indicate paths as the other PHY Port interface (see *Figure 3-5a*). The DP83251, having only one port interface, uses the B_Request and A_Indicate paths as its external port. The A_Request and B_Indicate paths of the DP83251 are null connections and are not used by this device (see *Figure 3-5b*).

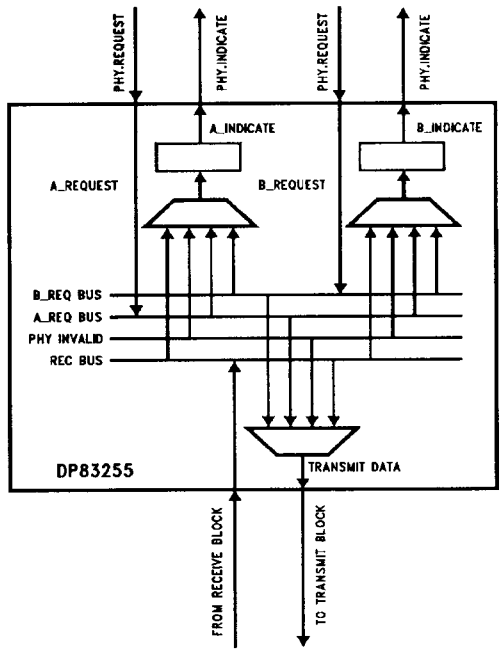

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FIGURE 3-5a. Configuration Switch Block Diagram for DP83255

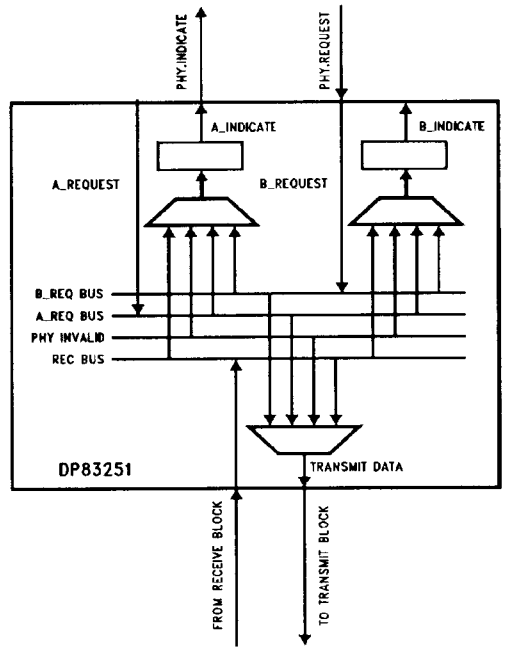

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FIGURE 3-5b. Configuration Switch Block Diagram for DP83251

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3.0 Functional Description (Continued)

STATION CONFIGURATIONS

Single Attach Station (SAS)

The Single Attach Station can be connected to either the Primary or Secondary ring via a Concentrator. Only 1 MAC is needed in a SAS.

Both the DP83251 and DP83255 can be used in a Single Attach Station. The DP83251 can be connected to the MAC via its only PHY Port Interface. The DP83255 can be connected to the MAC via either of the 2 PHY Port Interfaces.

See *Figures 3-6* and *3-7*.

Dual Attach Station (DAS)

A Dual Attach Station can be connected directly to the dual ring. There are two types of Dual Attach Stations: DAS with a Single MAC and DAS with Dual MACs. See *Figures 3-8* and *3-9*.

Although two DP83251s can be connected together to build a Dual Attach Station, it is recommended that the DP83255 is to be used for this type of station configuration.

A DAS with Single MAC can be configured as follows:

- B_Indicate data of PHY_A is connected to A_Request input of PHY_B. B_Request input of PHY_A is connected to A_Indicate output of PHY_B.
- The MAC can be connected to either the A_Request input and the A_Indicate output of PHY_A or the B_Request input and the B_Indicate output of PHY_B.

The DAS with Dual MACs can be configured as follows:

- B_Indicate data of PHY_A is connected to A_Request input of PHY_B. B_Request input of PHY_A is connected to A_Indicate output of PHY_B.
- The MAC_1 is connected to the B_Indicate output and the B_Request Input of PHY_B.
- The MAC_2 is connected to the A_Indicate output and the A_Request Input of PHY_A.

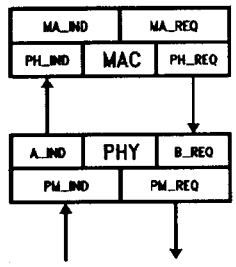

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FIGURE 3-6. Single Attach Station Using the DP83251

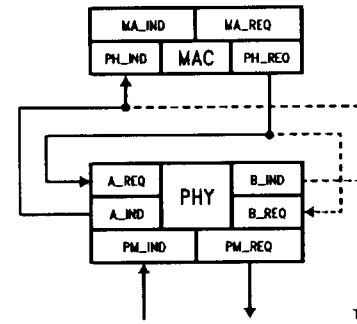

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FIGURE 3-7. Single Attachment Station (SAS) Using the DP83255

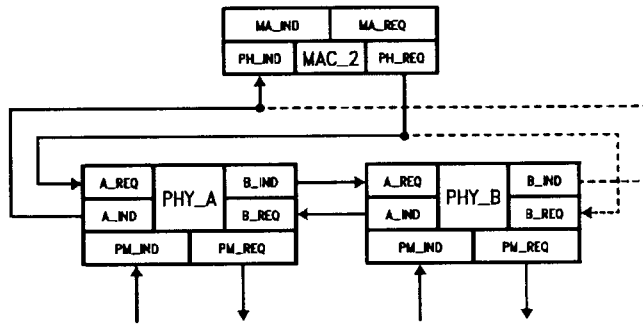

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FIGURE 3-8. Dual Attachment Station (DAS), Single MAC

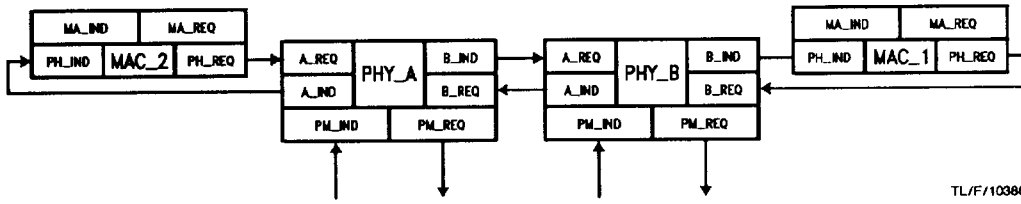

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FIGURE 3-9. Dual Attachment Station (DAS), Dual MACs

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3.0 Functional Description (Continued)

CONCENTRATOR CONFIGURATIONS

There are 2 types of Concentrators: Single Attach and Dual Attach. These Concentrators can be designed with or without the MAC(s). Its configuration is determined based upon its type and the number of active MACs in the Concentrator.

Using the PLAYER devices, a Concentrator can be built with many different configurations without the need of any external logic.

Both the DP83251 and DP83255 can be used to build a Single Attach Concentrator. Only the DP83255 is recommended for the Dual Attach Concentrator design.

See Application Note 675, Designing FDDI Concentrators and Application Note 741, Differentiating FDDI Concentrators for futher information.

Concepts

A Concentrator is comprised of 2 parts: the Dual Ring Connect portion and the Master Ports.

The Dual Ring Connection portion connects the Concentrator to the dual ring directly or to another Concentrator. If the Concentrator is connected directly to the dual ring, it is a part of the "Dual Ring Tree". If the Concentrator is connected to another Concentrator, it is a "Branch" of the "Dual Ring Tree".

The Master Ports connect the Concentrator to its "Slaves". A Slave could be a Single Attach Station or another Concentrator (thus forming another Branch of the Dual Ring Tree).

When a MAC in a concentrator is connected to the Primary or Secondary Ring, it is required to be situated at the exit port of that concentrator (i.e. its PH_IND is connected to the IND Interface of the last Master Port in the Concentrator (PHY_M n) that is connected to that ring).

A Concentrator can have two MACs connected to both the Primary and Secondary rings. In addition, a Roving MAC can be included in the Concentrator configuration. A Roving MAC can be used to test the stations connected to the Concentrator before allowing them to join the Dual Ring. This may require external multiplexers.

Single Attach Concentrator

A Single Attach Concentrator is a Concentrator that has only one PHY at the Dual Ring Connect side. It cannot, therefore, be connected directly to the Dual Ring. A Single Attach Concentrator is a Branch to the Dual Ring Tree. It is connected to the ring as a Slave of another Concentrator.

Multiple Single Attach Concentrators can be connected together hierarchically to build multiple levels of branches in a Dual Ring.

The Single Attach Concentrator can be connected to either the Primary or Secondary ring depending on the connection with its Concentrator (the Concentrator that it is connected to a slave).

Figure 3-10 shows a Single Attach Concentrator with a Single MAC.

Dual Attach Concentrator

A Dual Attach Concentrator is a Concentrator that has two PHYs at the Dual Ring Connect side. It is connected directly to the dual ring and is a part of the Dual Ring Tree.

The Dual Attach Concentrator is connected to both the Primary and Secondary rings.

Dual Attach Concentrator with Single MAC

Figure 3-11 shows a Dual Attach Concentrator with a Single MAC.

Because the Concentrator has one MAC, it can only transmit and receive frames on the ring where the MAC is connected. The Concentrator can only repeat frames on the other ring.

Dual Attach Concentrator with Dual MACs

Figure 3-12 shows Dual Attach Concentrator wih Dual MACs.

Because the Concentrator has two MACs, it can transmit and receive frames on both the Primary and Secondary rings.

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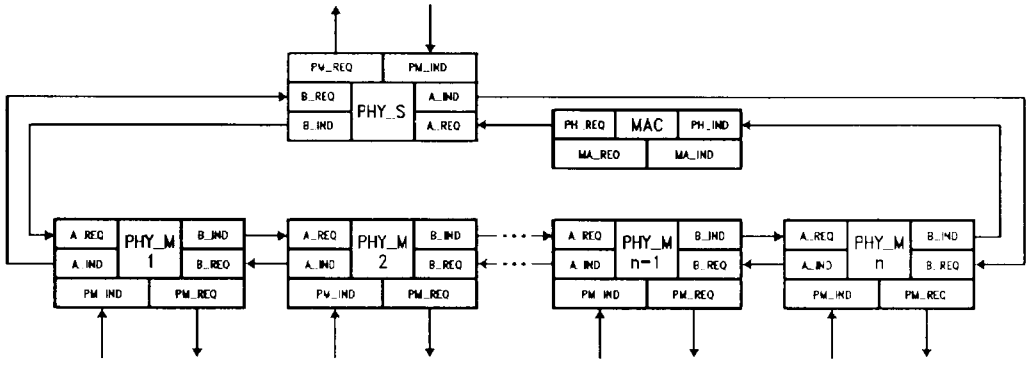

FIGURE 3-10. Single Attach Concentrator (SAC), Single MAC

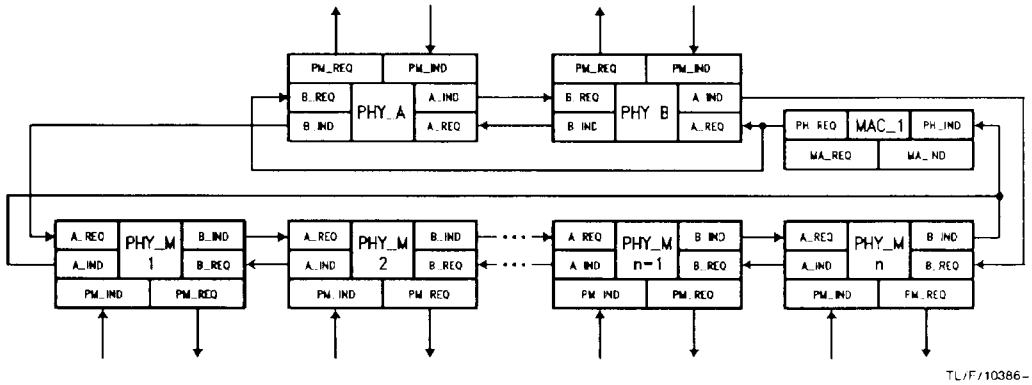

FIGURE 3-11. Dual Attach Concentrator (DAC), Single MAC

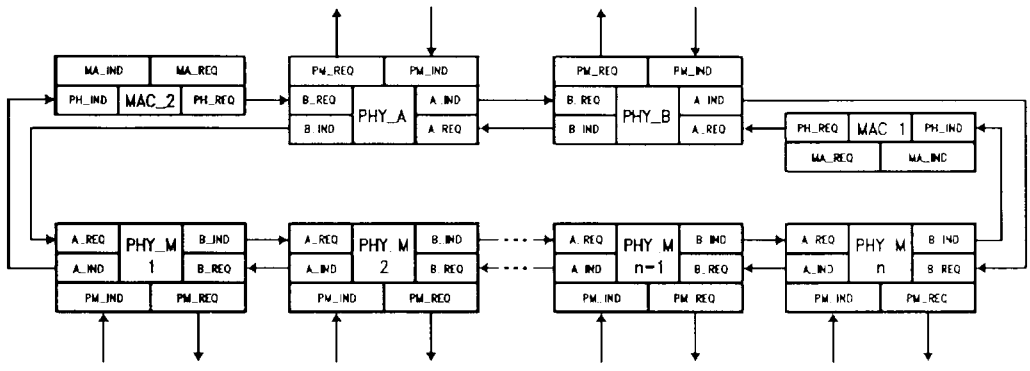

FIGURE 3-12. Dual Attach Concentrator (DAC), Dual MACs

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4.0 Modes of Operation

The PLAYER device can operate in 4 basic modes: RUN, STOP, LOOPBACK, and CASCADE.

4.1 RUN MODE

RUN is the normal mode of operation.

In this mode, the PLAYER device is configured to be connected to the media via the Fiber Optic Transmitter and Receiver at the Serial Interface. It is also connected to other PLAYER device(s) and/or BMAC device(s) via the Port A and Port B Interfaces.

While operating in the Run mode, the PLAYER device receives and transmits Line States (Quiet, Halt, Master, Idle) and frames (Active Line State).

4.2 STOP MODE

The PLAYER device operates in the STOP mode while it is being initialized or configured.

The PLAYER device is also reset to the STOP mode automatically when the $\overline{RST}$ pin (pin 71 on the DP83251 and pin 111 on the DP83255) is set to ground.

When in STOP mode, the PLAYER device performs the following functions:

- Resets the Repeat Filter.
- Resets the Smoother.
- Resets the Receiver Block Line State Counters.
- Flushes the Elasticity Buffer.
- Forces Line State Unknown in the Receiver Block.
- Outputs LSU symbol pairs (0 1 0011 1010) through the PHY Data Indicate pins (AIP, AIC, AID <7:0>, BIP, BIC, BID<7:0>).
- Outputs Quiet symbol pairs through the PMD Data Request pins (TXD±).
- Resets all Control Bus register contents to zero or default values.

4.3 LOOPBACK MODE

The PLAYER device provides three types of loopback tests: Configuration Switch Loopback, Internal Loopback, and External Loopback. These Loopback modes can be used to test different portions of the device.

4.3.1 Configuration Switch Loopback

The Configuration Switch Loopback can be used to test the data paths of the BMAC device(s) that are connected to the PLAYER device before transmitting and receiving data through the network.

In the Configuration Switch Loopback mode, the PLAYER device performs the following functions:

- Selects Port A PHY Request Data, Port B PHY Request Data, or PHY Invalid to connect to Port A PHY Indicate Data via the A_IND Mux.
- Selects Port A PHY Request Data, Port B PHY Request Data, or PHY Invalid to connect to Port B PHY Indicate Data via the B_IND Mux.
- Connects data from the Receiver Block to the Transmitter Block via the Transmitter_Mux. (The PLAYER device is repeating incoming data from the media in the Configuration Switch Loopback mode.)

See *Figure 4-1a* and *4-1b* for block diagrams.

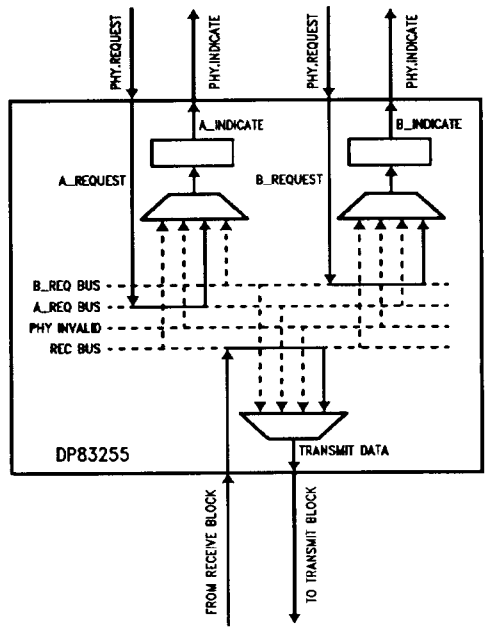

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FIGURE 4-1a. Configuration Switch Loopback for DP83255

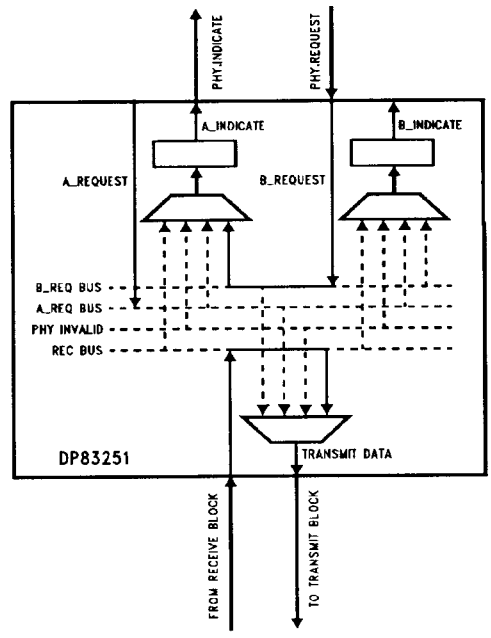

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FIGURE 4-1b. Configuration Switch Loopback for DP83251

FIGURE 4-1.

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4.0 Modes of Operation (Continued)

4.3.2 Internal Loopback

The Internal Loopback mode can be used to test the functionality of the PLAYER device and to test the data paths between the PLAYER and BMAC devices before ring insertion.

When in the Internal Loopback mode, the PLAYER device performs the following functions:

- Directs the output data of the Transmitter Block to the input of the Receiver Block through internal paths (see *Figure 2-1* PLAYER Device Block Diagram).
- Ignores the PMD Data Indicate pins (RXD± and RXC±),
- Outputs Quiet symbols through the PMD Data Request pins (TXD±), and
- Outputs Quiet symbols through the External Loopback Data pins (LBD±).

The level of the Quiet symbols transmitted through the TXC± pins is programmable through the Transmit Quiet Level bit of the Mode Register.

The level of the Quiet symbols transmitted through the LBD± pins is always high, regardless of the Transmit Quiet Level bit of the Mode Register.

If both Internal Loopback and External Loopback modes are selected, Internal Loopback mode will have priority over External Loopback mode.

See *Figure 4-2* for a block diagram.

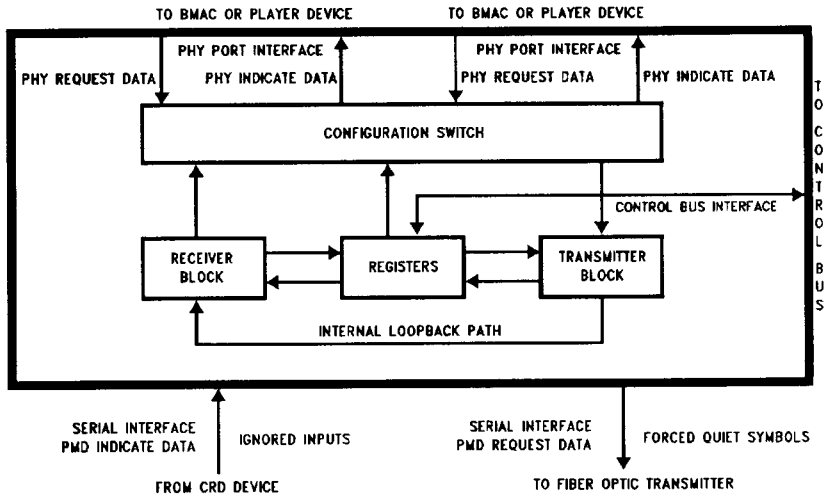

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FIGURE 4-2. Internal Loopback

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4.0 Modes of Operation (Continued)

4.3.3 External Loopback

The External Loopback mode can be used to test the functionality of the PLAYER device and to test the data paths between the PLAYER, CRD, and BMAC devices before transmitting and receiving data through the network.

When in the External Loopback mode, the PLAYER device performs the following functions:

- Directs the output data of the Transmitter Block to the external Loopback Data pins (LBD±), which are normally connected to the Clock Recovery Device (see *Figure 2.* PLAYER Device Block Diagram).
- Outputs Quiet symbols through the PMD Data Request pins (TXD±).

The level of the Quiet symbols transmitted through the TXC± pins is programmable through the Transmit Quiet Level bit of the Mode Register.

If both Internal Loopback and External Loopback modes are selected, Internal Loopback mode will have priority over External Loopback mode.

See *Figure 4-3* for a block diagram.

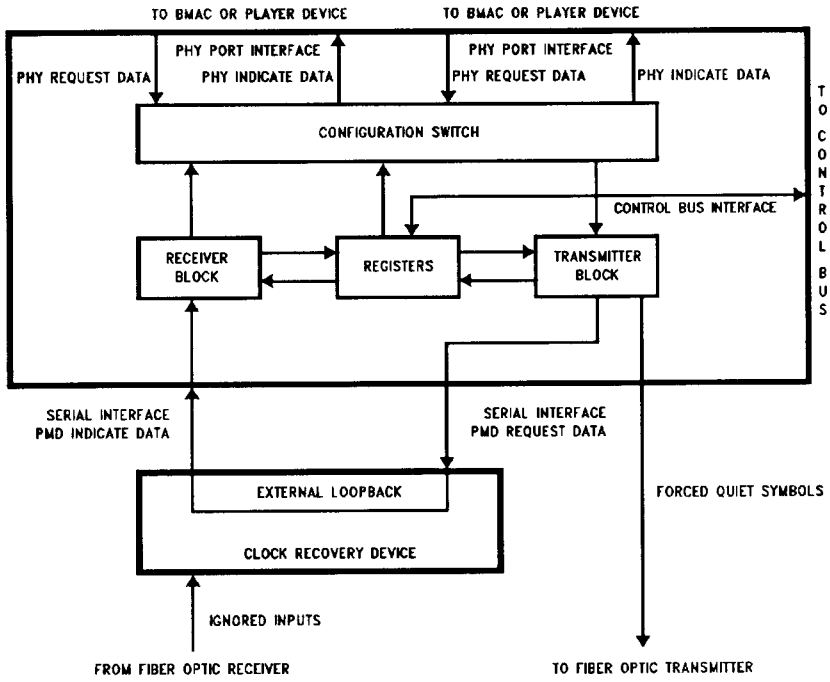

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FIGURE 4-3. External Loopback

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4.0 Modes of Operation (Continued)

4.4 CASCADE MODE

The PLAYER device can operate in the Cascade (parallel) mode—*Figure 4-4*—which is used in high bandwidth, point-to-point data transfer applications. This is a non-FDDI mode of operation.

CONCEPTS

In the Cascade mode, multiple PLAYER devices are connected together to provide data transfer at multiples of the FDDI data rate. Two cascaded PLAYER devices provide a data rate twice the FDDI data rate; three cascaded PLAYER devices provide a data rate three times the FDDI data rate, etc.

Multiple data streams are transmitted in parallel over each pair of cascaded PLAYER devices. All data streams start simultaneously and begin with the JK symbol pair on each PLAYER device.

Data is synchronized at the receiver of each PLAYER device by the JK symbol pair. Upon receiving a JK symbol pair, a PLAYER device asserts the Cascade Ready signal to indicate the beginning of data reception.

The Cascade Ready signals of all PLAYER devices are open drain ANDed together to create the Cascade Start signal. The Cascade Start signal is used as the input to indicate that all PLAYER devices have received the JK symbol pair. Data is now being received at every PLAYER device and can be transferred from the cascaded PLAYER devices to the host system.

See *Figure 4-5* for more information.

OPERATING RULES

When the PLAYER device is operating in Cascade mode, the following rules apply:

1. Data integrity can be guaranteed if the worst case fiber optic transmission skew between parallel fiber cables is less than 40 ns. This amounts to about 785 meters of fiber, assuming a 1% worst case variance.
2. Even though this is a non-FDDI application, the general rules for FDDI frames must be obeyed.
   - Data frames must be a minimum of three bytes long (including the JK symbol pair). Smaller frames will cause Elasticity Buffer errors.
   - Data frames must have a maximum size of 4500 bytes, with a JK starting delimiter and a (T or R or S)x or x(T or R or S) ending delimiter byte.
3. Due to the different clock rates, the JK symbol pair may arrive at different times at each PLAYER device. The total skew between the fastest and slowest cascaded PLAYER devices receiving the JK starting delimiter must not exceed 80 ns.
4. The first PLAYER device to receive a JK symbol pair will present it to the host system and assert the Cascade Ready signal. The PLAYER device will present one more JK as it waits for the other PLAYER devices to recognize their JK. The maximum number of consecutive JKs that can be presented to the host is 2.
5. The Cascade Start signal is set to 1 when all the cascaded PLAYER devices release their Cascade Ready signals.
6. Bit 4 (CSE) of the Receive Condition Register B (RCRB) is set to 1 if the Cascade Start signal (CS) is *not* set before the second falling edge of clock signal LBC from when Cascade Ready (CR) was released. CS has to be set within approximately 80 ns of CR release. This condition signifies that not all cascaded PLAYERs have received their respective JK symbol pair within the allowed skew range.
7. If the JK symbols are corrupted in the point-to-point links, some PLAYER devices may not report a Cascaded Synchronization Error.
8. To guarantee integrity of the interframe information, the user must put at least 8 Idle symbol pairs between frames. The PLAYER device will function properly with only 4 Idle symbol pairs, however the interframe symbols may be corrupted with random non-JK symbols.

The BMAC device could be used to provide required framing and optical FCS support.

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4.0 Modes of Operation (Continued)

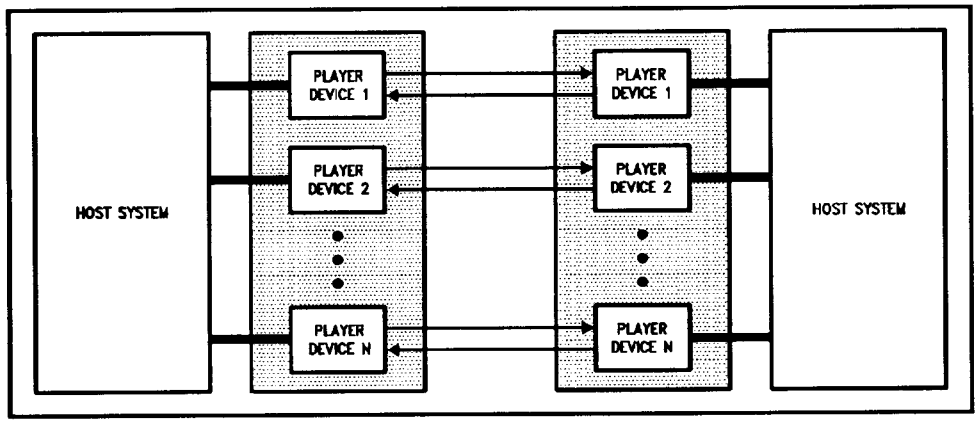

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FIGURE 4-4. Parallel Transmission

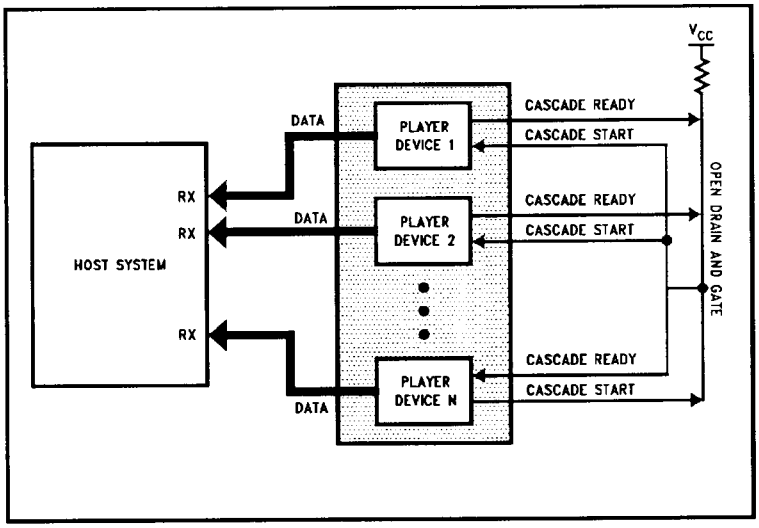

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FIGURE 4-5. Cascade Mode of Operation

Note: N is recommended to be less than 3 for this mode. See Application Note 679 for larger values of N.

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5.0 Registers

The PLAYER device is initialized, configured, and monitored via 32 8-bit registers. These registers are accessible through the Control Bus Interface.

Table 5-1 is a Register Summary List. Table 5-2 shows the contents of each register.

TABLE 5-1. Register Summary

Register Address	Register Symbol	Register Name	Access Rules	
			Read	Write
00h	MR	Mode Register	Always	Always
01h	CR	Configuration Register	Always	Always
02h	ICR	Interrupt Condition Register	Always	Conditional
03h	ICMR	Interrupt Condition Mask Register	Always	Always
04h	CTSR	Current Transmit State Register	Always	Conditional
05h	IJTR	Injection Threshold Register	Always	Always
06h	ISRA	Injection Symbol Register A	Always	Always
07h	ISRB	Injection Symbol Register B	Always	Always
08h	CRSR	Current Receive State Register	Always	Write Reject
09h	RCRA	Receive Condition Register A	Always	Conditional
0Ah	RCRB	Receive Condition Register B	Always	Conditional
0Bh	RCMRA	Receive Condition Mask Register A	Always	Always
0Ch	RCMRB	Receive Condition Mask Register B	Always	Always
0Dh	NTR	Noise Threshold Register	Always	Always
0Eh	NPTR	Noise Prescale Threshold Register	Always	Always
0Fh	CNCR	Current Noise Count Register	Always	Write Reject
10h	CNPCR	Current Noise Prescale Count Register	Always	Write Reject
11h	STR	State Threshold Register	Always	Always
12h	SPTR	State Prescale Threshold Registger	Always	Always
13h	CSCR	Current State Count Register	Always	Write Reject
14h	CSPCR	Current State Prescale Count Register	Always	Write Reject
15h	LETR	Link Error Threshold Register	Always	Always
16h	CLECR	Current Link Error Count Register	Always	Write Reject
17h	UDR	User Definable Register	Always	Always
18h	IDR	Device ID Register	Always	Write Reject
19h	CIJCR	Current Injection Count Register	Always	Write Reject
1Ah	ICCR	Interrupt Condition Comparison Register	Always	Always
1Bh	CTSCR	Current Transmit State Comparison Register	Always	Always
1Ch	RCCRA	Receive Condition Comparison Register A	Always	Always
1Dh	RCCRB	Receive Condition Comparison Register B	Always	Always
1Eh	RR0	Reserved Register 0	Always	Write Reject
1Fh	RR1	Reserved Register 1	Always	Write Reject

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5.0 Registers (Continued)

TABLE 5-2. Register Content Summary

Register Address	Register Symbol	Bit Symbols							
		D7	D6	D5	D4	D3	D2	D1	D0
00h	MR	RNRZ	TNRZ	TE	TQL	CM	EXLB	ILB	RUN
01h	CR	BIE	AIE	TRS1	TRS0	BIS1	BIS0	AIS1	AIS0
02h	ICR	UDI	RCB	RCA	LEMT	CWI	CCR	CPE	DPE
03h	ICMR	UDIM	RCBM	RCAM	LEMTM	CWIM	CCRM	CPEM	DPEM
04h	CTSR	RES	PRDPE	SE	IC1	IC0	TM2	TM1	TM0
05h	IJTR	IJT7	IJT6	IIJ5	IJT4	IJT3	IJT2	IJT1	IJT0
06h	ISRA	RES	RES	RES	IJS4	IJS3	IJS2	IJS1	IJS0
07h	ISRB	RES	RES	RES	IJS9	IJS8	IJS7	IJS6	IJS5
08h	CRSR	RES	RES	RES	RES	LSU	LS2	LS1	LS0
09h	RCRA	LSUPI	LSC	NT	NLS	MLS	HLS	QLS	NSD
0Ah	RCRB	RES	SILS	EBOU	CSE	LSUPV	ALS	ST	ILS
0Bh	RCMRA	LSUPIM	LSCM	NTM	NLSM	NLSM	HLSM	QLSM	NSDM
0Ch	RCMRB	RES	SILSM	EBOUM	CSEM	LSUPVM	ALSM	STM	ILSM
0Dh	NTR	RES	NT6	NT5	NT4	NT3	NT2	NT1	NT0
0Eh	NPTR	NPT7	NPT6	NPT5	NPT4	NPT3	NPT2	NPT1	NPT0
0Fh	CNCR	NCLSCD	CNC6	CNC5	CNC4	CNC3	CNC2	CNC1	CNC0
10h	CNPCR	CNPC7	CNPC6	CNPC5	CNPC4	CNPC3	CNPC2	CNPC1	CNPC0
11h	STR	RES	ST6	ST5	ST4	ST3	ST2	ST1	ST0
12h	SPTR	SPT7	SPT6	SPT5	SPT4	SPT3	SPT2	SPT1	SPT0
13h	CSCR	SCLSCD	CSC6	CSC5	CSC4	CSC3	CSC2	CSC1	CSC0
14h	CSPCR	CSPC7	CSPC6	CSPC5	CSPC4	CSPC3	CSPC2	CSPC1	CSPC0
15h	LETR	LET7	LET6	LET5	LET4	LET3	LET2	LET1	LET0
16h	CLECR	LEC7	LEC6	LEC5	LEC4	LEC3	LEC2	LEC1	LEC0
17h	UDR	RES	RES	RES	RES	EB1	EB0	SB1	SB0
18h	IDR	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
19h	CIJCR	IJC7	IJC6	IJC5	IJC4	IJC3	IJC2	IJC1	IJC0
1Ah	ICCR	UDIC	RCBC	RCAC	LEMTC	CWIC	CCRC	CPEC	DPEC
1Bh	CTSCR	RESC	PRDPEC	SEC	IC1C	IC0C	TM2C	TM1C	TM0C
1Ch	RCCRA	LSUPIC	LSCC	NTC	NLSC	MLSC	HLSC	QLSC	NSDC
1Dh	RCCRB	RESC	SILSC	EBOUC	CSEC	LSUPVC	ALSC	STC	ILSC
1Eh	RR1	RES	RES	RES	RES	RES	RES	RES	RES
1Fh	RR2	RES	RES	RES	RES	RES	RES	RES	RES

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5.0 Registers (Continued)

MODE REGISTER (MR)

The Mode Register is used to initialize and configure the PLAYER device.

In order to minimize interruptions on the network, it is recommended that the PLAYER device first be put in STOP mode (i.e. set the RUN bit to zero) before programming the Mode Register, the Configuration Register, or the Current Transmit State Register.

ACCESS RULES

ADDRESS	READ	WRITE
00h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RNRZ	TNRZ	TE	TQL	CM	EXLB	ILB	RUN

Bit	Symbol	Description
D0	RUN	**RUN /STOP** 0: Enables the STOP mode. Refer to Section 4.2, STOP Mode of Operation, for more information. 1: Normal Operation (i.e. RUN mode). **Note:** The RUN bit is automatically set to 0 when the RST pin is asserted (i.e. set to ground).
D1	ILB	**INTERNAL LOOPBACK:** 0: Disables Internal Loopback mode (i.e. normal operation). 1: Enables Internal Loopback mode. Refer to Section 4.3, Loopback Mode of Operation, for more information.
D2	EXLB	**EXTERNAL LOOPBACK** 0: Disables External Loopback mode (i.e. normal operation). 1: Enables External Loopback mode. Refer to Section 4.3, Loopback Mode of Operation, for more information.
D3	CM	**CASCADE MODE:** 0: Disables synchronization of cascaded PLAYER devices. 1: Enables the synchronization of cascaded PLAYER devices. Refer to Section 4.4, Cascade Mode of Operation, for more information.
D4	TQL	**TRANSMIT QUIET LEVEL:** This bit is used to program the transmission level of the Quiet symbols. 0: Low level Quiet symbols are transmitted through the PMD Data Request pins (i.e. TXD+ = low, TXD− = high). 1: High level Quiet symbols are transmitted through the PMD Data Request pins (i.e. TXD+ = high, TXD− = low).
D5	TE	**TRANSMIT ENABLE:** The TE bit controls the action of FOTX Enable (TXE) pin independent of the current transmit mode. When TE is 0, the TXE output disables the optical transmitter; when TE is 1, the optical transmitter is disabled during the Off Transmit Mode (OTM) and enabled otherwise. The On and Off level of the TXE is dependent on the FOTX Enable Level (TEL) pin to the PLAYER device. The following rules summarizes the output of TXE: (1) If TE = 0, then TXE = Off (2) If TE = 1 and OTM, then TXE = 0ff (3) If TE = 1 and not OTM, then TXE = On.
D6	TNRZ	**TRANSMIT NRZ DATA:** 0: Transmits data in Non-Return-To-Zero-Invert-On-Ones format. 1: Transmits data in Non-Return-To-Zero format.
D7	RNRZ	**RECEIVE NRZ DATA:** 0: Receives data in Non-Return-To-Zero-Invert-On-Ones format. 1: Receives data in Non-Return-To-Zero format.

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5.0 Registers (Continued)

CONFIGURATION REGISTER (CR)

The Configuration Register controls the Configuration Switch Block and enables/disables both the A and B Indicate output ports.

Note that the B_Indicate output port is offered only on the DP83255 (for Dual Attach Stations), and not in the DP83251 (for Single Attach Stations).

For further information, refer to Section 3.3, Configuration Switch.

ACCESS RULES

ADDRESS	READ	WRITE
01h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
BIE	AIE	TRS1	TRS0	BIS1	BIS0	AIS1	AIS0

Bit	Symbol	Description
D0, D1	AIS0, AIS1	**A_INDICATE SELECTOR <0, 1>:** The A_Indicate Selector <0, 1> bits select one of the four Configuration Switch data buses for the A_Indicate output port (AIP, AIC, AID <7:0>). **AIS1 AIS0** 0 0 PHY Invalid Bus 0 1 Receiver Bus 1 0 A_Request Bus 1 1 B_Request Bus
D2, D3	BIS0, BIS1	**B_INDICATE SELECTOR <0, 1>:** The B_Indicate Selector <0, 1> bits select one of the four Configuration Switch data buses for the B_Indicate output port (BIP, BIC, BID <7:0>). **BIS1 BIS0** 0 0 PHY Invalid Bus 0 1 Receiver Bus 1 0 A_Request Bus 1 1 B_Request Bus **Note:** Even though this bit can be set and/or cleared in the DP83251 (for Single Attach Stations), it will not affect any I/Os since the DP83251 does not offer a B_Indicate port.
D4, D5	TRS0, TRS1	**TRANSMIT REQUEST SELECTOR <0, 1>:** The Transmit Request Selector <0, 1> bits select one of the four Configuration Switch data buses for the input to the Transmitter Block. **TRS1 TRS0** 0 0 PHY Invalid Bus 0 1 Receiver Bus 1 0 A_Request Bus 1 1 B_Request Bus **Note:** If the PLAYER device is in Active Transmit Mode (i.e. the Transmit Mode bits (TM <2:0>) of the Current Transmit State Register (CTSR) are set to 000) and the PHY Invalid Bus is selected, then the PLAYER device will transmit a maximum of four Halt symbol pairs and then continuous Idle symbols due to the Repeat Filter.
D6	AIE	**A_INDICATE ENABLE:** 0: Disables the A_Indicate output port. The A_Indicate port pins will be at TRI-STATE when the port is disabled. 1: Enables the A_Indicate output port (AIP, AIC, AID<7:0>).
D7	BIE	**B_INDICATE ENABLE:** 0: Disable the B_Indicate output port. The B_Indicate port pins will be at TRI-STATE when the port is disabled. 1: Enables the B_Indicate output port (BIP, BIC, BID<7:0>). **Note:** Even though this bit can be set and/or cleared in the DP83251 (for Single Attach Stations), it will not affect any I/Os since the DP83251 does not offer a B_Indicate port.

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5.0 Registers (Continued)

INTERRUPT CONDITION REGISTER (ICR)

The Interrupt Condition Register records the occurrence of an internal error event, the detection of Line State, an unsuccessful write by the Control Bus Interface, the expiration of an internal counter, or the assertion of one or more of the User Definable Sense pins.

The Interrupt Condition Register will assert the Interrupt pin ($\overline{INT}$) when one or more bits within the register are set to 1 and the corresponding mask bits in the Interrupt Condition Mask Register (ICMR) are also set to 1.

ACCESS RULES

ADDRESS	READ	WRITE
02h	Always	Conditional

D7	D6	D5	D4	D3	D2	D1	D0
UDI	RCB	RCA	LEMT	CWI	CCR	CPE	DPE

Bit	Symbol	Description
D0	DPE	**PHY_REQUEST_DATA PARITY ERROR:** This bit will be set to 1 when: (1) The PHY Request Data Parity Enable bit (PRDPE) of the Current Transmit State Register (CTSR) is set to 1 and (2) The Transmitter Block detects a parity error in the incoming PHY Request Data. The source of the data can be from the PHY Invalid Bus, the Receiver Bus, the A_Bus, or the B_Bus of the Configuration Switch.
D1	CPE	**CONTROL BUS DATA PARITY ERROR:** This bit will be set to 1 when: (1) The Control Bus Parity Enable pin is asserted (CBPE = V_{CC}) and (2) The Control Bus Interface detects a parity error in the incoming Control Bus Data (CBD<7:0>) during a write cycle.
D2	CCR	**CONTROL BUS WRITE COMMAND REJECT:** This bit will be set to 1 when an attempt to write into one of the following read-only registers is made: Current Receive State Register (Register 08, CRSR) Current Noise Count Register (Register 0F, CNCR) Current Noise Prescale Count Register (Register 10, CNPCR) Current State Count Register (Register 13, CSCR) Current State Prescale Count Register (Register 14, CSPCR) Current Link Error Count Register (Register 16, CLECR) Device ID Register (Register 18, IDR) Current Injection Count Register (Register 19, CIJCR) Reserved Register 0 (Register 1E, RR0) Reserved Register 1 (Register 1F, RR1)
D3	CWI	**CONDITIONAL WRITE INHIBIT:** Set to 1 when bits within mentioned registers do not match bits in compare register. This bit ensures that new (i.e. unread) data is not inadvertently cleared while old data is being cleared through the Control Bus Interface. This bit is set to 1 to prevent the setting or clearing of any bit within the following registers: Interrupt Condition Register (Register 02, ICR) Current Transmit State Register (Register 04, CTSR) Receive Condition Register A (Register 09, RCRA) Receive Condition Register B (Register 0A, RCRB) when they differ from the value of the corresponding bit in the following registers respectively: Interrupt Condition Compare Register (Register 1A, ICCR) Current Transmit State Compare Register (Register 1B, CTSCR) Receive Condition Compare Register A (Register 1C, RCCRA) Receive Condition Compare Register B (Register 1D, RCCRB) This bit must be cleared by software. Note that this differs from the BMAC device bit of the same name.

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5.0 Registers (Continued)

INTERRUPT CONDITION REGISTER (ICR) (Continued)

Bit	Symbol	Description
D4	LEMT	**LINK ERROR MONITOR THRESHOLD:** This bit is set to 1 when the internal 8-bit Link Error Monitor Counter reaches zero. It will remain set until cleared by software. During the reset process (i.e. $\overline{RST}$ = GND), the Link Error Monitor Threshold bit is set to 1 because the Link Error Monitor Counter is initialized to zero.
D5	RCA	**RECEIVE CONDITION A:** This bit is set to 1 when: (1) One or more bits in the Receive Condition Register A (RCRA) is set to 1 and (2) The corresponding mask bits in the Receive Condition Mask Register A (RCMRA) are also set to 1. In order to clear (i.e. set to 0) the Receive Condition A bit, the bits within the Receive Condition Register A that are set to 1 must first be either cleared or masked.
D6	RCB	**RECEIVE CONDITION B:** This bit is set to 1 when: (1) One or more bits in the Receive Condition Register B (RCRB) is set to 1 and (2) The corresponding mask bits in the Receive Condition Mask Register B (RCMRB) are also set to 1. In order to clear (i.e. set to 0) the Receive Condition B bit, the bits within the Receive Condition Register B that are set to 1 must first be either cleared or masked.
D7	UDI	**USER DEFINABLE INTERRUPT:** This bit is set to 1 when one or both of the Sense Bits (SB0 or SB1) in the User Definable Register (UDR) is set to 1. In order to clear (i.e. set to 0) the User Definable Interrupt Bit, both Sense Bits must be set to 0.

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5.0 Registers (Continued)

INTERRUPT CONDITION MASK REGISTER (ICMR)

The Interrupt Condition Mask Register allows the user to dynamically select which events will generate an interrupt.

The Interrupt pin will be asserted (i.e. INT = GND) when one or more bits within the Interrupt Condition Register (ICR) are set to 1 and the corresponding mask bits in this register are also set to 1.

This register is cleared (i.e. set to 0) and all interrupts are initially masked during the reset process.

ACCESS RULES

ADDRESS	READ	WRITE
03h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
UDIM	RCBM	RCAM	LEMTM	CWIM	CCRM	CPEM	DPEM

Bit	Symbol	Description
D0	DPEM	**PHY_REQUEST_DATA PARITY ERROR MASK:** The mask bit for the PHY_Request Data Parity Error bit (DPE) of Interrupt Condition Register (ICR).
D1	CPEM	**CONTROL BUS DATA PARITY ERROR MASK:** The mask bit for the Control Bus Data Parity Error bit (CPE) of the Interrupt Condition Register (ICR).
D2	CCRM	**CONTROL BUS WRITE COMMAND REJECT MASK:** The mask bit for the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR).
D3	CWIM	**CONDITIONAL WRITE INHIBIT MASK:** The mask bit for the Conditional Write Inhibit bit (CWI) of the Interrupt Condition Register (ICR).
D4	LEMTM	**LINK ERROR MONITOR THRESHOLD MASK:** The mask bit for the Link Error Monitor Threshold bit (LEMT) of the Interrupt Condition Register (ICR).
D5	RCAM	**RECEIVE CONDITION A MASK:** The mask bit for the Receive Condition A bit (RCA) of the Interrupt Condition Register (ICR).
D6	RCBM	**RECEIVE CONDITION B MASK:** The mask bit for the Receive Condition B bit (RCB) of the Interrupt Condition Register (ICR).
D7	UDIM	**USER DEFINABLE INTERRUPT MASK:** The mask bit for the User Definable Interrupt bit (UDI) of the Interrupt Condition Register (ICR).

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5.0 Registers (Continued)

CURRENT TRANSMIT STATE REGISTER (CTSR)

The Current Transmit State Register can program the Transmitter Block to internally generate and transmit Idle, Master, Halt, Quiet, or user programmable symbol pairs, in addition to the normal transmission of incoming PHY Request data. The Smoother and PHY Request Data Parity may also be enabled and disabled through this register.

The Transmit Modes overwrite the Repeat Filter and Smoother outputs, while the Injection Symbols overwrite the Transmit Modes.

During the reset process (i.e. $\overline{RST}$ = GND) the Transmit Mode is set to Off (TM<2:0> = 010), the Smoother is enabled (i.e. SE is set to 1), and the Reserved bit (b7) is set to 1. All other bits of this register are cleared (i.e. set to 0) during the reset process.

ACCESS RULES

ADDRESS	READ	WRITE
04h	Always	Conditional

D7	D6	D5	D4	D3	D2	D1	D0
RES	PRDPE	SE	IC1	IC0	TM2	TM1	TM0

Bit	Symbol	Description
D0, D1, D2	TM0, TM1, TM2	**Transmit Mode <0, 1, 2>:** These bits select one of the 6 transmission modes for the PMD Request Data output port (TXD±).

TM2	TM1	TM0	
0	0	0	**Active Transmit Mode (ATM):** Normal transmission of incoming PHY Request data.
0	0	1	**Idle Transmit Mode (ITM):** Transmission of Idle symbol pairs (11111 11111).
0	1	0	**Off Transmit Mode (OTM):** Transmission of Quiet symbol pairs (00000 00000) and deassertion of the FOTX Enable pin (TXE).
0	1	1	**Reserved:** Reserved for future use. Users are discouraged from using this transmit mode. If selected, however, the transmitter will generate Quiet symbol pairs (00000 00000).
1	0	0	**Master Transmit Mode (MTM):** Transmission of Halt and Quiet symbol pairs (00100 00000).
1	0	1	**Halt Transmit Mode (HTM):** Transmission of Halt symbol pairs (00100 00100).
1	1	0	**Quiet Transmit Mode (QTM):** Transmission of Quiet symbol pairs (00000 00000).
1	1	1	**Reserved:** Reserved for future use. Users are discouraged from using this transmit mode. If selected, however, the transmitter will generate Quiet symbol pairs (00000 00000).

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5.0 Registers (Continued)

CURRENT TRANSMIT STATE REGISTER (CTSR) (Continued)

Bit	Symbol	Description
D3, D4	IC0, IC1	**Injection Control <0, 1>:** These bits select one of the 4 injection modes. The injection modes overwrite data from the Smoother, Repeat Filter, Encoder, and Transmit Modes. IC0 is the only bit of the register that is automatically cleared by the PLAYER device after the One Shot Injection is executed. The automatic clear of IC0 during the One Shot mode can be interpreted as an acknowledgment that the One Shot has been completed. **IC1** **IC0** 0 0 **No Injection:** The normal transmission of incoming PHY Request data (i.e. symbols are not injected). 0 1 **One Shot:** In one shot mode, Injection Symbol Register A (ISRA) and Injection Symbol Register B (ISRB) are injected n symbol pairs after a JK, where n is the programmed value of the Injection Count Register (IJCR). If IJCR is set to 0, the JK symbol pair is replaced by ISRA and ISRB. Once the One Shot is executed, the PLAYER device automatically sets IC0 to 0, thereby returning to normal transmission of data. 1 0 **Periodic:** In Periodic mode, Injection Symbol Register A (ISRA) and Injection Symbol Register B (ISRB) are injected every (n + 1)th symbol pair, where n is the programmed value of the Injection Count Register (IJCR). If IJCR is set to 0, all data symbols are replaced with ISRA and ISRB. 1 1 **Continuous:** In Continuous mode, all data symbols are replaced with Injection Symbol Register A (ISRA) and Injection Symbol Register B (ISRB).
D5	SE	**SMOOTHER ENABLE:** 0: Disables the Smoother. 1: Enables the Smoother. When enabled, the Smoother can redistribute Idle symbol pairs which were added or deleted by the local or upstream receivers. **Note:** Once the counter has started, it will continue to count irrespective of the incoming symbols with the exception of a JK symbol pair. This bit should be enabled for interoperable operation.
D6	PRDPE	**PHY_REQUEST DATA PARITY ENABLE:** 0: Disables PHY_Request Data parity. 1: Enables PHY_Request Data parity.
D7	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using this bit. The reserved bit is set to 1 during the reset process. It may be set or cleared without any effects to the functionality of the PLAYER device.

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5.0 Registers (Continued)

INJECTION THRESHOLD REGISTER (IJTR)

The Injection Threshold Register, in conjunction with the Injection Control bits (IC<1:0>) in the Current Transmit State Register (CTSR), set the frequency at which the Injection Symbol Register A (ISRA) and Injection Symbol Register B (ISRB) are inserted into the data stream. It contains the start value for the Injection Counter.

The Injection Threshold Register value is loaded into the Injection Counter when the counter reaches zero or during every Control Bus Interface write-cycle of this register.

The Injection Counter is an 8-bit down-counter which decrements every 80 ns. Its current value is read for CIJCR.

The counter is active only during One Shot or Periodic Injection Modes (i.e. Injection Control<1:0> bits (IC<1:0>) of the Current Transmit State Register (CTSR) are set to either 01 or 10). The Transmitter Block will replace a data symbol pair with ISRA and ISRB when the counter reaches 0 and the Injection Mode is either One Shot or Periodic.

If the Injection Threshold Register is set to 0 during the One Shot mode, the JK will be replaced with ISRA and ISRB. If the Injection Threshold Register is set to 0 during the Periodic mode, all data symbols are replaced with ISRA and ISRB.

The counter is initialized to 0 during the reset process (i.e. $\overline{RST}$ = GND).

For further information, see the Injection Control Logic subsection within Section 3.2.

ACCESS RULES

ADDRESS	READ	WRITE
05h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
IJT7	IJT6	IJT5	IJT4	IJT3	IJT2	IJT1	IJT0

Bit	Symbol	Description
D0	IJT0	**INJECTION THRESHOLD BIT <0>:** Least significant bit (LSB) of the start value for the Injection Counter.
D1–6	IJT1–6	**INJECTION THRESHOLD BIT <1–6>:** Intermediate bits of start value for the Injection Counter.
D7	IJT7	**INJECTION THRESHOLD BIT <7>:** Most significant bit (MSB) of the start value for the Injection Counter.

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5.0 Registers (Continued)

INJECTION SYMBOL REGISTER A (ISRA)

The Injection Symbol Register A, along with Injection Symbol Register B, contains the programmable value (already in 5B code) that will replace the data symbol pairs.

The One Shot mode, ISRA and ISRB are injected n bytes after the next JK, where n is the programmed value of the Injection Threshold Register. In the Periodic mode, ISRA and ISRB are injected every nth symbol pair. In the Continuous mode, all data symbols are replaced with ISRA and ISRB.

ACCESS RULES

ADDRESS	READ	WRITE
06h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	IJS4	IJS3	IJS2	IJS1	IJS0

Bit	Symbol	Description
D0	IJS0	**INJECTION THRESHOLD BIT <0>:** Least significant bit (LSB) of Injection Symbol Register A.
D1–3	IJS1–3	**INJECTION THRESHOLD BIT <1–3>:** Intermediate bits of Injection Symbol Register A.
D4	IJS4	**INJECTION THRESHOLD BIT <4>:** Most significant bit (MSB) of Injection Symbol Register A.
D5	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using this bit. The reserved bit is set to 1 during the reset process. It may be set or cleared without any effects to the functionality of the PLAYER device.
D6	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using this bit. The reserved bit is set to 1 during the reset process. It may be set or cleared without any effects to the functionality of the PLAYER device.
D7	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using this bit. The reserved bit is set to 1 during the reset process. It may be set or cleared without any effects to the functionality of the PLAYER device.

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5.0 Registers (Continued)

INJECTION SYMBOL REGISTER B (ISRB)

The Injection Symbol Register B, along with Injection Symbol Register A, contains the programmable value (already in 5B code) that will replace the data symbol pairs.

The One Shot mode, ISRA and ISRB are injected n bytes after the next JK, where n is the programmed value of the Injection Threshold Register. In the Periodic mode, ISRA and ISRB are injected every nth symbol pair. In the Continuous mode, all data symbols are replaced with ISRA and ISRB.

ACCESS RULES

ADDRESS	READ	WRITE
07h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	IJS9	IJS8	IJS7	IJS6	IJS5

Bit	Symbol	Description
D0	IJS5	**INJECTION THRESHOLD BIT<5>:** Least significant bit (LSB) of Injection Symbol Register B.
D1–3	IJS6–8	**INJECTION THRESHOLD BIT <6–8>:** Intermediate bits of Injection Symbol Register B.
D4	IJS9	**INJECTION THRESHOLD BIT<9>:** Most significant bit (MSB) of Injection Symbol Register B.
D5	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using this bit. The reserved bit is set to 1 during the reset process. It may be set or cleared without any effects to the functionality of the PLAYER device.
D6	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using this bit. The reserved bit is set to 1 during the reset process. It may be set or cleared without any effects to the functionality of the PLAYER device.
D7	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using this bit. The reserved bit is set to 1 during the reset process. It may be set or cleared without any effects to the functionality of the PLAYER device.

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5.0 Registers (Continued)

CURRENT RECEIVE STATE REGISTER (CRSR)

The Current Receive State Register represents the current line state being detected by the Receiver Block. Once the Receiver Block recognizes a new Line State, the bits corresponding to the previous line state are cleared, and the bits corresponding to the new line state are set.

During the reset process ($\overline{RST}$ = GND), the Receiver Block is forced to Line State Unknown (i.e. the Line State Unknown bit (LSU) is set to 1).

ACCESS RULES

ADDRESS	READ	WRITE
08h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	RES	LSU	LS2	LS1	LS0

Bit	Symbol	Description
D0, D1 D2	LS0, LS1, LS2	**LINE STATE<0, 1, 2>:** These bits represent the current Line State being detected by the Receiver Block. Once the Receiver Block recognizes a new line state, the bits corresponding to the previous line state are cleared, and the bits corresponding to the new line state are set.
		LS2 **LS1** **LS0**
		0 0 0 — **Active Line State (ALS):** Received a JK symbol pair (11000 10001), and possibly followed by data symbols.
		0 0 1 — **Idle Line State (ILS):** Received a minimum of two consecutive Idle symbol pairs (11111 11111).
		0 1 0 — **No Signal Detect (NSD):** The Signal Detect pin (TTLSD) has been deasserted, indicating that the Clock Recovery Device is not receiving data from the Fiber Optic Receiver.
		0 1 1 — **Reserved:** Reserved for future use.
		1 0 0 — **Master Line State (MLS):** Received a minimum of 8 consecutive Halt-Quiet symbol pairs (00100 00000).
		1 0 1 — **Halt Line State (HLS):** Received a minimum of 8 consecutive Halt symbol pairs (00100 00100).
		1 1 0 — **Quiet Line State (QLS):** Received a minimum of 8 consecutive Quiet symbol pairs (00000 00000).
		1 1 1 — **Noise Line State (NLS):** Detected a minimum of 16 noise events. Refer to the Receiver Block for further information on noise events.
D3	LSU	**LINE STATE UNKNOWN:** The Receiver Block has not detected the minimum conditions to enter a known line state. When the Line State Unknown bit is set, LS<2:0> represent the most recently known line state.
D4	RES	**RESERVED:** Reserved for future use. The reserved bit is set to 0. **Note:** Users are discouraged from using this bit. An attempt to write into this bit will cause the PLAYER device to ignore the Control Bus write cycle and set the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) to 1.

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5.0 Registers (Continued)

CURRENT RECEIVE STATE REGISTER (CRSR) (Continued)

Bit	Symbol	Description
D5	RES	**RESERVED:** Reserved for future use. The reserved bit is set to 0. **Note:** Users are discouraged from using this bit. An attempt to write into this bit will cause the PLAYER device to ignore the CBUS write cycle and set the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) to 1.
D6	RES	**RESERVED:** Reserved for future use. The reserved bit is set to 0. **Note:** Users are discouraged from using this bit. An attempt to write into this bit will cause the PLAYER device to ignore the CBUS write cycle and set the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) to 1.
D7	RES	**RESERVED:** Reserved for future use. The reserved bit is set to 0. **Note:** Users are discouraged from using this bit. An attempt to write into this bit will cause the PLAYER device to ignore the CBUS write cycle and set the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) to 1.

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5.0 Registers (Continued)

RECEIVE CONDITION REGISTER A (RCRA)

The Receive Condition Register A maintains a historical record of the Line States recognized by the Receiver Block.

When a new Line State is entered, the bit corresponding to that line state is set to 1. The bits corresponding to the previous Line States are not cleared by the PLAYER device, thereby maintaining a record of the Line States detected.

The Receive Condition A bit (RCA) of the Interrupt Condition Register (ICR) will be set to 1 when one or more bits within the Receive Condition Register A is set to 1 and the corresponding mask bit(s) in Receive Condition Mask Register A (RCMRA) is also set to 1.

ACCESS RULES

ADDRESS	READ	WRITE
09h	Always	Conditional

D7	D6	D5	D4	D3	D2	D1	D0
LSUPI	LSC	NT	NLS	MLS	HLS	QLS	NSD

Bit	Symbol	Description
D0	NSD	**NO SIGNAL DETECT:** Indicates that the Signal Detect pin (TTLSD) has been deasserted and that the Clock Recovery Device is not receiving data from the Fiber Optic Receiver.
D1	QLS	**QUIET LINE STATE:** Received a minimum of eight consecutive Quiet symbol pairs (00000 00000).
D2	HLS	**HALT LINE STATE:** Received a minimum of eight consecutive Halt symbol pairs (00100 00100).
D3	MLS	**MASTER LINE STATE:** Received a minimum of eight consecutive Halt-Quiet symbol pairs (00100 00000).
D4	NLS	**NOISE LINE STATE:** Detected a minimum of sixteen noise events.
D5	NT	**NOISE THRESHOLD:** This bit is set to 1 when the internal Noise Counter reaches 0. It will remain set until a value equal to or greater than one is loaded into the Noise Threshold Register or Noise Prescale Threshold Register. During the reset process (i.e. $\overline{RST}$ = GND), since the Noise Counter is initialized to 0, the Noise Threshold bit will be set to 1.
D6	LSC	**LINE STATE CHANGE:** A line state change has been detected.
D7	LSUPI	**LINE STATE UNKNOWN & PHY INVALID:** The Receiver Block has not detected the minimum conditions to enter a known line state. In addition, the most recently known line state was one of the following line states: No Signal Detect, Quiet Line State, Halt Line State, Master Line State, or Noise Line State.

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5.0 Registers (Continued)

RECEIVE CONDITION REGISTER B (RCRB)

The Receive Condition Register B maintains a historical record of the Line States recognized by the Receiver Block.

When a new Line State is entered, the bit corresponding to that line state is set to 1. The bits corresponding to the previous Line States are not clear by the PLAYER device, thereby maintaining a record of the Line States detected.

The Receive Condition B bit (RCB) of the Interrupt Condition Register (ICR) will be set to 1 when one or more bits within the Receive Condition Register B is set to 1 and the corresponding mask bits in Receive Condition Mask Register B (RCMRB) is also set to 1.

ACCESS RULES

ADDRESS	READ	WRITE
0Ah	Always	Conditional

D7	D6	D5	D4	D3	D2	D1	D0
RES	SILS	EBOU	CSE	LSUPV	ALS	ST	ILS

Bit	Symbol	Description
D0	ILS	**IDLE LINE STATE:** Received a minimum of two consecutive Idle symbol pairs (11111 11111).
D1	ST	**STATE THRESHOLD:** This bit will be set to 1 by the PLAYER device when the internal State Counter reaches zero. It will remain set until a value equal to or greater than one is loaded into the State Threshold Register or State Prescale Threshold Register, and this register is cleared. During the reset process (i.e. $\overline{RST}$ = GND), since the State Counter is initialized to 0, the State Threshold bit is set to 1.
D2	ALS	**ACTIVE LINE STATE:** Received a JK symbol pair (11000 10001), and possibly data symbols following.
D3	LSUPV	**LINE STATE UNKNOWN & PHY VALID:** Receiver Block has not detected the minimum conditions to enter a know line state when the most recently known line state was one of the following line states: Active Line State or Idle Line State
D4	CSE	**CASCADE SYNCHRONIZATION ERROR:** When a synchronization error occurs, the Cascade Synchronization Error bit is set to 1. A synchronization error occurs if the Cascade Start signal (CS) is not asserted within approximately 80 ns of Cascade Ready (CR) release.
D5	EBOU	**ELASTICITY BUFFER UNDERFLOW/OVERFLOW:** The Elasticity Buffer has either overflowed or underflowed. The Elasticity Buffer will automatically recover if the condition which caused the error is only transient.
D6	SILS	**SUPER IDLE LINE STATE:** Received a minimum of eight Idle symbol pairs (11111 11111).
D7	RES	**RESERVED:** Reserved for future use. The reserved bit is set to 0 during the reset process. **Note:** Users are discouraged from using this bit. It may be set or cleared without any effects to the functionality of the PLAYER device.

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5.0 Registers (Continued)

RECEIVE CONDITION MASK REGISTER A (RCMRA)

The Receive Condition Mask Register A allows the user to dynamically select which events will generate an interrupt.

The Receive Condition A bit (RCA) of the Interrupt Condition Register (ICR) will be set to 1 when one or more bits within the Receive Condition Register A (RCRA) is set to 1 and the corresponding mask bit(s) in this register is also set to 1.

Since this register is cleared (i.e. set to 0) during the reset process, all interrupts are initially masked.

ACCESS RULES

ADDRESS	READ	WRITE
0Bh	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
LSUPIM	LSCM	NTM	NLSM	MLSM	HLSM	QLSM	NSDM

Bit	Symbol	Description
D0	NSDM	**NO SIGNAL DETECT MASK:** The mask bit for the No Signal Detect bit (NSD) of the Receive Condition Register A (RCRA).
D1	QLSM	**QUIET LINE STATE MASK:** The mask bit for the Quiet Line State bit (QLS) of the Receive Condition Register A (RCRA).
D2	HLSM	**HALT LINE STATE MASK:** The mask bit for the Halt Line State bit (HLS) of the Receive Condition Register A (RCRA).
D3	MLSM	**MASTER LINE STATE MASK:** The mask bit for the Master Line State bit (MLS) of the Receive Condition Register A (RCRA).
D4	NLSM	**NOISE LINE STATE MASK:** The mask bit for the Noise Line State bit (NLS) of the Receive Condition Register A (RCRA)
D5	NTM	**NOISE THRESHOLD MASK:** The mask bit for the Noise Threshold bit (NT) of the Receive Condition Register A (RCRA).
D6	LSCM	**LINE STATE CHANGE MASK:** The mask bit for the Line State Change bit (LSC) of the Receive Condition Register A (RCRA).
D7	LSUPIM	**LINE STATE UNKNOWN & PHY INVALID MASK:** The mask bit for the line State Unknown & PHY Invalid bit (LSUPI) of the Receive Condition Register A (RCRA).

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5.0 Registers (Continued)

RECEIVE CONDITION MASK REGISTER B (RCMRB)

The Receive Condition Mask Register B allows the user to dynamically select which events will generate an interrupt.

The Receiver Condition B bit (RCB) of the Interrupt Condition Register (ICR) will be set to 1 when one or more bits within the Receive Condition B (RCRA) is set to 1 and the corresponding mask bits in this register is also set to 1.

Since this register is cleared (i.e. set to 0) during the reset process, all interrupts are initially masked.

ACCESS RULES

ADDRESS	READ	WRITE
0Ch	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RES	SILSM	EBOUM	CSEM	LSUPVM	ALSM	STM	ILSM

Bit	Symbol	Description
D0	ILSM	**IDLE LINE STATE MASK:** The mask bit for the Idle Line State bit (ILS) of the Receive Condition Register B (RCRB).
D1	STM	**STATE THRESHOLD MASK:** The mask bit of the State Threshold bit (ST) of the Receive Condition Register B (RCRB).
D2	ALSM	**ACTIVE LINE STATE MASK:** The mask bit for the Active Line State bit (ALS) of the Receive Condition Register B (RCRB).
D3	LSUPVM	**LINE STATE UNKNOWN & PHY VALID MASK:** The mask bit for the Line State Unknown & PHY Valid bit (LSUPV) of the Receive Condition Register B (RCRB).
D4	CSEM	**CASCADE SYNCHRONIZATION ERROR MASK:** The mask bit for the Cascade Synchronization Error bit (CSE) of the Receive Condition Register B (RCRB).
D5	EBOUM	**ELASTICITY BUFFER OVERFLOW/UNDERFLOW MASK:** The mask bit for the Elasticity Buffer Overflow/Underflow bit (EBOU) of the Receive Condition Register B (RCRB).
D6	SILSM	**SUPER IDLE LINE STATE MASK:** The mask bit for the Super Idle Line State bit (SILS) of the Receive Condition Register B (RCRB).
D7	RESM	**RESERVED MASK:** The mask bit for the Reserved bit (RES) of the Receive Condition Register B (RCRB).

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5.0 Registers (Continued)

NOISE THRESHOLD REGISTER (NTR)

The Noise Threshold Register contains the start value for the Noise Counter. This counter may be used in conjunction with the Noise Prescale Counter for counting the Noise events. Definiton of Noise event is explained in detail in Section 8.2. The Noise Counter decrements once every 80 ns if the noise Prescale counter is zero and there is a noise event. As a result, the internal noise counter takes

$$((NPTR + 1) \times (NTR + 1)) \times 80\ ns$$

to reach zero in the event of continuous Noise event.

The threshold values for the Noise Counter and Noise Prescale Counter are simultaneously loaded into both counters if one of the following conditions is true:

(1) Both the Noise Counter and Noise Prescale Counter reach zero and the current Line State is either Noise Line State, Active Line State, or Line State Unknown.

or

(2) The current Line State is either Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect

or

(3) The Noise Threshold Register or Noise Prescale Threshold Register goes through a Control Bus Interface write cycle.

In addition, the value of the Noise Prescale Threshold register is loaded into the Noise Prescale Counter if the Noise Prescale Counter reaches zero.

The Noise Counter and Noise Prescale Counter will continue to count, without resetting or reloading the threshold values, if a Line State change occurs and the new line state is either Noise Line State, Active Line State or Line State Unknown.

When both the Noise Threshold Counter and Noise Counter both reach zero, the Noise Threshold bit of the Receive Condition Register A will be set.

ACCESS RULES

ADDRESS	READ	WRITE
0Dh	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
NT7	NT6	NT5	NT4	NT3	NT2	NT1	NT0

Bit	Symbol	Description
D0	NT0	**NOISE THRESHOLD BIT <0>:** Least significant bit (LSB) of the start value for the Noise Counter.
D1–5	NT1–5	**NOISE THRESHOLD BIT <1–5>:** Intermediate bits of start value for the Noise Counter.
D6	NT6	**NOISE THRESHOLD BIT <6>:** Most significant bit (MSB) of the start value for the Noise Counter.
D7	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using this bit. Write data is ignored since the reserved bit is permanently set to 0.

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5.0 Registers (Continued)

NOISE PRESCALE THRESHOLD REGISTER (NPTR)

The Noise Prescale Threshold Register contains the start value for the Noise Prescale Counter. The Noise Prescale Counter is a count-down counter and it is used in conjunction with the Noise Counter for counting the Noise events. The Noise Prescale Counter decrements once every 80 ns while there is a noise event. When the Noise Prescale Counter reaches zero, it reloads the count with the content of the Noise Prescale Threshold Register and also causes the Noise Counter to decrement.

The threshold values for the Noise Counter and Noise Prescale Counter are simultaneously loaded into both counters if one of the following conditions is true:

(1) Both the Noise Counter and Noise Prescale Counter reach zero and the current Line State is either Noise Line State, Active Line State, or Line State Unknown.

or

(2) The current Line State is either Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect

or

(3) The Noise Threshold Register or Noise Prescale Threshold Register goes through a Control Bus Interface write cycle.

In addition, the value of the Noise Prescale Threshold register is loaded into the Noise Prescale Counter if the Noise Prescale Counter reaches zero.

The Noise Counter and Noise Prescale Counter will continue to count, without resetting or reloading the threshold values, if a Line State change occurs and the new line state is either Noise Line State, Active Line State, or Line State Unknown.

When both the Noise Threshold Counter and Noise Counter both reach zero, the Noise Threshold bit of the Receive Condition Register A will be set.

ACCESS RULES

ADDRESS	READ	WRITE
0Eh	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
NPT7	NPT6	NPT5	NPT4	NPT3	NPT2	NPT1	NPT0

Bit	Symbol	Description
D0	NPT0	**NOISE PRESCALE THRESHOLD BIT** <0>: Least significant bit (LSB) of the start value of the Noise Prescale Counter.
D1–6	NPT1–6	**NOISE PRESCALE THRESHOLD BIT**<1–6>: Intermediate bits of start value for the Noise Prescale Counter.
D7	NPT7	**NOISE PRESCALE THRESHOLD BIT** <7>: Most significant bit (MSB) of the start value for the Noise Prescale Counter.

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5.0 Registers (Continued)

CURRENT NOISE COUNT REGISTER (CNCR)

The Current Noise Count Register takes a snap-shot of the Noise Counter during every Control Bus Interface read-cycle of this register.

During a Control Bus Interface write-cycle to the Current Noise Count Register, the PLAYER device will set the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) to 1 and will ignore a write-cycle.

ACCESS RULES

ADDRESS	READ	WRITE
0Fh	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
NCLSCD	CNC6	CNC5	CNC4	CNC3	CNC2	CNC1	CNC0

Bit	Symbol	Description
D0–6	CNC0–6	**CURRENT NOISE COUNT BIT <0–6>**
D7	NCLSCD	**NOISE COUNTER LINE STATE CHANGE DETECTION**

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5.0 Registers (Continued)

CURRENT NOISE PRESCALE COUNT REGISTER (CNPCR)

The Current Noise Prescale Count Register takes a snap-shot of the Noise Prescale Counter during every Control Bus Interface read-cycle of this register.

During a Control Bus Interface write-cycle to the Current Noise Prescale Count Register, the PLAYER device will set the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) to 1 and will ignore a write-cycle.

ACCESS RULES

ADDRESS	READ	WRITE
10h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
CNPC7	CNPC6	CNPC5	CNPC4	CNPC3	CNPC2	CNPC1	CNPC0

Bit	Symbol	Description
D0–7	CNPC0–7	**CURRENT NOISE PRESCALE COUNT BY <0–7>**

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5.0 Registers (Continued)

STATE THRESHOLD REGISTER (STR)

The State Threshold Register contains the start value of the State Counter. This counter is used in conjunction with the State Prescale Counter to count the Line State duration. The State Counter will decrement every 80 ns if the State Prescale Counter is zero and the current Line State is Halt Line, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect. State The State Counter takes

$$((SPTR + 1) \times (STR + 1)) \times 80\ ns$$

to reach zero during a continuous line state condition.

The threshold values for the State Counter and State Prescale Counter are simultaneously loaded into both counters if one of the following conditions is true:

(1) Both the State Counter and State Prescale Counter reach zero and the current Line State is Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect

or

(2) A line state change occurs and the new Line State is Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect

or

(3) The State Threshold Register or State Prescale Threshold Register goes through a Control Bus Interface write cycle.

In addition, the value of the State Prescale Threshold register is loaded into the State Prescale Counter if the State Prescale Counter reaches zero.

The State Counter and State Prescale Counter will reset by reloading the threshold values, if a Line State change occurs and the new Line State is Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect.

ACCESS RULES

ADDRESS	READ	WRITE
11h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0

Bit	Symbol	Description
D0	ST0	**STATE THRESHOLD BIT <0>:** Least significant bit (LSB) of the start value for the State Counter.
D1–5	ST1–5	**STATE THRESHOLD BIT <1–5>:** Intermediate bits of start value for the State Counter.
D6	ST6	**STATE THRESHOLD BIT <6>:** Most significant bit (MSB) of the start value for the State Counter.
D7	RES	**RESERVED:** Reserved for future use. **Note:** Users are discouraged from using this bit. Write data is ignored since the reserved bit is permanently set to 0.

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5.0 Registers (Continued)

STATE PRESCALE THRESHOLD REGISTER (SPTR)

The State Prescale Threshold Register contains the start value for the State Prescale Counter. The State Prescale Counter is a down counter. The Register is used in conjunction with the State Counter to count the Line State duration.

The State Prescale Counter will decrement every 80 ns if the current Line State is Halt Line, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect. As a result, the State Prescale Counter takes SPTR x 80 ns to reach zero during a continuous line state condition. When the State Prescale Counter reaches zero, the State Prescale Threshold Register will be reloaded into the State Prescale Counter.

The threshold values for the State Counter and State Prescale Counter are simultaneously loaded into both counters if one of the following conditions is true:

(1) Both the State Counter and State Prescale Counter reach zero and the current Line State is Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect.

or

(2) A Line State change occurs and the new Line State is Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect

or

(3) The State Threshold Register or State Prescale Threshold Register goes through a Control Bus Interface write cycle.

The State Counter and State Prescale Counter will reset by reloading the threshold values, if a Line State change occurs and the new Line State is Halt Line State, Idle Line State, Master Line State, Quiet Line State, or No Signal Detect.

ACCESS RULES

ADDRESS	READ	WRITE
12h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
SPT7	SPT6	SPT5	SPT4	SPT3	SPT2	SPT1	SPT0

Bit	Symbol	Description
D0	SPT0	**STATE PRESCALE THRESHOLD BIT <0>:** Least significant bit (LSB) of the start value for the State Prescale Counter.
D1–6	SPT1–6	**STATE PRESCALE THRESHOLD BIT <1–6>:** Intermediate bits of start value for the State Prescale Counter.
D7	SPT7	**STATE PRESCALE THRESHOLD BIT <7>:** Most significant bit (MSB) of the start value for the State Prescale Counter.

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5.0 Registers (Continued)

CURRENT STATE COUNT REGISTER (CSCR)

The Current State Count Register takes a snap-shot of the State Counter during every Control Bus Interface read-cycle of this register.

During a Control Bus Interface write-cycle to the Current State Count Register, the PLAYER device will set the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) to 1 and will ignore a write-cycle.

ACCESS RULES

ADDRESS	READ	WRITE
13h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
SCLSCD	CSC6	CSC5	CSC4	CSC3	CSC2	CSC1	CSC0

Bit	Symbol	Description
D0–6	CSC0–6	**CURRENT STATE COUNT BIT <0–6>**
D7	SCLSCD	**STATE COUNTER LINE STATE CHANGE DETECTION**

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5.0 Registers (Continued)

CURRENT STATE PRESCALE COUNT REGISTER (CSPCR)

The Current State Prescale Count Register takes a snap-shot of the State Prescale Counter during every Control Bus interface read-cycle of this register.

During a Control Bus Interface write-cycle to the Current State Prescale Count Register, the PLAYER device will set the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) to 1 and will ignore a write-cycle.

ACCESS RULES

ADDRESS	READ	WRITE
14h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
CSPC7	CSPC6	CSPC5	CSPC4	CSPC3	CSPC2	CSPC1	CSPC0

Bit	Symbol	Description
D0–7	CSPC0–7	**CURRENT STATE PRESCALE COUNT <0–7>**

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5.0 Registers (Continued)

LINK ERROR THRESHOLD REGISTER (LETR)

The Link Error Threshold Register contains the start value for the Link Error Monitor Counter, which is an 8-bit down-counter that decrements if link errors are detected.

When the Counter reaches 0, the Link Error Monitor Threshold Register value is loaded into the Link Error Monitor Counter and the Link Error Monitor Threshold bit (LEMT) of the Interrupt Condition Register (ICR) is set to 1.

The Link Error Monitor Threshold Register value is also loaded into the Link Error Monitor Counter during every Control Bus Interface write-cycle of LETR.

The Counter is initialized to 0 during the reset process (i.e. $\overline{RST}$ = GND).

ACCESS RULES

ADDRESS	READ	WRITE
15h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
LET7	LET6	LET5	LET4	LET3	LET2	LET1	LET0

Bit	Symbol	Description
D0	LET0	**LINK ERROR THRESHOLD BIT** <0>: Least significant bit of the start value for the Link Error Monitor Counter.
D1–6	LET1–6	**LINK ERROR THRESHOLD BIT** <1–6>: Intermediate bits of start value for the Link Error Monitor Counter.
D7	LET7	**LINK ERROR THRESHOLD BIT** <7>: Most significant bit of the start value for the Link Error Monitor Counter.

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5.0 Registers (Continued)

CURRENT LINK ERROR COUNT REGISTER (CLECR)

The Current Link Error Count Register takes a snap-shot of the Link Error Monitor Counter during every Control Bus Interface read-cycle of this register.

During a Control Bus Interface write-cycle, the PLAYER device will set the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) to 1 and will ignore a write-cycle.

ACCESS RULES

ADDRESS	READ	WRITE
16h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
LEC7	LEC6	LEC5	LEC4	LEC3	LEC2	LEC1	LEC0

Bit	Symbol	Description
D0–7	LEC0–7	LINK ERROR COUNT BIT <0–7>

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5.0 Registers (Continued)

USER DEFINABLE REGISTER (UDR)

The User Definable Register is used to monitor and control events which are external to the PLAYER device.

The value of the Sense Bits reflects the asserted/deasserted state of their corresponding Sense pins. On the other hand, the Enable bits assert/deassert the Enable pins.

ACCESS RULES

ADDRESS	READ	WRITE
17h	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RES	RES	RES	RES	EB1	EB0	SB1	SB0

Bit	Symbol	Description
D0	SB0	**SENSE BIT 0:** This bit is set to 1 if the Sense Pin 0 (SP0) is asserted (i.e. SP0 = V_{CC}) for a minimum of 160 ns. Once the asserted signal is latched, Sense Bit 0 can only be cleared through the Control Bus Interface, even if the signal is deasserted. This ensures that the Control Bus Interface will record the source of events which can cause interrupts in a traceable manner.
D1	SB1	**SENSE BIT 1:** This bit is set to 1 if the Sense Pin 1 (SP1) is asserted (i.e. SP1 = V_{CC}) for a minimum of 160 ns. Once the asserted signal is latched, Sense Bit 1 can only be cleared through the Control Bus Interface, even if the signal is deasserted. This ensures that the Control Bus Interface will record the source of events which can cause interrupts in a traceable manner.
D2	EB0	**ENABLE BIT 0:** The Enable Bit 0 allows control of external logic through the Control Bus Interface. The User Definable Enable Pin 0 (EP0) is asserted/deasserted by this bit. 0: EP0 is deasserted (i.e. EP0 = GND). 1: EP0 is asserted (i.e. EP0 = V_{CC}).
D3	EB1	**ENABLE BIT 1:** This bit allows control of external logic through the Control Bus Interface. The User Definable Enable Pin 0 (EP0) is asserted/deasserted by this bit. 0: EP1 is deasserted (i.e. EP1 = GND). 1: EP1 is asserted (i.e. EP1 = V_{CC}).
D4–7	RES	**RESERVED:** Reserved for future use. The reserved bit is set to 0 during the initialization process (i.e. $\overline{RST}$ = GND). **Note:** Users are discouraged from using this bit. It may be set or cleared without any effects to the functionality of the PLAYER device.

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5.0 Registers (Continued)

DEVICE ID REGISTER (IDR)

The Device ID Register contains the binary equivalent of the revision number for this device. It can be used to ensure proper software and hardware versions are matched.

During the Control Bus Interface write-cycle, the PLAYER device will set the Control Bus Write Command Register bit (CCR) of the Interrupt Condition Register (ICR) to 1, and will ignore write-cycle.

ACCESS RULES

ADDRESS	READ	WRITE
18h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0

Bit	Symbol	Description
D0	DID0	**DEVICE ID BIT <0>:** Least significant bit (LSB) of the revision number.
D1–6	DID1–6	**DEVICE ID BIT <1-0-6>:** Intermediate bits of the revision number.
D7	DID7	**DEVICE ID BIT <7>:** Most significant bit (MSB) of the revision number.

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5.0 Registers (Continued)

CURRENT INJECTION COUNT REGISTER (CIJCR)

The Current Injection Count Register takes a snap-shot of the Injection Counter during every Control Bus Interface read-cycle of this register.

During a Control Bus Interface write-cycle, the PLAYER device will set the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR) to 1 and will ignore a write-cycle.

The Injection Counter is an 8-bit down-counter which decrements every 80 ns.

The counter is active only during One Shot or Periodic Injection Modes (i.e. Injection Control <1:0> bits (IC<1:0>) of the Current Transmit State Register (CTSR) are set to either 01 or 10).

The Injection Threshold Register (IJTR) value is loaded into the Injection Counter when the counter reaches zero and during every Control Bus Interface write-cycle of IJTR.

The counter is initialized to 0 during the reset process (i.e. $\overline{RST}$ = GND).

ACCESS RULES

ADDRESS	READ	WRITE
19h	Always	Write Reject

D7	D6	D5	D4	D3	D2	D1	D0
IJC7	IJC6	IJC5	IJC4	IJC3	IJC2	IJC1	IJC0

Bit	Symbol	Description
D0	IJC0	**INJECTION COUNT BIT <0>:** Least significant bit (LSB) of the current value of the Injection Counter.
D1–6	IJC1–6	**INJECTION COUNT BIT <1–6>:** Intermediate bits representing the current value of the Injection Counter.
D7	IJC7	**INJECTION COUNT BIT <7>:** Most significant bit (MSB) of the current value of the Injection Counter.

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5.0 Registers (Continued)

INTERRUPT CONDITION COMPARISON REGISTER (ICCR)

The Interrupt Condition Comparison Register ensures that the Control Bus must first read a bit modified by the PLAYER device before it can be written to by the Control Bus Interface.

The current state of the Interrupt Condition Register (ICR) is automatically written into the Interrupt Condition Comparison Register (i.e. ICCR = ICR) during a Control Bus Interface read-cycle of ICR.

During a Control Bus Interface write-cycle, the PLAYER device will set the Conditional Write Inhibit bit (CWI) of the Interrupt Condition Register (ICR) to 1 and disallow the setting or clearing of a bit within ICR when the value of a bit in ICR differs from the value of the corresponding bit in the Interrupt Condition Comparison Register.

ACCESS RULES

ADDRESS	READ	WRITE
1Ah	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
UDIC	RCBC	RCAC	LEMTC	CWIC	CCRC	CPEC	DPEC

Bit	Symbol	Description
D0	DPEC	**PHY_REQUEST DATA PARITY ERROR COMPARISON:** The comparison bit for the PHY_Request Data Parity Error bit (DPE) of the Interrupt Condition Register (ICR).
D1	CPEC	**CONTROL BUS DATA PARITY ERROR COMPARISON:** The comparison bit for the Control Bus Data Parity Error bit (CPE) of the Interrupt Condition Register (ICR).
D2	CCRC	**CONTROL BUS WRITE COMMAND REJECT COMPARISON:** The comparison bit for the Control Bus Write Command Reject bit (CCR) of the Interrupt Condition Register (ICR).
D3	CWIC	**CONDITIONAL WRITE INHIBIT COMPARISON:** The comparison bit for the Conditional Write Inhibit bit (CWI) of the Interrupt Condition Register (ICR).
D4	LEMTC	**LINK ERROR MONITOR THRESHOLD COMPARISON:** The comparison bit for the Link Error Monitor Threshold bit (LEMT) of the Interrupt Condition Register (ICR).
D5	RCAC	**RECEIVE CONDITION A COMPARISON:** The comparison bit for the Receive Condition A bit (RCA) of the Interrupt Condition Register (ICR).
D6	RCBC	**RECEIVE CONDITION B COMPARISON.:** The comparison bit for the Receive Condition B bit (RCB) of the Interrupt Condition Register (ICR).
D7	UDIC	**USER DEFINABLE INTERRUPT COMPARISON:** The comparison bit for the User Definable Interrupt bit (UDIC) of the Interrupt Condition Register (ICR).

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5.0 Registers (Continued)

CURRENT TRANSMIT STATE COMPARISON REGISTER (CTSCR)

The Current Transmit State Comparison Register ensures that the Control Bus must first read a bit modified by the PLAYER device before it can be written to by the Control Bus Interface.

The current state of the Current Transmit State Register (CTSR) is automatically written into the Current Transmit State Comparison Register A (i.e. CTSCR = CTSR) during a Control Bus Interface read-cycle of CTSR.

During a Control Bus Interface write-cycle, the PLAYER device will set the Conditional Write Inhibit bit (CWI) of the Interrupt Condition Register (ICR) to 1 and disallow the setting or clearing of a bit within the CTSR when the value of a bit in the CTSR differs from the value of the corresponding bit in the Current Transmit State Comparison Register.

ACCESS RULES

ADDRESS	READ	WRITE
1Bh	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RESC	PRDPEC	SEC	IC1C	IC0C	TM2C	TM1C	TM0C

Bit	Symbol	Description
D0	TM0C	**TRANSMIT MODE <0> COMPARISON:** The comparison bit for the Transmit Mode <0> (TM0) of the Current Transmit State Register (CTSR).
D1	TM1C	**TRANSMIT MODE <1> COMPARISON:** The comparison bit for the Transmit Mode <1> bit (TM1) of the Current Transmit State Register (CTSR).
D2	TM2C	**TRANSMIT MODE <2> COMPARISON:** The comparison bit for the Transmit Mode <2> bit (TM2) of the Current Transmit State Register (CTSR).
D3	IC0C	**INJECTION CONTROL <0> COMPARISON:** The comparison bit for the Injection Control <0> bit (IC0) of the Current Transmit State Register (CTSR).
D4	IC1C	**INJECTION CONTROL <1> COMPARISON:** The comparison bit for the Injection Control <1> bit (IC1) of the Current Transmit Register (CTSR).
D5	SEC	**SMOOTHER ENABLE COMPARISON:** The comparison bit for the Smoother Enable bit (SE) to the Current Transmit State Register (CTSR).
D6	PRDPEC	**PHY_REQUEST DATA PARITY ENABLE COMPARISON:** The comparison bit for the PHY_Request Data Parity Enable bit (PRDPE) of the Current Transmit State Register (CTSR).
D7	RESC	**RESERVED COMPARISON:** The comparison bit for the Reserved bit (RES) of the Current Transmit State Register (CTSR).

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5.0 Registers (Continued)

RECEIVE CONDITION COMPARISON REGISTER A (RCCRA)

The Receive Condition Comparison Register A ensures that the Control Bus must first read a bit modified by the PLAYER device before it can be written to by the Control Bus Interface.

The current state of RCRA is automatically written into the Receive Condition Comparison Register A (i.e. RCCRA = RCRA) during a Control Bus Interface read-cycle of RCRA.

During a Control Bus Interface write-cycle, the PLAYER device will set the Conditional Write Inhibit bit (CWI) of the Interrupt Condition Register (ICR) to 1 and prevent the setting or clearing of a bit within RCRA when the value of a bit in RCRA differs from the value of the corresponding bit in the Receive Condition Comparison Register A.

ACCESS RULES

ADDRESS	READ	WRITE
1Ch	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
LSUPIC	LSCC	NTC	NLSC	MLSC	HLSC	QLSC	NSDC

Bit	Symbol	Description
D0	NSDC	**NO SIGNAL DETECT COMPARISON:** The comparison bit for the No Signal Detect bit (NSD) of the Receive Condition Register A (RCRA).
D1	QLSC	**QUIET LINE STATE COMPARISON:** The comparison bit for the Quiet Line State bit (QLS) of the Receive Condition Register A (RCRA).
D2	HLSC	**HALT LINE STATE COMPARISON:** The comparison bit for the Halt Line State bit (HLS) of the Receive Condition Register A (RCRA).
D3	MLSC	**MASTER LINE STATE COMPARISON:** The comparison bit for the Master Line State bit (MLS) of the Receive Condition Register A (RCRA).
D4	NLSC	**NOISE LINE STATE COMPARISON:** The comparison bit for the Noise Line State bit (NLS) of the Receive Condition Register A (RCRA).
D5	NTC	**NOISE THRESHOLD COMPARISON:** The comparison bit for the Noise Threshold bit (NT) of the Receive Condition Register A (RCRA).
D6	LSCC	**LINE STATE CHANGE COMPARISON:** The comparison bit for the Line State Change bit (LSC) of the Receive Condition Register A (RCRA).
D7	LSUPIC	**LINE STATE UNKNOWN & PHY INVALID COMPARISON:** The comparison bit for the Line State Unknown & PHY Invalid bit (LSUPI) of the Receive Condition Register A (RCRA).

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5.0 Registers (Continued)

RECEIVE CONDITION COMPARISON REGISTER B (RCCRB)

The Receive Condition Comparison Register B ensures that the Control Bus must first read a bit modified by the PLAYER device before it can be written to by the Control Bus Interface.

The current state of RCRB is automatically written into the Receive Condition Comparison Register B (i.e. RCCRB = RCRB) during a Control Bus Interface read-cycle RCRB.

During a Control Bus Interface write-cycle, the PLAYER device will set the Conditional Write Inhibit bit (CWI) of the Interrupt Condition Register (ICR) to 1 and prevent the setting or clearing of a bit within RCRB when the value of a bit in RCRB differs from the value of the corresponding bit in the Receive Condition Comparison Register B.

ACCESS RULES

ADDRESS	READ	WRITE
1Dh	Always	Always

D7	D6	D5	D4	D3	D2	D1	D0
RESC	SILSC	EBOUC	CSEC	LSUPVC	ALSC	STC	ILSC

Bit	Symbol	Description
D0	ILSC	**IDLE LINE STATE COMPARISON:** The comparison bit for the Idle State bit (ILS) of the Receive Condition Register B (RCRB).
D1	STC	**STATE THRESHOLD COMPARISON:** The comparison bit for the State Threshold bit (ST) of the Receive Condition Register B (RCRB).
D2	ALSC	**ACTIVE LINE STATE COMPARISON:** The comparison bit for the Active Line State bit (ALS) of the Receive Condition Register B (RCRB).
D3	LSUPVC	**LINE STATE UNKNOWN & PHY VALID COMPARISON:** The comparison bit for the Line State Unknown & PHY Valid bit (LSUPV) of the Receive Condition Register B (RCRB).
D4	CSEC	**CASCADE SYNCHRONIZATION ERROR COMPARISON:** The comparison bit for the Cascade Synchronization Error bit (CSE) of the Receive Condition Register B (RCRB).
D5	EBOUC	**ELASTICITY BUFFER OVERFLOW/UNDERFLOW COMPARISON:** The comparison bit for the Elasticity Buffer Overflow/Underflow bit (EBOU) of the Receive Condition Register B (RCRB).
D6	SILSC	**SUPER IDLE LINE STATE COMPARISON:** The comparison bit for the Super Idle Line State bit (SILS) of the Receive Condition Register B (RCRB).
D7	RESC	**RESERVED COMPARISON:** The comparison bit for the Reserved bit (RES) of the Receive Condition Register B (RCRB).

RESERVED REGISTER 0 (RR0) ADDRESS 1Eh—DO NOT USE

RESERVED REGISTER 1 (RR1) ADDRESS 1Fh—DO NOT USE

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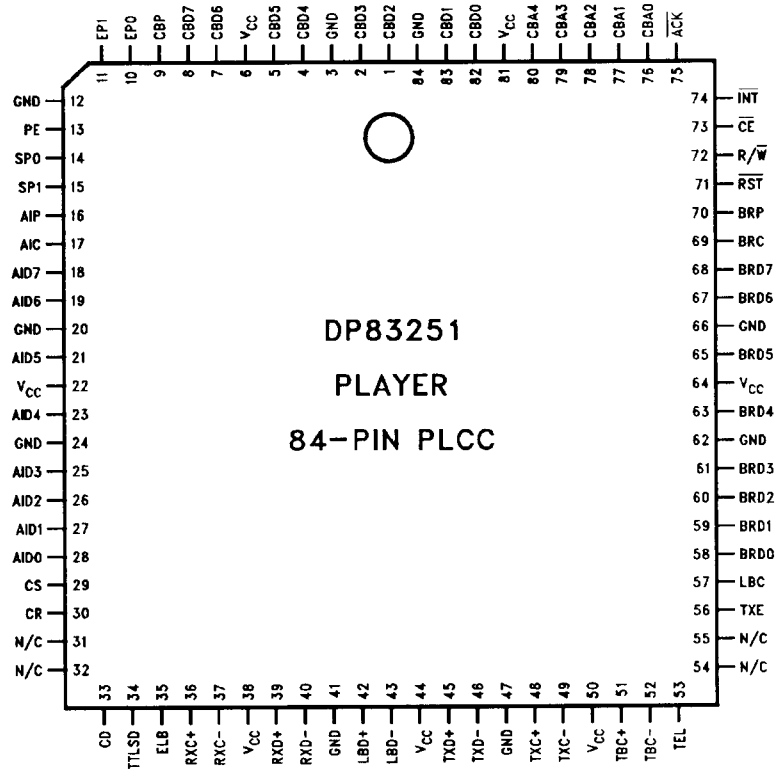
6.0 Pin Descriptions

6.1 DP83251

The pin descriptions for the DP83251 are divided into 5 functional interfaces: Serial Interface, PHY Port Interface, Control Bus Interface, Clock Interface, and Miscellaneous Interface.

For a Pinout Summary List, refer to Table 6-1.



TL/F/10366-20

Order Number DP83251V
See NS Package Number V84A

FIGURE 6-1. DP83251 84-Pin PLCC Pinout

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6.0 Pin Descriptions (Continued)

TABLE 6-1. DP83251 Pinout Summary

Pin No.	Signal Name	Symbol	I/O	ECL/TTL/Open Drain/Power
1	Control Bus Data<2>	CBD2	I/O	TTL
2	Control Bus Data<3>	CBD3	I/O	TTL
3	CMOS I/O Ground	GND		+0V
4	Control Bus Data<4>	CBD4	I/O	TTL
5	Control Bus Data<5>	CBD5	I/O	TTL
6	CMOS I/O Power	V_{CC}		+5V
7	Control Bus Data<6>	CBD6	I/O	TTL
8	Control Bus Data<7>	CBD7	I/O	TTL
9	Control Bus Data Parity	CBP	I/O	TTL
10	Enable Pin 0	EP0	O	TTL
11	Enable Pin 1	EP1	O	TTL
12	CMOS Logic Ground	GND		+0V
13	Control Bus Data Parity Enable	CBPE	I	TTL
14	Sense Pin 0	SP0	I	TTL
15	Sense Pin 1	SP1	I	TTL
16	PHY Port A Indicate Parity	AIP	O	TTL
17	PHY Port A Indicate Control	AIC	O	TTL
18	PHY Port A Indicate Data<7>	AID7	O	TTL
19	PHY Port A Indicate Data<6>	AID6	O	TTL
20	CMOS I/O Ground	GND		+0V
21	PHY Port A Indicate Data<5>	AID5	O	TTL
22	CMOS I/O Power	V_{CC}		+5V
23	PHY Port A Indicate Data<4>	AID4	O	TTL
24	CMOS Logic Ground	GND		+0V
25	PHY Port A Indicate Data<3>	AID3	O	TTL
26	PHY Port A Indicate Data<2>	AID2	O	TTL
27	PHY Port A Indicate Data<1>	AID1	O	TTL
28	PHY Port A Indicate Data<0>	AID0	O	TTL
29	Cascade Start	CS	O	TTL
30	Cascade Ready	CR	I	Open Drain
31	No Connect	N/C		
32	No Connect	N/C		
33	Clock Detect	CD	I	TTL
34	Signal Detect	TTLSD	I	TTL
35	External Loopback Enable	ELB	O	TTL

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6.0 Pin Descriptions (Continued)

TABLE 6-1. DP83251 Pinout Summary (Continued)

Pin No.	Signal Name	Symbol	I/O	ECL/TTL/Open Drain/Power
36	Receive Bit Clock +	RXC+	I	ECL
37	Receive Bit Clock −	RXC−	I	ECL
38	ECL Logic Power	V_{CC}		+ 5V
39	Receive Data +	RXD+	I	ECL
40	Receive Data −	RXD−	I	ECL
41	ECL Logic Ground	GND		+ 0V
42	External Loopback Data +	LBD+	O	ECL
43	External Loopback Data −	LBD−	O	ECL
44	ECL I/O Power	V_{CC}		+ 5V
45	Transmit Data+	TXD+	O	ECL
46	Transmit Data+	TXD−	O	ECL
47	ECL Logic Ground	GND		+ 0V
48	Transmit Bit Clock +	TXC+	I	ECL
49	Transmit Bit Clock −	TXC−	I	ECL
50	ECL Logic Power	V_{CC}		+ 5V
51	Transmit Byte Clock +	TBC+	I	ECL
52	Transmit Byte Clock −	TBC−	I	ECL
53	FOTX Enable Level	TEL	I	TTL
54	No Connect	N/C		
55	No Connect	N/C		
56	FOTX Enable	TXE	O	TTL
57	Local Byte Clock	LBC	I	TTL
58	PHY Port B Request Data<0>	BRD0	I	TTL
59	PHY Port B Request Data<1>	BRD1	I	TTL
60	PHY Port B Request Data<2>	BRD2	I	TTL
61	PHY Port B Request Data<3>	BRD3	I	TTL
62	CMOS Logic Ground	GND		+ 0V
63	PHY Port B Request Data<4>	BRD4	I	TTL
64	CMOS I/O Power	V_{CC}		+ 5V
65	PHY Port B Request Data<5>	BRD5	I	TTL
66	CMOS I/O Ground	GND		+ 0V
67	PHY Port B Request Data<6>	BRD6	I	TTL
68	PHY Port B Request Data<7>	BRD7	I	TTL
69	PHY Port B Request Control	BRC	I	TTL
70	PHY Port B Request Parity	BRP	O	TTL

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6.0 Pin Descriptions (Continued)

TABLE 6-1. DP83251 Pinout Summary (Continued)

Pin No.	Signal Name	Symbol	I/O	ECL/TTL/Open Drain/Power
71	~PLAYER Device Reset	$\overline{RST}$	I	TTL
72	Read/~Write	R/$\overline{W}$	I	TTL
73	Chip Enable	$\overline{CE}$	I	TTL
74	~Interrupt	$\overline{INT}$	O	Open Drain
75	~Acknowledge	$\overline{ACK}$	O	Open Drain
76	Control Bus Address<0>	CBA0	I	TTL
77	Control Bus Address<1>	CBA1	I	TTL
78	Control Bus Address<2>	CBA2	I	TTL
79	Control Bus Address<3>	CBA3	I	TTL
80	Control Bus Address<4>	CBA4	I	TTL
81	CMOS Logic Power	V_{CC}		+5V
82	Control Bus Data<0>	CBD0	I/O	TTL
83	Control Bus Data<1>	CBD1	I/O	TTL
84	CMOS Logic Ground	GND		+0V

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6.0 Pin Descriptions (Continued)

SERIAL INTERFACE

The Serial Interface consists of I/O signals used to connect the PLAYER device to the Physical Medium Dependent (PMD) sublayer.

The PLAYER device uses these signals to interface to a Fiber Optic Transmitter (FOTX), Fiber Optic Receiver (FOXR), Clock Recovery Device (CRD device), and Clock Distribution Device (CDD device).

Symbol	Pin No.	I/O	Description
CD	33	I	**Clock Detect:** A TTL input signal from the Clock Recovery Device indicating that the Receive Clock (RXC ±) is properly synchronized with the Receive Data RXD ±).
TTLSD	34	I	**Signal Detect:** A TTL signal from the clock Recovery Device indicating that a signal is being received by the Fiber Optic Receiver.
RXD+ RXD−	39 40	I	**Receive Data:** Differential 100K ECL, 125 Mbps serial data input signals from the Clock Recovery Device.
TXD+ TXD−	45 46	O	**Transmit Data:** Differential, 100K ECL, 125 Mbps serial data output signals to the Fiber Optic Transmitter.
ELB	35	O	**External Loopback Enable:** A TTL output signal to the Clock Recovery Device which enables/disables loopback data through the Clock Recovery Device. This signal is controlled by the Mode Register.
LBD+ LBD−	42 43	O	**Loopback Data:** Differential, 100K ECL, 125 Mbps, external serial loopback data output signals to the Clock Recovery Device. When the PLAYER device is not in external loopback mode, the LBD+ signal is kept high and the LBD− signal is kept low.
TEL	53	I	**FOTX Enable Level:** A TTL input signal to select the Fiber Optic Transmitter Enable (TXE) signal level.
TXE	56	O	**FOTX Enable:** A TTL output signal to enable/disable the Fiber Optic Transmitter. The output level of the TXE pin is determined by three parameters, the Transmit Enable (TE) bit in the Mode Register, the TM2–TM0 bits in the Current Transmit State Register, and also the input to the TEL pin. The following rules summarizes the output of the TXE pin: (1) If TE = 0 and TEL = GND, then TXE = V_{CC} (2) If TE = 0 and TEL = V_{CC}, then TXE = GND (3) If TE = 1 and OTM and TEL = GND, then TXE = V_{CC} (4) If TE = 1 and OTM and TEL = V_{CC}, then TXE = GND (5) If TE = 1 and not OTM and TEL = GND, then TXE = GND (6) If TE = 1 and not OTM and TEL = V_{CC}, then TXE = V_{CC}

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6.0 Pin Descriptions (Continued)

PHY PORT INTERFACE

The PHY Port Interface consists of I/O signals used to connect the PLAYER Device to the Media Access Control (MAC) sublayer or other PLAYER Devices. The DP83251 Device has one PHY Port Interface which consists of the B__Request and the A__Indicate paths.

Each path consists of an odd parity bit, a control bit, and two 4-bit symbols.

Refer to Section 3.3, the Configuration Switch, for further information.

Symbol	Pin No.	I/O	Description
AIP	16	O	**PHY Port A Indicate Parity:** A TTL output signal representing odd parity for the 10-bit wide Port A Indicate signals (AIP, AIC, and AID<7:0>).
AIC	17	O	**PHY Port A Indicate Control:** A TTL output signal indicating that the two 4-bit symbols (AID<7:4> and AID<3:0>) are either control symbols (AIC = 1) or data symbols (AIC = 0).
AID7 AID6 AID5 AID4	18 19 21 23	O	**PHY Port A Indicate Data:** TTL output signals representing the first 4-bit data/control symbol. AID7 is the most significant bit and AID4 is the least significant bit of the first symbol.
AID3 AID2 AID1 AID0	25 26 27 28	O	**PHY Port A Indicate Data:** TTL output signals representing the second 4-bit data/control symbol. AID3 is the most significant bit and AID0 is the least significant bit of the second symbol.
BRP	70	I	**PHY Port B Request Parity:** A TTL input signal representing odd parity for the 10-bit wide Port A Request signals (BRP, BRC, and BRD<7:0>).
BRC	69	I	**PHY Port B Request Control:** A TTL input signal indicating that the two 4-bit symbols (BRD<7:4>) and BRD<3:0>) are either control symbols (BRC = 1) or data symbols (BRC = 0).
BRD7 BRD6 BRD5 BRD4	68 67 65 63	I	**PHY Port B Request Data:** TTL input signals representing the first 4 bit data/control symbol. BRD7 is the most significant bit and BRD4 is the least significant bit of the first symbol.
BRD3 BRD2 BRD1 BRD0	61 60 59 58	I	**PHY Port B Request Data:** TTL input signals representing the second 4-bit data/control symbol. BRD3 is the most significant bit and BRD0 is the least significant bit of the second symbol.

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6.0 Pin Descriptions (Continued)

CONTROL BUS INTERFACE

The Control Bus Interface consists of I/O signals used to connect the PLAYER device to Station Management (SMT).

The Control Bus is an asynchronous interface between the PLAYER device and a general purpose microprocessor. It provides access to 32 8-bit internal registers.

Refer to *Figure 22*, Control Bus Timing Diagram, for more information.

Symbol	Pin No.	I/O	Description
$\overline{CE}$	73	I	**Chip Enable:** An active-low, TTL, input signal which enables the Control Bus port for a read or write cycle. R/$\overline{W}$, CBA<4:0>, CBP, and CBD<7:0> must be valid at the time $\overline{CE}$ is low.
R/$\overline{W}$	72	I	**Read/~Write:** A TTL input signal which indicates a read Control Bus cycle (R/$\overline{W}$ = 1), or a write Control Bus cycle (R/$\overline{W}$ = 0). This signal must be valid when $\overline{CE}$ is low and held valid until $\overline{ACK}$ becomes low.
$\overline{ACK}$	75	O	**~Acknowledge:** An active low, TTL, open drain output signal which indicates the completion of a read or write cycle. During a read cycle, CBD<7:0> are valid as long as $\overline{ACK}$ is low ($\overline{ACK}$ = 0). During a write cycle, a microprocessor must hold CBD<7:0> valid until $\overline{ACK}$ becomes low. Once $\overline{ACK}$ is low, it will remain low as long as $\overline{CE}$ remains low ($\overline{CE}$ = 0).
$\overline{INT}$	74	O	**~Interrupt:** An active low, open drain, TTL, output signal indicating that an interrupt condition has occurred. The Interrupt Condition Register (ICR) should be read in order to find out the source of the interrupt. Interrupts can be masked through the use of the Interrupt Condition Mask Register (ICMR).
CBA4 CBA3 CBA2 CBA1 CBA0	80 79 78 77 76	I	**Control Bus Address:** TTL input signals used to select the address of the register to be read or written. CBA4 is the most significant bit (MSB), CBA0 is the least significant bit (LSB) of the address signals. These signals must be valid when $\overline{CE}$ is low and held valid until $\overline{ACK}$ becomes low.
CBPE	13	I	**Control Bus Parity Enable:** A TTL input signal which, during write cycles, will enable or disable the Control Bus parity checker. Note that the Control Bus will always generate parity during read cycles, regardless of the state of this signal.
CBP	9	I/O	**Control Bus Parity:** A bidirectional, TTL signal representing odd parity for the Control Bus data (CBD<7:0>). During a read cycle, the signal is held valid by the PLAYER device as long as $\overline{ACK}$ is low. During a write cycle, the signal must be valid when $\overline{CE}$ is low, and must be held valid until $\overline{ACK}$ becomes low. If incorrect parity is used during a write cycle, the PLAYER device will inhibit the write cycle and set the Control Bus Data Parity Error (CPE) bit in the Interrupt Condition Register (ICR).
CBD7 CBD6 CBD5 CBD4 CBD3 CBD2 CBD1 CBD0	8 7 5 4 2 1 83 82	I/O	**Control Bus Data:** Bidirectional, TTL signals containing the data to be read from or written to a register. During a read cycle, the signal is held valid by the PLAYER device as long as $\overline{ACK}$ is low. During a write cycle, the signal must be valid when $\overline{CE}$ is low, and must be held valid until $\overline{ACK}$ becomes low.

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6.0 Pin Descriptions (Continued)

CLOCK INTERFACE

The Clock Interface consists of 12.5 MHz and 125 MHz clocks used by the PLAYER device. The clocks are generated by either the Clock Distribution Device or Clock Recovery Device.

Symbol	Pin No.	I/O	Description
LBC	57	I	**Local Byte Clock:** A TTL, 12.5 MHz, 50% duty cycle, input clock from the Clock Distribution Device. The Local Byte Clock is used by the PLAYER device's internal CMOS logic and to latch incoming/outgoing data of the Control Bus Interface, Port A Interface, Port B Interface, and other miscellaneous I/Os.
RXC+ RXC −	36 37	I	**Receive Bit Clock:** Differential 100k ECL, 125 MHz clock input signals from the Clock Recovery Device. The Receive Bit Clock is used by the Serial Interface to latch the Receive Data (RXD ±).
TXC+ TXC−	48 49	I	**Transmit Bit Clock:** Differential 100k ECL, 125 MHz clock input signals from the Clock Distribution Device. The Transmit Bit Clock is used by the Serial Interface to latch the Transmit Data (TXD ±).
TBC+ TBC−	51 52	I	**Transmit Byte Clock:** Differental 100k ECL, 12.5 MHz clock input signals from the Clock Distribution Device. The Transmit Byte Clock is used by the PLAYER device's internal Shift Register Block.

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6.0 Pin Descriptions (Continued)

MISCELLANOUS INTERFACE

The Miscellaneous Interface consists of a reset signal, user definable sense signals, user definable enable signals, Cascaded PLAYER devices synchronization signals, ground signals, and power signals.

Symbol	Pin No.	I/O	Description
$\overline{RST}$	71	I	**Reset:** An active low, TTL, input signal which clears all registers. The signal must be kept asserted for a minimum of 160 ns. Once the $\overline{RST}$ signal is asserted, the PLAYER device should be allowed 960 ns to reset internal logic. Note that bit zero of the Mode Register will be set to zero (i.e. Stop Mode). See Section 4.2, Stop Mode of Operation for more information.
SP0	14	I	**User Definable Sense Pin 0:** A TTL input signal from a user defined source. Bit zero (Sense Bit 0) of the User Definable Register (UDR) will be set to one if the signal is asserted for a minimum of 160 ns. Once the asserted signal is latched, Sense Bit 0 can only be cleared through the Control Bus Interface, even if the signal is deasserted. This ensures that the Control Bus Interface will record the source of events which can cause interrupts.
SP1	15	I	**User Definable Sense Pin 1:** A TTL input signal from a user defined source. Bit one (Sense Bit 1) of the User Definable Register (UDR) will be set to one if the signal is asserted for a minimum of 160 ns. Once the asserted signal is latched, Sense Bit 1 can only be cleared through the Control Bus Interface, even if the signal is deasserted. This ensures that the Control Bus Interface will record the source of events which can cause interrupts.
EP0	10	O	**User Definable Enable Pin 0:** A TTL output signal allowing control of external logic through the CBUS Interface. EP0 is asserted/deasserted through bit two (Enable Bit 0) of the User Definable Register (UDR). When Enable Bit 0 is set to zero, EP0 is deasserted. When Enable Bit 0 is set to one, EP0 is asserted.
EP1	11	O	**User Definable Enable Pin 1:** A TTL output signal allowing control of external logic through the CBUS Interface. EP1 is asserted/deasserted through bit two (Enable Bit 1) of the User Definable Register (UDR). When Enable Bit 1 is set to zero, EP1 is deasserted. When Enable Bit 1 is set to one, EP1 is asserted.
CS	29	I	**Cascade Start:** A TTL input signal used to synchronize cascaded PLAYER devices in point-to-point applications. The signal is asserted when all of the cascaded PLAYER devices have the Cascade Mode (CM) bit of Mode Register (MR) set to one, and all of the Cascade Ready pins of the cascaded PLAYER devices have been released. For further information, refer to Section 4.4, Cascade Mode of Operation.
CR	30	O	**Cascade Ready:** An Open Drain output signal used to synchronize cascaded PLAYER devices in point-to-point applications. The signal is released (i.e. an Open Drain line is released) when all the cascaded PLAYER devices have the Cascade Mode (CM) bit of the Mode Register (MR) set to one and a JK symbol pair has been received. For further information, refer to Section 4.4, Cascade Mode of Operation.

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6.0 Pin Descriptions (Continued)

POWER AND GROUND

All power pins should be connected to a single 5V power supply. All ground pins should be connected to a common 0V supply.

Symbol	Pin No.	I/O	Description
GND	3		**Ground:** Power supply return for Control Bus Interface CMOS I/Os.
V_{CC}	6		**Power:** Positive 5V power supply (±5% relative to ground) for Control Bus Interface CMOS I/Os.
GND	12		**Ground:** Power supply return for internal CMOS logic.
GND	20		**Ground:** Power supply return for Port A Interface CMOS I/Os.
V_{CC}	22		**Power:** Positive 5V power supply (±5% relative to ground) for the Port A Interface CMOS I/Os.
GND	24		**Ground:** Power supply return to internal CMOS logic.
V_{CC}	38		**Power:** Positive 5V power supply (±5% relative to ground) for internal ECL logic.
GND	41		**Ground:** Power supply return for internal ECL logic.
V_{CC}	44		**Power:** Positive 5V power supply (±5% relative to ground) for the Serial Interface ECL I/Os.
GND	47		**Ground:** Power supply return for internal ECL logic.
V_{CC}	50		**Power:** Positive 5V power supply (±5% relative to ground) for the Serial Interface ECL I/Os.
GND	62		**Ground:** Power supply return for internal CMOS logic.
V_{CC}	64		**Power:** Positive 5V power supply (±5% relative to ground) for the Port A Interface CMOS I/Os.
GND	66		**Ground:** Power supply return for Port A Interface CMOS I/Os.
V_{CC}	81		**Power:** Positive 5V power supply (±5% relative to ground) for internal CMOS logic.
GND	84		**Ground:** Power supply return for internal CMOS logic.

NO CONNECT PINS

Symbol	Pin No.	I/O	Description
N/C	31		**No Connect:** Not used by the PLAYER device
N/C	32		**No Connect:** Not used by the PLAYER device
N/C	54		**No Connect:** Not used by the PLAYER device
N/C	55		**No Connect:** Not used by the PLAYER device

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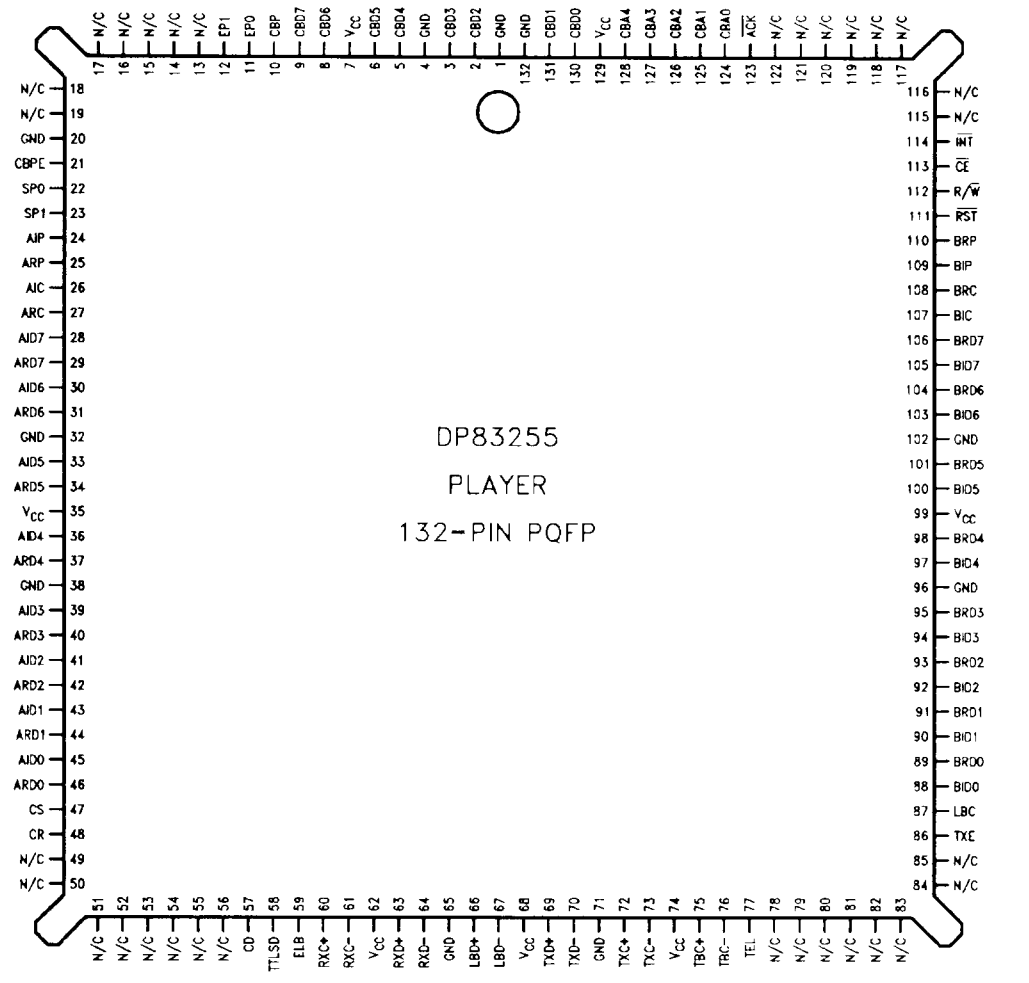
6.0 Pin Descriptions (Continued)

6.2 DP83255

The pin descriptions for the DP83255 are divided into six functional interfaces; Serial Interface, PHY Port Interface, Control Bus Interface, Clock Interface, and Miscellaneous Interface.

For a Pinout Summary List, refer to Table 6-2.



TL/F/10386–21

Order Number DP83255AVF
See NS Package Number VF132A

FIGURE 6-2. DP83255 132-Pin PQFP Pinout

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6.0 Pin Descriptions (Continued)

TABLE 6-2. DP83255 Pinout Summary

Pin No.	Signal Name	Symbol	I/O	ECL/TTL/Open Drain/Power
1	CMOS Logic Ground	GND		+ 0V
2	Control Bus Data<2>	CBD2	I/O	TTL
3	Control Bus Data<3>	CBD3	I/O	TTL
4	CMOS I/O Ground	GND		+ 0V
5	Control Bus Data<4>	CBD4	I/O	TTL
6	Control Bus Data<5>	CBD5	I/O	TTL
7	CMOS I/O Power	V_{CC}		+ 5V
8	Control Bus Data<6>	CBD6	I/O	TTL
9	Control Bus Data<7>	CBD7	I/O	TTL
10	Control Bus Data Parity	CBP	I/O	TTL
11	Enable Pin 0	EP0	O	TTL
12	Enable Pin 1	EP1	O	TTL
13	No Connect	N/C		
14	No Connect	N/C		
15	No Connect	N/C		
16	No Connect	N/C		
17	No Connect	N/C		
18	No Connect	N/C		
19	No Connect	N/C		
20	CMOS Logic Ground	GND		+ 0V
21	Control Bus Data Parity Enable	CBPE	I	TTL
22	Sense Pin 0	SP0	I	TTL
23	Sense Pin 1	SP1	I	TTL
24	PHY Port A Indicate Parity	AIP	O	TTL
25	PHY Port A Request Parity	ARP	I	TTL
26	PHY Port A Indicate Control	AIC	O	TTL
27	PHY Port A Request Control	ARC	I	TTL
28	PHY Port A Indicate Data<7>	AID7	O	TTL
29	PHY Port A Request Data<7>	ARD7	I	TTL
30	PHY Port A Indicate Data<6>	AID6	O	TTL
31	PHY Port A Request Data<6>	ARD6	I	TTL
32	CMOS I/O Ground	GND		+ 0V
33	PHY A Indicate Data<5>	AID5	O	TTL
34	PHY A Request Data<5>	ARD5	I	TTL
35	CMOS I/O Power	V_{CC}		+ 5V

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6.0 Pin Descriptions (Continued)

TABLE 6-2. DP83255 Pinout Summary (Continued)

Pin No.	Signal Name	Symbol	I/O	ECL/TTL/Open Drain/Power
36	PHY A Indicate Data<4>	AID4	O	TTL
37	PHY A Request Data<4>	ARD4	I	TTL
38	CMOS Logic Ground	GND		+0V
39	PHY Port A Indicate Data<3>	AID3	O	TTL
40	PHY Port A Request Data<3>	ARD3	I	TTL
41	PHY Port A Indicate Data<2>	AID2	O	TTL
42	PHY Port A Request Data<2>	ARD2	I	TTL
43	PHY Port A Indicate Data<1>	AID1	O	TTL
44	PHY Port A Request Data<1>	ARD1	I	TTL
45	PHY Port A Indicate Data<0>	AID0	O	TTL
46	Port A Request Data<0>	ARD0	I	TTL
47	Cascade Start	CS	I	TTL
48	Cascade Ready	CR	O	Open Drain
49	No Connect	N/C		
50	No Connect	N/C		
51	No Connect	N/C		
52	No Connect	N/C		
53	No Connect	N/C		
54	No Connect	N/C		
55	No Connect	N/C		
56	No Connect	N/C		
57	Clock Detect	CD	I	TTL
58	Signal Detect	TTLSD	I	TTL
59	External Loopback Enable	ELB	O	TTL
60	Receive Bit Clock +	RXC+	I	ECL
61	Receive Bit Clock −	RXC−	I	ECL
62	ECL Logic Power	V_{CC}		+5V
63	Receive Data +	RXD+	I	ECL
64	Receive Data −	RXD−	I	ECL
65	ECL Logic Ground	GND		+0V
66	External Loopback Data +	LBD+	O	ECL
67	External Loopback Data −	LBD−	O	ECL
68	ECL I/O Power	V_{CC}		+5V
69	Transmit Data +	TXD+	O	ECL
70	Transmit Data −	TXD−	O	ECL

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6.0 Pin Descriptions (Continued)

TABLE 6-2. DP83255 Pinout Summary (Continued)

Pin No.	Signal Name	Symbol	I/O	ECL/TTL/Open Drain/Power
71	ECL Logic Ground	GND		+ 0V
72	Transmit Bit Clock +	TXC+	I	ECL
73	Transmit Bit Clock −	TXC−	I	ECL
74	ECL Logic Power	V_{CC}		+ 5V
75	Transmit Byte Clock +	TBC+	I	ECL
76	Transmit Byte Clock −	TBC−	I	ECL
77	FOTX Enable Level	TEL	I	TTL
78	No Connect	N/C		
79	No Connect	N/C		
80	No Connect	N/C		
81	No Connect	N/C		
82	No Connect	N/C		
83	No Connect	N/C		
84	No Connect	N/C		
85	No Connect	N/C		
86	FOTX Enable	TXE	O	TTL
87	Local Byte Clock	LBC	I	TTL
88	PHY Port B Indicate Data<0>	BID0	O	TTL
89	PHY Port B Request Data<0>	BRD0	I	TTL
90	PHY Port B Indicate Data<1>	BID1	O	TTL
91	PHY Port B Request Data<1>	BRD1	I	TTL
92	PHY Port B Indicate Data<2>	BID2	O	TTL
93	PHY Port B Request Data<2>	BRD2	I	TTL
94	PHY Port B Indicate Data<3>	BID3	O	TTL
95	PHY Port B Request Data<3>	BRD3	I	TTL
96	CMOS Logic Ground	GND		+ 0V
97	PHY Port B Indicate Data<4>	BID4	O	TTL
98	PHY Port B Request Data<4>	BRD4	I	TTL
99	CMOS I/O Power	V_{CC}		+ 5V
100	PHY Port B Indicate Data<5>	BID5	O	TTL
101	PHY Port B Request Data<5>	BRD5	I	TTL
102	CMOS I/O Ground	GND		+ 0V
103	PHY Port B Indicate Data<6>	BID6	O	TTL
104	PHY Port B Request Data<6>	BRD6	I	TTL
105	PHY Port B Indicate Data<7>	BID7	O	TTL

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6.0 Pin Descriptions (Continued)

TABLE 6-2. DP83255 Pinout Summary (Continued)

Pin No.	Signal Name	Symbol	I/O	ECL/TTL/Open Drain/Power
106	PHY Port B Request Data<7>	BRD7	I	TTL
107	PHY Port B Indicate Control	BIC	O	TTL
108	PHY Port B Request Control	BRC	I	TTL
109	PHY Port B Indicate Parity	BIP	O	TTL
110	PHY Port B Request Parity	BRP	I	TTL
111	~PLAYER Device Reset	$\overline{RST}$	I	TTL
112	Read/~Write	R/$\overline{W}$	I	TTL
113	Chip Enable	$\overline{CE}$	I	TTL
114	~Interrupt	$\overline{INT}$	O	Open Drain
115	No Connect	N/C		
116	No Connect	N/C		
117	No Connect	N/C		
118	No Connect	N/C		
119	No Connect	N/C		
120	No Connect	N/C		
121	No Connect	N/C		
122	No Connect	N/C		
123	~Acknowledge	$\overline{ACK}$	O	Open Drain
124	Control Bus Address<0>	CBA0	I	TTL
125	Control Bus Address<1>	CBA1	I	TTL
126	Control Bus Address<2>	CBA2	I	TTL
127	Control Bus Address<3>	CBA3	I	TTL
128	Control Bus Address<4>	CBA4	I	TTL
129	CMOS Logic Power	V_{CC}		+5V
130	Control Bus Data<0>	CBD0	I/O	TTL
131	Control Bus Data<1>	CBD1	I/O	TTL
132	CMOS Logic Ground	GND		+0V

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6.0 Pin Descriptions (Continued)

SERIAL INTERFACE

The Serial Interface consists of I/O signals used to connect the PLAYER device to the Physical Medium Dependent (PMD) sublayer.

The PLAYER device uses these signals to interface to a Fiber Optic Transmitter (FOTX), Fiber Optic Receiver (FORX), Clock Recovery Device (CRD device), and Clock Distribution Device (CDD device).

Symbol	Pin No.	I/O	Description
CD	57	I	**Clock Detect:** A TTL input signal from the Clock Recovery Device indicating that the Receive Clock (RXC ±) is properly synchronized with the Receive Data (RXD ±).
TTLSD	58	I	**Signal Detect:** A TTL input signal from the Clock Recovery Device indicating that a signal is being received by the Fiber Optic Receiver.
RXD+ RXD−	63 64	I	**Receive Data:** Differential 100K ECL, 125 Mbps serial data input signals from the Clock Recovery Device.
TXD+ TXD−	69 70	O	**Transmit Data:** Differential, 100K ECL, 125 Mbps serial data output signals to the Fiber Optic Transmitter.
ELB	59	O	**External Loopback Enable:** A TTL output signal to the Clock Recovery Device which enables/disables loopback data through the Clock Recovery Device. This signal is controlled by the Mode Register.
LBD+ LBD−	66 67	O	**Loopback Data:** Differential, 100K ECL, 125 Mbps, serial external loopback data output signals to the Clock Recovery Device. When the PLAYER device is not in external loopback mode, the LBD+ signal is kept high and the LBD− signal is kept low.
TEL	77	I	**FOTX Enable Level:** A TTL input signal to select the Fiber Optic Transmitter Enable (TXE) signal level.
TXE	86	O	**FOTX Enable:** A TTL output signal to enable/disable the Fiber Optic Transmitter. The output level of the TXE pin is determined by three parameters, the Transmit Enable (TE) bit in the Mode Register, the TM2–TM0 bits in the Current Transmit State Register, and also the input to the TEL pin. The following rules summarizes the output of the TXE pin: (1) If TE = 0 and TEL = GND, then TXE = V_{CC} (2) If TE = 0 and TEL = V_{CC}, then TXE = GND (3) If TE = 1 and OTM and TEL = GND, then TXE = V_{CC} (4) If TE = 1 and OTM and TEL = V_{CC}, then TXE = GND (5) If TE = 1 and not OTM and TEL = GND, then TXE = GND (6) If TE = 1 and not OTM and TEL = V_{CC}, then TXE = V_{CC}

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6.0 Pin Descriptions (Continued)

PHY PORT INTERFACE

The PHY Port Interface consists of I/O signals used to connect the PLAYER Device to the Media Access Control (MAC) sublayer or other PLAYER Devices. The DP83255 Device has two PHY Port Interfaces. The A_Request and A_Indicate paths form one PHY Port Interface and the B_Request and B_Indicate paths form the second PHY Port Interface. Each path consists of an odd parity bit, a control bit, and two 4-bit symbols.

Refer to Section 3.3, the Configuration Switch, for more information.

Symbol	Pin No.	I/O	Description
AIP	24	O	**PHY Port A Indicate Parity:** A TTL output signal representing odd parity for the 10-bit wide Port A Indicate signals (AIP, AIC, and AID<7:0>).
AIC	26	O	**PHY Port A Indicate Control:** A TTL output signal indicating that the two 4-bit symbols (AID<7:4> and AID<3:0>) are either control symbols (AIC = 1) or data symbols (AIC = 0).
AID7 AID6 AID5 AID4	28 30 33 36	O	**PHY Port A Indicate Data:** TTL output signals representing the first 4-bit data/control symbol. AID7 is the most significant bit and AID4 is the least significant bit of the first symbol.
AID3 AID2 AID1 AID0	39 41 43 45	O	**PHY Port A Indicate Data:** TTL output signals representing the second 4-bit data/control symbol. AID3 is the most significant bit and AID0 is the least significant bit of the second symbol.
ARP	25	I	**PHY Port A Request Parity:** A TTL input signal representing odd parity for the 10-bit wide Port A Request signals (ARP, ARC, and ARD<7:0>).
ARC	27	I	**PHY Port A Request Control:** A TTL input signal indicating that the two 4-bit symbols (ARD<7:4> and ARD<3:0>) are either control symbols (ARC = 1) or data symbols (ARC = 0).
ARD7 ARD6 ARD5 ARD4	29 31 34 37	I	**PHY Port A Request Data:** TTL input signals representing the first 4 bit data/control symbol. ARD7 is the most significant bit and ARD4 is the least significant bit of the first symbol.
ARD3 ARD2 ARD1 ARD0	40 42 44 46	I	**PHY Port A Request Data:** TTL input signals representing the second 4-bit data/control symbol. ARD3 is the most significant bit and ARD0 is the least significant bit of the second symbol.

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6.0 Pin Descriptions (Continued)

PHY PORT INTERFACE (Continued)

Symbol	Pin No.	I/O	Description
BIP	109	O	**PHY Port B Indicate Parity:** A TTL output signal representing odd parity for the 10-bit wide Port B Indicate signals (BIP, BIC, and BID<7:0>).
BIC	107	O	**PHY Port B Indicate Control:** A TTL output signal indicating that the two 4-bit symbols (BID<7:4> and BID<3:0>) are either control symbols (BIC = 1) or data symbols (BIC = 0).
BID7 BID6 BID5 BID4	105 103 100 97	O	**PHY Port B Indicate Data:** TTL output signals representing the first 4-bit data/control symbol. BID7 is the most significant bit and BID4 is the least significant bit of the first symbol.
BID3 BID2 BID1 BID0	94 92 90 88	O	**PHY Port B Indicate Data:** TTL output signals representing the second 4-bit data/control symbol. BID3 is the most significant bit and BID0 is the least significant bit of the second symbol.
BRP	110	I	**PHY Port B Request Parity:** A TTL input signal representing odd parity for the 10-bit wide Port B Request signals (BRP, BRC, and BRD<7:0>).
BRC	108	I	**PHY Port B Request Control:** A TTL input signal indicating that the two 4-bit symbols (BRD<7:4>) and BRD<3:0>) are either control symbols (BRC = 1) or data symbols (BRC = 0).
BRD7 BRD6 BRD5 BRD4	106 104 101 98	I	**PHY Port B Request Data:** TTL input signals representing the first 4-bit data/control symbol. BRD7 is the most significant bit and BRD4 is the least significant bit of the first symbol.
BRD3 BRD2 BRD1 BRD0	95 93 91 89	I	**PHY Port B Request Data:** TTL input signals representing the second 4-bit data/control symbol. BRD3 is the most significant bit and BRD0 is the least significant bit of the second symbol.

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6.0 Pin Descriptions (Continued)

CONTROL BUS INTERFACE

The Control Bus Interface consists of I/O signals used to connect the PLAYER device to Station Management (SMT).

The Control Bus is an asynchronous interface between the PLAYER device and a general purpose microprocessor. It provides access to 32 8-bit internal registers.

Refer to *Figure 22*, Control Bus Timing Diagram, for further information.

Symbol	Pin No.	I/O	Description
$\overline{CE}$	113	I	**Chip Enable:** An active-low, TTL, input signal which enables the Control Bus port for a read or write cycle. R/$\overline{W}$, CBA<4:0>, CBP, and CBD<7:0> must be valid at the time $\overline{CE}$ is low.
R/$\overline{W}$	112	I	**Read/~Write:** A TTL input signal which indicates a read Control Bus cycle (R/$\overline{W}$ = 1), or a write Control Bus cycle (R/$\overline{W}$ = 0). This signal must be valid when $\overline{CE}$ is low and held valid until $\overline{ACK}$ becomes low.
$\overline{ACK}$	123	O	**~Acknowledge:** An active low, TTL, open drain output signal which indicates the completion of a read or write cycle. During a read cycle, CBD<7:0> are valid as long as $\overline{ACK}$ is low ($\overline{ACK}$ = 0). During a write cycle, a microprocessor must hold CBD<7:0> valid until $\overline{ACK}$ becomes low. Once $\overline{ACK}$ is low, it will remain low as long as $\overline{CE}$ remains low ($\overline{CE}$ = 0).
$\overline{INT}$	114	O	**~Interrupt:** An active low, open drain, TTL, output signal indicating that an interrupt condition has occurred. The Interrupt Condition Register (ICR) should be read in order to determine the source of the interrupt. Interrupts can be masked through the use of the Interrupt Condition Mask Register (ICMR)
CBA4 CBA3 CBA2 CBA1 CBA0	128 127 126 125 124	I	**Control Bus Address:** TTL input signals used to select the address of the register to be read or written. CBA4 is the most significant bit and CBA0 is the least significant bit of the address signals. These signals must be valid when $\overline{CE}$ is low and held valid until $\overline{ACK}$ becomes low.
CBPE	21	I	**Control Bus Parity Enable:** A TTL input signal which, during write cycles, will enable or disable the Control Bus parity checker. Note that the Control Bus will always generate parity during read cycles, regardless of the state of this signal.
CBP	10	I/O	**Control Bus Parity:** A bidirectional, TTL signal representing odd parity for the Control Bus data (CBD<7:0>). During a read cycle, the signal is held valid by the PLAYER device as long as $\overline{ACK}$ is low. During a write cycle, the signal must be valid when $\overline{CE}$ is low, and must be held valid until $\overline{ACK}$ becomes low. If incorrect parity is used during a write cycle, the PLAYER device will inhibit the write cycle and set the Control Bus Data Parity Error (CPE) bit in the Interrupt Condition Register (ICR).
CBD7 CBD6 CBD5 CBD4 CBD3 CBD2 CBD1 CBD0	9 8 6 5 3 2 131 130	I/O	**Control Bus Data:** Bidirectional, TTL signals containing the data to be read from or written to a register. During a read cycle, the signal is held valid by the PLAYER device as long as $\overline{ACK}$ is low. During a write cycle, the signal must be valid when $\overline{CE}$ is low, and must be held valid until $\overline{ACK}$ becomes low.

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6.0 Pin Descriptions (Continued)

CLOCK INTERFACE

The Clock Interface consists of 12.5 MHz and 125 MHz clocks used by the PLAYER device. The clocks are generated by either the Clock Distribution Device or Clock Recovery Device.

Symbol	Pin No.	I/O	Description
LBC	87	I	**Local Byte Clock:** A TTL, 12.5 MHz, 50% duty cycle, input clock from the Clock Distribution Device. The Local Byte Clock is used by the PLAYER device's internal CMOS logic and to latch incoming/outgoing data of the Control Bus Interface, Port A Interface, Port B Interface, and other miscellaneous I/Os.
RXC+ RXC−	60 61	I	**Receive Bit Clock:** Differential, 100k ECL, 125 MHz clock input signals from the Clock Recovery Device. The Receive Bit Clock is used by the Serial Interface to latch the Receive Data (RXD ±).
TXC+ TXC−	72 73	I	**Transmit Bit Clock:** Differential, 100k ECL, 125 MHz clock input signals from the Clock Distribution Device. The Transmit Bit Clock is used by the Serial Interface to latch the Transmit Data (TXD ±).
TBC+ TBC−	75 76	I	**Transmit Byte Clock:** Differental, 100k ECL, 12.5 MHz clock input signals from the Clock Distribution Device. The Transmit Byte Clock is used by the PLAYER device's internal Shift Register Block.

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6.0 Pin Descriptions (Continued)

MISCELLANEOUS INTERFACE

The Miscellaneous Interface consists of a reset signal, user definable sense signals, user definable enable signals, Cascaded PLAYER device's synchronization signals, ground signals, and power signals.

Symbol	Pin No.	I/O	Description
$\overline{RST}$	111	I	**Reset:** An active low, TTL, input signal which clears all registers. The signal must be kept asserted for a minimum of 160 ns. Once the $\overline{RST}$ signal is asserted, the PLAYER device should be allowed 960 ns to reset internal logic. Note that bit zero of the Mode Register will be set to zero (i.e. Stop Mode). See Section 4.2, Stop Mode of Operation for more information.
SP0	22	I	**User Definable Sense Pin 0:** A TTL input signal from a user defined source. Bit zero (Sense Bit 0) of the User Definable Register (UDR) will be set to one if the signal is asserted for a minimum of 160 ns. Once the asserted signal is latched, Sense Bit 0 can only be cleared through the Control Bus Interface, even if the signal is deasserted. This ensures that the Control Bus Interface will record the source of events which can cause interrupts.
SP1	23	I	**User Definable Sense Pin 1:** A TTL input signal from a user defined source. Bit one (Sense Bit 1) of the User Definable Register (UDR) will be set to one if the signal is asserted for a minimum of 160 ns. Once the asserted signal is latched, Sense Bit 0 can only be cleared through the Control Bus Interface, even if the signal is deasserted. This ensures that the Control Bus Interface will record the source of events which can cause interrupts.
EP0	11	O	**User Definable Enable Pin 0:** A TTL output signal allowing control of external logic through the Control Bus Interface. EP0 is asserted/deasserted through bit two (Enable Bit 0) of the User Definable Register (UDR). When Enable Bit 0 is set to zero, EP0 is deasserted. When Enable Bit 0 is set to one, EP0 is asserted.
EP1	12	O	**User Definable Enable Pin 1:** A TTL output signal allowing control of external logic through the Control Bus Interface. EP1 is asserted/deasserted through bit two (Enable Bit 1) of the User Definable Register (UDR). When Enable Bit 1 is set to zero, EP1 is deasserted. When Enable Bit 1 is set to one, EP1 is asserted.
CS	47	I	**Cascade Start:** A TTL input signal used to synchronize cascaded PLAYER devices in point-to-point applications. The signal is asserted when all of the cascaded PLAYER devices have the Cascade Mode (CM) bit of the Mode Register (MR) set to one, and all of the Cascade Ready (CR) pins of the cascaded PLAYER devices have been released. For further information, refer to Section 4.4, Cascade Mode of Operation.
CR	48	O	**Cascade Ready:** An Open Drain output signal used to synchronize cascaded PLAYER devices in point-to-point applications. The signal is released when all the cascaded PLAYER devices have the Cascade Mode (CM) bit of the Mode Register (MR) set to one and a JK symbol pair has been received. For further information, refer to section 4.4, Cascade Mode of Operation.

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6.0 Pin Descriptions (Continued)

POWER AND GROUND

All power pins should be connected to a single 5V power supply. All ground pins should be connected to a common 0V ground supply.

Symbol	Pin No.	I/O	Description
GND	1		**Ground:** Power supply return for internal CMOS logic.
GND	4		**Ground:** Power supply return for Control Bus Interface CMOS I/Os.
V_{CC}	7		**Power:** Positive 5V power supply (±5% relative to ground) for Control Bus Interface CMOS I/Os.
GND	20		**Ground:** Power supply return for internal CMOS logic.
GND	32		**Ground:** Power supply return for Port A Interface CMOS I/Os.
V_{CC}	35		**Power:** Positive 5V power supply (±5% relative to ground) for the Port A Interface CMOS I/Os.
GND	38		**Ground:** Power supply return for internal CMOS logic.
V_{CC}	62		**Power:** Positive 5V power supply (±5% relative to ground) for internal ECL logic.
GND	65		**Ground:** Power supply return for internal ECL logic.
V_{CC}	68		**Power:** Positive 5V power supply (±5% relative to ground) for the Serial Interface ECL I/Os.
GND	71		**Ground:** Power supply return for internal ECL logic.
V_{CC}	74		**Power:** Positive 5V power supply (±5% relative to ground) for internal ECL logic.
GND	96		**Ground:** Power supply return for internal CMOS logic.
V_{CC}	99		**Power:** Positive 5V power supply (±5% relative to ground) for Port B Interface CMOS I/Os.
GND	102		**Ground:** Power supply return for Port B Interface CMOS I/Os.
V_{CC}	129		**Power:** 5V power supply (±5% relative to ground) for internal CMOS logic.
GND	132		**Ground:** Power supply return for internal CMOS logic.

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6.0 Pin Descriptions (Continued)

NO CONNECT PINS

Symbol	Pin No.	I/O	Description
N/C	13		**No Connect:** Not used by the PLAYER device
N/C	14		**No Connect:** Not used by the PLAYER device
N/C	15		**No Connect:** Not used by the PLAYER device
N/C	16		**No Connect:** Not used by the PLAYER device
N/C	17		**No Connect:** Not used by the PLAYER device
N/C	18		**No Connect:** Not used by the PLAYER device
N/C	19		**No Connect:** Not used by the PLAYER device
N/C	49		**No Connect:** Not used by the PLAYER device
N/C	50		**No Connect:** Not used by the PLAYER device
N/C	51		**No Connect:** Not used by the PLAYER device
N/C	52		**No Connect:** Not used by the PLAYER device
N/C	53		**No Connect:** Not used by the PLAYER device
N/C	54		**No Connect:** Not used by the PLAYER device
N/C	55		**No Connect:** Not used by the PLAYER device
N/C	56		**No Connect:** Not used by the PLAYER device
N/C	78		**No Connect:** Not used by the PLAYER device
N/C	79		**No Connect:** Not used by the PLAYER device
N/C	80		**No Connect:** Not used by the PLAYER device
N/C	81		**No Connect:** Not used by the PLAYER device
N/C	82		**No Connect:** Not used by the PLAYER device
N/C	83		**No Connect:** Not used by the PLAYER device
N/C	84		**No Connect:** Not used by the PLAYER device
N/C	85		**No Connect:** Not used by the PLAYER device
N/C	115		**No Connect:** Not used by the PLAYER device
N/C	116		**No Connect:** Not used by the PLAYER device
N/C	117		**No Connect:** Not used by the PLAYER device
N/C	118		**No Connect:** Not used by the PLAYER device
N/C	119		**No Connect:** Not used by the PLAYER device
N/C	120		**No Connect:** Not used by the PLAYER device
N/C	121		**No Connect:** Not used by the PLAYER device
N/C	122		**No Connect:** Not used by the PLAYER device

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7.0 Electrical Characteristics

7.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		−0.5		7.0	V
DC_{IN}	Input Voltage		−0.5		V_{CC} + 0.5	V
DC_{OUT}	Output Voltage		−0.5		V_{CC} + 0.5	V
	Storage Temperature		−65		150	°C

7.2 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.75		5.25	V
T_A	Operating Temperature		0		70	°C

7.3 DC ELECTRICAL CHARACTERISTICS

The DC characteristics are over the operating range, unless otherwise specified.

DC electrical characteristics for the TTL, TRI-STATE output signals of PHY, Port Interfaces, and CBUS Interface.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OZ1}	TRI-STATE Leakage (CBP & CBD7–0)	$V_{OUT} = V_{CC}$			10	µA
I_{OZ2}	TRI-STATE Leakage (CBP & CBD7–0)	$V_{OUT} = V_{GND}$			−10	µA
I_{OZ3}	TRI-STATE Leakage (AID & BID)	$V_{OUT} = V_{CC}$ (Note 1)			60	µA
I_{OZ4}	TRI-STATE Leakage (AID & BID)	V_{OUT} = GND			−500	µA

Note 1: Output buffer has a p-channel pullup device.

DC electrical characteristics for all TTL input signals and the following TTL output signals: External Loopback (ELB), Fiber Optic Transmitter Enable (TXE), Enable Pin 0 (EP0), and Enable Pin 1 (EP1).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage	$I_{OH} = -2$ mA	$V_{CC} - 0.5$			V
V_{OL}	Output Low Voltage	$I_{OL} = 4$ mA			0.5	V
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
V_{IC}	Input Clamp Voltage	$I_{IN} = -18$ mA			−1.5	V
I_{IL}	Input Low Current	V_{IN} = GND			−10	µA
I_{IH}	Input High Current	$V_{IN} = V_{CC}$			+10	µA

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7.0 Electrical Characteristics (Continued)

DC electrical characteristics for all Open Drain output signals ($\overline{INT}$, $\overline{ACK}$ and CR).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low Voltage	I_{OL} = 8 mA			0.5	V
I_{OZ}	TRI-STATE Leakage	$V_{OUT} = V_{CC}$			10	μA

DC electrical characteristics for all 100k ECL input and output signals.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage	$V_{IN} = V_{IH}$ (max)	V_{CC} − 1.025		V_{CC} − 0.880	V
V_{OL}	Output Low Voltage	$V_{IN} = V_{IL}$(min)	V_{CC} − 1.810		V_{CC} − 1.620	V
V_{IH}	Input High Voltage		V_{CC} − 1.165		V_{CC} − 0.880	V
V_{IL}	Input Low Voltage		V_{CC} − 1.810		V_{CC} − 1.475	V
I_L	Input Low Current	V_{IN} = GND			−10	μA
I_H	Input High Current	$V_{IN} = V_{CC}$			100	μA

Supply Current electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Total Supply Current	LBC = 12.5 MHz TXC = 125 MHz			440*	mA

***Note:** The PLAYER device has two pairs of differential ECL outputs, therefore 60 mA of the total supply current is actually consumed by external termination resistors and the maximum current consumed by the PLAYER device alone is only 380 mA. The ECL termination current is calculated as follows:

$V_{OH\_max} = V_{CC} - 0.88V$

$V_{OL\_max} = V_{CC} - 1.62V$

Since the outputs are differential, the average output level is $V_{CC} - 1.25V$. The test load per output is 50Ω at $V_{CC} - 2V$, therefore the external load current through the 50Ω resistor is:

$I_{LOAD} = [(V_{CC} - 1.25) - (V_{CC} - 2)]/50$

$= 0.015A$

$= 15$ mA.

As result, two pairs of ECL outputs consume 60 mA.

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7.0 Electrical Characteristics (Continued)

7.4 AC ELECTRICAL CHARACTERISTICS

The AC Electrical characteristics are over the operating range, unless otherwise specified.

AC Characteristics for the Control Bus Interface

Symbol	Parameter	Min	Max	Units
T1	$\overline{CE}$ Setup to LBC	5		ns
T2	LBC Period	80		ns
T3	LBC to $\overline{ACK}$ Low		45	ns
T4	$\overline{CE}$ Low to $\overline{ACK}$ Low	290	540	ns
T5	LBC Low to CBD(7-0) and CBP Valid		60	ns
T6	LBC to CBD(7-0) and CBP Active		60	ns
T7	$\overline{CE}$ Low to CBD(7-0) and CBP Active	225	475	ns
T8	$\overline{CE}$ Low to CBD(7-0) and CBP Valid	265	515	ns
T9	LBC Pulse Width High	35	45	ns
T10	LBC Pulse Width Low	35	45	ns
T11	$\overline{CE}$ High to $\overline{ACK}$ High		45	ns
T12	R/$\overline{W}$, CBA(7-0), CBD(7-0) and CBP Set up to $\overline{CE}$ Low	5		ns
T13	$\overline{CE}$ High to R/$\overline{W}$, CBA(7-0), CBD(7-0) and CBP Hold Time	0		ns
T14a	R/$\overline{W}$ to LBC Setup Time	0		ns
T14b	CBA to LBC Setup Time	10		ns
T14c	CBD and CBP to LBC Setup Time	0		ns
T15	$\overline{ACK}$ Low to $\overline{CE}$ High Lead Time	0		ns
T16	$\overline{CE}$ Minimum Pulse Width High	20		ns
T17	$\overline{CE}$ High to CBD(7-0) and CBP TRI-STATE		55	ns
T18	$\overline{ACK}$ High to $\overline{CE}$ Low	0		ns
T19	CBD(7-0) Valid to $\overline{ACK}$ Low Setup	20		ns
T20a	LBC to R/$\overline{W}$ Hold Time	10		ns
T20b	LBC to CBA Hold Time	10		ns
T20c	LBC to CBD and CBP Hold Time	20		ns
T21	LBC to $\overline{INT}$ Low		55	ns
T22	LBC to $\overline{INT}$ High		60	ns

Asynchronous Definitions

T4 (min)	T1 + (3 * T2) + T3
T4 (max)	T1 + (4 * T2) + T3
T7 (min)	T1 + (2 * T2) + T6
T7 (max)	T1 + (3 * T2) + T6
T8 (min)	T1 + (2 * T2) + T9 + T5
T8 (max)	T1 + (3 * T2) + T9 + T5

Note: Min/Max numbers are based on T2 = 80 ns and T9 = T10 = 40ns.

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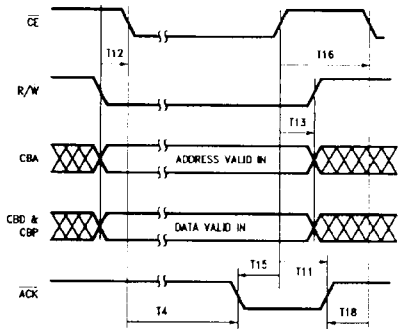
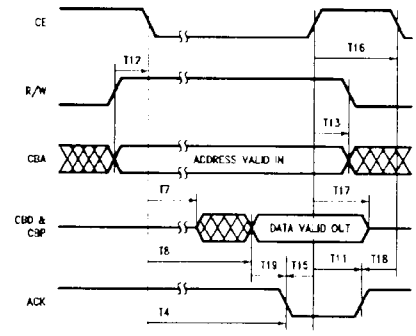
7.0 Electrical Characteristics (Continued)



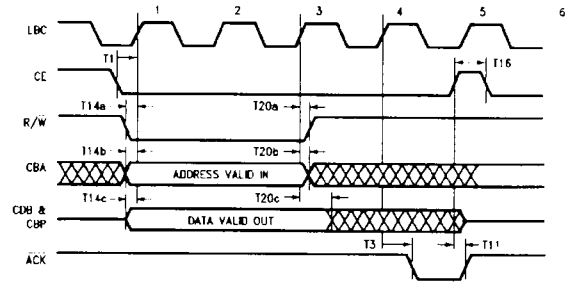
TL/F/10386–22

FIGURE 7-1. Control Bus Write Cycle Timing



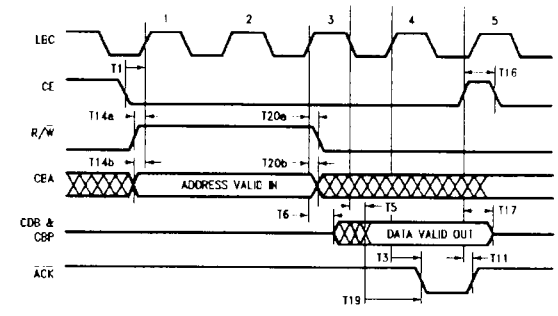
TL/F/10386–23

FIGURE 7-2. Control Bus Read Cycle Timing



TL/F/10386–35

FIGURE 7-3. Control Bus Synchronous Write Cycle Timing



TL/F/10386–24

FIGURE 7-4. Control Bus Synchronous Read Cycle Timing

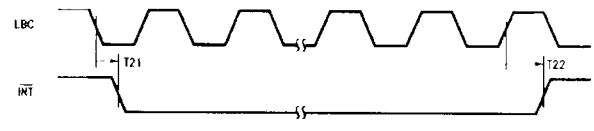


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FIGURE 7-5. Control Bus Interrupt Timing

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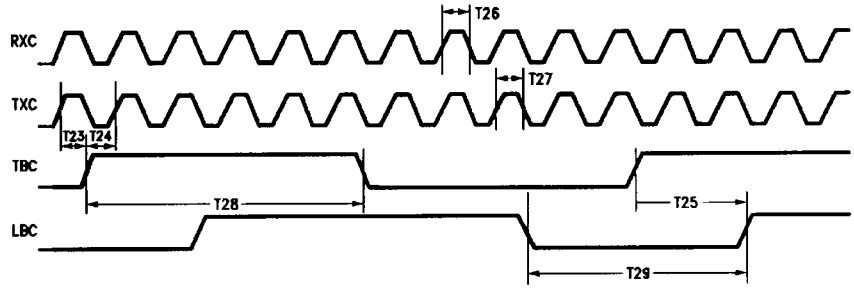
7.0 Electrical Characteristics (Continued)

AC Characteristics for the Clock Signals

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T23	TBC to TXC Hold Time	(Note 1)	2			ns
T24	TBC to TXC Setup Time	(Note 1)	2.5			ns
T25	TBC to LBC Skew		10		22	ns
T26	RXC Duty Cycle	(Note 1)	3.0		5.0	ns
T27	TXC Duty Cycle	(Note 1)	3.5		4.5	ns
T28	TBC Duty Cycle		37		43	ns
T29	LBC Duty Cycle		35		45	ns

Note 1: RXC duty cycle, TXC duty cycle, and TBC to TXC setup time are not tested, but are assured by correlation with characterization data.

Note 2: When PLAYER is used in FDDI applications, TBC and LBC periods will be 80 ns and RXC and TXC periods will be 8 ns.



TL/F/10386–36

FIGURE 7-6. Clock Signals

7.0 Electrical Characteristics (Continued)

AC Characteristics for PHY Port Interfaces

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T30	LBC to Indicate Data Changes from TRI-STATE to Data Valid				70	ns
T31	LBC to Indicate Data Changes from Active to TRI-STATE				70	ns
T32	LBC to Indicate Data Sustain		7			ns
T33	LBC to Valid Indicate Data				45	ns
T34	Request Data to LBC Setup Time		15			ns
T35	Request Data to LBC Hold Time		5			ns

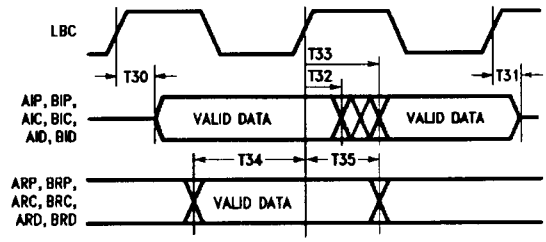


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FIGURE 7-7. PHY Port Interface Timing

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7.0 Electrical Characteristics (Continued)

AC Characteristics for the Serial Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T36	RXD to RXC Setup Time		2			ns
T37	RXD to RXC Hold Time		2			ns
T38	TXC to TXD Change Time				8	ns
T39	TXC to LBD Change Time				8	ns
T40	CD Min Pulse Width		120			ns
T41	SD Min Pulse Width		120			ns

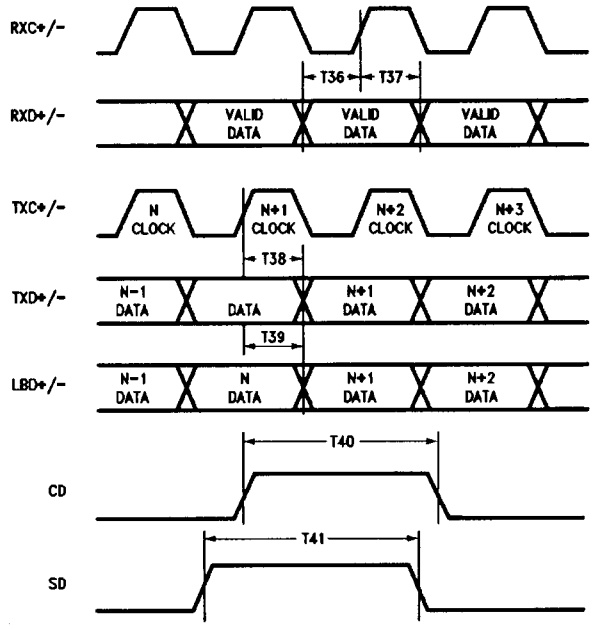

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FIGURE 7-8. Serial Interface Timing

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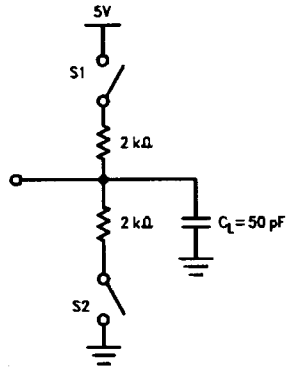
7.0 Electrical Characteristics (Continued)

7.5 AC TEST CIRCUITS



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Note: S_1 is closed for T_{PZL} and T_{PLZ}
S_2 is closed for T_{PZH} and T_{PHZ}
S_1 and S_2 are open otherwise

FIGURE 7-9. Switching Test Circuit for All TRI-STATE Output Signals

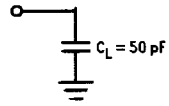

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FIGURE 7-10. Switching Test Circuit for All TTL Output Signals

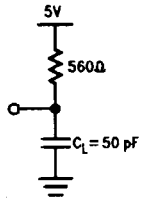

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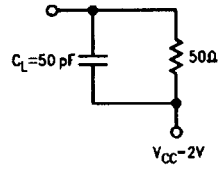
FIGURE 7-11. Switching Test Circuit for All Open Drain Output Signals (INT, ACK and CR)



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Note: C_L = 30 pF includes scope and all stray capacitance without device in test fixture

FIGURE 7-12. Switching Test Circuit for All ECL Input and Output Signals

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Test Waveforms

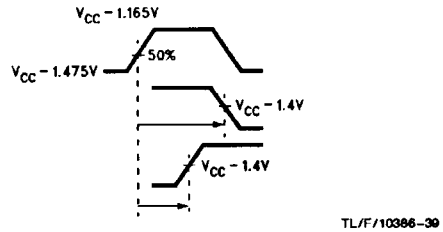

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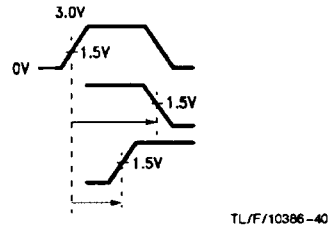
FIGURE 7-13. ECL Output Test Waveform



TL/F/10386–40

Note: All CMOS inputs and outputs are TTL compatible

FIGURE 7-14. TTL Output Test Waveform

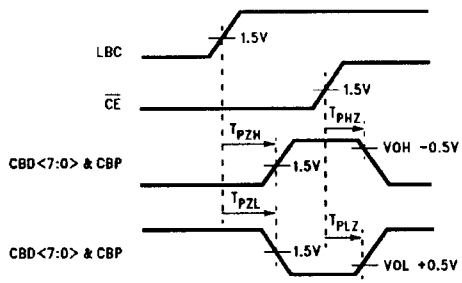


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FIGURE 7-15. TRI-STATE Output Test Waveform

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8.0 Detailed Descriptions

This section describes in detail several functions that had been discussed previously in Section 3.0, Functional Descriptions.

8.1 FRAMING HOLD RULES

DETECTING JK

The JK symbol pair can be used to detect the beginning of a frame during Active Line State (ALS) and Idle Line State (ILS).

While the Line State Detector is in the Idle Line State the PLAYER device "reframes" upon detecting a JK symbol pair and enters the Active Line State.

During Active Line State, acceptance of a JK symbol (reframing) is allowed on any on-boundary JK which is detected at least 1.5 byte times after the previous JK.

During Active Line State, once reframed on a JK, the subsequent off-boundary JK is ignored, even if it is detected beyond 1.5 byte times after the previous JK.

During Active Line State, an Idle or Ending Delimiter (T) symbol will allow reframing on any subsequent JK, if a JK is detected at least 1.5 bytes times after the previous JK.

DETECTING HALT-HALT & HALT-QUIET

During Idle Line State, the detection of a Halt-Halt, or Halt-Quiet symbol pair will still allow the reframing of any subsequent on-boundary JK.

Once a JK is detected during Active Line State, off-boundary Halt-Halt, or Halt-Quiet symbol pairs are ignored until the Elasticity Buffer (EB) has an opportunity to recenter. They are treated as violations.

After recentering on a Halt-Halt, or Halt-Quiet symbol pair, all off-boundary Halt-Halt or Halt-Quiet symbol pairs are ignored until the EB has a chance to recenter during a line state other than Active Line State (which may be as long as 2.8 byte times).

8.2 NOISE EVENTS

A Noise Event is defined as follows:

A noise event is a noise byte, a byte of data which is not in line with the current line state, indicating error or corruption.

Noise Event = [SD • ~CD] +
[SD • CD • PI • ~(II + JK + AB)] +
[SD • CD • ~PI • (PB = II) • AB]

Where:

- • = Logical AND
- + = Logical OR
- ~ = Logical NOT

SD = Signal Detect
CD = Clock Detect
PB = Previous Byte
PLS = Previous Line State
PI = PHY Invalid = HLS + QLS + MLS + NLS + {ULS • [PLS = (ALS + ILS)]}

ILS = Idle Line State
ALS = Active Line State
ULS = Unknown Line State
HLS = Halt Line State
QLS = Quiet Line State
MLS = Master Line State
NLS = Noise Line State
ULS = Unknown Line State

I = Idle symbol
J = First symbol of start delimiter
K = Second symbol of start delimiter
R = Reset symbol
S = Set symbol
T = End delimiter
A = n + R + S + T
B = n + R + S + T + I
n = Any data symbol

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8.0 Detailed Descriptions (Continued)

8.3 LINK ERRORS

A Link Error is defined as follows:

Link Error Event = [ALS • (I~I + xV + Vx + H~H)] + [ALS • ~SD] + [ILS • ~(II + JK)] + [ILS • ~SD)] + [ULS • (PLS = ALS) • Link_Error_Flag • ~SB • ~(HH + HI + II + JK)]

Set Link_Error_Flag = [ALS • (HH + NH + RH + SH + TH)]

Clear Link_Error_Flag = [ALS • JK] + [ILS • JK] + [ULS • (PLS = ALS • Link_Error_Flag • ~SB • ~(HH + HI + II + JK)]

Where:

~ = Logical NOT
+ = Logical OR
• = Logical AND

ILS = Idle Line State
ALS = Active Line State
ULS = Unknown Line State

x = Any symbol
I = Idle symbol
H = Halt symbol
J = First Symbol of start delimiter
K = Second symbol of start delimiter
V = Violation symbol
R = Reset symbol
S = Set symbol
T = End delimiter symbol
N = Data symbol converted to 0000 by the PLAYER device Receiver Block in symbol pairs that contain a data and a control symbol
PLS = Previous Line State
SD = Signal Detect
SB = Stuff Byte: Byte inserted by EB before a JK symbol pair for recentering or due to off-axis JK

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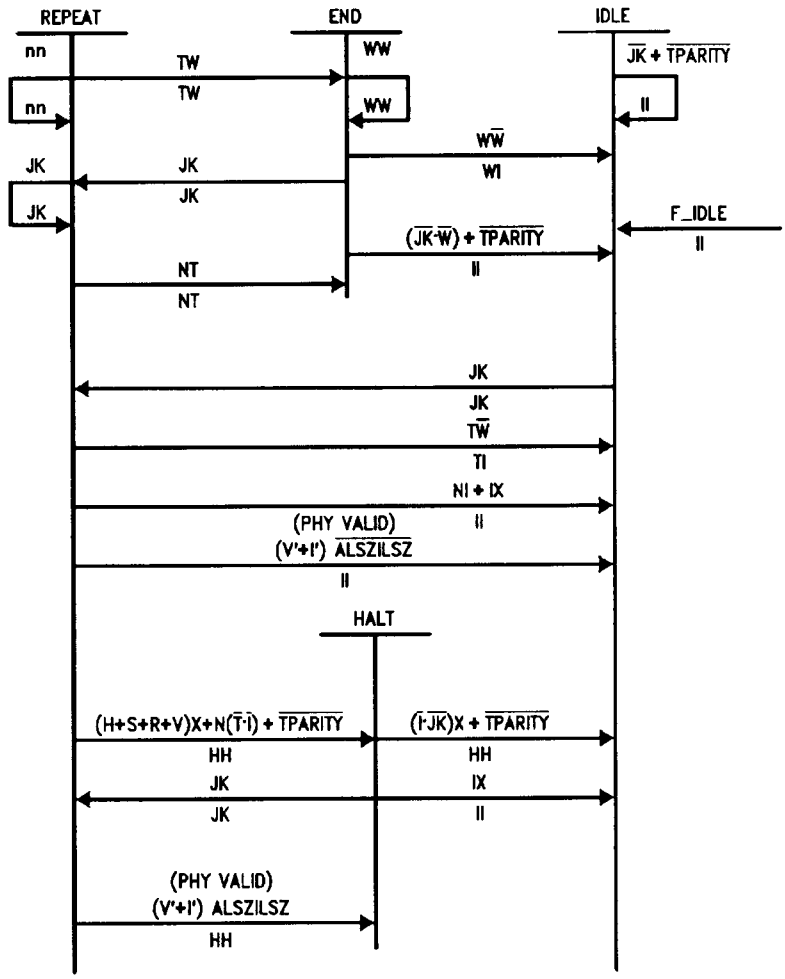
8.0 Detailed Description (Continued)

8.4 REPEAT FILTER

The repeat filter prevents the propagation of code violations to the downstream station.



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Note: Inputs to the Repeat Filter state machine are shown above the transition lines, while outputs from the state machine are shown below the transition lines.

Note: Abbreviations used in the Repeat Filter State Diagram are shown in Table VIII.

FIGURE 8-1. Repeat Filter State Diagram

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TABLE 8-1. Abreviations used in the Repeat Filter State Diagram

F_IDLE:	Force Idle—True when not in Active Transmit Mode
W:	Represents the symbols R, or S, or T
~TPARITY:	Parity error
nn:	Data symbols (for C = 0 in the PHY-MAC Interface)
N:	Data portion of a control and data symbol mixture
X:	Any symbol (i.e. don't care)
V':	Violation symbols or symbols inserted by the Receiver Block
I':	Idle symbols or symbols inserted by the Receiver Block
ALSZILSZ:	Active Line State or Idle Line State (i.e. PHY Invalid)
~ALSZILSZ:	Not in Active Line State nor in Idle Line State (i.e. PHY Valid)
H:	Halt symbol
R:	Reset symbol
S:	Set symbol
T:	Frame ending delimiter
JK:	Frame start delimiter
I:	Idle symbol (Preamble)
V:	Code violations

The Repeat Filter complies with the FDDI standard by observing the following:

1. In Repeat State, violations cause transitions to the Halt State and two Halt symbol pairs are transmitted (unless JK or Ix occurs) followed by transition to the Idle State.
2. When Ix is encountered, the Repeat Filter goes to the Idle State, during which Idle symbol pairs are transmitted until a JK is encountered.
3. The Repeat Filter goes to the Repeat State following a JK from any state.

The END State, which is not part of the FDDI standard, allows an R or S prior to a T within a frame to be recognized as a violation. It also allows NT to end a frame as opposed to being treated as a violation.

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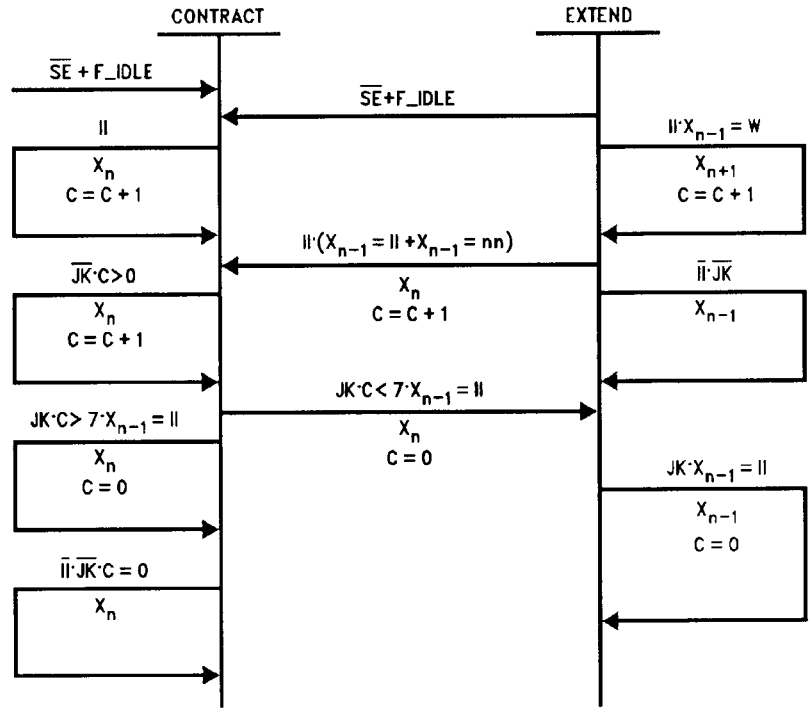
8.5 SMOOTHER



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Notes:
SE: Smoother Enable
C: Preamble Counter
F_IDLE: Force_Idle (Stop or ATM)
X_n: Current Byte
X_{n-1}: Previous Byte
W: RST

FIGURE 8-2. Smoother State Diagram

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8.6 NATIONAL BYTE-WIDE CODE FOR PHY-MAC INTERFACE

The PLAYER device outputs the National byte-wide code from its PHY Port Indicate Output to the MAC device. Each National byte-wide code may contain data or control codes or the line state information of the connection. Table 8-2 lists all the possible outputs.

During Active Line State all data and control symbols are being repeated to the PHY Port Indicate Output with the exception of data in data-control mixture bytes. That data sybmol is replaced by zero. If only one symbol in a byte is a control symbol, the data symbol will be replaced by 0000 and the whole byte will be presented as control code. Note that the Line State Detector recognizes the incoming data to be in the Active Line State upon reception of the Starting Delimiter (JK symbol pair).

During Idle Line State any non Idle symbols will be reflected as the code I'uILS. If both symbols received during Idle Line State are Idle symbols, then the Symbol Decoder generates I'kILS as its output. Note that in this case the coded byte is represented in the form Receive State (b7–4), Known/Unknown Bit (b3) and the Last Known Line State (b2–0). The Receive State is 4 bits long and it represents either the PHY Invalid (0011) or the Idle Line State (1011) condition. The Known/Unknown Bit shows if the symbols received match the line state information in the last 3 bits.

During any line state other than Idle Line State or Active Line State, the Symbol Decoder generates the code V'kLS if the incoming symbols match the current line state. The symbol decoder generates V'uLS if the incoming symbols do not match the current line state.

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Table 8-2.

Current Line State	Symbol 1		Symbol 2		National Code	
	Control Bit	Data	Control Bit	Data	Control Bit	Data
ALS	0,	n	0,	n	0,	n-n
ALS	0,	n	1,	C	1,	N-C
ALS	1,	C	0,	n	1,	C-N
ALS	1,	C	1,	C	1,	C-C
ILS	1,	I	1,	I	1,	I'-k-LS
ILS	1,	I	x,	Not I	1,	I'-u-LS
ILS	x,	Not I	1,	I	1,	I'-u-LS
ILS	x,	Not I	x,	Not I	1,	I'-u-LS
Stuff Byte during ILS	x,	x	x,	x	1,	I'-k-ILS
Not ALS and Not ILS	1,	M	1,	M	1,	V'-k-LS
Not ALS and Not ILS	1,	M	x,	Not M	1,	V'-u-LS
Not ALS and Not ILS	x,	Not M	1,	M	1,	V'-u-LS
Not ALS and Not ILS	x,	Not M	x,	Not M	1,	V'-u-LS
Stuff Byte during Not ILS	x,	x	x,	x	1,	V'-k-LS, V'-u-LS or I'-u-ILS
EB Overflow/Underflow					1,	0011 1011
SMT PI Connnection (LSU)					1,	0011 1010

Where:
n = Any data symbol in {0, 1, 2, ... F}
C = Any control symbol in {V, R, S, T, I, H}
N = 0000 = Code for data symbol in a data control mixture byte
I = Idle Symbol
M = Any symbol that matches the current line state
I' = 1011 = First symbols of the byte in Idle Line State
V' = 0011 = PHY Invalid
LS = Line State
ALS = 000
ILS = 001
NSD = 010
MLS = 100
HLS = 101
QLS = 110
NLS = 111
u = 1 = Indicates symbol received does not match current line state
k = 0 = Indicates symbol received matches current line state
x = Don't care

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8.0 Detailed Descriptions (Continued)

Example:

Incoming 5B Code	Decoded 4B Code	National Byte-Wide Code (w/o parity)
98765 43210	C3210 C 3210	C 7653 3210
11111 11111 (II)	1 1010 1 1010 (II)	1 1011 0001 (I'-k-ILS)*
11111 11111 (II)	1 1010 1 1010 (II)	1 1011 0001 (I'-k-ILS)
11111 11111 (II)	1 1010 1 1010 (II)	1 1011 0001 (I'-k-ILS)
11000 10001 (JK)	1 1101 1 1101 (JK)	1 1101 1101 (JK Symbols)
----- ----- (xx)	0 - - - - 0 - - - - (xx)	0 - - - - - - - - (Data Symbols)
----- ----- (xx)	0 - - - - 0 - - - - (xx)	0 - - - - - - - - (Data Symbols)
----- ----- (xx)	0 - - - - 0 - - - - (xx)	0 - - - - - - - - (Data Symbols)
(More data ...)		
----- ----- (xx)	0 - - - - 0 - - - - (xx)	0 - - - - - - - - (Data Symbols)
----- ----- (xx)	0 - - - - 0 - - - - (xx)	0 - - - - - - - - (Data Symbols)
----- ----- (xx)	0 - - - - 0 - - - - (xx)	0 - - - - - - - - (Data Symbols)
01101 00111 (TR)	1 0101 1 0110 (TR)	1 0101 0110 (T and R Symbols)
00111 00111 (RR)	1 0110 1 0110 (RR)	1 0110 0110 (Two R Symbols)
11111 11111 (II)	1 1010 1 1010 (II)	1 1010 1010 (Idle Symbols)
11111 11111 (II)	1 1010 1 1010 (II)	1 1010 1010 (Idle Symbols)
11111 11111 (II)	1 1010 1 1010 (II)	1 1011 0001 (I'-k-ILS)
11111 11111 (II)	1 1010 1 1010 (II)	1 1011 0001 (I'-k-ILS)
11111 11111 (II)	1 1010 1 1010 (II)	1 1011 0001 (I'-k-ILS)
00100 00100 (HH)	1 0001 1 0001 (HH)	1 1011 1001 (I'-u-ILS)
00100 00100 (HH)	1 0001 1 0001 (HH)	1 1011 1001 (I'-u-ILS)
00100 00100 (HH)	1 0001 1 0001 (HH)	1 1011 1001 (I'-u-ILS)
00100 00100 (HH)	1 0001 1 0001 (HH)	1 1011 1001 (I'-u-ILS)
00100 00100 (HH)	1 0001 1 0001 (HH)	1 1011 1001 (I'-u-ILS)
00100 00100 (HH)	1 0001 1 0001 (HH)	1 1011 1001 (I'-u-ILS)
00100 00100 (HH)	1 0001 1 0001 (HH)	1 1011 1001 (I'-u-ILS)
00100 00100 (HH)	1 0001 1 0001 (HH)	1 0011 0101 (V'-k-HLS)
00100 00100 (HH)	1 0001 1 0001 (HH)	1 0011 0101 (V'-k-HLS)
00100 00100 (HH)	1 0001 1 0001 (HH)	1 0011 0101 (V'-k-HLS)
11111 11111 (II)	1 1010 1 1010 (II)	1 0011 1101 (V'-u-HLS)
11111 11111 (II)	1 1010 1 1010 (II)	1 1011 0001 (I'-k-ILS)
11111 11111 (II)	1 1010 1 1010 (II)	1 1011 0001 (I'-k-ILS)

*Assume the receiver is in the Idle Line State.

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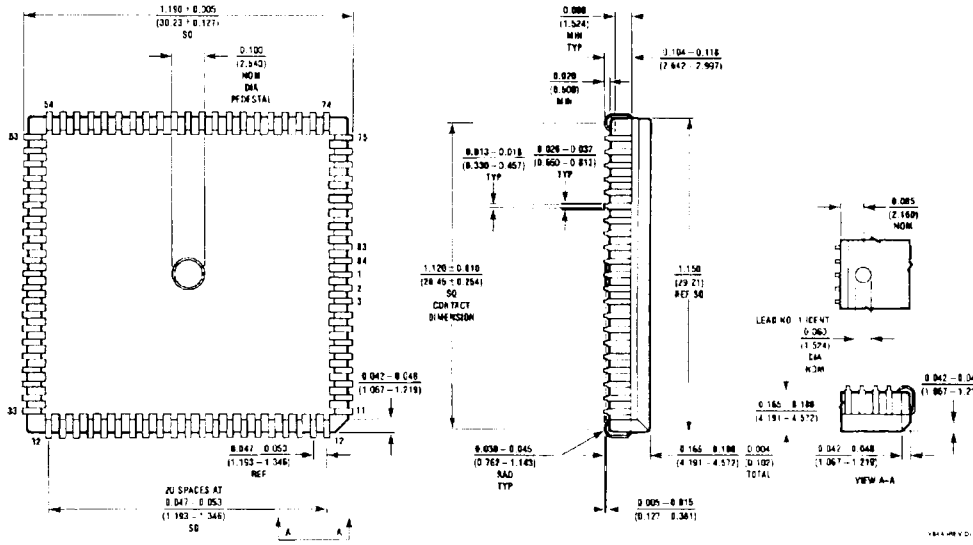
Physical Dimensions inches (millimeters)



Plastic Leaded Chip Carrier
Order Number DP83251V
NS Package Number V84A

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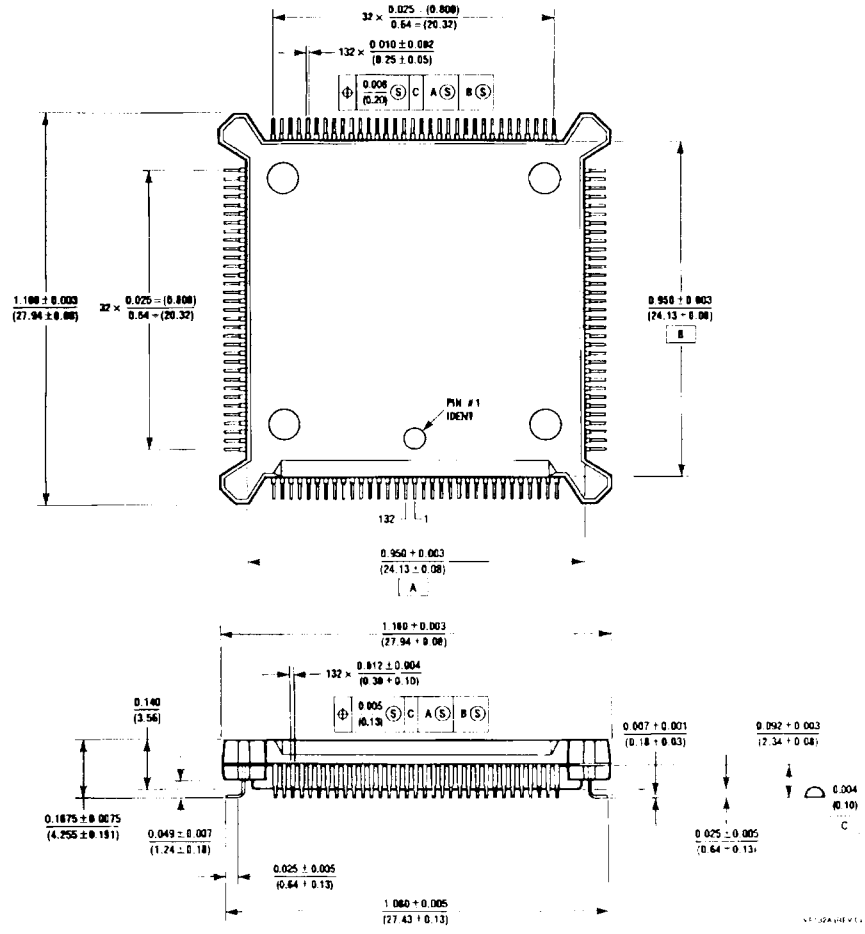
Physical Dimensions inches (millimeters) (Continued)



Plastic Quad Pack (VF)
Order Number DP83255AVF
NS Package Number VF132A

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