

**PRELIMINARY**  
 Notice: This is not a final specification. Some  
 parameter limits are Subject to change.

# MITSUBISHI HIGH SPEED CMOS M74HC646P/FP/DWP

## OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER AND D-TYPE FLIP-FLOP

### DESCRIPTION

The M74HC646 is a semiconductor integrated circuit consisting of eight bus transceivers with noninverted outputs.

### FEATURES

- High-fanout 3-state outputs ( $I_{OL}=6\text{mA}$ ,  $I_{OH}=-6\text{mA}$ )
- High-speed: 70MHz clock frequency typ.  
 ( $C_L=50\text{pF}$ ,  $V_{CC}=5\text{V}$ )
- Low power dissipation:  $20\mu\text{W}/\text{package}$ , max  
 ( $V_{CC}=5\text{V}$ ,  $T_a=25^\circ\text{C}$ , quiescent state)
- High noise margin: 30% of  $V_{CC}$ , min ( $V_{CC}=4.5\text{V}$ ,  $6\text{V}$ )
- Capable of driving 15 74LSTTL loads
- Wide operating voltage range:  $V_{CC}=2\sim 6\text{V}$
- Wide operating temperature range:  $T_a=-40\sim +85^\circ\text{C}$

### APPLICATION

General purpose, for use in industrial and consumer digital equipment.

### FUNCTIONAL DESCRIPTION

Use of silicon gate technology allows the M74HC646 to maintain of the low power dissipation and high noise margin the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS646.

The M74HC646 consists of eight bidirectional buffers by interconnecting the I/O buffers of two D-type flip flops with 3-state noninverted outputs. The I/O direction is controlled by output-enable input  $\overline{OE}$  and direction input DIR. The signals are routed from input to output or from the flip flop to output by source select inputs  $S_{AB}$  and  $S_{BA}$ .

None of the signals are inverted.

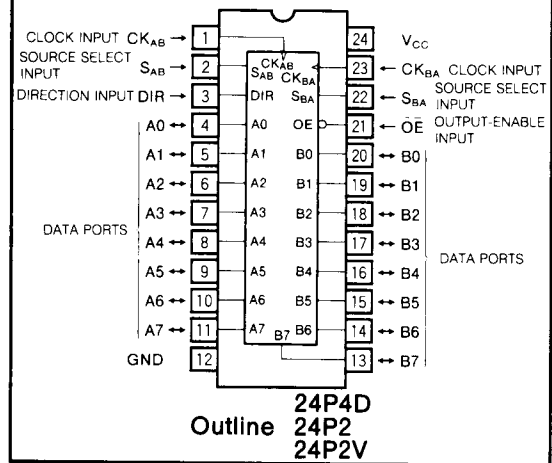
When  $\overline{OE}$  is low and DIR is high, the data ports A will become input terminals and the data ports B will become output terminals. When  $S_{AB}$  goes low, the signal A, which was stored in flip flop (A) as  $Q_A$  when  $S_{AB}$  was high, appears at B. When  $S_{AB}$  is held low and when clock input  $CK_{AB}$  changes from low to high, the signal present at A is stored in flip flop (A). When  $S_{AB}$  is held high and when  $CK_{AB}$  changes from low to high, the signal present at A is inverted and stored in flip flop (A). At the same time, the signal  $Q_A$  which was stored in flip flop (A), appears at B.

When  $\overline{OE}$  and DIR are both low, the I/O direction is reversed: B will become input terminals and A will become output terminals. When  $S_{BA}$  goes low, the signal B, which was stored in flip flop (B) as  $Q_B$  when  $S_{BA}$  was high, appears at A. When  $S_{BA}$  is held low and clock input  $CK_{BA}$  changes from low to high, the signal present at B is stored in flip flop (B).

When  $S_{BA}$  is held high and  $CK_{BA}$  changes from low to high, the signal present at B is stored in flip flop (B). At the same time, the signal  $Q_B$  which was stored in flip flop (B), appears at A.

When  $\overline{OE}$  is high, both A and B will become high impedance state and they will be separated. When  $CK_{AB}$

### PIN CONFIGURATION (TOP VIEW)



changes from low to high, the signal present at A is stored in flip flop (A). When  $CK_{BA}$  changes from low to high, the signal present at B is stored in flip flop (B).

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER AND D-TYPE FLIP-FLOP

FUNCTION TABLE (Note 1)

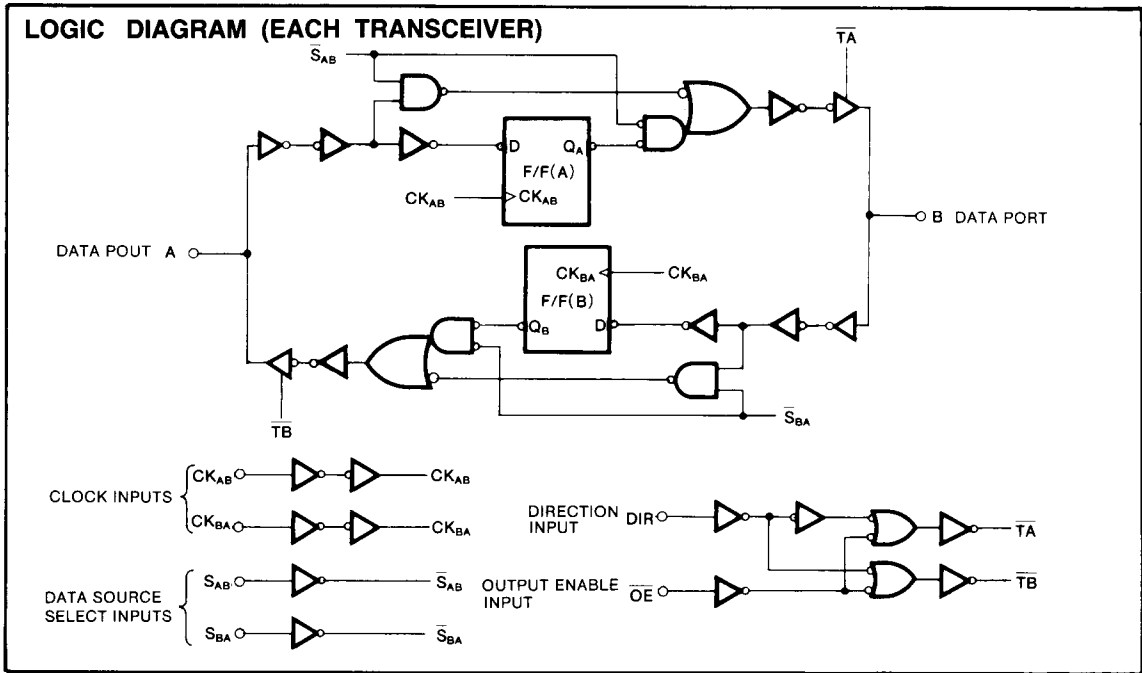
Control inputs						Data ports		Flip flop		Operational description	
OE	DIR	CK <sub>AB</sub>	CK <sub>BA</sub>	S <sub>AB</sub>	S <sub>BA</sub>	A	B	Q <sub>A</sub> <sup>0</sup>	Q <sub>B</sub> <sup>0</sup>		
H	X	X	X	X	X	X		X	Q <sub>A</sub> <sup>0</sup>	Q <sub>B</sub> <sup>0</sup>	The output of data ports A and B are disabled.
H	X	↑	X	X	X	L		X	Q <sub>A</sub> <sup>0</sup>	X	Data ports A and B are stroed by the flip flops at the rising edge of CK <sub>AB</sub> and CK <sub>BA</sub> . The output of data ports A and B is disabled.
H	X	↑	X	X	X	H	I	X	Q <sub>A</sub> <sup>0</sup>	X	
H	X	X	↑	X	X	X		L	X	Q <sub>B</sub> <sup>0</sup>	
H	X	X	↑	X	X	X		H	X	Q <sub>B</sub> <sup>0</sup>	
L	H	X	X*	L	X	L		L	Q <sub>A</sub> <sup>0</sup>	Q <sub>B</sub> <sup>0</sup>	
L	H	X	X*	L	X	H		H	Q <sub>A</sub> <sup>0</sup>	Q <sub>B</sub> <sup>0</sup>	1) When S <sub>AB</sub> is low, data port A appears at data port B. The state of the flip flop (A) is unchanged.
L	H	X	X*	H	X	X		Q <sub>A</sub> <sup>0</sup>	Q <sub>A</sub> <sup>0</sup>	Q <sub>B</sub> <sup>0</sup>	2) When S <sub>AB</sub> is high, the output of flip flop (A) appears at data port B.
L	H	↑	X*	L	X	L	I	L	Q <sub>A</sub> <sup>0</sup>	Q <sub>B</sub> <sup>0</sup>	3) When S <sub>AB</sub> is low, the data port A appears at data port B and is stored in flip flop (A) at the rising edge of CK <sub>AB</sub> .
L	H	↑	X*	L	X	H		H	Q <sub>A</sub> <sup>0</sup>	Q <sub>B</sub> <sup>0</sup>	
L	H	↑	X*	H	X	L		Q <sub>A</sub> <sup>0</sup>	Q <sub>A</sub> <sup>0</sup>	Q <sub>B</sub> <sup>0</sup>	4) When S <sub>AB</sub> is high, the data port A is stored in flip flop (A) at the rising edge of CK <sub>AB</sub> , and the output of flip flop (A) appears at data port B.
L	H	↑	X*	H	X	H		Q <sub>A</sub> <sup>0</sup>	Q <sub>A</sub> <sup>0</sup>	Q <sub>B</sub> <sup>0</sup>	
L	L	X*	X	X	L	L		L	Q <sub>A</sub> <sup>0</sup>	Q <sub>B</sub> <sup>0</sup>	The output of data port A is enabled. (Note 3)
L	L	X*	X	X	L	H		H	Q <sub>A</sub> <sup>0</sup>	Q <sub>B</sub> <sup>0</sup>	
L	L	X*	X	X	H	Q <sub>B</sub> <sup>0</sup>		X	Q <sub>A</sub> <sup>0</sup>	Q <sub>B</sub> <sup>0</sup>	2) When S <sub>BA</sub> is high, the output of flip flop (B) appears at data port A.
L	L	X*	↑	X	L	L	O	L	Q <sub>A</sub> <sup>0</sup>	Q <sub>B</sub> <sup>0</sup>	3) When S <sub>BA</sub> is low, the data port B appears at data port A and is stored is flip flop (B) at the rising edge of CK <sub>AB</sub> .
L	L	X*	↑	X	L	H		H	Q <sub>A</sub> <sup>0</sup>	Q <sub>B</sub> <sup>0</sup>	
L	L	X*	↑	X	H	Q <sub>B</sub> <sup>0</sup>		L	Q <sub>A</sub> <sup>0</sup>	Q <sub>B</sub> <sup>0</sup>	4) When S <sub>BA</sub> is high, the data port B is stored in flip flop (B) and the output of flip flop (B) appears at data port A.
L	L	X*	↑	X	H	Q <sub>B</sub> <sup>0</sup>		H	Q <sub>A</sub> <sup>0</sup>	Q <sub>B</sub> <sup>0</sup>	

Note 1 : X : Irrelevant  
 ↑ : Change from low to high  
 Q<sub>A</sub><sup>0</sup>, Q<sub>B</sub><sup>0</sup> : Output state of flip flops before the rise of CK<sub>AB</sub> and CK<sub>BA</sub>.  
 I : Input terminal of data port  
 O : Output terminal of data port  
 \* : As CK<sub>AB</sub> and CK<sub>BA</sub> are not selected by the I/O directional signal, data from data ports A and B can be stored in the corresponding flip flops at the rising edge of CK<sub>AB</sub> or CE<sub>BA</sub>.

Note 2 : The output at port B is given by :  
 $B = (A \cdot S_{AB}) + (Q_A \cdot S_{AB})$

Note 3 : The output at port B is given by:  
 $A = (B \cdot S_{BA}) + (Q_B \cdot S_{BA})$

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**ABSOLUTE MAXIMUM RATINGS** ( $T_a = -40 \sim +85^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC}$	Supply voltage		$-0.5 \sim +7.0$	V
$V_i$	Input voltage		$-0.5 \sim V_{CC} + 0.5$	V
$V_o$	Output voltage		$-0.5 \sim V_{CC} + 0.5$	V
$I_{IK}$	Input protection diode current	$V_i < 0V$	-20	mA
		$V_i > V_{CC}$	20	
$I_{OK}$	Output parasitic diode current	$V_o < 0V$	-20	mA
		$V_o > V_{CC}$	20	
$I_o$	Output current per output pin		$\pm 35$	mA
$I_{CC}$	Supply/GND current	$V_{CC}$ , GND	$\pm 75$	mA
$P_d$	Power dissipation	(Note 4)	500	mW
$T_{stg}$	Storage temperature range		$-65 \sim +150$	$^\circ\text{C}$

Note 4 : M74HC646FP,  $T_a = -40 \sim +80^\circ\text{C}$  and  $T_a = 80 \sim 85^\circ\text{C}$  are derated at  $-7\text{mW}/^\circ\text{C}$ .  
M74HC646DWP,  $T_a = -40 \sim +80^\circ\text{C}$  and  $T_a = 80 \sim 85^\circ\text{C}$  are derated at  $-7\text{mW}/^\circ\text{C}$ .

**RECOMMENDED OPERATING CONDITIONS** ( $T_a = -40 \sim +85^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$V_{CC}$	Supply voltage	2		6	V
$V_i$	Input voltage	0		$V_{CC}$	V
$V_o$	Output voltage	0		$V_{CC}$	V
$T_{opr}$	Operating temperature range	-40		+85	$^\circ\text{C}$
$t_r, t_f$	Input risetime, falltime	$V_{CC} = 2.0V$	0	1000	ns
		$V_{CC} = 4.5V$	0	500	
		$V_{CC} = 6.0V$	0	400	

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER AND D-TYPE FLIP-FLOP

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits					Unit	
			V <sub>CC</sub> (V)	25°C			-40~+85°C		
				Min	Typ	Max	Min		Max
V <sub>IH</sub>	High-level input voltage	V <sub>O</sub> = 0.1V, V <sub>CC</sub> = 0.1V  I <sub>O</sub>   = 20μA	2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2	V	
V <sub>IL</sub>	Low-level input voltage	V <sub>O</sub> = 0.1V, V <sub>CC</sub> = 0.1V  I <sub>O</sub>   = 20μA	2.0 4.5 6.0			0.5 1.35 1.8	0.5 1.35 1.8	V	
V <sub>OH</sub>	High-level output voltage	V <sub>I</sub> = V <sub>IH</sub> , V <sub>IL</sub>	I <sub>OH</sub> = -20μA	2.0	1.9		1.9	V	
			I <sub>OH</sub> = -20μA	4.5	4.4		4.4		
			I <sub>OH</sub> = -20μA	6.0	5.9		5.9		
			I <sub>OH</sub> = -6.0mA	4.5	4.18		4.13		
			I <sub>OH</sub> = -7.8mA	6.0	5.68		5.63		
V <sub>OL</sub>	Low-level output voltage	V <sub>I</sub> = V <sub>IH</sub> , V <sub>IL</sub>	I <sub>OL</sub> = 20μA	2.0			0.1	0.1	V
			I <sub>OL</sub> = 20μA	4.5			0.1	0.1	
			I <sub>OL</sub> = 20μA	6.0			0.1	0.1	
			I <sub>OL</sub> = 6.0mA	4.5			0.26	0.33	
			I <sub>OL</sub> = 7.8mA	6.0			0.26	0.33	
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = 6V	6.0			0.1	1.0	μA	
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> = 0V	6.0			-0.1	-1.0	μA	
I <sub>OZH</sub>	Off-state high-level output current	V <sub>I</sub> = V <sub>IH</sub> , V <sub>IL</sub> , V <sub>O</sub> = V <sub>CC</sub>	6.0			0.5	5.0	μA	
I <sub>OZL</sub>	Off-state low-level output current	V <sub>I</sub> = V <sub>IH</sub> , V <sub>IL</sub> , V <sub>O</sub> = GND	6.0			-0.5	-5.0	μA	
I <sub>CC</sub>	Quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> , GND, I <sub>O</sub> = 0μA	6.0			4.0	40.0	μA	

SWITCHING CHARACTERISTICS (V<sub>CC</sub> = 5V, T<sub>a</sub> = 25°C)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
f <sub>max</sub>	Maximum clock frequency	C <sub>L</sub> = 50pF (Note 6)	30			MHz	
t <sub>TLH</sub>	Low-level to high-level and high-level to low-level output transition time	C <sub>L</sub> = 50pF (Note 6)			10	ns	
t <sub>THL</sub>					10	ns	
t <sub>PLH</sub>	Low-level to high-level and high-level to low-level output propagation time (A - B, B - A)				30	ns	
t <sub>PHL</sub>					30	ns	
t <sub>PLH</sub>	Low-level to high-level and high-level to low-level output propagation time (CK <sub>AB</sub> - B, CK <sub>BA</sub> - A)				40	ns	
t <sub>PHL</sub>					40	ns	
t <sub>PLH</sub>	Low-level to high-level and high-level to low-level output propagation time (S <sub>AB</sub> - B, S <sub>BA</sub> - A)				30	ns	
t <sub>PHL</sub>					30	ns	
t <sub>PLZ</sub>	Output disable time from low-level and high-level (DIR - A, B)		C <sub>L</sub> = 5pF (Not 6)			30	ns
t <sub>PHZ</sub>	Output enable time to low-level and high-level (DIR - A, B)		C <sub>L</sub> = 50pF (Note 6)			30	ns
t <sub>PZL</sub>	Output disable time from low-level and high-level (OE - A, B)	C <sub>L</sub> = 50pF (Note 6)			33	ns	
t <sub>PZH</sub>					33	ns	
t <sub>PLZ</sub>	Output enable time to low-level and high-level (OE - A, B)	C <sub>L</sub> = 5pF (Note 6)			30	ns	
t <sub>PZH</sub>					30	ns	
t <sub>PZL</sub>	Output enable time to low-level and high-level (OE - A, B)	C <sub>L</sub> = 50pF (Note 6)			33	ns	
t <sub>PZH</sub>					33	ns	

**MITSUBISHI HIGH SPEED CMOS**  
**M74HC646P/FP/DWP**

**OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER AND D-TYPE FLIP-FLOP**

**SWITCHING CHARACTERISTICS** ( $V_{CC} = 2\sim 6V$ ,  $T_a = -40\sim +85^\circ C$ )

Symbol	Parameter	Test conditions	Limits						Unit
			$V_{CC}(V)$	25°C			-40~+85°C		
				Min	Typ	Max	Min	Max	
$f_{max}$	Maximum clock frequency		2.0	5			4		MHz
			4.5	27			21		
			6.0	32			25		
$t_{TLH}$	Low-level to high-level and high-level to low-level		2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
$t_{THL}$	output transition time	$C_L = 50pF$ (Note 6)	2.0			60		75	ns
			4.5			12		15	
			6.0			10		13	
$t_{PLH}$			2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
$t_{PHL}$	Low-level to high-level and high-level to low-level		2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
$t_{PLH}$	output propagation time (A - B, B - A)	$C_L = 150pF$ (Note 6)	2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
$t_{PHL}$			2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
$t_{PLH}$	Low-level to high-level and high-level to low-level	$C_L = 50pF$ (Note 6)	2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
$t_{PLH}$	output propagation time ( $CK_{AB} - B$ , $CK_{BA} - A$ )	$C_L = 150pF$ (Note 6)	2.0			270		340	ns
			4.5			54		68	
			6.0			46		58	
$t_{PHL}$			2.0			270		340	ns
			4.5			54		68	
			6.0			46		58	
$t_{PLH}$	Low-level to high-level and high-level to low-level	$C_L = 50pF$ (Note 6)	2.0			170		214	ns
			4.5			34		43	
			6.0			29		36	
$t_{PHL}$	output propagation time ( $S_{AB} - B$ , $S_{BA} - A$ )	$C_L = 150pF$ (Note 6)	2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
$t_{PHL}$			2.0			220		277	ns
			4.5			44		55	
			6.0			37		47	
$t_{PLZ}$	Output disable time from low-level and high-level	$C_L = 50pF$ (Note 6)	2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	
$t_{PHZ}$	(DIR - A, B)		2.0			175		221	ns
			4.5			35		44	
			6.0			30		37	

OCTAL 3-STATE NONINVERTING BUS TRANSCEIVER AND D-TYPE FLIP-FLOP

SWITCHING CHARACTERISTICS ( $V_{CC} = 2\sim 6V$ ,  $T_A = -40\sim +85^\circ C$ )

Symbol	Parameter	Test conditions	Limits					Unit			
			$V_{CC}(V)$	25°C			-40~+85°C				
				Min	Typ	Max	Min		Max		
$t_{PZL}$	Output enable time to low-level and high-level (DIR - A, B)	$C_L = 50pF$ (Note 6)	2.0			175		221	ns		
			4.5			35		44			
			6.0			30		37			
$t_{PZH}$			$C_L = 150pF$ (Note 6)	2.0			175			221	ns
				4.5			35			44	
				6.0			30			37	
$t_{PZL}$	Output disable time from low-level and high-level ( $\overline{OE} - A, B$ )	$C_L = 50pF$ (Note 6)		2.0			225		284	ns	
				4.5			45		57		
				6.0			38		48		
$t_{PZH}$			$C_L = 150pF$ (Note 6)	2.0			225		284		ns
				4.5			45		57		
				6.0			38		48		
$t_{PLZ}$	Output enable time to low-level and high-level ( $\overline{OE} - A, B$ )	$C_L = 50pF$ (Note 6)		2.0			175		221	ns	
				4.5			35		44		
				6.0			30		37		
$t_{PHZ}$			$C_L = 150pF$ (Note 6)	2.0			175		221		ns
				4.5			35		44		
				6.0			30		37		
$t_{PZL}$	Output enable time to low-level and high-level ( $\overline{OE} - A, B$ )	$C_L = 50pF$ (Note 6)		2.0			175		221	ns	
				4.5			35		44		
				6.0			30		37		
$t_{PZH}$			$C_L = 150pF$ (Note 6)	2.0			175		221		ns
				4.5			35		44		
				6.0			30		37		
$t_{PZL}$	Output enable time to low-level and high-level ( $\overline{OE} - A, B$ )	$C_L = 50pF$ (Note 6)		2.0			225		284	ns	
				4.5			45		57		
				6.0			38		48		
$t_{PZH}$			$C_L = 150pF$ (Note 6)	2.0			225		284		ns
				4.5			45		57		
				6.0			38		48		
$C_I$	Input capacitance					10		10	pF		
$C_O$	Off-state output capacitance	$\overline{OE} = V_{CC}$				15		15	pF		
$C_{PD}$	Power dissipation capacitance (Note 5)								pF		

Note 5 :  $C_{PD}$  is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per flip flop)

The power dissipation during operation under no-load conditions is calculated using the following formula:

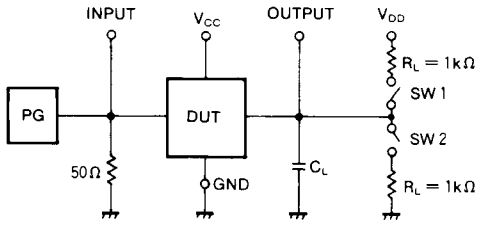
$$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_t + I_{CC} \cdot V_{CC}$$

TIMING REQUIREMENTS ( $V_{CC} = 2\sim 6V$ ,  $T_A = -40\sim +85^\circ C$ )

Symbol	Parameter	Test conditions	Limits					Unit	
			$V_{CC}(V)$	25°C			-40~+85°C		
				Min	Typ	Max	Min		Max
$t_w$	CK <sub>AB</sub> , CK <sub>BA</sub> pulse width		2.0	80			101	ns	
			4.5	16			20		
			6.0	14			17		
$t_{su}$	A, B setup time with respect to CK <sub>AB</sub> , CK <sub>BA</sub>		2.0	100			125	ns	
			4.5	20			25		
			6.0	17			21		
$t_h$	A, B hold time with respect to CK <sub>AB</sub> , CK <sub>BA</sub>		2.0	0			0	ns	
			4.5	0			0		
			6.0	0			0		

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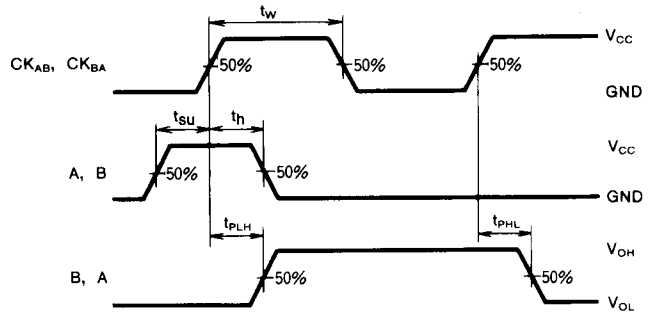
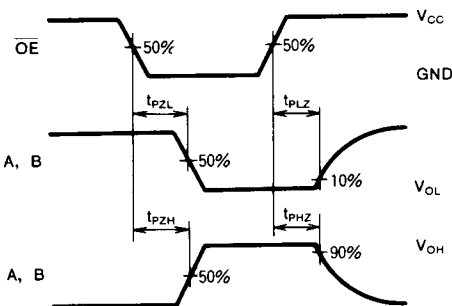
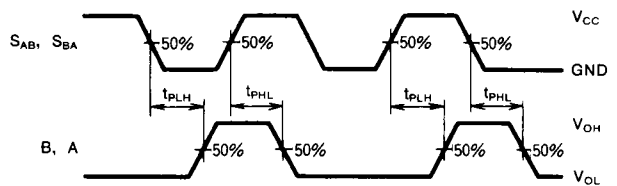
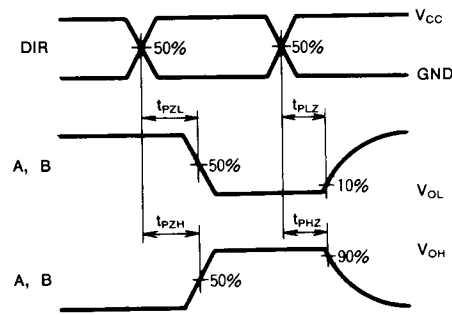
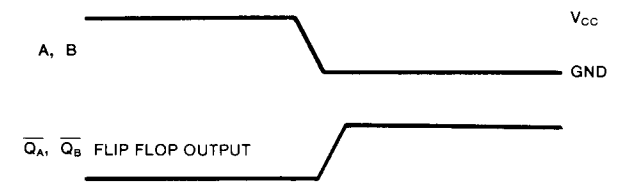
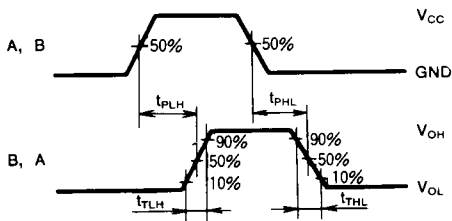
Note 6 : Test Circuit



Parameter	SW 1	SW 2
$t_{TLH}, t_{THL}$	Open	Open
$t_{PLH}, t_{PHL}$	Closed	Open
$t_{PHZ}$	Open	Closed
$t_{PZL}$	Closed	Open
$t_{PZH}$	Open	Closed

- (1) The pulse generator (PG) has the following characteristics (10%~90%):  $t_r = 6ns$ ,  $t_f = 6ns$
- (2) The capacitance  $C_L$  includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM



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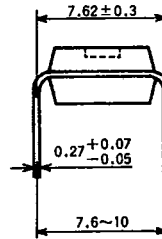
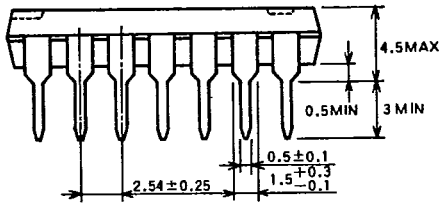
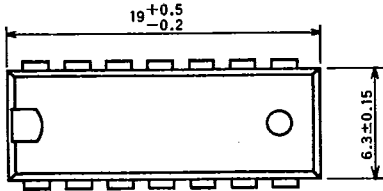
6249827 MITSUBISHI (DGTL LOGIC)

91D 12849

D T-90-20

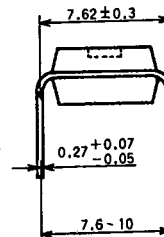
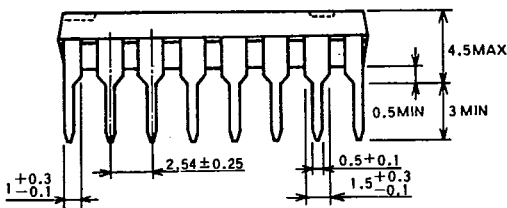
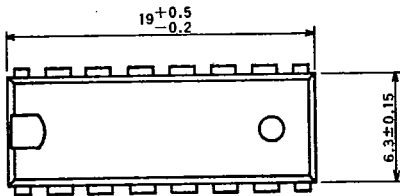
TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIP

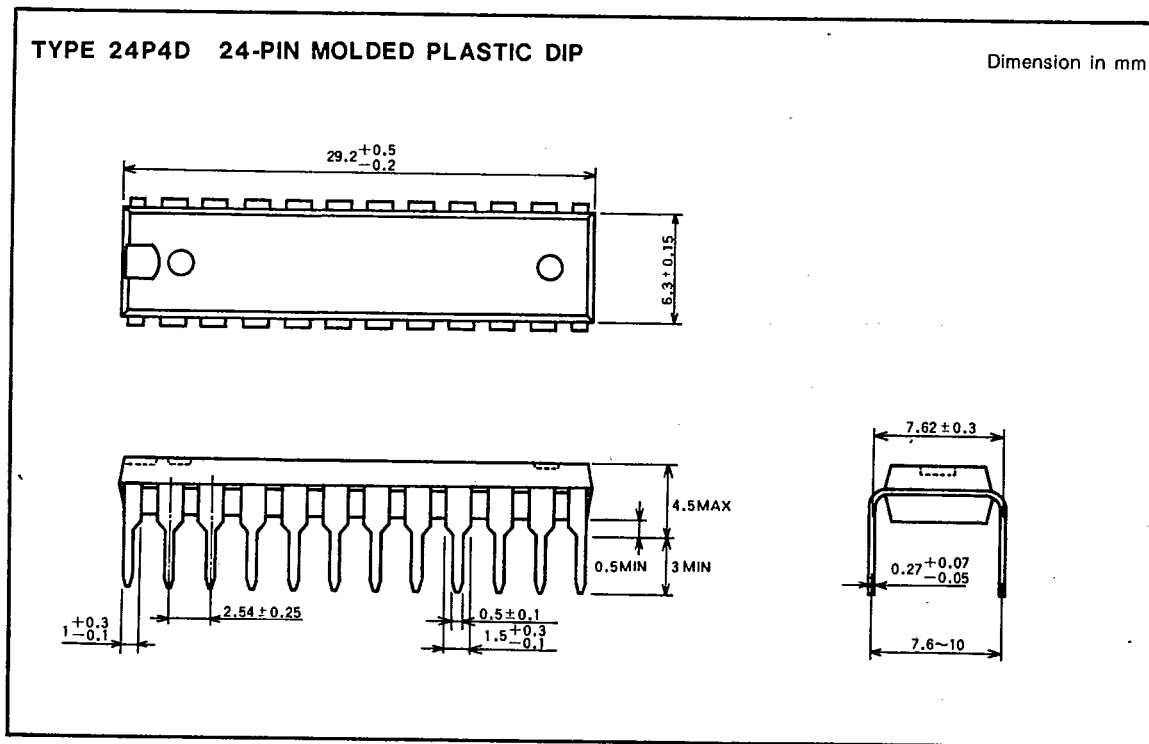
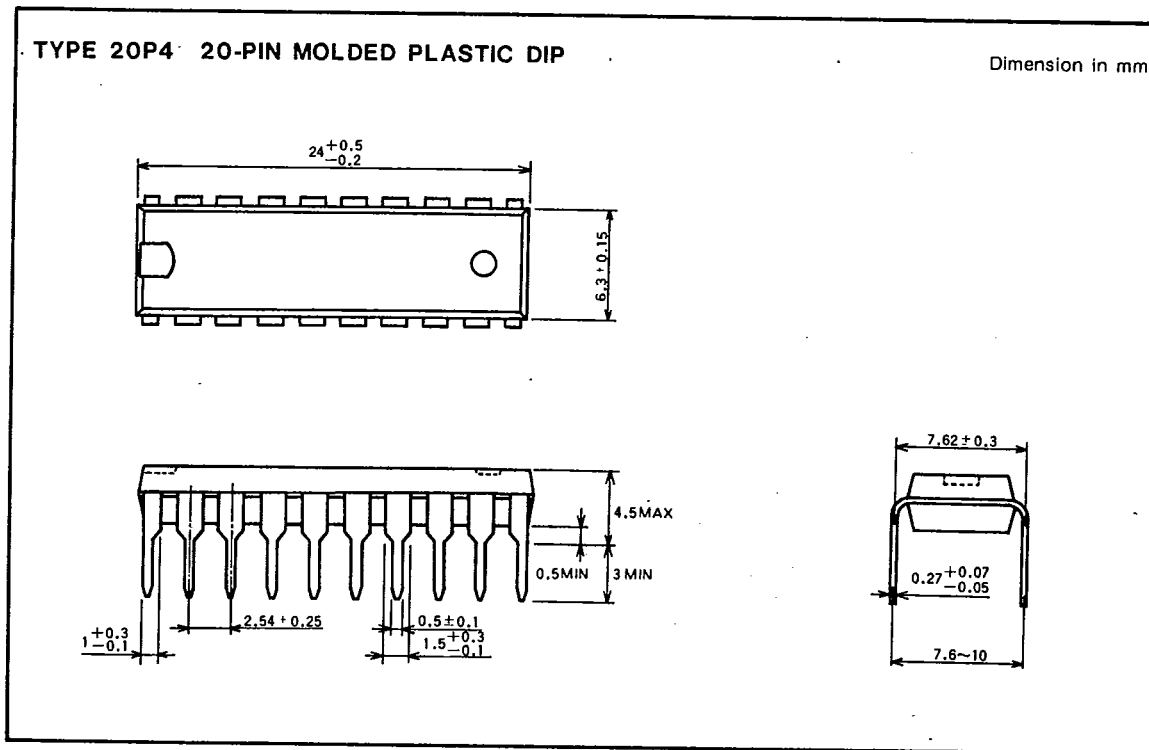
Dimension in mm



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**PACKAGE OUTLINES**

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91D 12850 D.T-90-20



2933

G-02

1-52

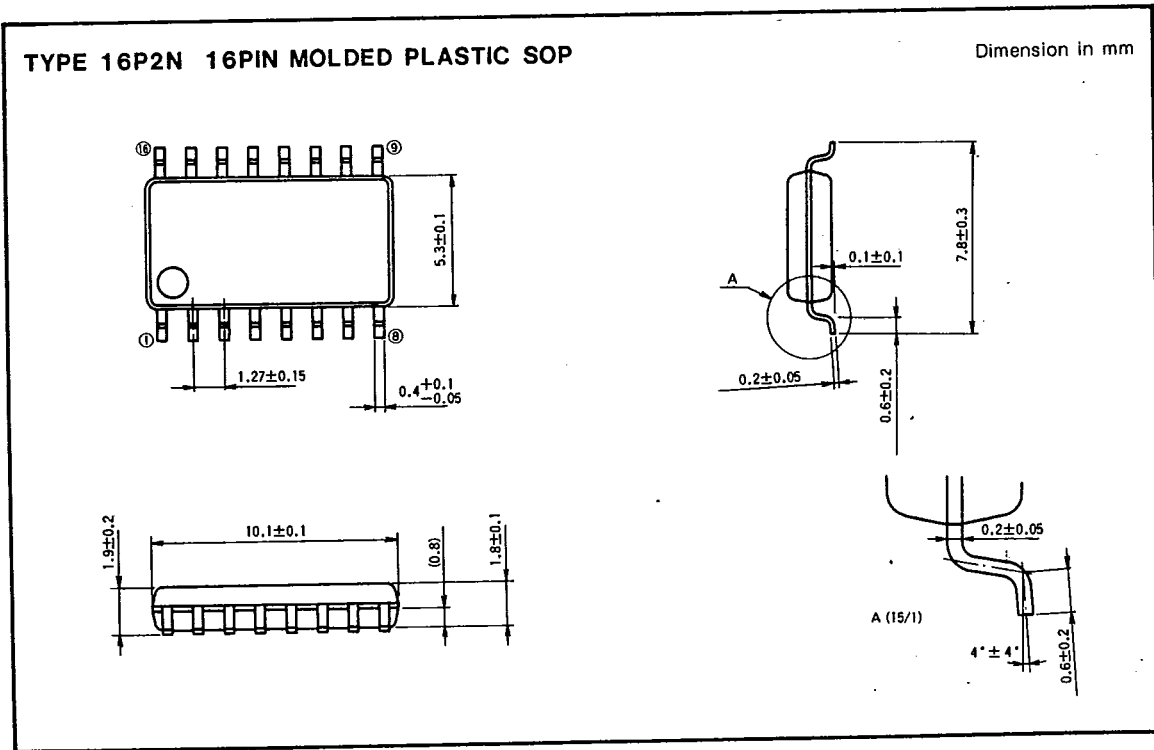
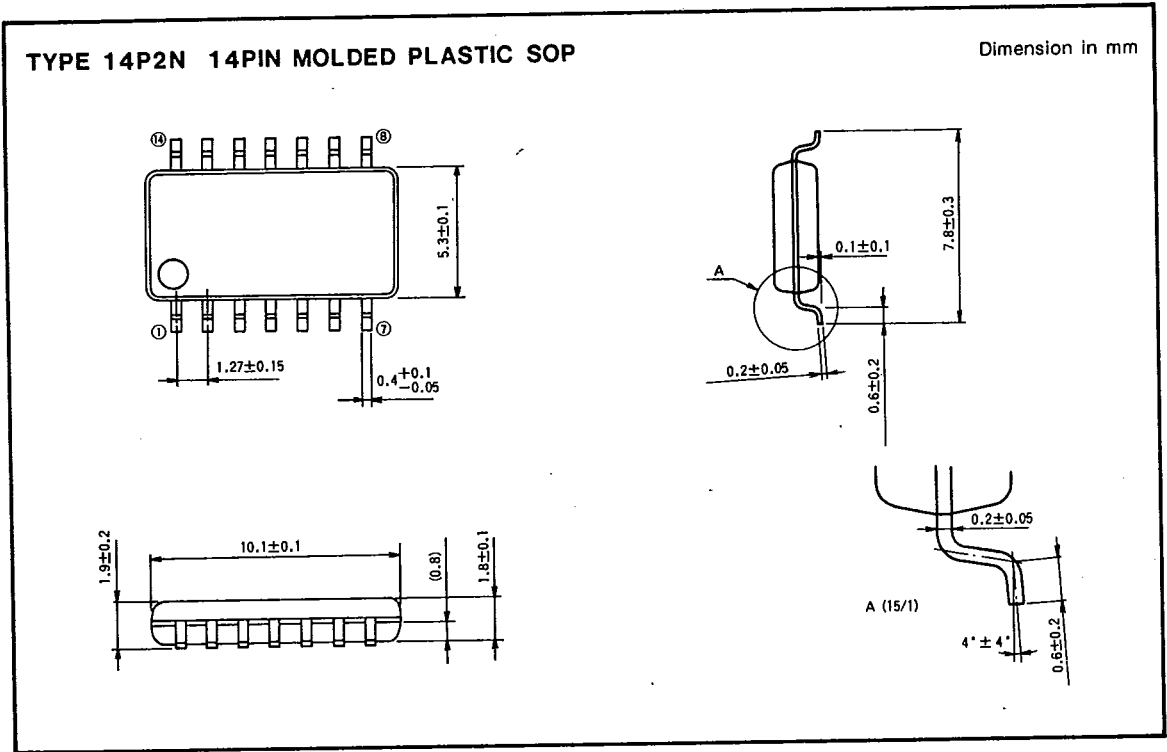


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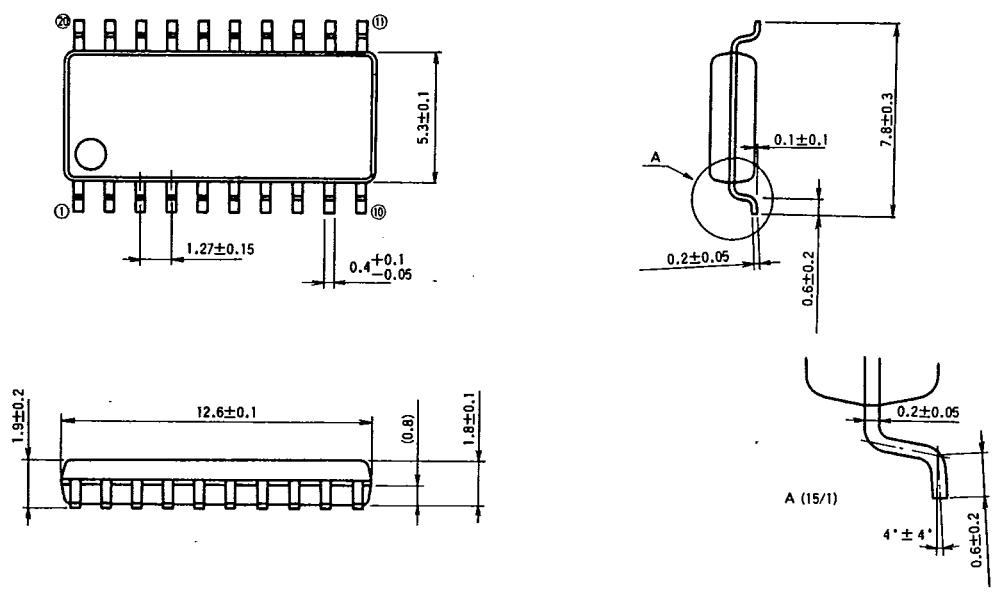
6249827 MITSUBISHI (DGTL LOGIC)

91D 12851 D T-90.20



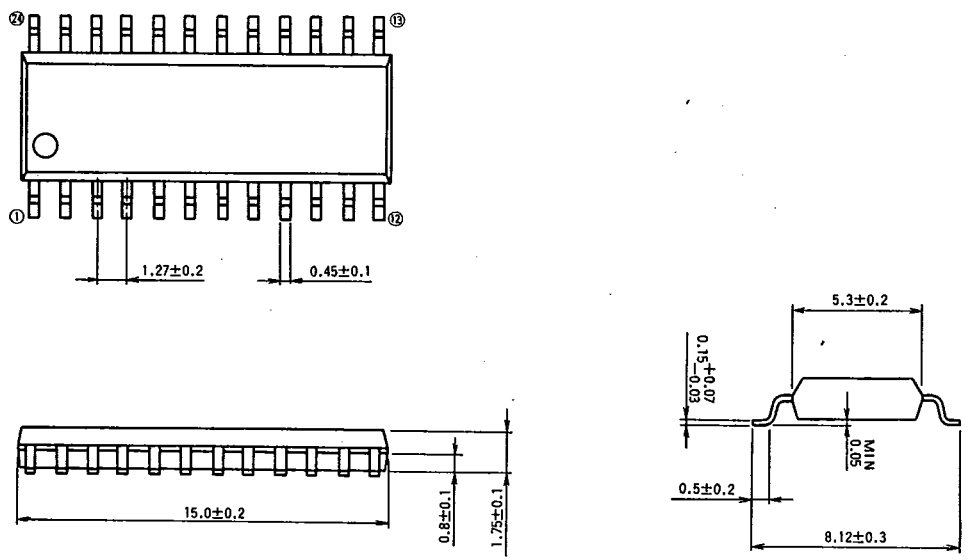
TYPE 20P2N 20PIN MOLDED PLASTIC SOP

Dimension in mm



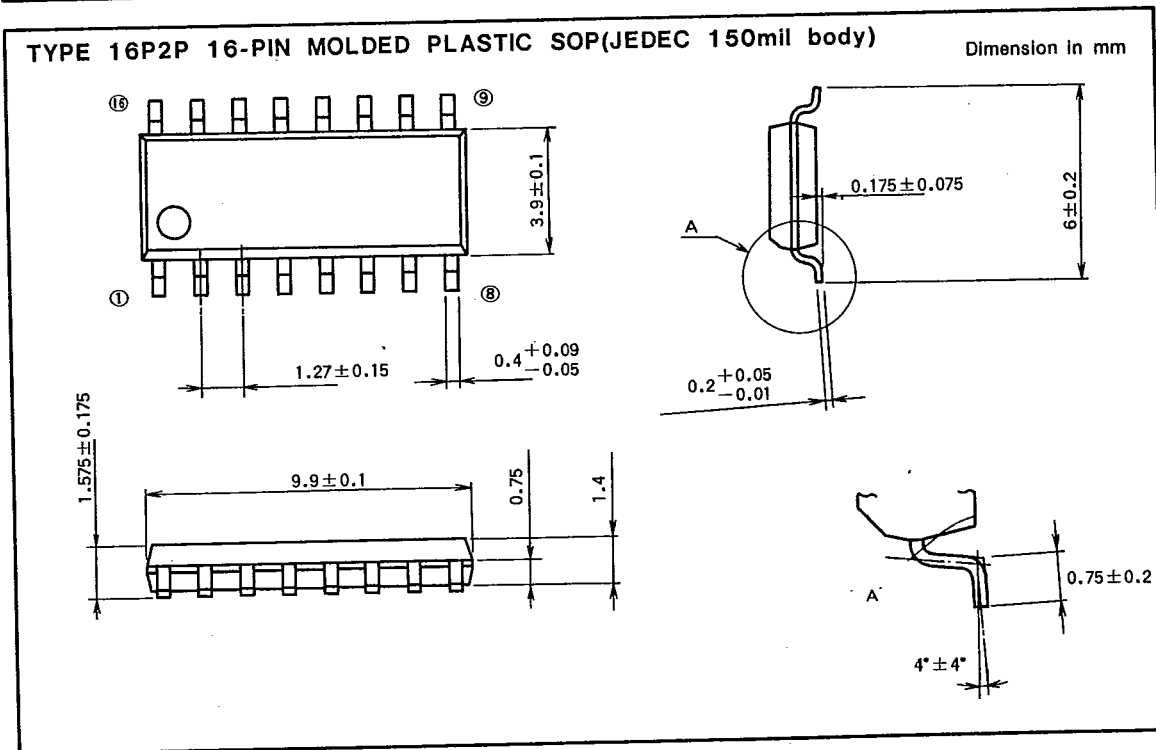
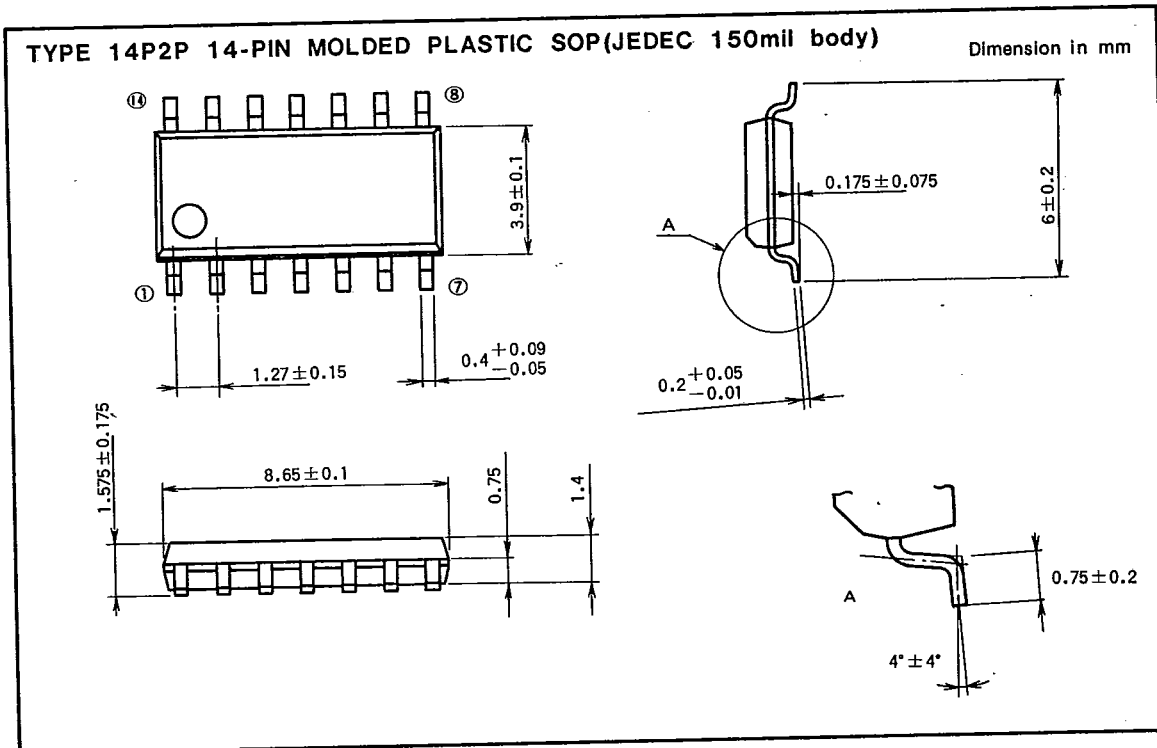
TYPE 24P2 24PIN MOLDED PLASTIC SOP

Dimension in mm



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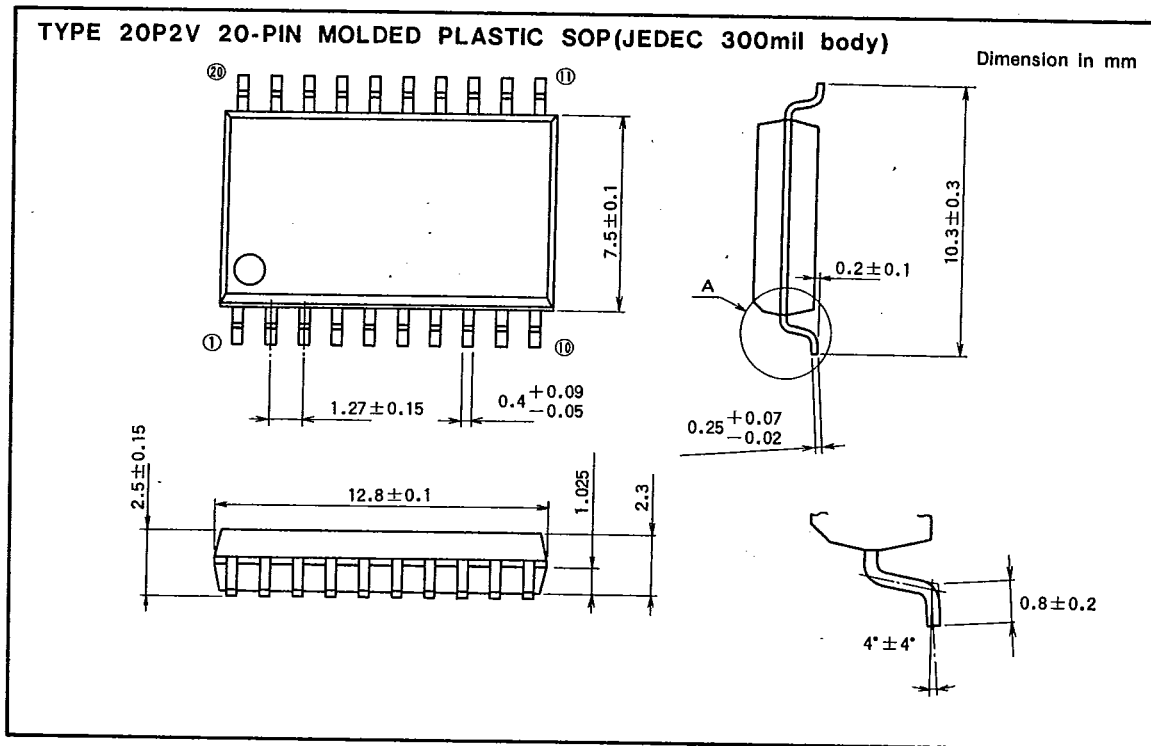
91D 12853 D T90-20



MITSUBISHI HIGH SPEED CMOS  
PACKAGE OUTLINES

6249827 MITSUBISHI (DGTL LOGIC)

91D 12854 D T-90-20



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