SRAM MODULE

32K x 16 SRAM

FEATURES

- High speed: 20*, 25 and 30ns
- High-performance, low-power CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- Upper and lower byte select
- All inputs and outputs are TTL compatible

OPTIONS

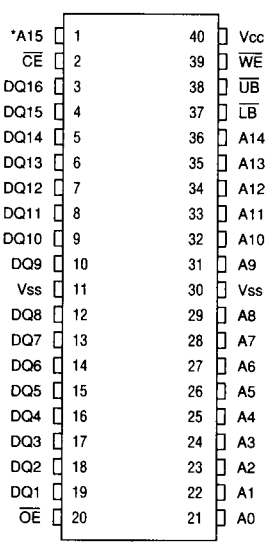
	MARKING
• Timing	
20ns access	-20*
25ns access	-25
30ns access	-30
• Packages	
40-pin DIP (600 mil)	D

- Part Number Example: MT2S3216D-20

*Preliminary

PIN ASSIGNMENT (Top View)

40-Pin DIP
(SI-2)



*Address A15 must be connected to Vss.

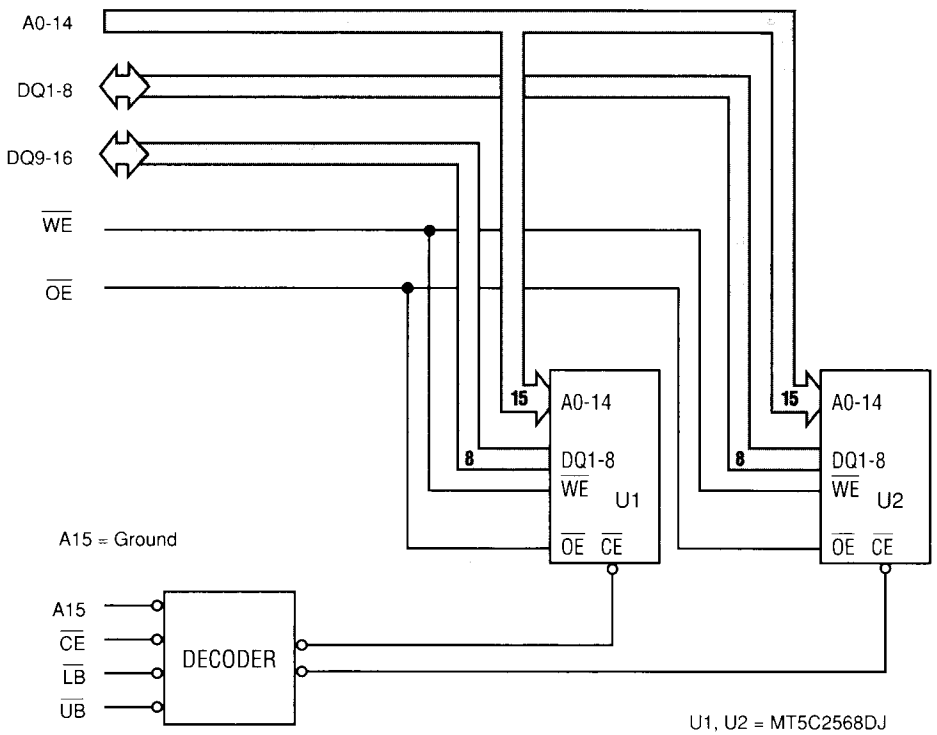
GENERAL DESCRIPTION

The MT2S3216 is a high-speed SRAM memory module containing 32,768 words organized in a x16-bit configuration. The module consists of two 32K x 8 fast static RAMs and a single decoder mounted on a 40-pin DIP, FR4 printed circuit board.

Data is written into the SRAM memory when both write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{LB}$ and $\overline{UB}$ control the lower and upper byte selection. $\overline{CE}$ sets the output in High-Z for additional system design flexibility, and memory expansion may be achieved through use of the $\overline{OE}$ and $\overline{CE}$ functions.

The Micron SRAM family uses high-speed, low-power CMOS designs featuring a four-transistor memory cell and double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5V supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	A15	DQ OPERATION	POWER
STANDBY	H	X	X	X	X	L	HIGH-Z	STANDBY
STANDBY	L	H	H	X	X	L	HIGH-Z	STANDBY
READ: WORD	L	L	L	L	H	L	Q1-16	ACTIVE (x16)
READ: LOWER BYTE	L	H	L	L	H	L	Q1-8	ACTIVE (x8)
READ: UPPER BYTE	L	L	H	L	H	L	Q9-16	ACTIVE (x8)
READ: WORD	L	L	L	H	H	L	HIGH-Z	ACTIVE (x16)
READ: LOWER BYTE	L	H	L	H	H	L	HIGH-Z	ACTIVE (x8)
READ: UPPER BYTE	L	L	H	H	H	L	HIGH-Z	ACTIVE (x8)
WRITE: WORD	L	L	L	X	L	L	D1-16	ACTIVE (x16)
WRITE: LOWER BYTE	L	H	L	X	L	L	D1-8	ACTIVE (x8)
WRITE: UPPER BYTE	L	L	H	X	L	L	D9-16	ACTIVE (x8)

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature ..... -55°C to +125°C
Power Dissipation 2W
Short Circuit Output Current 50mA
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	A0-A14, $\overline{WE}$, $\overline{OE}$		V_{IH}	2.2	Vcc+1	V	1
	A15, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$		V_{IH}	2.0	Vcc+1	V	1
Input Low (Logic 0) Voltage	A0-A14, $\overline{WE}$, $\overline{OE}$		V_{IL}	-0.5	0.8	V	1, 2
	A15, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	A0-A14, $\overline{WE}$, $\overline{OE}$	I_{LI}	-10	10	µA	
		A15, $\overline{CE}$			1,200	µA	
		$\overline{UB}$, $\overline{LB}$			600	µA	
Input/Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ Vcc	DQ1-DQ16	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		1	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1
Supply Voltage			Vcc	4.5	5.5	V	1

DESCRIPTION		CONDITIONS	SYMBOL	TYP	MAX -20*	MAX -25	MAX -30	UNITS	NOTES
Operating Current: TTL Input Levels	(x16)	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC Outputs Open	Icc	170	280	260	210	mA	3, 13
	(x8)			85	140	140	140	mA	3, 13
Standby Current: TTL Input Levels		$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX =1/ ^tRC Outputs Open	I_{SB1}	30	70	70	70	mA	13
Standby Current: CMOS Input Levels		$\overline{CE}$ ≥ Vcc -0.2; Vcc = MAX V_{IN} ≤ V_{SS} +0.2 or V_{IN} ≥ Vcc -0.2; f = 0	I_{SB2}	5	35	35	35	mA	13

*Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A14, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz Vcc = 5V	C_{I1}	14	pF	4
Input Capacitance: A15, $\overline{CE}$		C_{I2}	10	pF	4
Input Capacitance: $\overline{UB}$, $\overline{LB}$		C_{I3}	5	pF	4
Input/Output Capacitance: DQ		C_{IO}	8	pF	4

SRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-20*		-25		-30			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	20		25		30		ns	
Address access time	^tAA		20		25		30	ns	
Chip Enable access time	^tACE		20		25		30	ns	
Output hold from address change	^tOH	3		5		5		ns	
Chip Enable LOW to output in Low-Z	^tLZCE	4		6		5		ns	7
Chip Enable to output in High-Z	^tHZCE		8		9		20	ns	6, 7
Chip Enable LOW to power-up time	^tPU	0		0		0		ns	
Chip Enable HIGH to power-down time	^tPD		20		25		30	ns	
Output Enable access time	^tAOE		8		8		10	ns	
Output Enable LOW to output in Low-Z	^tLZOE	0		0		0		ns	
Output Enable HIGH to output in High-Z	^tHZOE		7		7		10	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	20		20		25		ns	
Chip Enable to end of write	^tCW	15		15		25		ns	
Address valid to end of write	^tAW	15		15		18		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
WRITE pulse width	$^tWP1$	10		15		25		ns	
WRITE pulse width	$^tWP2$	12		15		25		ns	
Data setup time	^tDS	7		10		15		ns	
Data hold time	^tDH	0		0		0		ns	
Write Enable LOW to output in Low-Z	^tLZWE	4		5		5		ns	7
Write Enable HIGH to output in High-Z	^tHZWE		7		10		12	ns	6, 7

*Preliminary

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

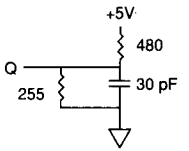


Fig. 1 OUTPUT LOAD EQUIVALENT

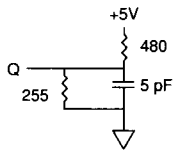
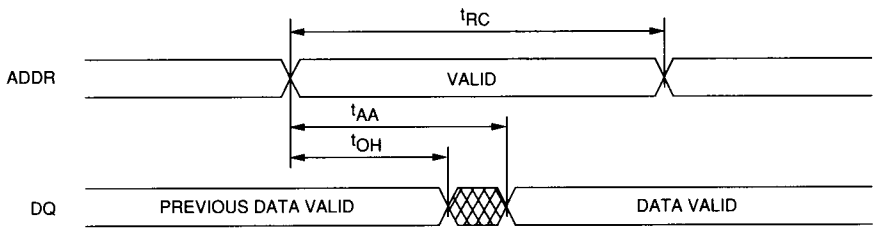


Fig. 2 OUTPUT LOAD EQUIVALENT

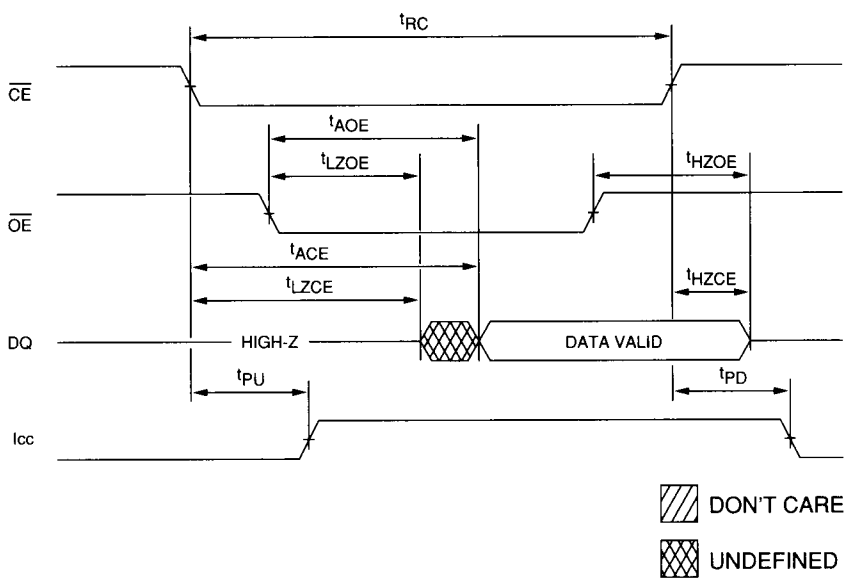
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC=Read Cycle Time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 20ns cycle time.

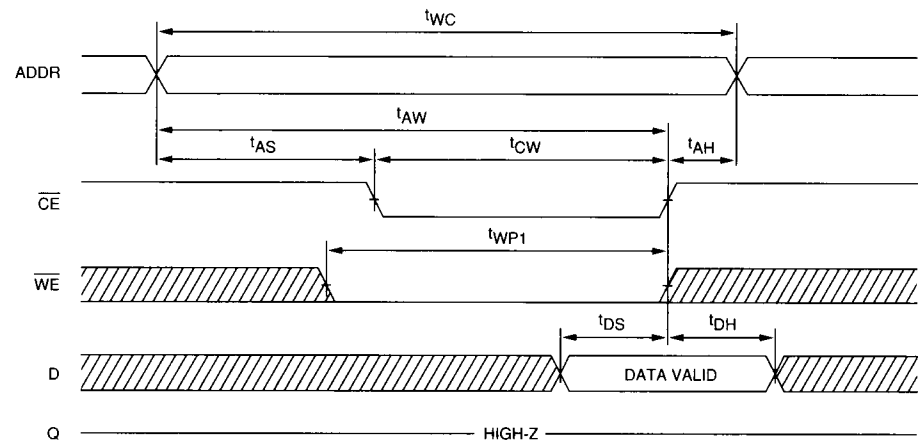
READ CYCLE NO. 1 [8, 9]



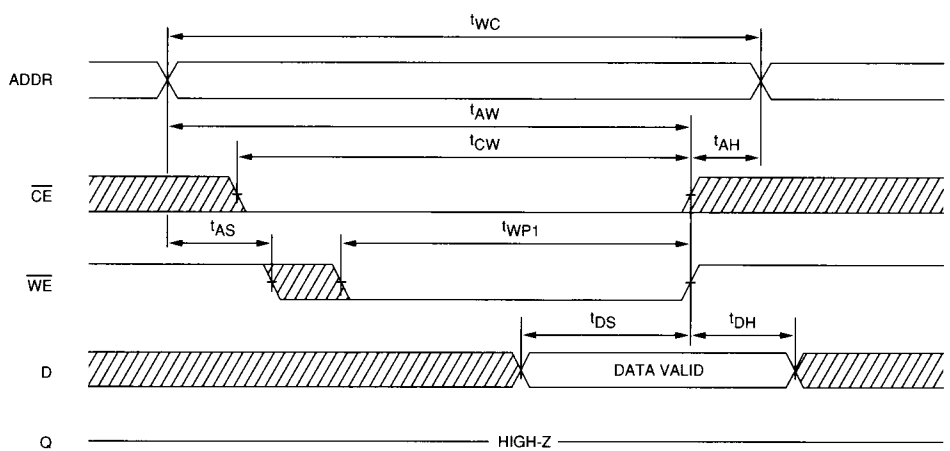
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)

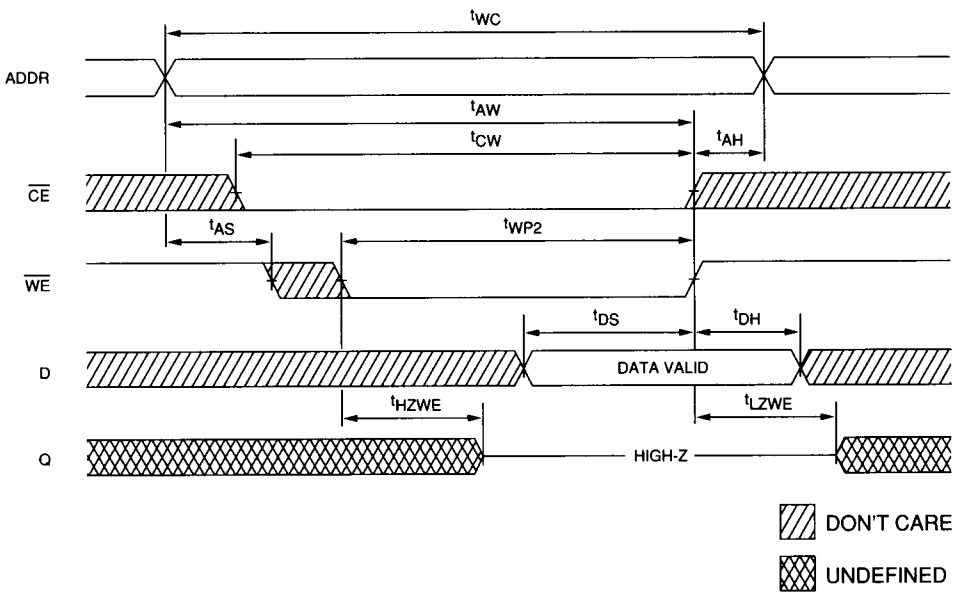


DON'T CARE

UNDEFINED

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).