HD66523R

(240-Channel Common Driver with Internal LCD Timing Circuit)

HITACHI

ADE-207-303(Z)
'99.9
Rev. 0.0

Description

The HD66523R is a common driver for liquid crystal dot-matrix graphic display system. This device incorporates a 240 liquid crystal driver and an oscillator, and generates timing signals (line scanning signals and frame synchronizing signals) required for the liquid crystal display. It features a new LCD driving technique for better quality of display and low power dissipation. Combined with the HD66522, a 160-channel column driver with an internal RAM, the HD66523R is optimal for use in displays for portable information tools.

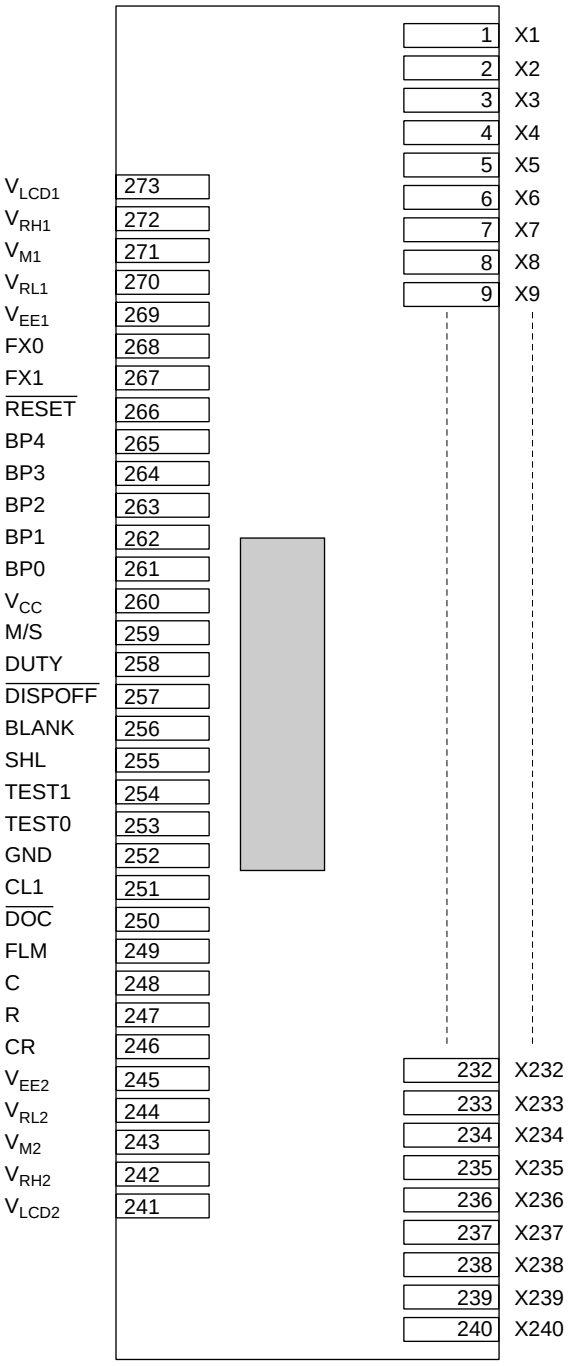
Features

- LCD timing generator: 1/200, 1/240 duty cycle timing are generated internally.
- Number of LCD drivers: 240
- Power supply voltage: 2.4V to 3.6V
- High voltage LCD drive circuit: ±21.5V
- LCD driving technique: Multi-line addressing for low power consumption.
- Programmable vertical retrace period: zero to 192 lines
- Low power consumption
- Internal display off function
- On-chip oscillator combined with external resistor and capacitor.
- TCP-273, chip with gold bump

Ordering Information

Type No.	Package	Outer Lead Pitch (μm)
HD66523RTA0	273 pin TCP	200
HCD66523RBP	Die with gold bump	—

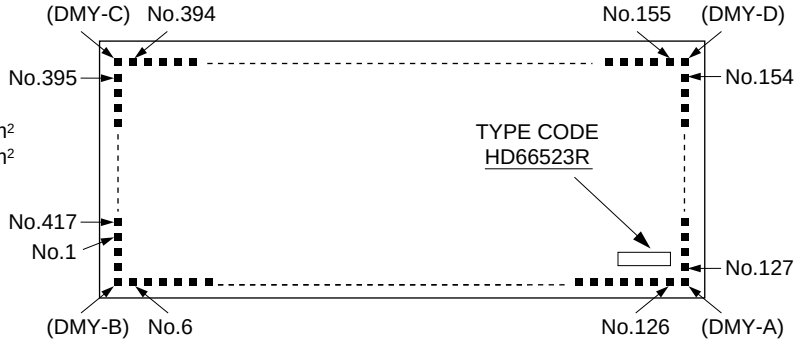
Pin Arrangement



Note: This figure is not drawn to a scale.

Pad Arrangement

Chip size : 17.43 × 3.60mm²
Coordinate : Pad center
Origin : Chip center
Bump size
No.418, 419, 420, 421 : 70 × 70µm²
Others : 40 × 70µm²



Pad No.	Pad Name	Coordinate X	Coordinate Y
1	VLCD1-1	–8555	–1100
2	VLCD1-2	–8555	–1170
3	VLCD1-3	–8555	–1240
4	VLCD1-4	–8555	–1310
5	VLCD1-5	–8555	–1380
6	VRH1-1	–8410	–1610
7	VRH1-2	–8340	–1610
8	VRH1-3	–8270	–1610
9	VRH1-4	–8200	–1610
10	VRH1-5	–8130	–1610
11	VM1-1	–8045	–1610
12	VM1-2	–7975	–1610
13	VM1-3	–7905	–1610
14	VM1-4	–7835	–1610
15	VM1-5	–7765	–1610
16	VRL1-1	–7660	–1610
17	VRL1-2	–7590	–1610
18	VRL1-3	–7520	–1610
19	VRL1-4	–7450	–1610
20	VRL1-5	–7380	–1610
21	VEE1-1	–7275	–1610
22	VEE1-2	–7205	–1610
23	VEE1-3	–7135	–1610
24	VEE1-4	–7065	–1610
25	VEE1-5	–6995	–1610
26	(DMY1)	–6925	–1610
27	(DMY2)	–6855	–1610
28	(DMY3)	–6785	–1610
29	(DMY4)	–6715	–1610
30	(DMY5)	–6485	–1582
31	FX0-1	–6218	–1582
32	FX0-2	–6148	–1582
33	FX1-1	–5732	–1582
34	FX1-2	–5662	–1582
35	(DMY6)	–5395	–1582
36	(DMY7)	–5325	–1582
37	$\overline{\text{RESET}}$-1	–5058	–1582
38	$\overline{\text{RESET}}$-2	–4988	–1582
39	BP4-1	–4572	–1582
40	BP4-2	–4502	–1582
41	(DMY8)	–4235	–1582
42	(DMY9)	–4165	–1582
43	BP3-1	–3898	–1582
44	BP3-2	–3828	–1582
45	BP2-1	–3412	–1582
46	BP2-2	–3342	–1582
47	(DMY10)	–3075	–1582
48	(DMY11)	–3005	–1582
49	BP1-1	–2738	–1582
50	BP1-2	–2668	–1582
51	BP0-1	–2252	–1582
52	BP0-2	–2182	–1582
53	(DMY12)	–1915	–1582
54	V_{CC}-1	–1805	–1582
55	V_{CC}-2	–1735	–1582
56	V_{CC}-3	–1665	–1582
57	V_{CC}-4	–1595	–1582
58	V_{CC}-5	–1525	–1582
59	(DMY13)	–1415	–1582
60	M/S-1	–1148	–1582
61	M/S-2	–1078	–1582
62	DUTY-1	–662	–1582
63	DUTY-2	–592	–1582
64	(DMY14)	–325	–1582
65	(DMY15)	–255	–1582
66	$\overline{\text{DISPOFF}}$-1	12	–1582
67	$\overline{\text{DISPOFF}}$-2	82	–1582
68	BLANK-1	498	–1582
69	BLANK-2	568	–1582
70	(DMY16)	835	–1582
71	(DMY17)	905	–1582
72	SHL-1	1172	–1582
73	SHL-2	1242	–1582
74	TEST1-1	1658	–1582
75	TEST1-2	1728	–1582
76	(DMY18)	1995	–1582
77	(DMY19)	2065	–1582
78	TEST0-1	2332	–1582
79	TEST0-2	2402	–1582
80	GND-1	2685	–1582
81	GND-2	2755	–1582
82	GND-3	2825	–1582
83	GND-4	2895	–1582
84	GND-5	2965	–1582
85	(DMY20)	3075	–1582
86	CL1-1	3342	–1582
87	CL1-2	3412	–1582
88	$\overline{\text{DOC}}$-1	3828	–1582
89	$\overline{\text{DOC}}$-2	3898	–1582
90	(DMY21)	4165	–1582

Pin No.	Function	Coordinate X	Coordinate Y
91	(DMY22)	4235	–1582
92	FLM-1	4502	–1582
93	FLM-2	4572	–1582
94	C-1	5038	–1582
95	C-2	5108	–1582
96	(DMY23)	5375	–1582
97	(DMY24)	5445	–1582
98	R-1	5712	–1582
99	R-2	5782	–1582
100	CR-1	6198	–1582
101	CR-2	6268	–1582
102	(DMY25)	6535	–1582
103	(DMY26)	6715	–1610
104	(DMY27)	6785	–1610
105	(DMY28)	6855	–1610
106	(DMY29)	6925	–1610
107	VEE2-1	6995	–1610
108	VEE2-2	7065	–1610
109	VEE2-3	7135	–1610
110	VEE2-4	7205	–1610
111	VEE2-5	7275	–1610
112	VRL2-1	7380	–1610
113	VRL2-2	7450	–1610
114	VRL2-3	7520	–1610
115	VRL2-4	7590	–1610
116	VRL2-5	7660	–1610
117	VM2-1	7765	–1610
118	VM2-2	7835	–1610
119	VM2-3	7905	–1610
120	VM2-4	7975	–1610
121	VM2-5	8045	–1610
122	VRH2-1	8130	–1610
123	VRH2-2	8200	–1610
124	VRH2-3	8270	–1610
125	VRH2-4	8340	–1610
126	VRH2-5	8410	–1610
127	VLCD2-1	8555	–1380
128	VLCD2-2	8555	–1310
129	VLCD2-3	8555	–1240
130	VLCD2-4	8555	–1170
131	VLCD2-5	8555	–1100
132	(DMY30)	8555	–650
133	(DMY31)	8555	–550
134	(DMY32)	8555	–450
135	(DMY33)	8555	–350
136	(DMY34)	8555	–250
137	(DMY35)	8555	–150
138	(DMY36)	8555	–50
139	(DMY37)	8555	50
140	(DMY38)	8555	150
141	(DMY39)	8555	250
142	(DMY40)	8555	350
143	(DMY41)	8555	450
144	(DMY42)	8555	550
145	(DMY43)	8555	650
146	(DMY44)	8555	850
147	(DMY45)	8555	920
148	(DMY46)	8555	990
149	(DMY47)	8555	1060
150	(DMY48)	8555	1130
151	(DMY49)	8555	1200
152	(DMY50)	8555	1270
153	(DMY51)	8555	1340
154	(DMY52)	8555	1410
155	X240	8365	1640
156	X239	8295	1640
157	X238	8225	1640
158	X237	8155	1640
159	X236	8085	1640
160	X235	8015	1640
161	X234	7945	1640
162	X233	7875	1640
163	X232	7805	1640
164	X231	7735	1640
165	X230	7665	1640
166	X229	7595	1640
167	X228	7525	1640
168	X227	7455	1640
169	X226	7385	1640
170	X225	7315	1640
171	X224	7245	1640
172	X223	7175	1640
173	X222	7105	1640
174	X221	7035	1640
175	X220	6965	1640
176	X219	6895	1640
177	X218	6825	1640
178	X217	6755	1640
179	X216	6685	1640
180	X215	6615	1640
181	X214	6545	1640
182	X213	6475	1640
183	X212	6405	1640
184	X211	6335	1640
185	X210	6265	1640
186	X209	6195	1640
187	X208	6125	1640
188	X207	6055	1640
189	X206	5985	1640
190	X205	5915	1640
191	X204	5845	1640
192	X203	5775	1640
193	X202	5705	1640
194	X201	5635	1640
195	X200	5565	1640
196	X199	5495	1640
197	X198	5425	1640
198	X197	5355	1640
199	X196	5285	1640
200	X195	5215	1640
201	X194	5145	1640
202	X193	5075	1640
203	X192	5005	1640
204	X191	4935	1640
205	X190	4865	1640
206	X189	4795	1640
207	X188	4725	1640
208	X187	4655	1640
209	X186	4585	1640
210	X185	4515	1640
211	X184	4445	1640
212	X183	4375	1640
213	X182	4305	1640
214	X181	4235	1640
215	X180	4165	1640
216	X179	4095	1640
217	X178	4025	1640
218	X177	3955	1640
219	X176	3885	1640
220	X175	3815	1640
221	X174	3745	1640
222	X173	3675	1640
223	X172	3605	1640
224	X171	3535	1640
225	X170	3465	1640
226	X169	3395	1640
227	X168	3325	1640
228	X167	3255	1640
229	X166	3185	1640
230	X165	3115	1640
231	X164	3045	1640

Pin No.	Function	Coordinate X	Coordinate Y
232	X163	2975	1640
233	X162	2905	1640
234	X161	2835	1640
235	X160	2765	1640
236	X159	2695	1640
237	X158	2625	1640
238	X157	2555	1640
239	X156	2485	1640
240	X155	2415	1640
241	X154	2345	1640
242	X153	2275	1640
243	X152	2205	1640
244	X151	2135	1640
245	X150	2065	1640
246	X149	1995	1640
247	X148	1925	1640
248	X147	1855	1640
249	X146	1785	1640
250	X145	1715	1640
252	X144	1645	1640
252	X143	1575	1640
253	X142	1505	1640
254	X141	1435	1640
255	X140	1365	1640
256	X139	1295	1640
257	X138	1225	1640
258	X137	1155	1640
259	X136	1085	1640
260	X135	1015	1640
261	X134	945	1640
262	X133	875	1640
263	X132	805	1640
264	X131	735	1640
265	X130	665	1640
266	X129	595	1640
267	X128	525	1640
268	X127	455	1640
269	X126	385	1640
270	X125	315	1640
271	X124	245	1640
272	X123	175	1640
273	X122	105	1640
274	X121	35	1640
275	X120	–35	1640
276	X119	–105	1640
277	X118	–175	1640
278	X117	–245	1640
279	X116	–315	1640
280	X115	–385	1640
281	X114	–455	1640
282	X113	–525	1640
283	X112	–595	1640
284	X111	–665	1640
285	X110	–735	1640
286	X109	–805	1640
287	X108	–875	1640
288	X107	–945	1640
289	X106	–1015	1640
290	X105	–1085	1640
291	X104	–1155	1640
292	X103	–1225	1640
293	X102	–1295	1640
294	X101	–1365	1640
295	X100	–1435	1640
296	X99	–1505	1640
297	X98	–1575	1640
298	X97	–1645	1640
299	X96	–1715	1640
300	X95	–1785	1640
301	X94	–1855	1640
302	X93	–1925	1640
303	X92	–1995	1640
304	X91	–2065	1640
305	X90	–2135	1640
306	X89	–2205	1640
307	X88	–2275	1640
308	X87	–2345	1640
309	X86	–2415	1640
310	X85	–2485	1640
311	X84	–2555	1640
312	X83	–2625	1640
313	X82	–2695	1640
314	X81	–2765	1640
315	X80	–2835	1640
316	X79	–2905	1640
317	X78	–2975	1640
318	X77	–3045	1640
319	X76	–3115	1640
320	X75	–3185	1640
321	X74	–3255	1640
322	X73	–3325	1640
323	X72	–3395	1640
324	X71	–3465	1640
325	X70	–3535	1640
326	X69	–3605	1640
327	X68	–3675	1640
328	X67	–3745	1640
329	X66	–3815	1640
330	X65	–3885	1640
331	X64	–3955	1640
332	X63	–4025	1640
333	X62	–4095	1640
334	X61	–4165	1640
335	X60	–4235	1640
336	X59	–4305	1640
337	X58	–4375	1640
338	X57	–4445	1640
339	X56	–4515	1640
340	X55	–4585	1640
341	X54	–4655	1640
342	X53	–4725	1640
343	X52	–4795	1640
344	X51	–4865	1640
345	X50	–4935	1640
346	X49	–5005	1640
347	X48	–5075	1640
348	X47	–5145	1640
349	X46	–5215	1640
350	X45	–5285	1640
351	X44	–5355	1640
352	X43	–5425	1640
353	X42	–5495	1640
354	X41	–5565	1640
355	X40	–5635	1640
356	X39	–5705	1640
357	X38	–5775	1640
358	X37	–5845	1640
359	X36	–5915	1640
360	X35	–5985	1640
361	X34	–6055	1640
362	X33	–6125	1640
363	X32	–6195	1640
364	X31	–6265	1640
365	X30	–6335	1640
366	X29	–6405	1640
367	X28	–6475	1640
368	X27	–6545	1640
369	X26	–6615	1640
370	X25	–6885	1640
371	X24	–6755	1640
372	X23	–6825	1640

Pin No.	Function	Coordinate X	Coordinate Y
373	X22	–6895	1640
374	X21	–6965	1640
375	X20	–7035	1640
376	X19	–7105	1640
377	X18	–7175	1640
378	X17	–7245	1640
379	X16	–7315	1640
380	X15	–7385	1640
381	X14	–7455	1640
382	X13	–7525	1640
383	X12	–7595	1640
384	X11	–7665	1640
385	X10	–7735	1640
386	X9	–7805	1640
387	X8	–7875	1640
388	X7	–7945	1640
389	X6	–8015	1640
390	X5	–8085	1640
391	X4	–8155	1640
392	X3	–8225	1640
393	X2	–8295	1640
394	X1	–8365	1640
395	(DMY53)	–8555	1410
396	(DMY54)	–8555	1340
397	(DMY55)	–8555	1270
398	(DMY56)	–8555	1200
399	(DMY57)	–8555	1130
400	(DMY58)	–8555	1060
401	(DMY59)	–8555	990
402	(DMY60)	–8555	920
403	(DMY61)	–8555	850
404	(DMY62)	–8555	650
405	(DMY63)	–8555	550
406	(DMY64)	–8555	450
407	(DMY65)	–8555	350
408	(DMY66)	–8555	250
409	(DMY67)	–8555	150
410	(DMY68)	–8555	50
411	(DMY69)	–8555	–50
412	(DMY70)	–8555	–150
413	(DMY71)	–8555	–250
414	(DMY72)	–8555	–350
415	(DMY73)	–8555	–450
416	(DMY74)	–8555	–550
417	(DMY75)	–8555	–650
418	(DMY-A)	–8555	–1610
419	(DMY-B)	–8555	–1610
420	(DMY-C)	–8555	1640
421	(DMY-D)	–8555	1640

Pin Description

Classi-fication	Symbol	Pin Name	I/O	Number of pins	Functions
Power supply	V_{CC}	V_{CC}	Power supply	1	V_{CC}–GND: logic power supply
	GND	GND	Power supply	1	
	VLCD1, VLCD2	VLCD	Power supply	2	Power supply for LCD driving circuit
	V_{EE1}, V_{EE2}	V_{EE}	Power supply	2	
	VRH1, VRH2	VRH	—	2	LCD drive level power supply
	VM1, VM2	VM	—	2	
	VRL1, VRL2	VRL	—	2	
Control signals	M/$\overline{S}$	Master/ Slave	I	1	Select master or slave mode.
	DUTY	Duty	I	1	Selects the display duty cycle. Low level: 1/200 display duty ratio High level: 1/240 display duty ratio
	BP4 to BP0	Blanking period	I	5	Set vertical retrace period
	$\overline{DOC}$	Display off control	I/O	1	Control the display-off function.
	$\overline{DISPOFF}$	Display off	I	1	Turn off the LCD. During display off, all LCD driver output VM level
	SHL	Shift left	I	1	Pin SHL switches the shift direction of the scanning direction.
	$\overline{RESET}$	Reset	I	1	Reset the LSI internally.
	CR, C, R	Oscillator	—	3	Oscillator with external resistor and capacitor
	TEST1, TEST0	Test	I	2	Test pins, must be connected to GND.
LCD timing	CL1	Clock 1	I/O	1	The bidirectional shift register shifts data at the falling edge of CL1. During master mode, this pin outputs a data transfer clock with a two times larger cycle than the internal oscillator (or the cycle of the external clock) with a duty of 50%. During slave mode, this pin inputs the external data transfer clock.
	FLM	First line marker	I/O	1	During master mode, pin FLM outputs the first line marker signal. During slave mode, this pin inputs the external data first line marker signal.
	FX1, FX0	Scanning function	I/O	2	Output scanning function signals during master mode. Input scanning function signals during slave mode.
	BLANK	Blank	O	1	This pin shows vertical retrace period.
LCD drive output	X1 to X240	X1 to X240	O	240	Select one from among three levels, VRH, VM and VRL.

Table 1 M/$\overline{S}$ Signal Status

M/$\overline{S}$	Mode	LCD Timing Generator	Status of CL1, FLM and $\overline{DOC}$
H	Master	1/200 or 1/240 duty cycle	Output
L	Slave	Stops	Input

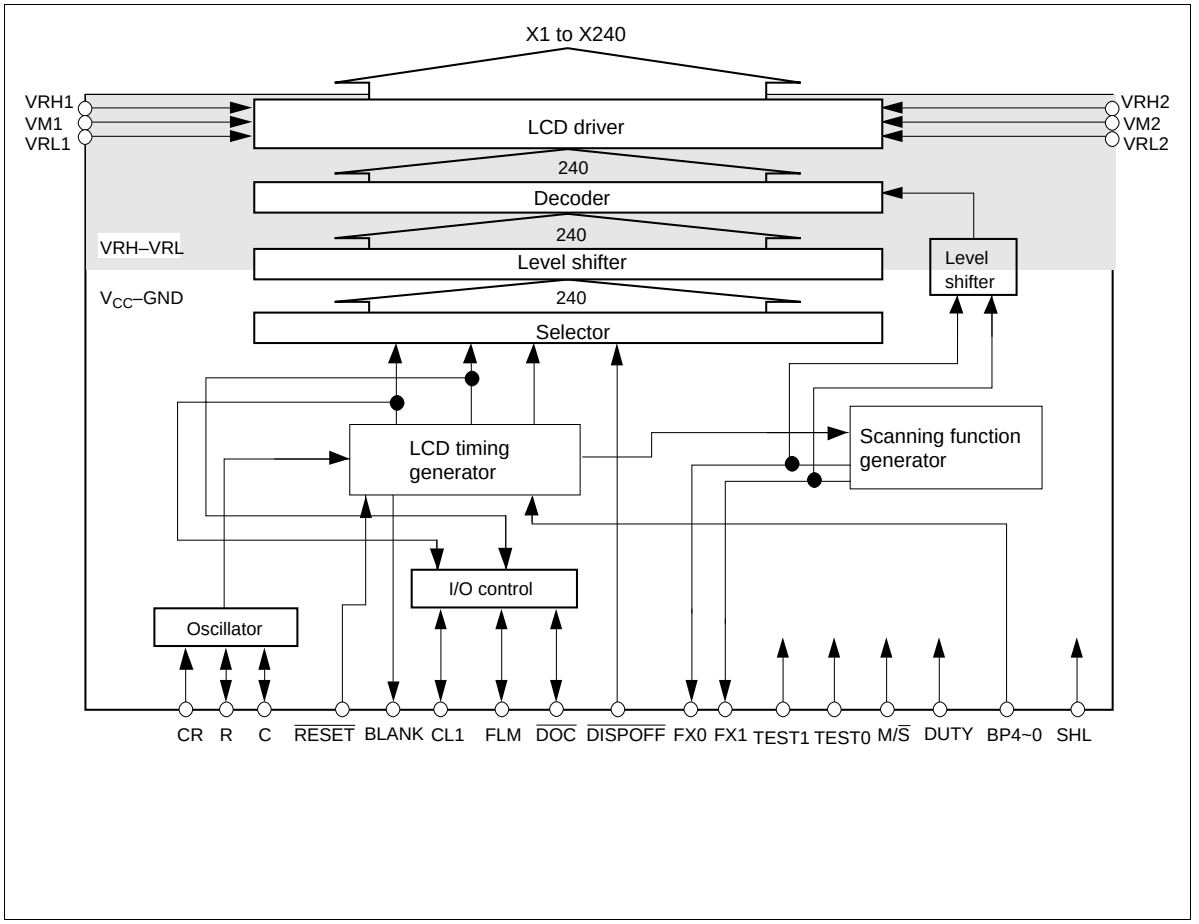
Table 2 Retrace period

BP4	BP3	BP2	BP1	BP0	Horizontal Retrace Period Number of lines
0	0	0	0	0	0
0	0	0	0	1	6
0	0	0	1	0	12
0	0	0	1	1	18
0	0	1	0	0	24
0	0	1	0	1	30
0	0	1	1	0	36
0	0	1	1	1	42
0	1	0	0	0	48
0	1	0	0	1	54
0	1	0	1	0	60
0	1	0	1	1	66
0	1	1	0	0	72
0	1	1	0	1	78
0	1	1	1	0	84
0	1	1	1	1	90
1	0	0	0	0	96
1	0	0	0	1	102
1	0	0	1	0	108
1	0	0	1	1	114
1	0	1	0	0	120
1	0	1	0	1	126
1	0	1	1	0	132
1	0	1	1	1	138
1	1	0	0	0	145
1	1	0	0	1	150
1	1	0	1	0	156
1	1	0	1	1	162
1	1	1	0	0	168
1	1	1	0	1	174
1	1	1	1	0	180
1	1	1	1	1	186

Table 3 Shift Direction

Mode	DUTY	SHL	
master	H	H	X240 → X1
		L	X1 → X240
	L	H	X220 → X21
		L	X21 → X220
slave	H	H	X240 → X1
		L	X1 → X240
	L	H	X220 → X21
		L	X21 → X220

Internal Block Diagram



1. **CR Oscillator:** The CR oscillator generates the HD66523R operation clock. During master mode, since the operation clock is needed, connect oscillation resistor R_f with oscillation capacitor C_f. When the external clock is used. Input external clock to pin CR and open pins C and R (Figure 1).

   When using the HD66523R during slave mode, the operation clock will not be needed; therefore, connect pin CR to V_{CC} and open pins C and R (Figure 2).

2. **Liquid Crystal Timing Generator:** The liquid crystal timing generator creates various signals for the LCD. During master mode ($M/\overline{S} = V_{CC}$), the generator operates the HD66523R's internal circuitry as a common internal driver using the generated LCD signals. In addition, signals CL1, FLM and $\overline{DOC}$ created by this generator can synchronously display data on a liquid crystal display by inputting them into the RAM-provided segment driver HD66522 used together with HD66523R. During slave mode ($M/\overline{S}$ = GND), this generator stops; the slave HD66523R operates based on signals CL1, $\overline{DOC}$ and FLM generated by the master HD66523R.

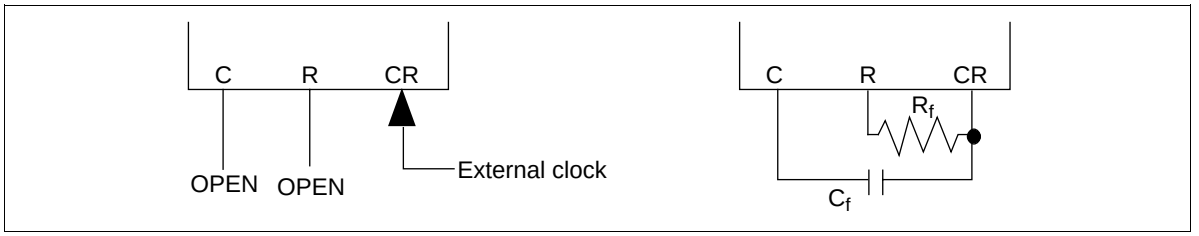


Figure 1 Oscillator Connection in Master Mode

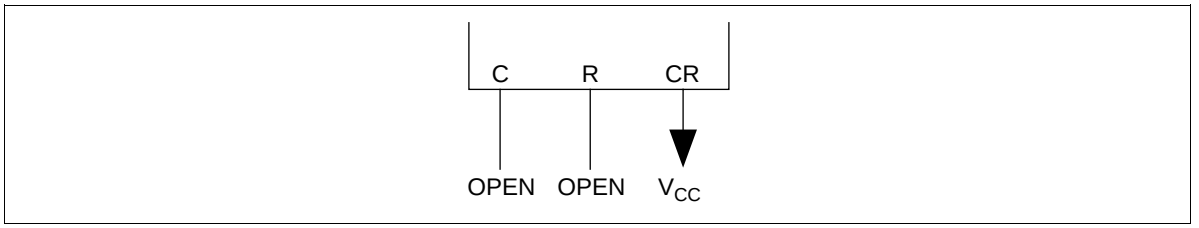


Figure 2 Oscillator Connection in Slave Mode

3. **Scanning Function Generator:** During master mode, this circuit generates the scanning function signals. During slave mode, this circuit stops working and FX1 and FX0 must be supplied from master HD66523R.
4. **Selector:** The selector generates signals which select two lines of LCD driver.
5. **Decoder:** Outputs data according to scanning function signals and data.
6. **LCD driver:** Outputs one of three levels according to outputs from decoder.

Internal Function Description

1. **Generation of Signals CL1 and FLM:** Signal CL1 shifts the scanning signal of the common driver. It is a 50% duty-ratio clock that changes level synchronously with the rising edge of oscillator clock CR.
   FLM is a clock signal that goes high once every frame. One frame consists of display lines, 240 lines if DUTY is high and 200 lines if DUTY is low, and vertical retrace period which is set with BP4 to BP0.
2. **Auto Display-off Control:** This functions prevents incorrect display after reset release. The display is turned off four frames following after reset release. In addition, the display off control signal shown in Figure 4 is output by pin $\overline{\text{DOC}}$. This pin is connected to pin $\overline{\text{DISPOFF}}$ of the HD66522.

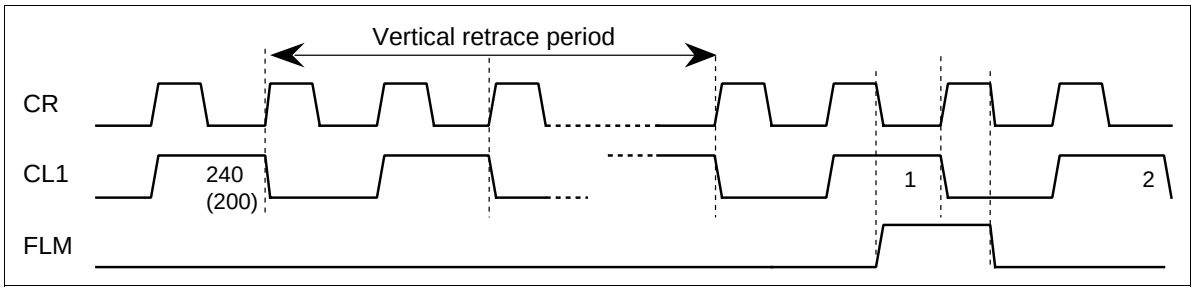


Figure 3 Generation of Signals CL1 and FLM

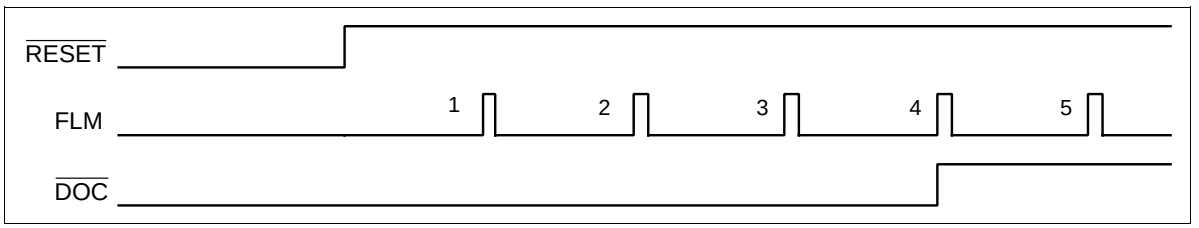


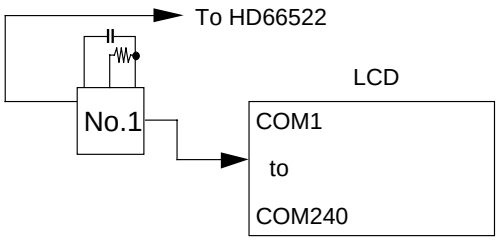
Figure 4 Automatic Display-off Control Function

Application Examples

Outline of HD66523R System Configuration

The HD66523R system configuration is outlined in Figure 5 and 6. Refer to the connection list (Table 4) for connection details.

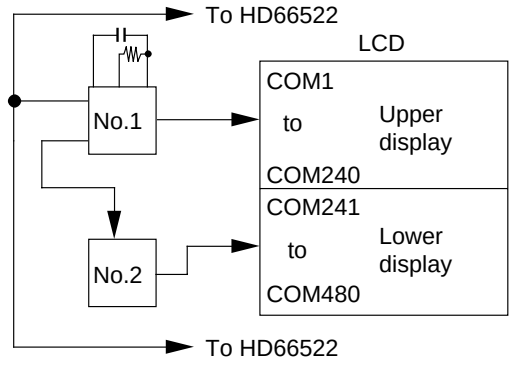
- When a signal HD66523R is used to configure a small display (Figure 5)
- When two HD66523Rs are used to configure a large display (Figure 6)



	No.1
When using the internal oscillator	Refer to connection list A
When using an external oscillator	Refer to connection list D

Note: One HD66523R drives common signals and supplies timing signal to the HD66522.

Figure 5 System Configuration When Using a Single HD66523R



	No.1	No.2
When using the internal oscillator	Refer to connection list B	Refer to connection list C
When using an external oscillator	Refer to connection list E	Refer to connection list C

Note: Upper and lower displays are driven by separate HD66523Rs to ensure display quality. No.1 operates in master mode, and No.2 operates in slave mode.

Figure 6 System Configuration When Using a Two HD66523R

Table 4 HD66523 Connection List

Connection Example	M/$\overline{S}$	DUTY	BP4 to BP0	$\overline{RESET}$	$\overline{DISPOFF}$	CR	R	C	CL1	FLM	$\overline{DOC}$	FX1 and FX0	SHL	X1 to X240
A	H	H	Sets the number of lines for retrace period	From MPU or external reset circuit	From controller	R_f C_f	R_f	C_f	To CL1 of HD66522	To FLM of HD66522	To $\overline{DISPOFF}$ of HD66522	To FX1 and FX0 of HD66522	H	COM240 to COM1
													L	COM1 to COM240
B	H	H	Sets the number of lines for retrace period	From MPU or external reset circuit	From controller	R_f C_f	R_f	C_f	To CL1 of HD66522, HD66523R	To FLM of HD66522, HD66523R	To $\overline{DISPOFF}$ of HD66522 To $\overline{DOC}$ of HD66523R	To FX1 and FX0 of HD66522, HD66523R	H	COM240 to COM1
													L	COM1 to COM240
C	L	H	Sets the number of lines for retrace period	From MPU or external reset circuit	H	H	—	—	From CL1 of HD66523R	From FLM of HD66523R	From $\overline{DOC}$ of HD66523R	To FX1 and FX0 of HD66523R	H	COM480 to COM241
													L	COM241 to COM480
D	H	H	Sets the number of lines for retrace period	From MPU or external reset circuit	From controller	External Clock	—	—	To CL1 of HD66522	To FLM of HD66522	To $\overline{DISPOFF}$ of HD66522	To FX1 and FX0 of HD66522	H	COM240 to COM1
													L	COM1 to COM240
E	H	H	Sets the number of lines for retrace period	From MPU or external reset circuit	From controller	External Clock	—	—	To CL1 of HD66522, HD66523R	To FLM of HD66522, HD66523R	To $\overline{DISPOFF}$ of HD66522 To $\overline{DOC}$ of HD66523R	To FX1 and FX0 of HD66522, HD66523R	H	COM240 to COM1
													L	COM1 to COM240

Notes: H = V_{CC} (Fixed)
L = GND (Fixed)
"—" means "open"
R_f: Oscillation resistor
C_f: Oscillarion capacitor

Example of System Configuration (1)

Figure 7 shows system configuration for a 240 * 160 dots LCD panel using segment driver HD66522 with internal bit-mapped RAM. All required functions can be prepared for liquid crystal display with just two LSIs except for liquid crystal display power supply circuit functions.

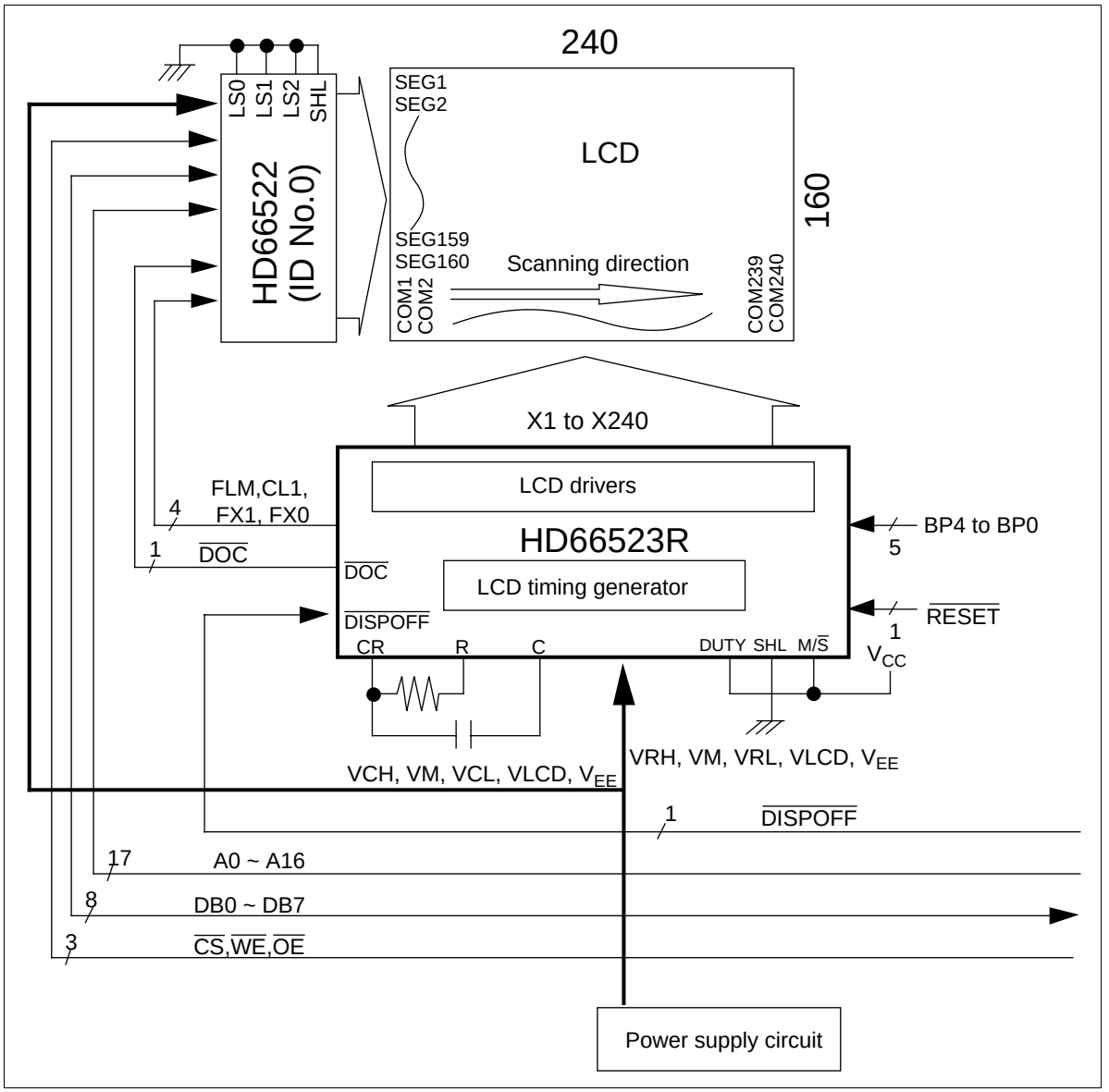


Figure 7 System Configuration (1)

Example of System Configuration (2)

Figure 8 shows a system configuration for a 240 * 320 dots LCD panel using segment driver HD66522 with internal bit-mapped RAM.

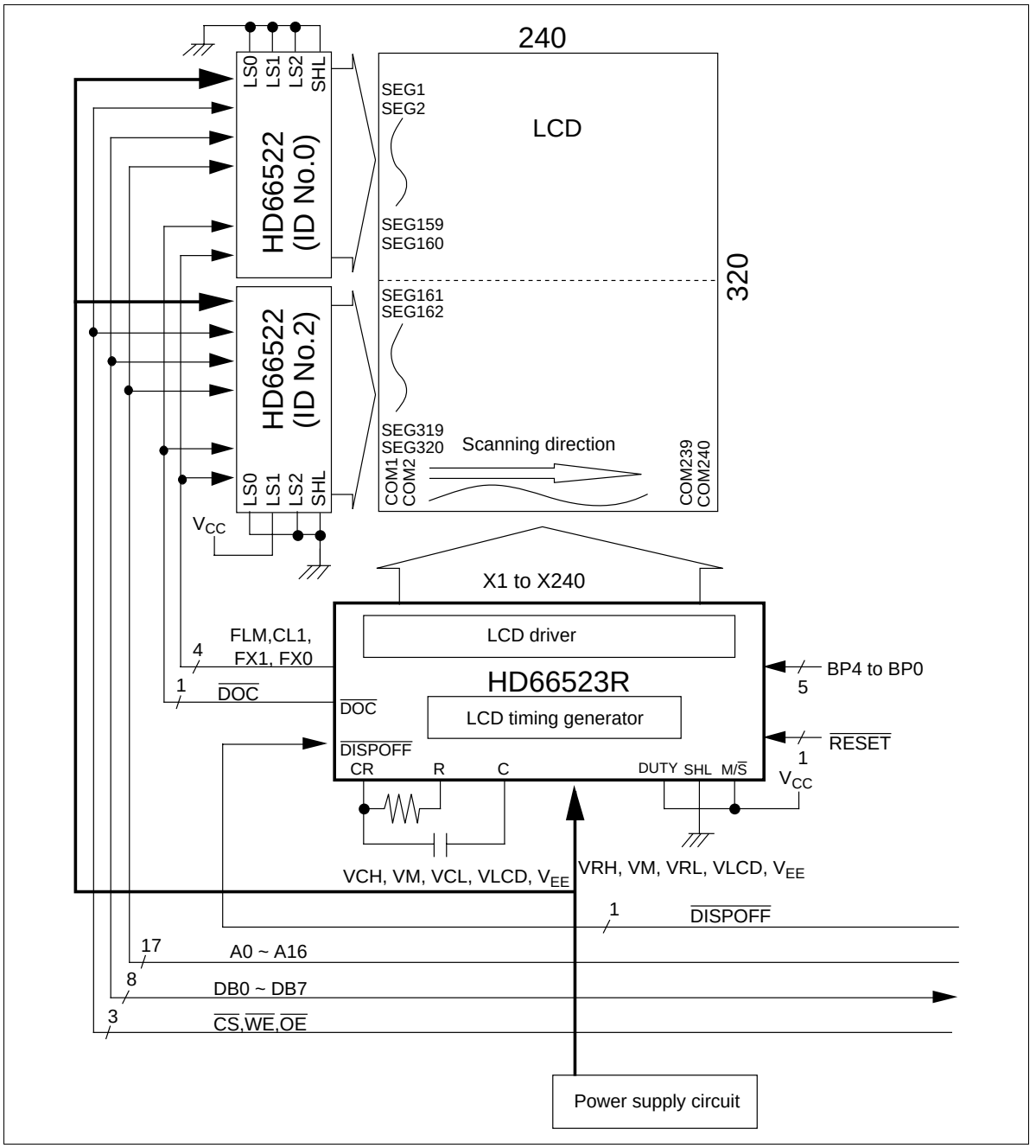


Figure 8 System Configuration (2)

Example of System Configuration (3)

Figure 9 shows a system configuration for a 320 * 480 dots LCD panel using segment driver HD66522 with internal bit-mapped RAM.

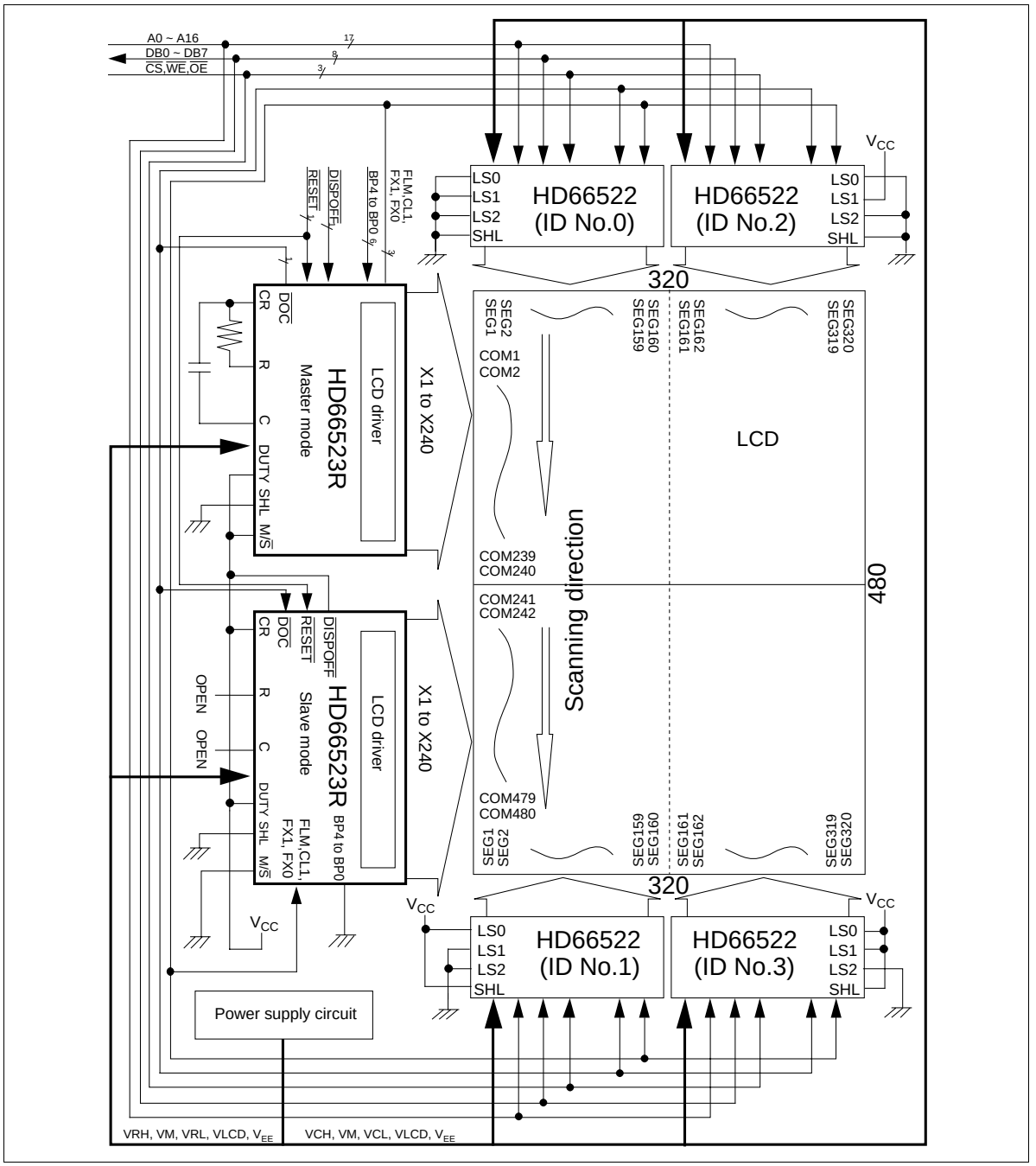


Figure 9 System Configuration (3)

Example of System Configuration (4)

Figure10 shows a system configuration for a 640 × 480 dots LCD panel using segment driver HD66522 with internal bit-mapped RAM.

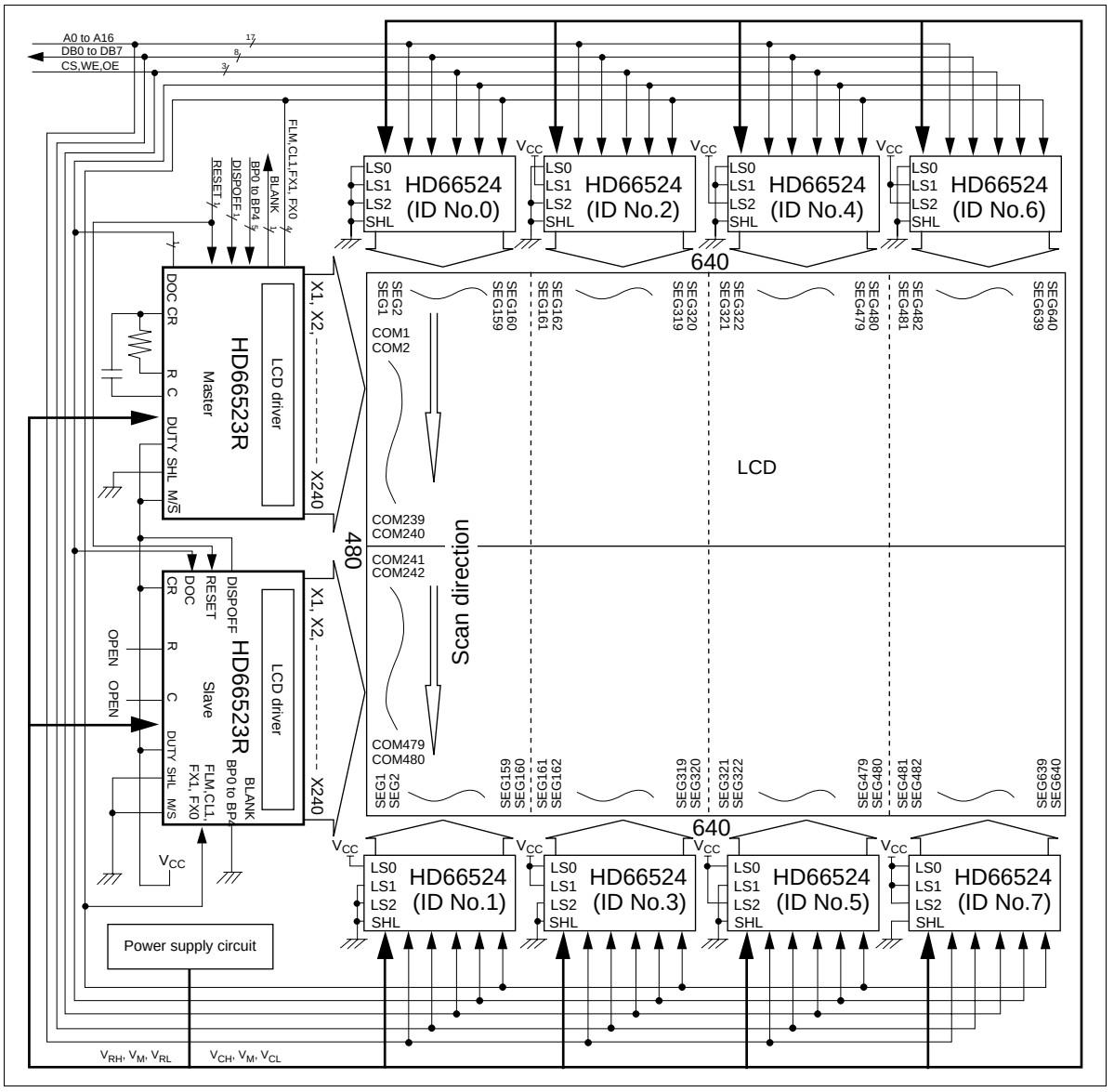


Figure 10 System Configuration (4)

LCD Drive Output

HD66523R outputs one of three levels, VRH, VM and VRL. VM is unselected level, VRH is high select level and VRL is low select level. Either VRH or VRL level is selected depending on the number of flames and lines. Output timings are showed in Figure 10 to 12.

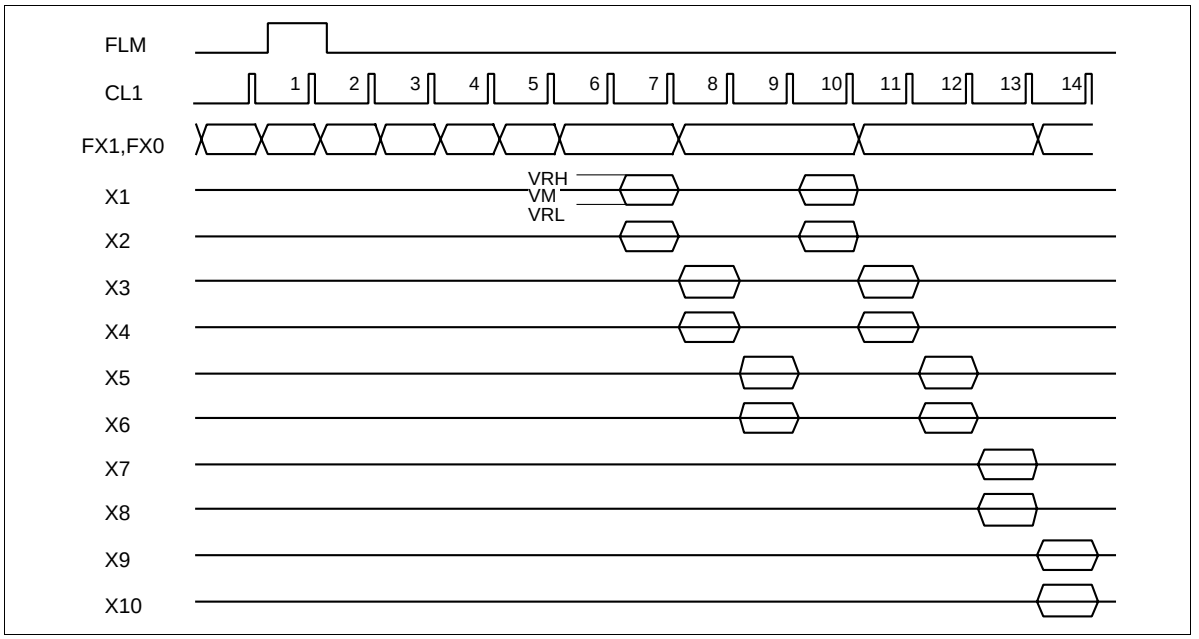


Figure 11 LCD Drive Output Timing at 3n + 1's frame (n = 1, 2, 3,)

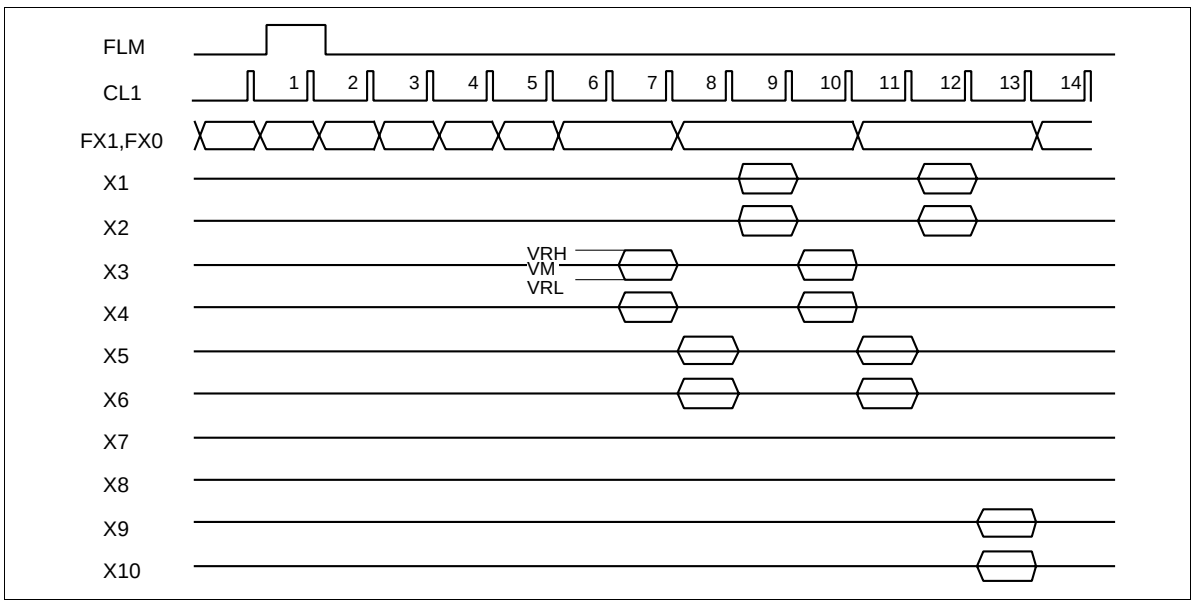


Figure 12 LCD Drive Output Timing at 3n + 2's frame (n = 1, 2, 3,)

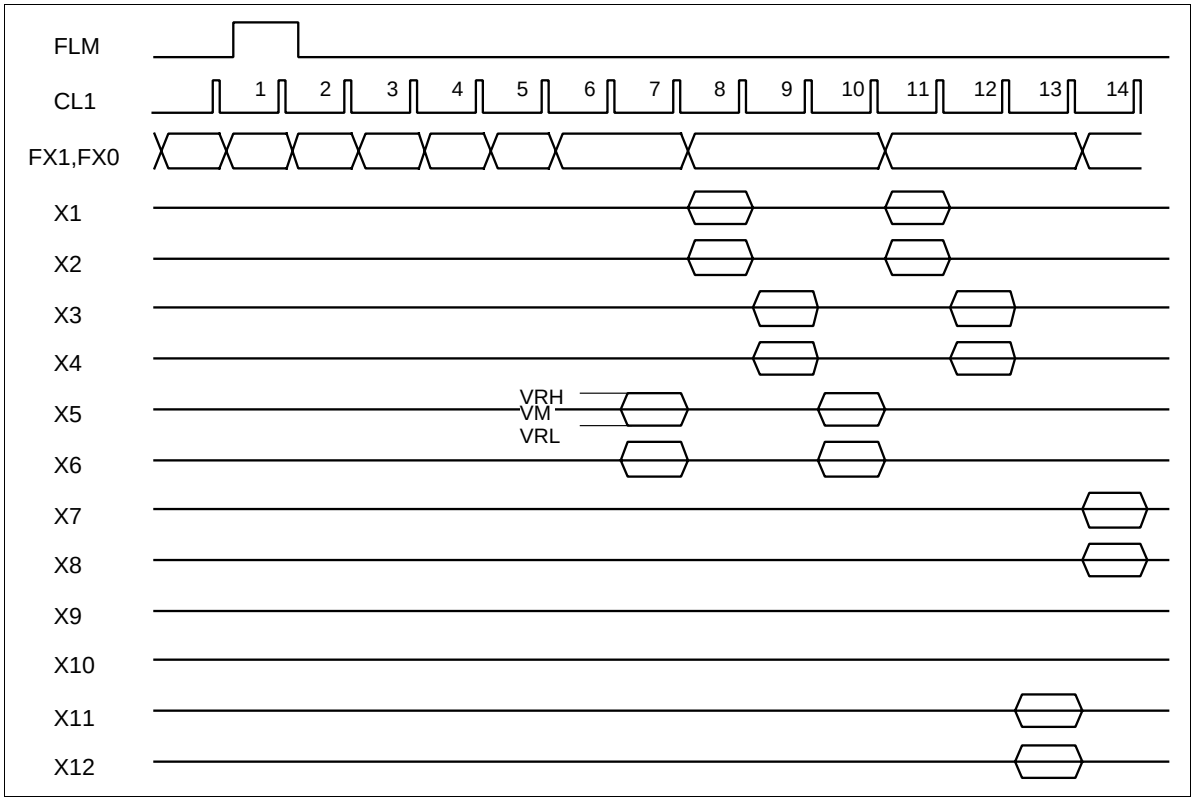
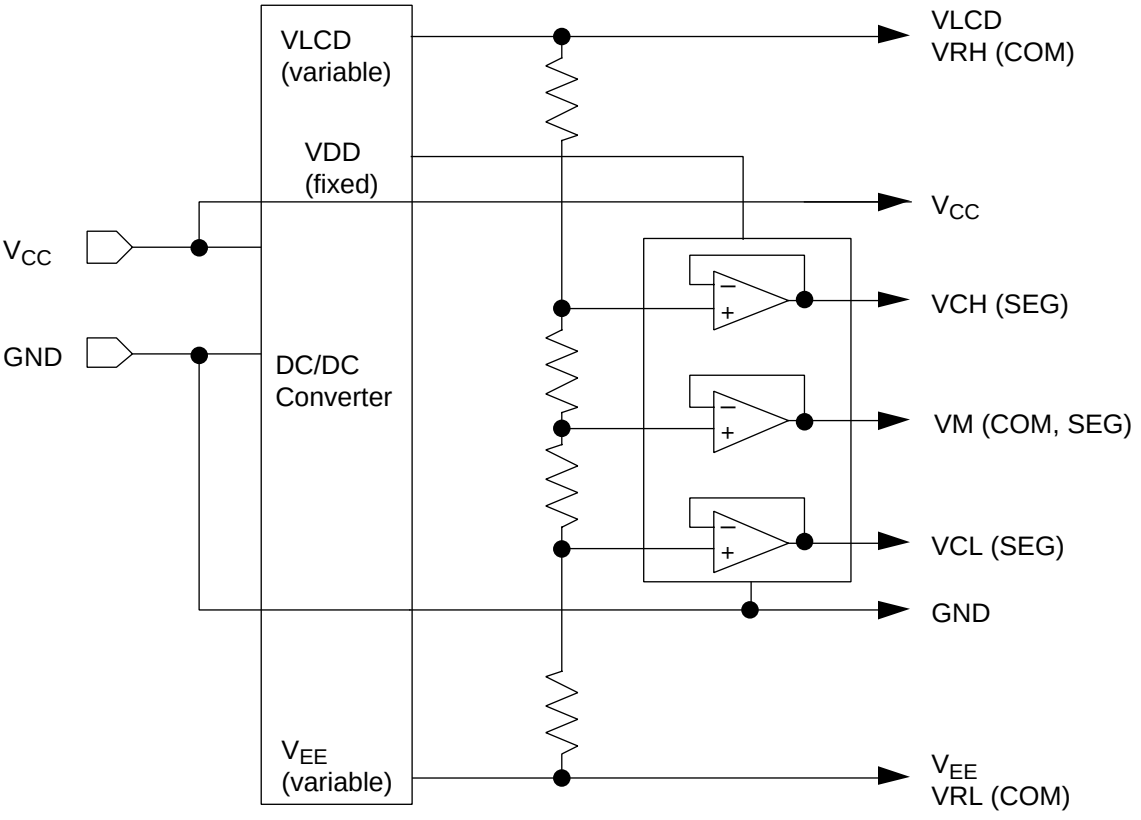


Figure 13 LCD Drive Output Timing at 3n + 3's frame (n = 1, 2, 3,)

Power Supply Circuit

The example of power circuit is shown in Figure 13. When you want to change contrast, both levels, VRH and VRL must be changed.



Note: VM level must keep following equations;

(VRH–VM) = (VM–VRL)
(VCH–VM) = (VM–VCL)
VCL > GND
VCH < VDD

Figure 14 Example of Power Supply Circuit

LCD Driving Voltage

The theoretical voltage which is needed for the best quality of display is calculated with the following equation. However, this voltage may be adjusted depending on the panel which is used.

$$VCH\text{-}VM,\ VM\text{-}VCL = \sqrt{\frac{\sqrt{N}}{\sqrt{N}-1}} \times Vth$$

$$VRH\text{-}VM,\ VM\text{-}VRL = \frac{1}{2}\sqrt{\frac{\sqrt{N} \times N}{\sqrt{N}-1}} \times Vth$$

Vth: Threshold voltage of LCD
N: Display duty ratio

Frame Frequency

HD66523R has a internal oscillator and generates all timing for driving LCD. The frame frequency varies with the frequency of oscillator. The frame frequency is calculated with the following equation.

$$f_{FRM} = \frac{f_{OSC}}{2\ (Nd + Nvr)}$$

f_{OSC}: Frequency of oscillator
Nd: Display duty ratio
Nvr: Vertical retrace period

Absolute Maximum Ratings

Item		Symbol	Rating	Unit	Note
Power voltage	Logic circuit	V_{CC}	–0.3 to + 7.0	V	1
	LCD drive circuit	VLCD	–0.3 to +25.0	V	1
		V_{EE}	–20.0 to +0.3	V	1
Input voltage (1)		VT1	–0.3 to V_{CC} +0.3	V	2
Input voltage (2)		VT2	≤ VLCD	V	3
Input voltage (3)		VT1	≥ V_{EE}	V	4
Input voltage (4)		VT2	V_{EE} – 0.3 to VLCD + 0.3	V	5
Operating temperature		T_{opr}	–30 to + 75	°C	6
Storage temperature		T_{stg}	–55 to + 110	°C	

Notes:
1. The reference point is GND (0V)
2. Applies to pins M/S, DUTY, BP4 to BP0, $\overline{DOC}$, $\overline{DISPOFF}$, SHL, $\overline{RESET}$, CR, CL1, FLM, TEST1, TEST0 and FX0 to FX1.
3. Applies to pins VRH1 and VRH2.
   Supply the same voltage to pairs VRH1 and VRH2.
4. Applies to pins VRL1 and VRL2.
   Supply the same voltage to pairs VRL1 and VRL2.
5. Applies to pins VM1 and VM2.
   Supply the same voltage to pairs VM1 and VM2.
6. DC and AC characteristics are guaranteed at +75°C
7. If the LSI is used beyond its absolute maximum rating, it may be permanently damaged. It should always be used within the limits of its electrical characteristics in order to prevent malfunction or unreliability.

Electrical Characteristics

DC Characteristics (V_{CC} = 2.4 to 3.6V, GND = 0V, VLCD – V_{EE} = 30 to 43V, Ta = –30 to +75°C)[*6]

Item	Symbol	min.	typ.	max.	Unit	Measurement Condition	Notes
Input high level voltage	V_{IH1}	$0.8 \times V_{CC}$	—	V_{CC}	V		1
Input low level voltage	V_{IL1}	0	—	$0.2 \times V_{CC}$	V		1
Output high level voltage	V_{OH}	$0.9 \times V_{CC}$	—	—	V	I_{OH} = –50 µA	2
Output low level voltage	V_{OL}	—	—	$0.1 \times V_{CC}$	V	I_{OL} = +50 µA	2
Input leakage current (1)	I_{IL1}	–2.5	—	2.5	µA	VIN = V_{CC} to GND	1
Input leakage current (2)	I_{IL2}	–25	—	25	µA	VIN = VLCD to V_{EE}	3
Vi-Xj ON resistance	R_{ON}	—	0.8	1.2	kΩ	VLCD to V_{EE} = 40V, I_{ON} = 100µA	4
Current consumption (1)	I_{MS}	—	—	80	µA	Master mode 1/240 duty cycle, C_f = 100pF R_f = 150kΩ V_{CC} = 3.0V VLCD to V_{EE} = 40V	5
Current consumption (2)	I_{SL}	—	—	20	µA	Slave mode 1/240 duty cycle, f_{CL} = 15 kHz, V_{CC} = 3.0V VLCD to V_{EE} = 40V	5
Current consumption (3)	I_{LCD}	—	—	30	µA	Master mode 1/240 duty cycle, C_f = 100pF R_f = 150kΩ V_{CC} = 3.0V VLCD to V_{EE} = 40V	5

Notes: 1. Applied to input pins M/S, DUTY, BP4 to BP0, $\overline{\text{DISPOFF}}$, SHL, $\overline{\text{RESET}}$, TEST1, TEST0 and CR, and I/O pins, $\overline{\text{DOC}}$, CL1, and FLM during input state.

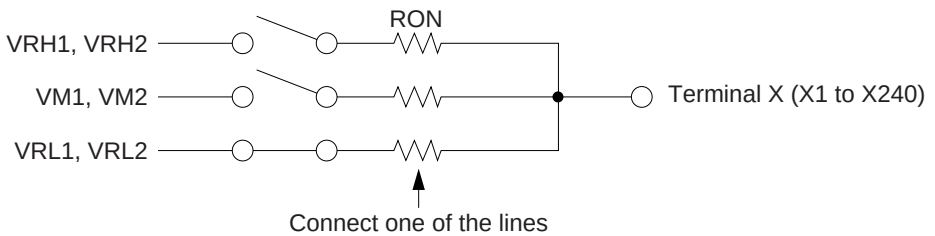
2. Applied to output pins, BLANK, FX1 and FX0, and I/O pins, DOC, CL1 and FLM, during output state.

3. Applied to VRH1, VRH2, VM1, VM2, VRL1 and VRL2. Don't connect any lines to X1 to X240.

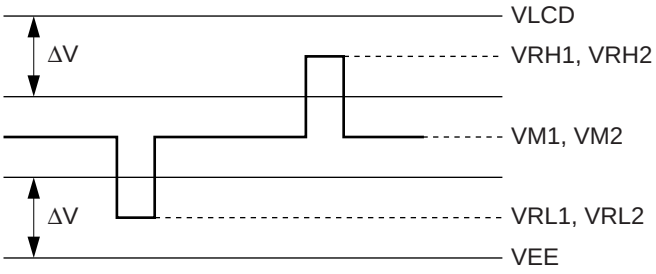
4 Resistance between terminal X and terminal V (one of VRH1, VRH2, VM1, VM2, VRL1 and VRL2) when load current flows through one of the terminals X1 to X240. This value is specified under the following conditions:

VRH = +23V, VRL = –17V

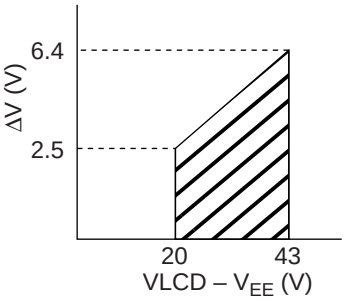
VM = 1/2 (VRH–VRL)



The following is a description of the range of power supply voltage for liquid crystal display drive. Apply positive voltage to VRH1 = VRH2 and negative voltage to VRL1 = VRL2 within the ΔV range. This range allows stable impedance on driver output (RON). Notice that ΔV depends on power supply voltage VLCD–VEE.



Correlation between driver output waveform and power supply voltage for liquid crystal display drive.

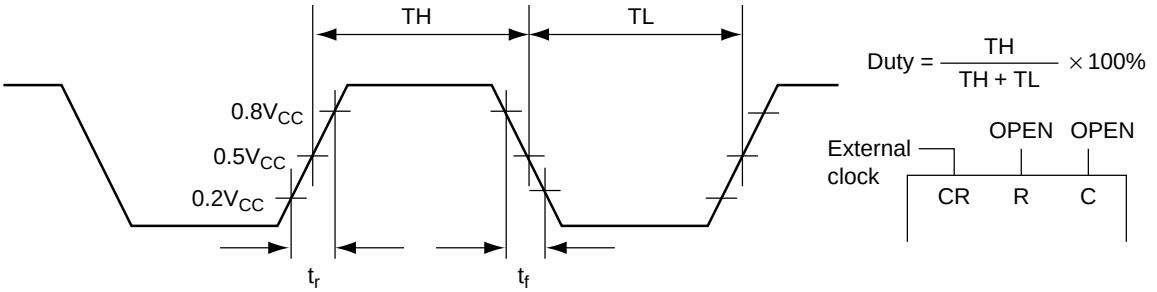


Correlation between power supply voltage VLCD – V_{EE} and ΔV.

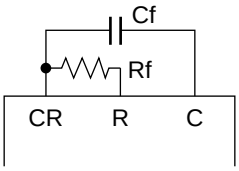
5. Input and Output currents are excluded. When a CMOS input is floating, excess current flows from the power supply to the input circuit. To avoid this, ViH and ViL must be held to V_{CC} and GND levels, respectively.
6. Specified at +75°C for die products.

Item	Symbol	min.	typ.	max.	Unit.	Measurement Condition	Notes
Operating frequency (1)	f_{opr1}	10	—	200	kHz	Master mode (External clock operation)	1
Operating frequency (2)	f_{opr2}	5	—	100	kHz	Slave mode frequency of CL1	2
Oscillation frequency	f_{OSC}	30	36	42	kHz	C_f = 100pF R_f = 150kΩ	4, 5
External clock duty	Duty	45	50	55	%	Master mode	3
External clock rising time	t_r	—	—	100	ns	Master mode	3
External clock falling time	t_f	—	—	100	ns	Master mode	3

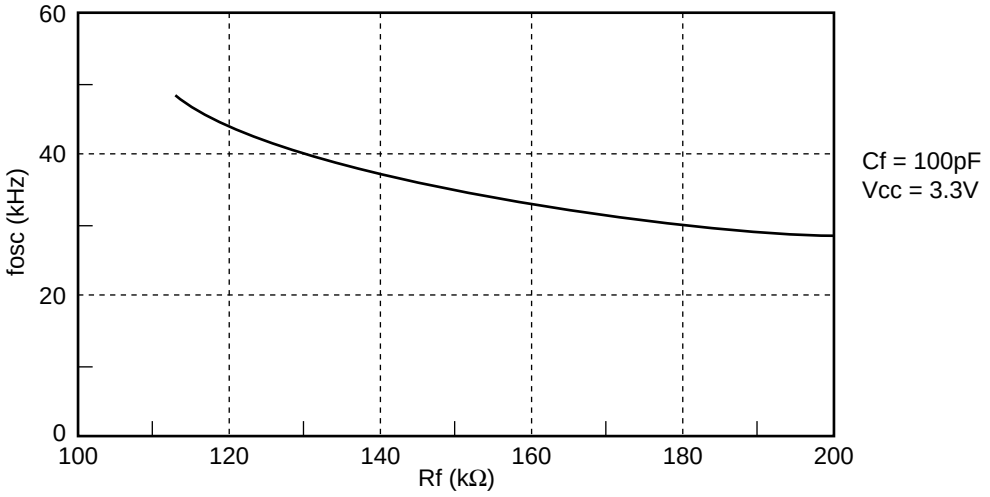
Notes: 1. External clock is supplied to CR pin during master mode, and C and R pins must be left open.
2. Applies to the clock which is supplied to CL1 during slave mode. CR must be connected to GND, and C and R pins must be left open.
3. Applies to the external clock which is supplied to CR during a master mode.



4. Connect resistance Rf and capacitance Cf as follows:



5. This figure shows a typical relation among oscillation frequency Rf and Cf. Oscillation frequency may vary with mounting conditions.



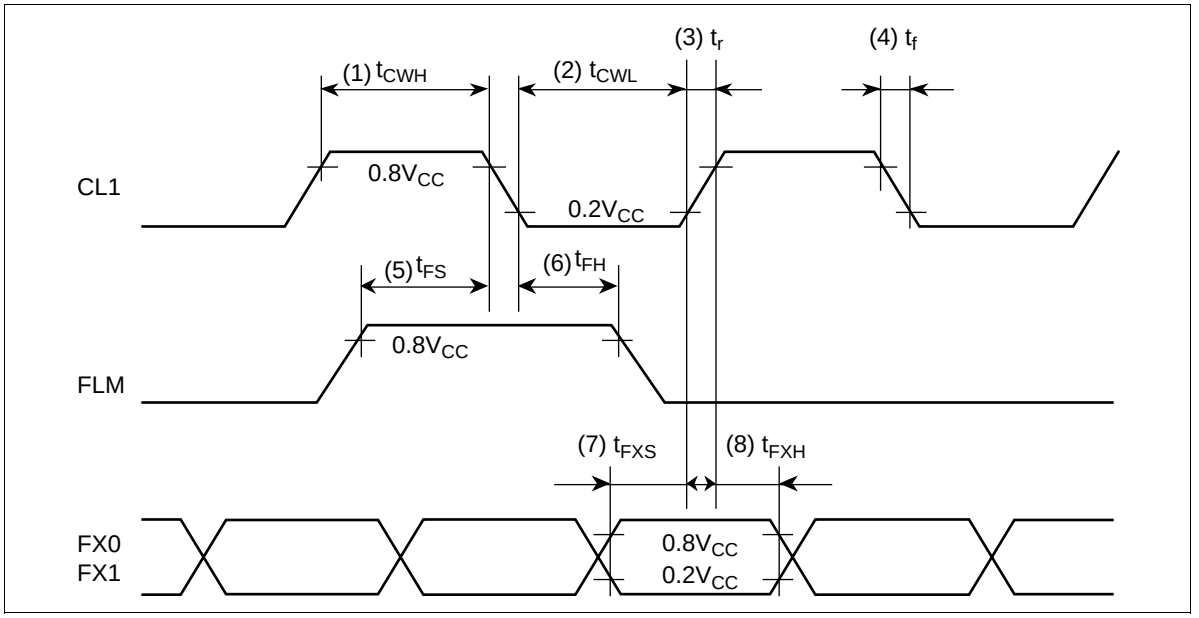
Oscillation Frequency Characteristics

AC Characteristic (V_{CC} = 2.4 to 3.6V, GND = 0V, Ta = –30 to +75°C)*

Slave Mode (M/$\overline{S}$ = GND)

No.	Item	Symbol	Applicable Pins	min.	max.	Units	Notes
(1)	CL1 high-level width	t_{CWH}	CL1	1.0	—	µs	
(2)	CL1 low-level width	t_{CWL}	CL1	1.0	—	µs	
(3)	CL1 rise time	t_r	CL1	—	100	ns	
(4)	CL1 fall time	t_f	CL1	—	100	ns	
(5)	FLM setup time	t_{FS}	FLM, CL1	2.0	—	µs	
(6)	FLM hold time	t_{FH}	FLM, CL1	1.0	—	µs	
(7)	FX0, FX1 setup time	t_{FXS}	FX0, FX1, CL1	2.0	—	µs	
(8)	FX0, FX1 hold time	t_{FXH}	FX0, FX1, CL1	1.0	—	µs	

Note: Specified at +75°C for die products.



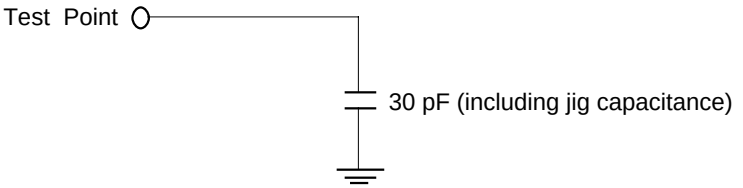
Slave Mode Timing

AC Characteristic (V_{CC} = 2.4 to 3.6V, GND = 0V, Ta = –30 to +75°C)[*2]

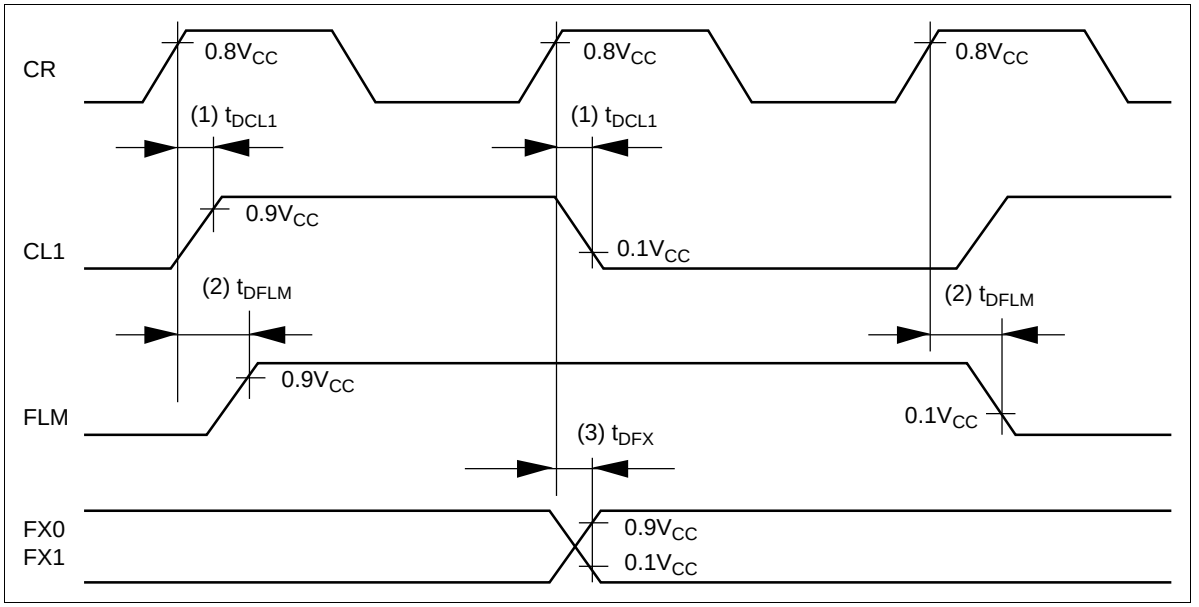
Master Mode (M/$\overline{S}$ = V_{CC})

No.	Item	Symbol	Applicable Pins	min.	max.	Units	Notes
(1)	CL1 delay time	t_{CL1}	CL1	1.0	—	µs	1
(2)	FLM delay time	t_{DFLM}	FLM	1.0	—	µs	1
(3)	FX0, FX1 delay time	t_{DFX}	FX0, FX1	1.0	—	µs	1

Notes: 1. The following load circuit is connected for specification



2. Specified at +75°C for die products.



Master Mode Timing

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