SMART
Modular Technologies

SM5322002
March 1993
Rev 0

SM5322002
8MByte (2M x 32) CMOS DRAM Module *(Static Column Mode)*

General Description

The SM5322002 is a high performance, 8-megabyte dynamic RAM module organized as 2M words by 32 bits, in a 72-pin, leadless, single-in-line memory module (SIMM) package. It offers static column mode capability at fast access times.

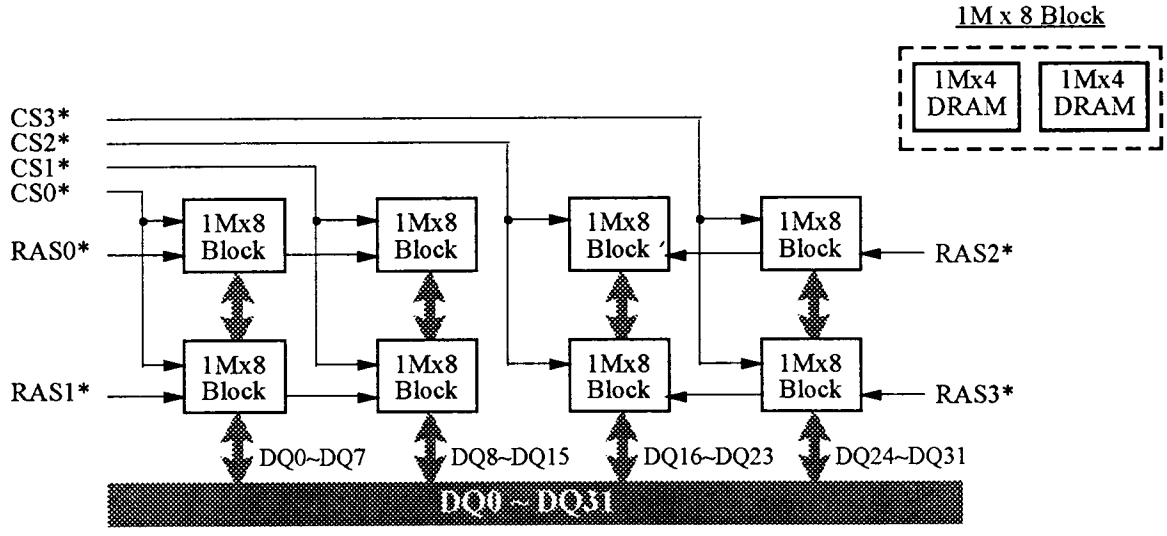
The module utilizes sixteen CMOS 1M x 4 dynamic RAMs in surface mount package on an epoxy laminate substrate. Each device is accompanied by a decoupling capacitor for improved noise immunity.

Control lines are provided such that byte control is possible.

Features

- High Density : 8Mbyte
- Fast Access Time of 60/70/80ns (max.)
- Low Power :
  4.93/4.49/3.96W (max.) - Active (60/70/80ns)
  0.176W (max.) - Standby (TTL)
  0.088W(max.) - Standby (CMOS)
- TTL-compatible inputs and outputs
- Separate power and ground planes to improve noise immunity
- Single power supply of 5V±10%
- PCB footprint of less than 1.49 sq. in. (Height: 0.95")

Functional Diagram



A0~A9 : To all devices
WE* : To all devices
OEs* of all devices are grounded

V_{CC} —||— V_{SS}
Decoupling Capacitors to all devices

Note: All specifications of this device are subject to change without notice.
"*" signifies complement signal.

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Pin Name

A0~A9	Addresses
DQ0~DQ31	Data Inputs/Outputs
CS0*~CS3*	Chip Select
RAS0*~RAS3*	Row Address Strobes
WE*	Read/Write
PD1~PD4	Presence Detects
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

Presence Detect Pins

Pin	60ns	70ns	80ns
PD1	NC	NC	NC
PD2	NC	NC	NC
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}

Ordering Information

Part Number	Speed
SM5322002-6	60 ns
SM5322002-7	70 ns
SM5322002-8	80 ns

Pin No.	Pin Designation	Pin No.	Pin Designation
1	V_{SS}	37	NC
2	DQ0	38	NC
3	DQ16	39	V_{SS}
4	DQ1	40	CS0*
5	DQ17	41	CS2*
6	DQ2	42	CS3*
7	DQ18	43	CS1*
8	DQ3	44	RAS0*
9	DQ19	45	RAS1*
10	V_{CC}	46	NC
11	NC	47	WE*
12	A0	48	NC
13	A1	49	DQ8
14	A2	50	DQ24
15	A3	51	DQ9
16	A4	52	DQ25
17	A5	53	DQ10
18	A6	54	DQ26
19	NC	55	DQ11
20	DQ4	56	DQ27
21	DQ20	57	DQ12
22	DQ5	58	DQ28
23	DQ21	59	V_{CC}
24	DQ6	60	DQ29
25	DQ22	61	DQ13
26	DQ7	62	DQ30
27	DQ23	63	DQ14
28	A7	64	DQ31
29	NC	65	DQ15
30	V_{CC}	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	RAS3*	69	PD3
34	RAS2*	70	PD4
35	NC	71	NC
36	NC	72	V_{SS}

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_T	- 1 to +7.0	V
Power Dissipation	P_T	16	W
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	Tstg	- 55 to +125	°C
Short Circuit Output Current	I_{OS}	50	mA

Recommended DC Operating Conditions
(T_A = 0 to +70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.4	-	6.5	V
V_{IL}	Input Low Voltage	-1	-	0.8	V

DC Characteristics
(V_{CC} = 5V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	Test Conditions	Max. -6	Max. -7	Max. -8	Unit	Note
Operating Current	I_{CC1}	t_{RC} = min.; RAS*, CS* cycling	896	816	736	mA	1, 2
Standby Current	I_{CC2}	TTL Interface RAS*, CS* = V_{IH} D_{out} = High-Z	32	32	32	mA	
		CMOS Interface RAS*, CS* ≥ V_{CC} - 0.2V D_{out} = High-Z	16	16	16	mA	
RAS* only Refresh Current	I_{CC3}	t_{RC} = Min	896	816	736	mA	2
Standby Current	I_{CC5}	RAS* = V_{IH}, CS* = V_{IL}, D_{out} = Enable	80	80	80	mA	1
CS*-Before-RAS* Refresh Current	I_{CC6}	t_{RC} = Min.	896	816	736	mA	
Static Column Mode Current	I_{CC7}	t_{SC} = Min.	896	816	736	mA	1, 3

DC Characteristics (contd.)

Parameter	Symbol	Test Conditions	-6		-7		-8		Unit
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	$0V \le V_{in} \le 7V$	-160	160	-160	160	-160	160	μA
Output Leakage Current	I_{LO}	$0V \le V_{out} \le 7V$	-20	20	-20	20	-20	20	μA
Output High Voltage	V_{OH}	High I_{out} = -5mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V
Output Low Voltage	V_{OL}	Low I_{out} = 4.2mA	0	0.4	0	0.4	0	0.4	V

Notes: 1. Values depend on output load condition when the device is selected. ICC max. is specified at the output open condition.
2. Address can be changed once or less while RAS* = V_{IL} .
3. Address can be changed once or less while CS* = V_{IH} .

Capacitance
(T_A =+25°C, V_{CC} = 5V±10%)

Parameter	Symbol	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	85	pF	1
Input Capacitance (WE*)	C_{I2}	115	pF	1
Input Capacitance (RAS* & CS*)	C_{I3}	31	pF	1
Input/Output Capacitance (DQ0~DQ31)	$C_{I/O}$	23	pF	1, 2

Notes: 1. Capacitance is measured with Boonton Meter or effective capacitance method.
2. CS* = V_{IH} to disable D_{out}.

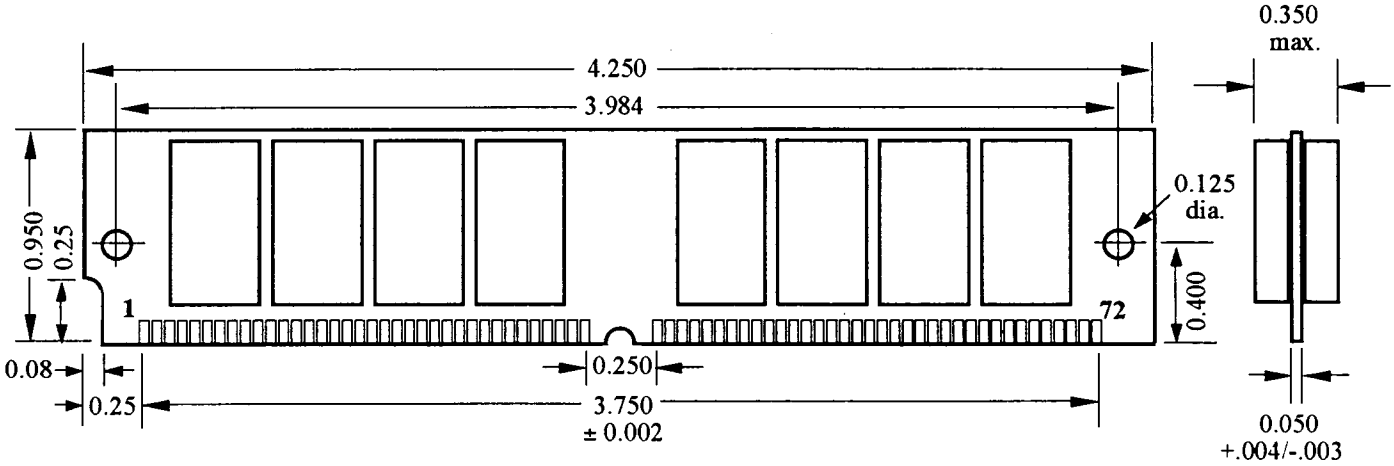
AC Characteristics (1, 2)
(T_A = 0 to +70 °C, V_{CC} = 5.0V±10%, V_{SS} = 0V)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read/write cycle time	t_{RC}	110	-	130	-	150	-	ns	
Access time from RAS*	t_{RAC}	-	60	-	70	-	80	ns	3, 4
Access time from CS*	t_{ACS}	-	15	-	20	-	20	ns	3, 4, 5
Access time from column address	t_{AA}	-	30	-	35	-	40	ns	3, 10
Output buffer turn-off time	t_{OFF}	0	15	0	20	0	20	ns	6
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
RAS* precharge time	t_{RP}	40	-	50	-	60	-	ns	
RAS* pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	
RAS* hold time	t_{RSH}	15	-	20	-	20	-	ns	
CS* hold time	t_{CSH}	60	-	70	-	80	-	ns	
CS* pulse width	t_{SP}	15	10000	20	10000	20	10000	ns	
RAS* to CS* delay time	t_{RCD}	20	45	20	50	20	60	ns	4
RAS* to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	10
CS* to RAS* precharge time	t_{SRS}	10	-	10	-	10	-	ns	
Row address set-up time	t_{ASR}	0	-	0	-	0	-	ns	
Row address hold time	t_{RAH}	10	-	10	-	10	-	ns	
Column address set-up time	t_{ASW}	0	-	0	-	0	-	ns	
Column address hold time	t_{AHW}	15	-	15	-	15	-	ns	
Column address to RAS* lead time	t_{RAL}	30	-	35	-	40	-	ns	
Read command set-up time	t_{RCS}	0	-	0	-	0	-	ns	
Read command hold time to CS*	t_{RCH}	0	-	0	-	0	-	ns	8
Read command hold time to RAS*	t_{RRH}	0	-	0	-	0	-	ns	
Write command hold time	t_{WCH}	15	-	15	-	15	-	ns	
Write command pulse width	t_{WP}	10	-	10	-	10	-	ns	
Write command to RAS* lead time	t_{RWL}	15	-	20	-	20	-	ns	
Write command to CS* lead time	t_{CWL}	15	-	20	-	20	-	ns	
Data-in set-up time	t_{DS}	0	-	0	-	0	-	ns	9
Data-in hold time	t_{DH}	15	-	15	-	15	-	ns	9
Refresh period (1024 cycles)	t_{REF}	-	16	-	16	-	16	ms	
Write command set-up time	t_{WCS}	0	-	0	-	0	-	ns	7
CS* set-up time (CBR refresh)	t_{CSR}	10	-	10	-	10	-	ns	1
CS* hold time (CBR refresh)	t_{CHR}	10	-	10	-	10	-	ns	1
RAS* precharge to CS* hold time	t_{ZRH}	10	-	10	-	10	-	ns	
Static Column mode cycle time	t_{SC}	40	-	45	-	50	-	ns	
CS* precharge time (Static Column Mode)	t_{SI}	10	-	10	-	10	-	ns	
RAS* pulse width (Static Column Mode)	t_{RASC}	-	100000	-	100000	-	100000	ns	11

Notes:
1. An initial pause of atleast 500µs is required after power-up followed by any eight RAS* cycles before device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are refernce levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measure with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) limit can be met; t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{ACS}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is non restrictive operating parameter. It is included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain at high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the CS* leading edge in early write cycles.
10. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
11. t_{RASC} defines RAS* pulse width in fast page mode cycles.

Physical Dimensions

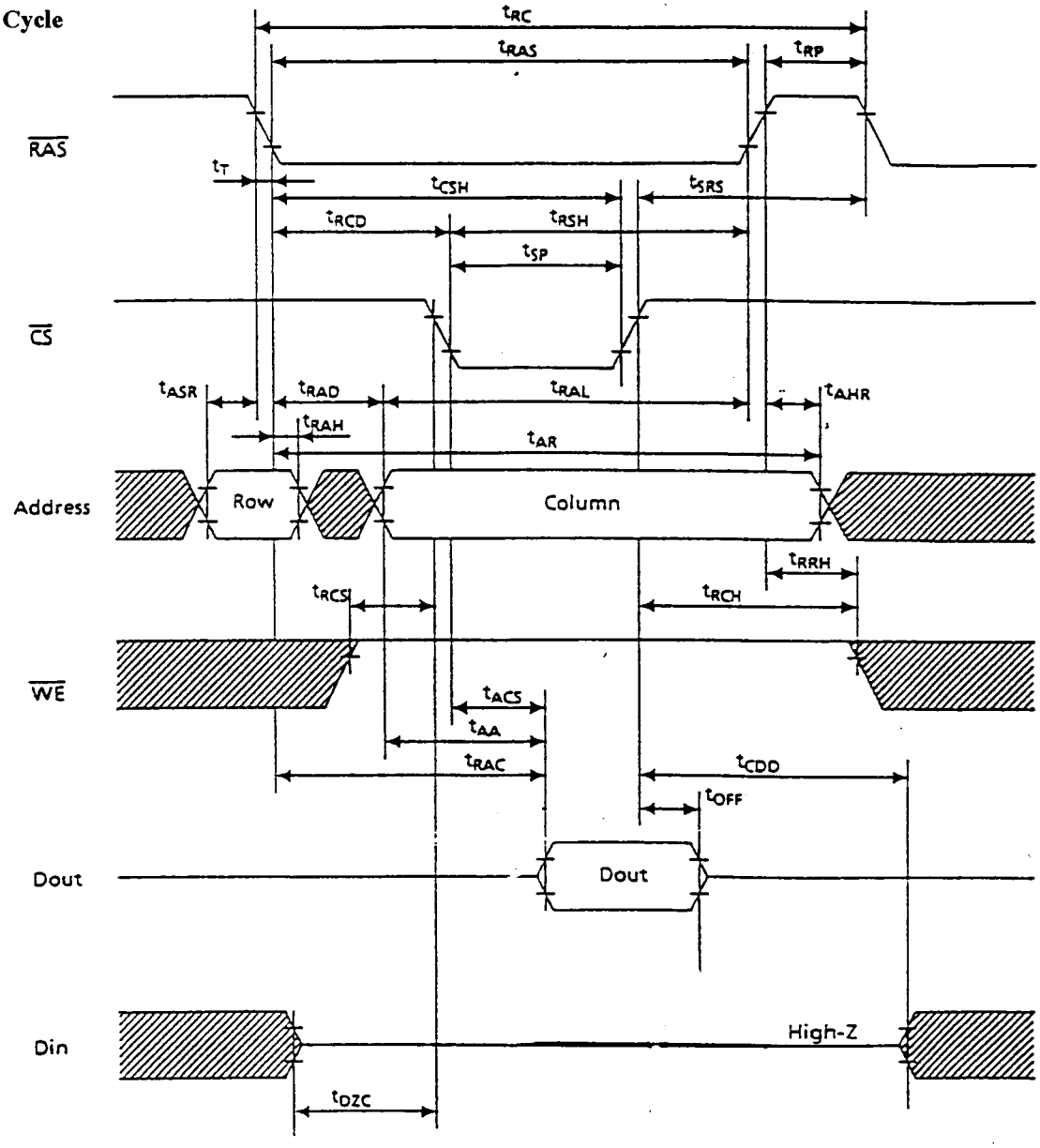
72-pin SIMM



(All dimensions are in inches with ±0.005" tolerance unless otherwise specified)

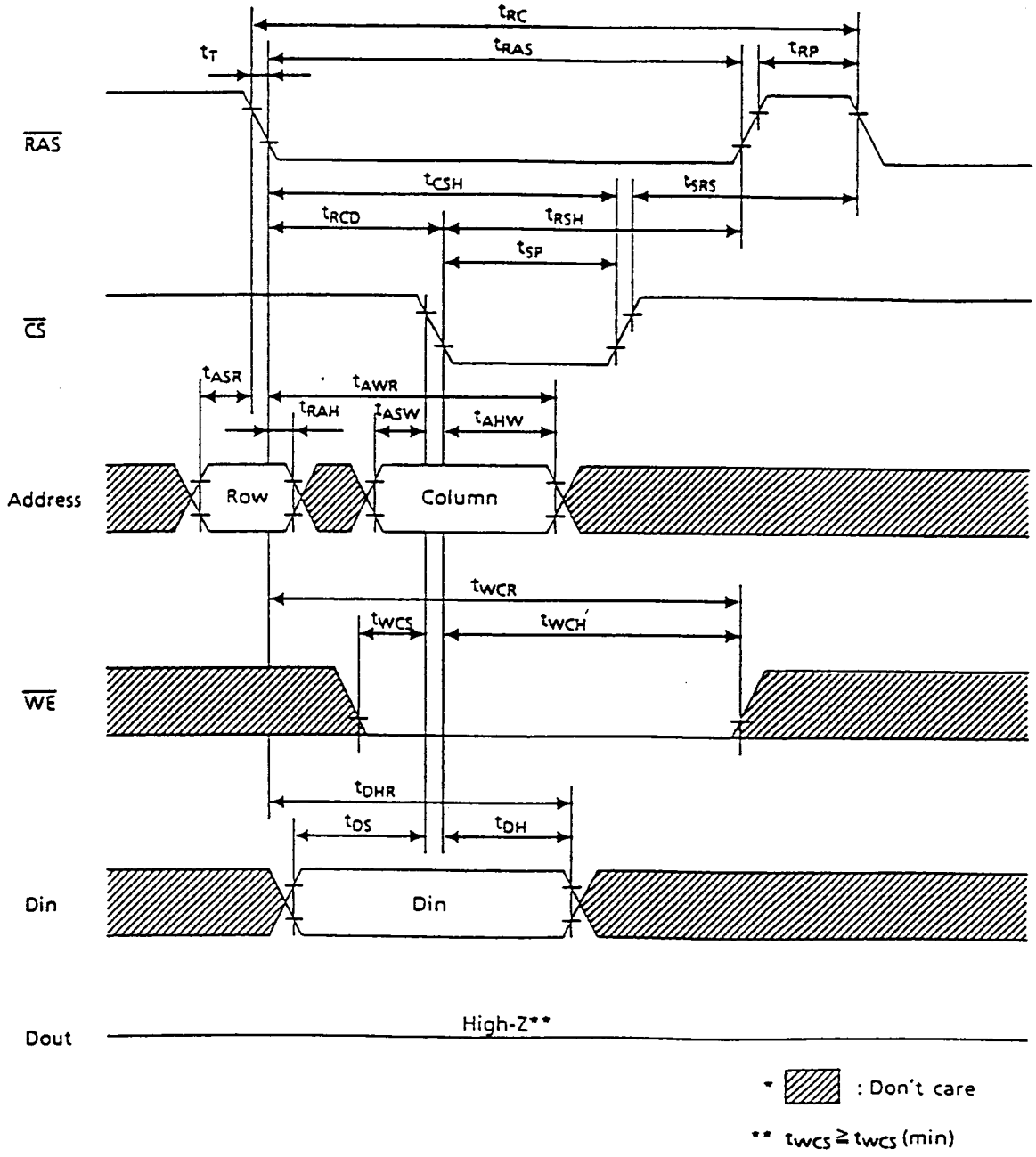
TIMING WAVEFORMS

Read Cycle

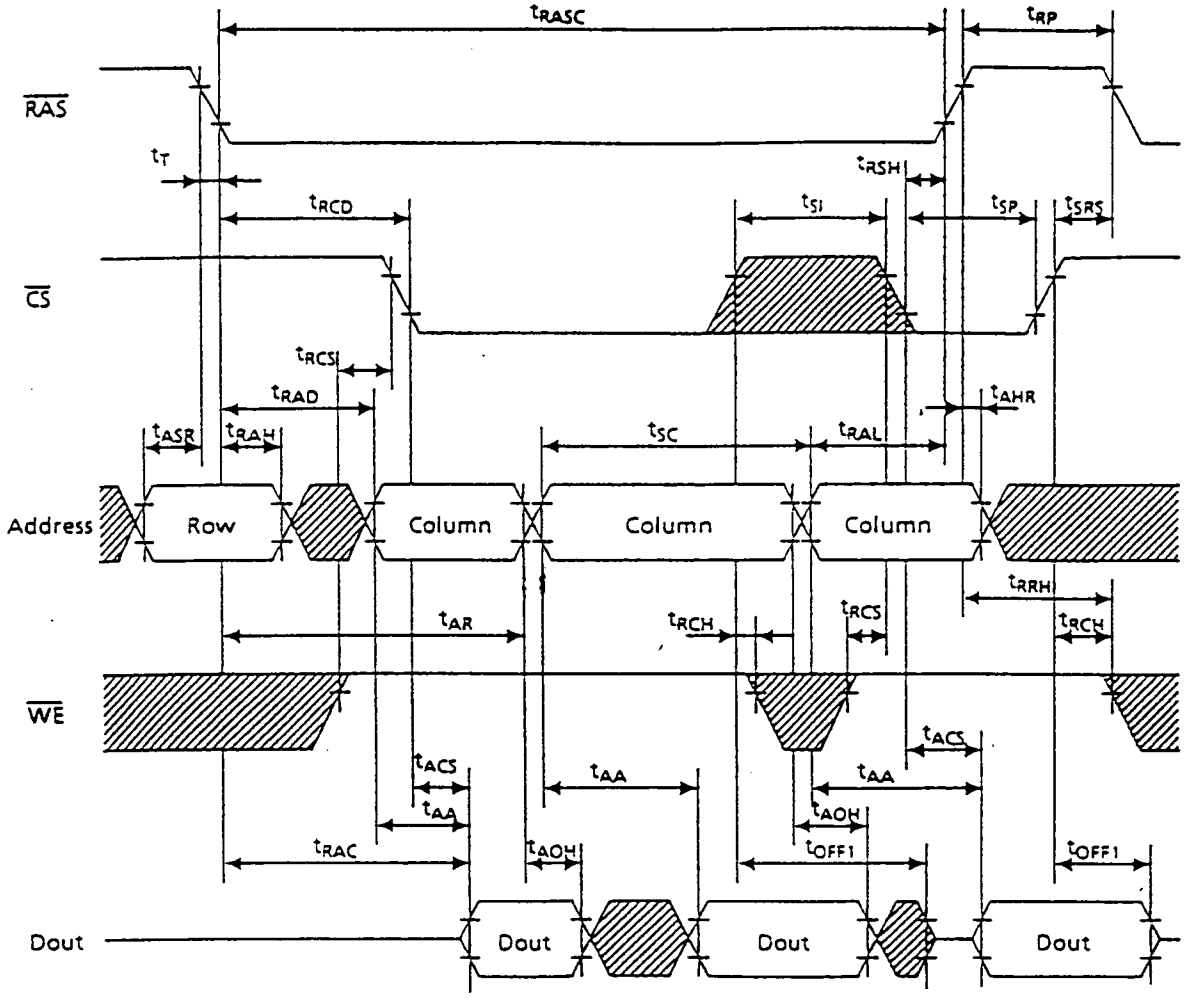


* ▨ : Don't care

Early Write Cycle

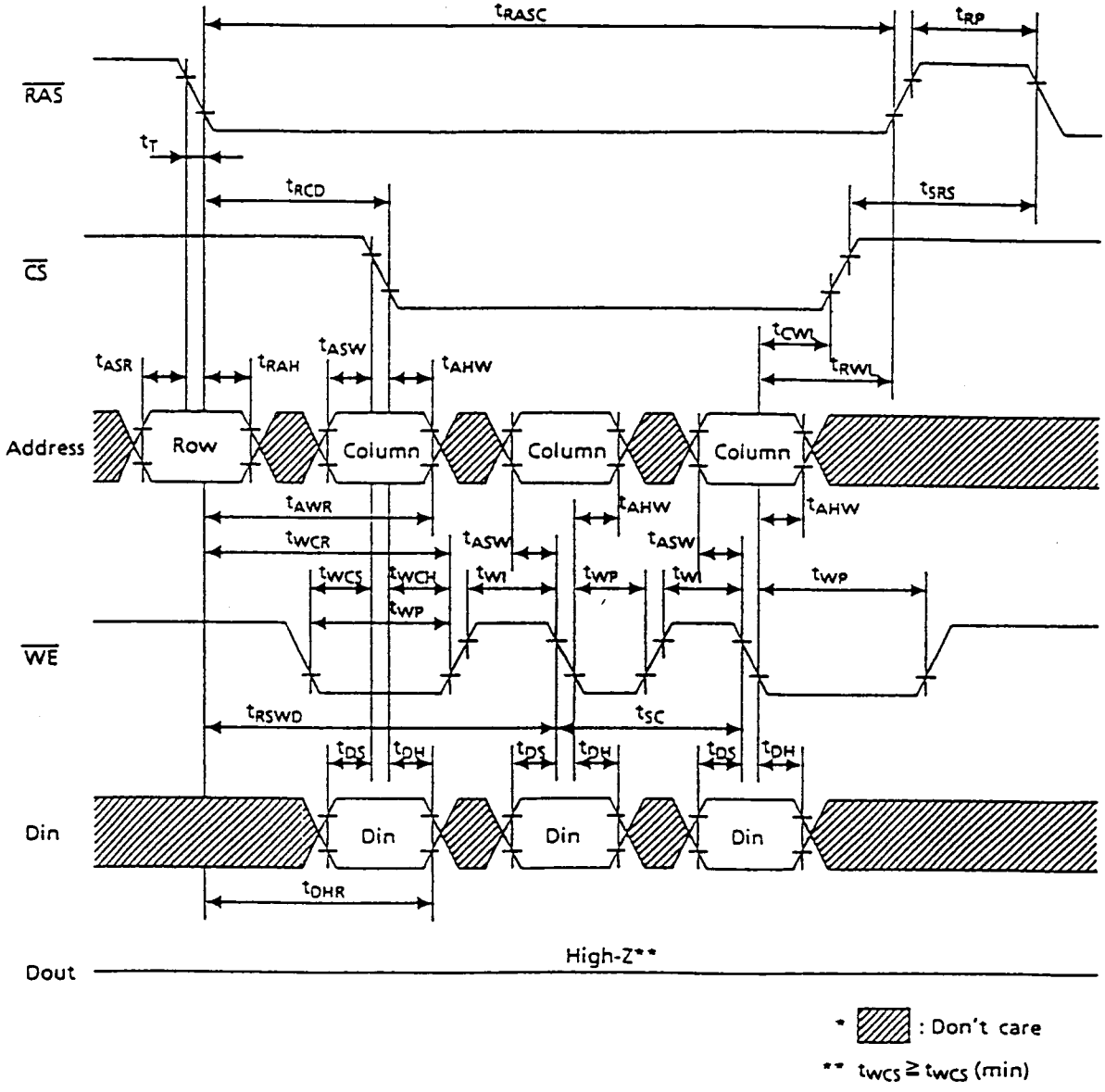


Static Column Mode Read Cycle

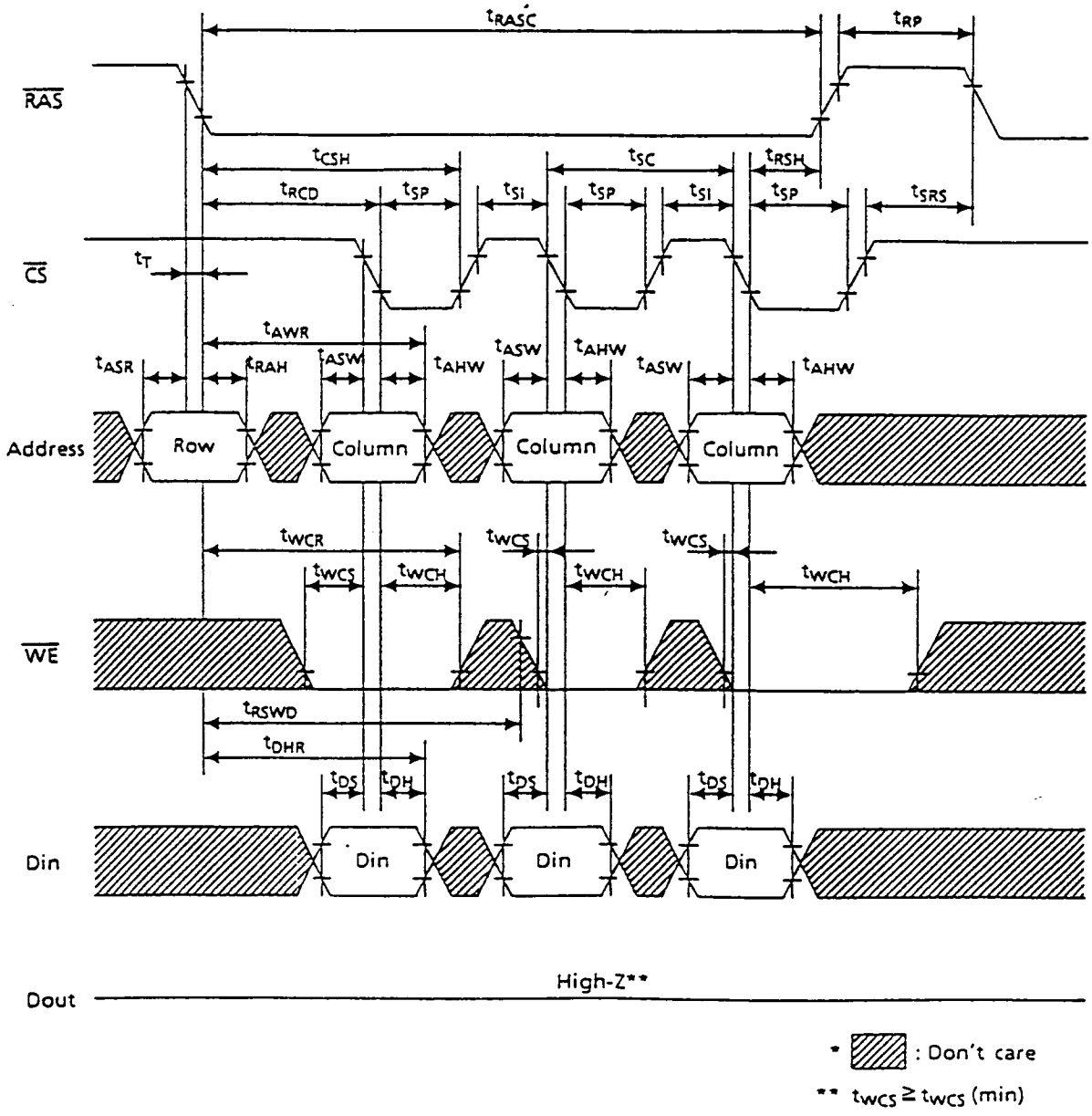


* : Don't care

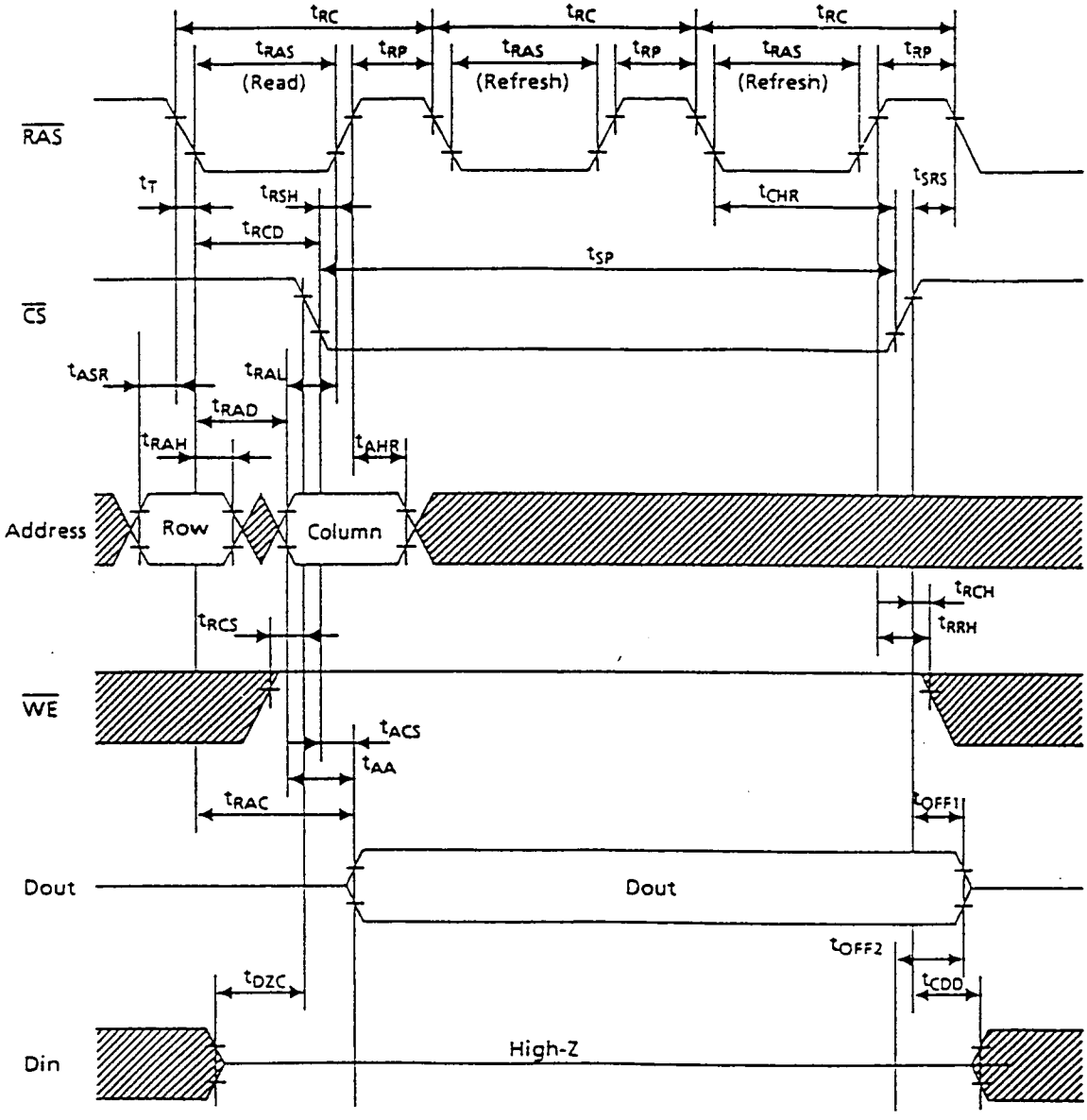
Static Column Mode Write Cycle (1)



Static Column Mode Write Cycle (2)

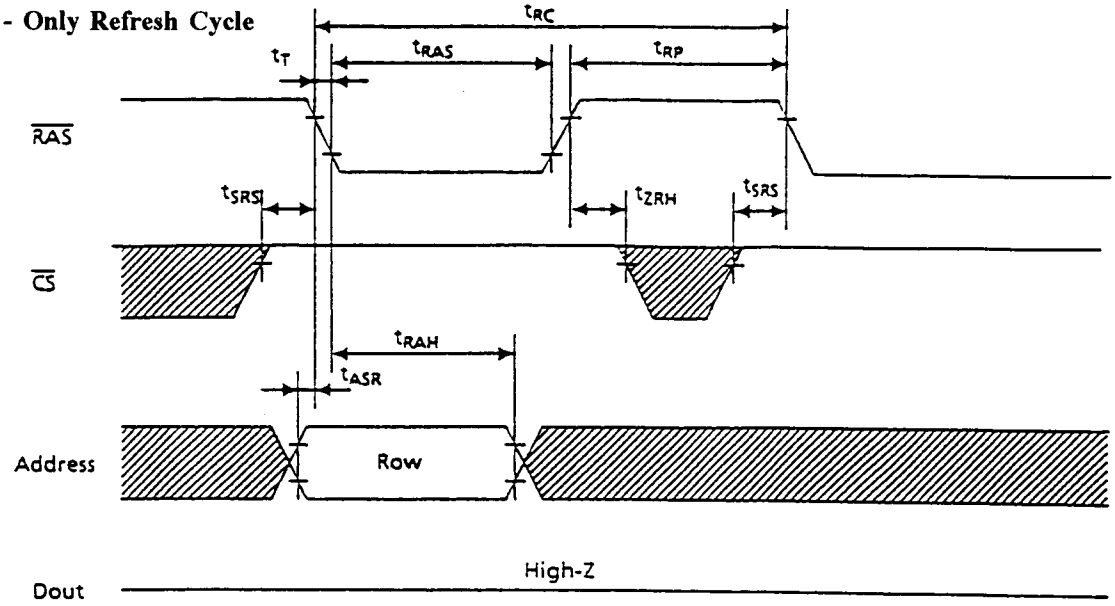


Hidden Refresh Cycle



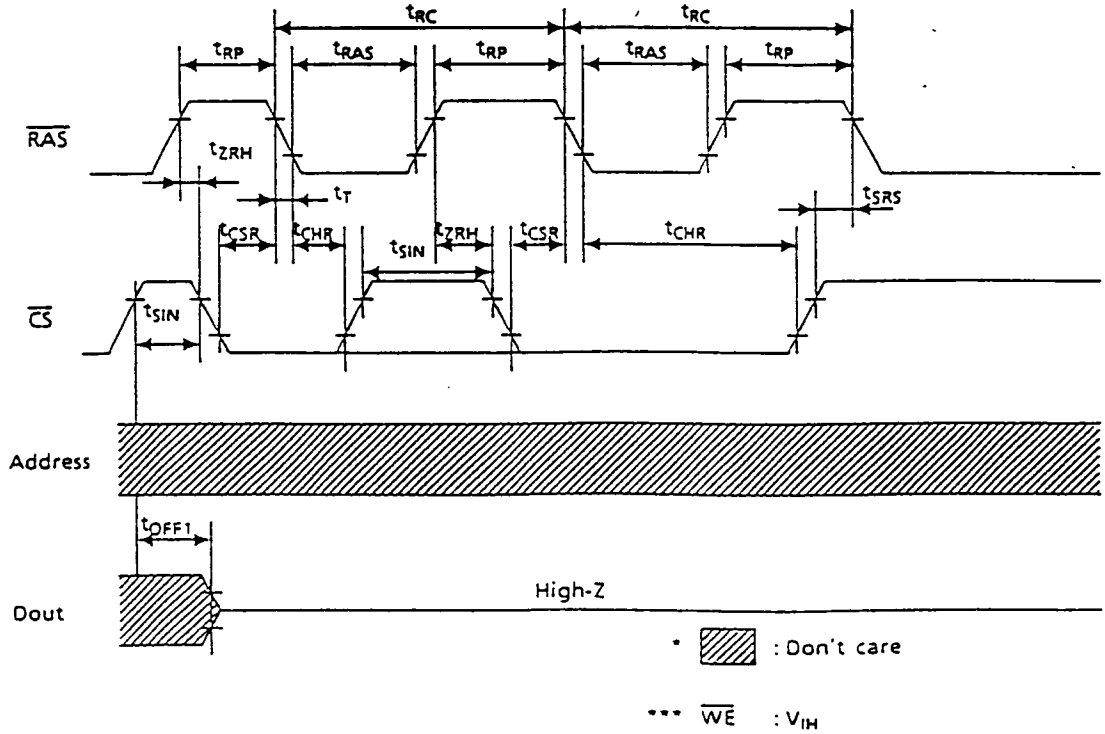
* : Don't care

RAS* - Only Refresh Cycle



* WE : Don't care
** : Don't care
*** Refresh address : A0 – A9 (AX0 – AX9)

CS* - Before - RAS* Refresh Cycle



* : Don't care

*** WE : V_{IH}