

SN54ABT8373, SN74ABT8373 SCAN TEST DEVICES WITH OCTAL D-TYPE LATCHES

SCBS487 – JULY 1994

- Members of the Texas Instruments **SCOPE™** Family of Testability Products
- Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture
- Functionally Equivalent to SN54/74F373 and SN54/74ABT373 in the Normal-Function Mode
- **SCOPE™** Instruction Set:
 - IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, CLAMP and HIGHZ
 - Parallel-Signature Analysis at Inputs With Masking Option
 - Pseudo-Random Pattern Generation From Outputs
 - Sample Inputs/Toggle Outputs
 - Binary Count From Outputs
 - Even-Parity Opcodes
- State-of-the-Art **EPIC-IIB™** BiCMOS Design Significantly Reduces Power Dissipation
- Package Options Include Plastic Small-Outline Packages (DW), Ceramic Chip Carriers (FK), and Standard Ceramic DIPs (JT)

description

The SN54ABT8373 and SN74ABT8373 scan test devices with octal D-type latches are members of the Texas Instruments SCOPE™ testability integrated circuit family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

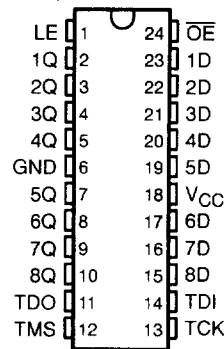
In the normal mode, these devices are functionally equivalent to the SN54/74F373 and SN54/74ABT373 octal D-type latches. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary-test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE™ octal D-type latches.

In the test mode, the normal operation of the SCOPE™ D-type latches is inhibited and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary-scan test operations as described in IEEE Standard 1149.1-1990.

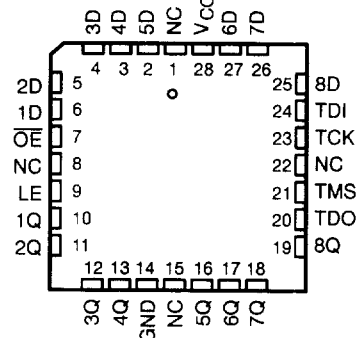
Four dedicated test pins are used to control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry performs other testing functions such as parallel-signature analysis (PSA) on data inputs and pseudo-random pattern generation (PRPG) from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54ABT8373 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT8373 is characterized for operation from –40°C to 85°C.

SN54ABT8373 ... JT PACKAGE
SN74ABT8373 ... DW PACKAGE
(TOP VIEW)



SN54ABT8373 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

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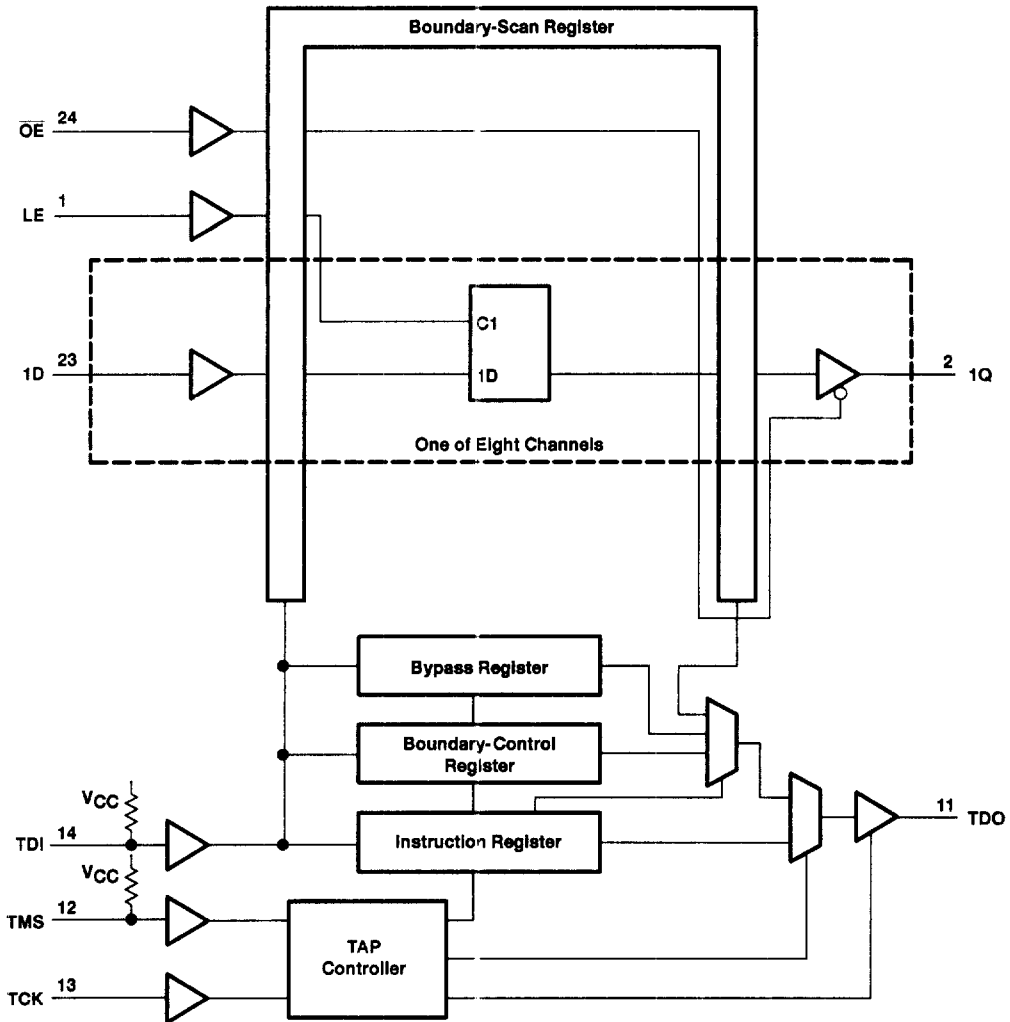
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FUNCTION TABLE
(normal mode)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

functional block diagram



Pin numbers shown are for the DW and JT packages.

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Terminal Functions

TERMINAL NAME	DESCRIPTION
GND	Ground
LE	Normal-function latch-enable input. See function table for normal-mode logic.
\overline{OE}	Normal-function output-enable input. See function table for normal-mode logic.
TCK	Test clock. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four terminals required by IEEE Standard 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four terminals required by IEEE Standard 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four terminals required by IEEE Standard 1149.1-1990. TMS input directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected.
VCC	Supply voltage
1D-8D	Normal-function data inputs. See function table for normal-mode logic.
1Q-8Q	Normal-function data outputs. See function table for normal-mode logic.

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test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, namely TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram illustrates the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As illustrated, the device contains an 8-bit instruction register and three test-data registers: an 18-bit boundary-scan register, an 11-bit boundary-control register, and a 1-bit bypass register.

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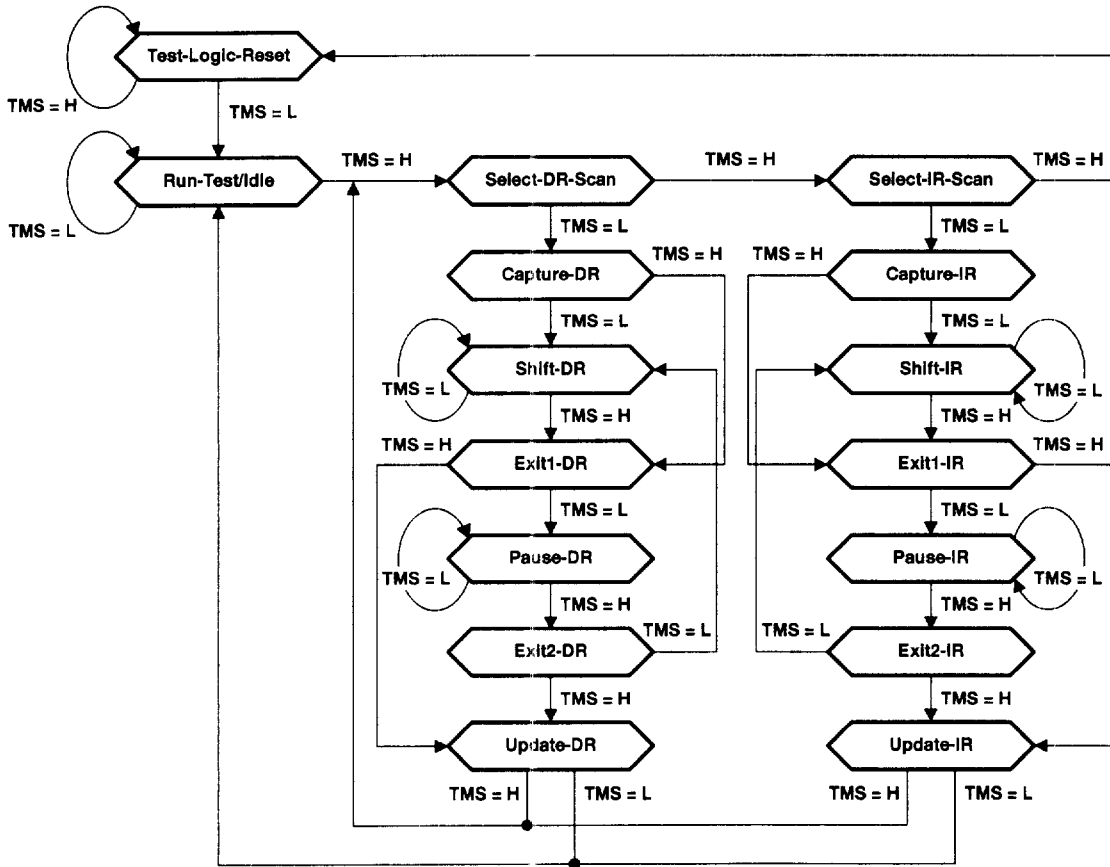


Figure 1. TAP-Controller State Diagram



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state diagram description

The TAP controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram is illustrated Figure 1 and is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As illustrated, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the 'ABT8373, the instruction register is reset to the binary value 11111111, which selects the BYPASS instruction. Each bit in the boundary-scan register is reset to logic 0 except bit 16 which is reset to logic 1. The boundary-control register is reset to the binary value 0000000010, which selects the PSA test operation with no input masking.

Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state can also be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic can be actively running a test or can be idle.

The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK upon which the TAP controller exits the Capture-DR state.

Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-DR state.

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Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register.

On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

Update-DR

If the current instruction calls for the selected data register to be updated with current data, then such update occurs on the falling edge of TCK following entry to the Update-DR state.

Capture-IR

When an instruction register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK upon which the TAP controller exits the Capture-IR state.

For the 'ABT8373, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to the active state. TDO enables to the logic level present in the least significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-IR state.

Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register.

On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

Update-IR

The current instruction is updated and takes effect on the falling edge of TCK following entry to the Update-IR state.

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register overview

With the exception of the bypass register, any test register can be thought of as a serial-shift register with a shadow latch on each bit. The bypass register differs in that it contains only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

instruction register description

The instruction register (IR) is eight bits long and specifies what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the three data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the 'ABT8373. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated, and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 11111111, which selects the BYPASS instruction. The IR order of scan is illustrated in Figure 2.

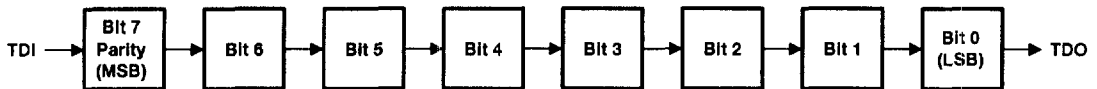


Figure 2. Instruction Register Order of Scan

data register description

boundary-scan register

The boundary-scan register (BSR) is 18 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin, and one BSC for each normal-function output pin. The BSR is used 1) to store test data that is to be applied internally to the inputs of the normal on-chip logic and/or externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, the value of each BSC is reset to logic 0 except bit 16 which is reset to logic 1.

The BSR order of scan is from TDI through bits 17–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

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Table 1. Boundary-Scan-Register Configuration

BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL
17	LE	15	D8	7	Q8
16	\overline{OE}	14	D7	6	Q7
—	—	13	D6	5	Q6
—	—	12	D5	4	Q5
—	—	11	D4	3	Q4
—	—	10	D3	2	Q3
—	—	9	D2	1	Q2
—	—	8	D1	0	Q1

boundary-control register

The boundary-control register (BCR) is 11 bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include PRPG, PSA with input masking, and binary count up (COUNT). Table 4 shows the test operations decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 00000000010, which selects the PSA test operation with no input masking.

The BCR order of scan is from TDI through bits 10–0 to TDO. Table 2 shows the BCR bits and their associated test control signals.

Table 2. Boundary-Control-Register Configuration

BCR BIT NUMBER	TEST CONTROL SIGNAL	BCR BIT NUMBER	TEST CONTROL SIGNAL	BCR BIT NUMBER	TEST CONTROL SIGNAL
10	MASK8	6	MASK4	2	OPCODE2
9	MASK7	5	MASK3	1	OPCODE1
8	MASK6	4	MASK2	0	OPCODE0
7	MASK5	3	MASK1	—	—

bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation.

During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is illustrated in Figure 3.

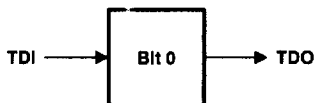


Figure 3. Bypass Register Order of Scan

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Instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

Table 3. Instruction-Register Opcodes

BINARY CODE† BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER	MODE
00000000	EXTEST	Boundary scan	Boundary scan	Test
10000001	BYPASS‡	Bypass scan	Bypass	Normal
10000010	SAMPLE/PRELOAD	Sample boundary	Boundary scan	Normal
00000011	INTEST	Boundary scan	Boundary scan	Test
10000100	BYPASS‡	Bypass scan	Bypass	Normal
00000101	BYPASS‡	Bypass scan	Bypass	Normal
00000110	HIGHZ	Control boundary to high impedance	Bypass	Modified test
10000111	CLAMP	Control boundary to 1/0	Bypass	Test
10001000	BYPASS‡	Bypass scan	Bypass	Normal
00001001	RUNT	Boundary run test	Bypass	Test
00001010	READBN	Boundary read	Boundary scan	Normal
10001011	READBT	Boundary read	Boundary scan	Test
00001100	CELLTST	Boundary self test	Boundary scan	Normal
10001101	TOPHIP	Boundary toggle outputs	Bypass	Test
10001110	SCANCN	Boundary-control register scan	Boundary control	Normal
00001111	SCANCT	Boundary-control register scan	Boundary control	Test
All others	BYPASS	Bypass scan	Bypass	Normal

† Bit 7 is used to maintain even parity in the 8-bit instruction.

‡ The BYPASS instruction is executed in lieu of a SCOPE * instruction that is not supported in the 'ABT8373.

boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST and INTEST instructions. The BSR is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. Data that has been scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data that has been scanned into the output BSCs is applied to the device output pins. The device operates in the test mode.

bypass scan

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. The device operates in the normal mode.

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control boundary to high impedance

This instruction conforms to the IEEE Standard 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

control boundary to 1/0

This instruction conforms to the IEEE Standard 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the output BSCs is applied to the device output pins. The device operates in the test mode.

boundary run test

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the BCR is executed during Run-Test/Idle. The five test operations decoded by the BCR are: sample inputs/toggle outputs (TOPSIP), PRPG, PSA, simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

boundary read

The BSR is selected in the scan path. The value in the BSR remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

boundary self test

The BSR is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift-register and shadow-latch elements of the BSR. The device operates in the normal mode.

boundary toggle outputs

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the output BSCs is toggled on each rising edge of TCK in Run-Test/Idle, updated in the shadow latches, and applied to the device output pins on each falling edge of TCK in Run-Test/Idle. Data in the input BSCs remains constant and is applied to the inputs of the normal on-chip logic. Data appearing at the device input pins is not captured in the input BSCs. The device operates in the test mode.

boundary-control-register scan

The BCR is selected in the scan path. The value in the BCR remains unchanged during Capture-DR. This operation must be performed before a boundary-run test operation to specify which test operation is to be executed.

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boundary-control-register opcode description

The BCR opcodes are decoded from BCR bits 2–0 as shown in Table 4. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

Table 4. Boundary-Control-Register Opcodes

BINARY CODE BIT 2 → BIT 0 MSB → LSB	DESCRIPTION
X00	Sample inputs/toggle outputs (TOPSIP)
X01	Pseudo-random pattern generation/16-bit mode (PRPG)
X10	Parallel-signature analysis/16-bit mode (PSA)
011	Simultaneous PSA and PRPG/8-bit mode (PSA/PRPG)
111	Simultaneous PSA and binary count up/8-bit mode (PSA/COUNT)

It should be noted, in general, that while the control input BSCs (bits 17–16) are not included in the sample, toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSC (bit 16 of the BSR) does control the drive state (active or high impedance) of the device output pins.

PSA Input masking

Bits 10–3 of the BCR specify device input pins to be masked from PSA operations. Bit 10 selects masking for device input pin D8. Bit 3 selects masking for device input pin D1. Bits intermediate to 10 and 3 mask corresponding device input pins in order from most significant to least significant, as indicated in Table 3. When the mask bit that corresponds to a particular device input has a logic 1 value, the device input pin is masked from any PSA operation, meaning that the state of the device input pin is ignored and has no effect on the generated signature. Otherwise, when a mask bit has a logic 0 value, the corresponding device input is not masked from the PSA operation.

sample inputs/toggle outputs (TOPSIP)

Data appearing at the device input pins is captured in the shift-register elements of the input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. Data in the shift-register elements of the output BSCs is toggled on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK.

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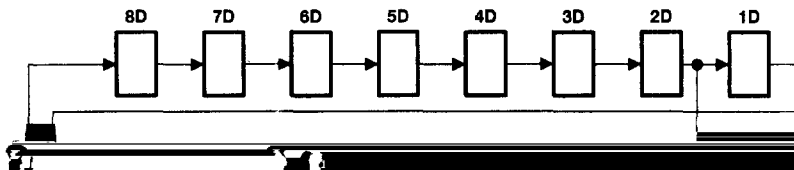


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pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the device output pins on each falling edge of TCK. This data also is updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. Figure 4 illustrates the 16-bit linear-feedback shift-register algorithm through which the patterns are generated. An initial seed value should be scanned into the BSR before to performing this operation. Note that a seed value of all zeroes does not produce additional patterns.



simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the device input pins is compressed into an 8-bit parallel signature in the shift-register elements of the input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. At the same time, an 8-bit pseudo-random pattern is generated in the shift-register elements of the output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the device output pins on each falling edge of TCK. Figure 6 illustrates the 8-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the BSR before performing this operation. A seed value of all zeroes does not produce additional patterns.

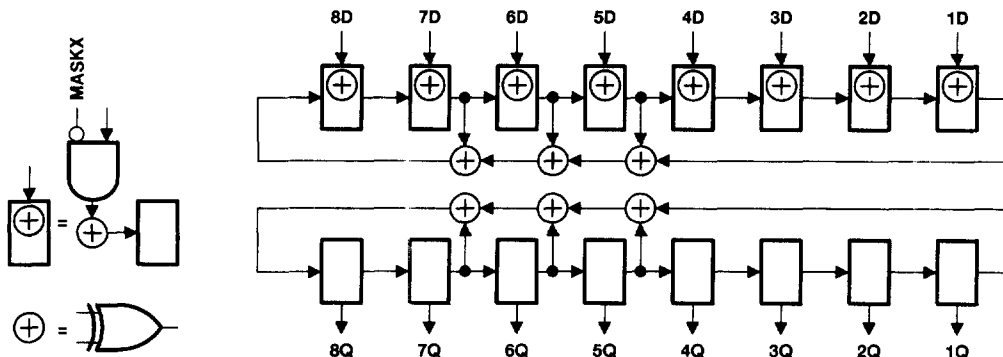


Figure 6. 8-Bit PSA/PRPG Configuration

simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the device input pins is compressed into an 8-bit parallel signature in the shift-register elements of the input BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the input BSCs and applied to the inputs of the normal on-chip logic. At the same time, an 8-bit binary count-up pattern is generated in the shift-register elements of the output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the device output pins on each falling edge of TCK. Figure 7 illustrates the 8-bit linear-feedback shift-register algorithm through which the signature is generated. An initial seed value should be scanned into the BSR before performing this operation.

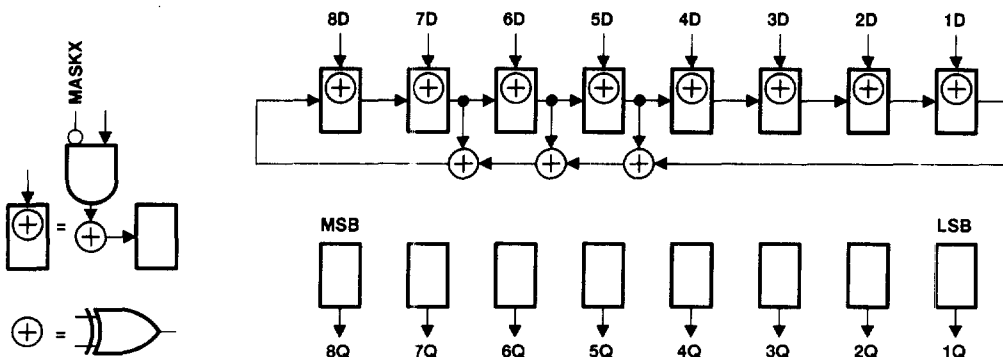


Figure 7. 8-Bit PSA/COUNT Configuration

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timing description

All test operations of the 'ABT8373 are synchronous to TCK. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as illustrated in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is illustrated in Figure 8. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 5 explains the operation of the test circuitry during each TCK cycle.

Table 5. Explanation of Timing Example

TCK CYCLE(S)	TAP STATE AFTER TCK	DESCRIPTION
1	Test-Logic-Reset	TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state.
2	Run-Test/Idle	
3	Select-DR-Scan	
4	Select-IR-Scan	
5	Capture-IR	The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state.
6	Shift-IR	TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
7-13	Shift-IR	One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR.
14	Exit1-IR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
15	Update-IR	The IR is updated with the new instruction (BYPASS) on the falling edge of TCK.
16	Select-DR-Scan	
17	Capture-DR	The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state.
18	Shift-DR	TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
19-20	Shift-DR	The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO.
21	Exit1-DR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
22	Update-DR	In general, the selected data register is updated with the new data on the falling edge of TCK.
23	Select-DR-Scan	
24	Select-IR-Scan	
25	Test-Logic-Reset	Test operation completed

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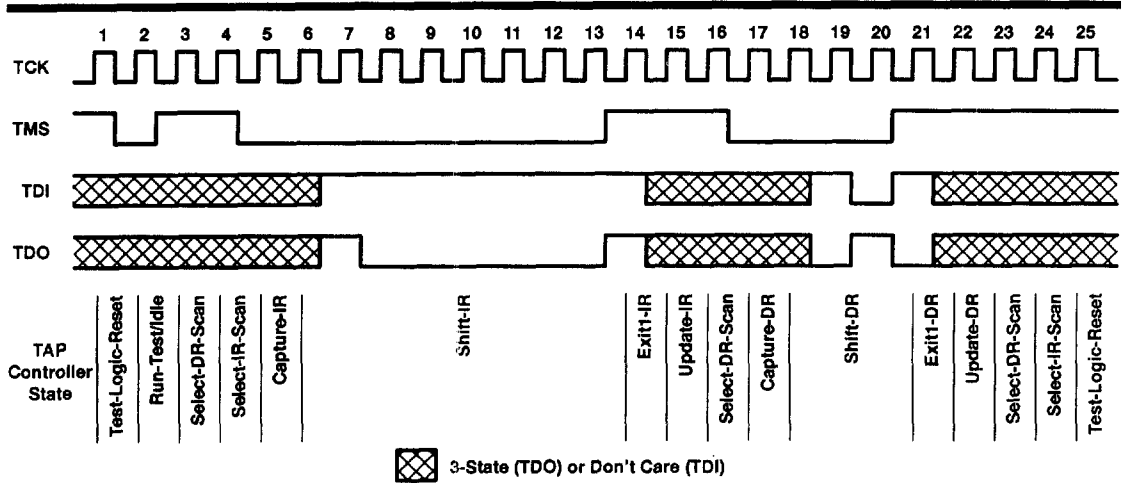


Figure 8. Timing Example

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1)	-0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_{O1} : SN54ABT8373	96 mA
SN74ABT8373	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT8373		SN74ABT8373		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage	0.8		0.8		V
V_I	input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	-24		-32		mA
I_{OL}	Low-level output current	48		64		mA
$\Delta t/\Delta v$	Input transition rise or fall rate	10		10		ns/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54ABT8373		SN74ABT8373		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2		-1.2		-1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$	2.5			2.5		2.5		V
	$V_{CC} = 5\text{ V}$, $I_{OH} = -3\text{ mA}$	3			3		3		
	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -24\text{ mA}$	2			2				
	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -32\text{ mA}$	2*					2		
V_{OL}	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 48\text{ mA}$			0.55		0.55			V
	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 64\text{ mA}$			0.55*			0.55		
I_I	$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}$ or GND	D, LE, \overline{OE} , TCK		± 1		± 1		± 1	μA
I_{IH}	$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}$	TDI, TMS		10		10		10	μA
I_{IL}	$V_{CC} = 5.5\text{ V}$, $V_I = \text{GND}$	TDI, TMS		-160		-160		-160	μA
I_{OZH}	$V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$			50		50		50	μA
I_{OZL}	$V_{CC} = 5.5\text{ V}$, $V_O = 0.5\text{ V}$			-50		-50		-50	μA
I_{off}	$V_{CC} = 0$, V_I or $V_O \leq 5.5\text{ V}$			± 100				± 100	μA
I_{CEX}	$V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$	Outputs high		50		50		50	μA
$I_{O^{\pm}}$	$V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$	-50	-100	-180	-50	-180	-50	-180	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}$ or GND	$I_O = 0$,	Outputs high	2		2		2	mA
			Outputs low	30		30		30	
			Outputs disabled	2		2		2	
ΔI_{CC}^{\S}	$V_{CC} = 5.5\text{ V}$, Other inputs at V_{CC} or GND	One input at 3.4 V		1.5		1.5		1.5	mA
C_i	$V_I = 2.5\text{ V}$ or 0.5 V			3					pF
C_o	$V_O = 2.5\text{ V}$ or 0.5 V			8					pF

* On products compliant to MIL-STD-883, Class B, this parameter does not apply.

† All typical values are at $V_{CC} = 5\text{ V}$.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 3 and Figure 9)

			SN54ABT8373		SN74ABT8373		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	TCK	0	50	0	50	MHz
t_w	Pulse duration	TCK high or low			5		ns
t_{su}	Setup time	D or LE or \overline{OE} before TCK↑			5		ns
		TDI before TCK↑			6		
		TMS before TCK↑			6		
t_h	Hold time	D or LE or \overline{OE} after TCK↑			0		ns
		TDI after TCK↑			0		
		TMS after TCK↑			0		
t_d	Delay time	Power up to TCK↑			50		ns
t_r	Rise time	V_{CC} power up			1		μs

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 3 and Figure 9)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			SN54ABT8373		SN74ABT8373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	Q						2	7	ns
t _{PHL}								2	7	
t _{PLH}	LE	Q						2	7	ns
t _{PHL}								2	7	
t _{PZH}	OE	Q						2	8	ns
t _{PZL}								2	8	
t _{PHZ}	OE	Q						2	8	ns
t _{PLZ}								2	8	

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 3 and Figure 9)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			SN54ABT8373		SN74ABT8373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f _{max}	TCK		50	90		50		50	MHz	
t _{PLH}	TCK↓	Q						2	12	ns
t _{PHL}								2	12	
t _{PLH}	TCK↓	TDO						2	7	ns
t _{PHL}								2	7	
t _{PZH}	TCK↓	Q						2	13	ns
t _{PZL}								2	13	
t _{PZH}	TCK↓	TDO						2	7	ns
t _{PZL}								2	7	
t _{PHZ}	TCK↓	Q						2	14	ns
t _{PLZ}								2	14	
t _{PHZ}	TCK↓	TDO						2	9	ns
t _{PLZ}								2	9	

NOTE 3: Product preview specifications are design goals only and are subject to change without notice.

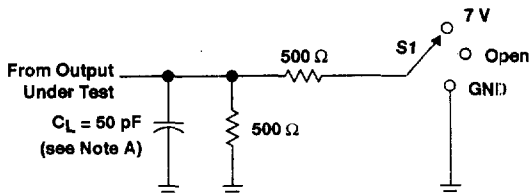
PRODUCT PREVIEW



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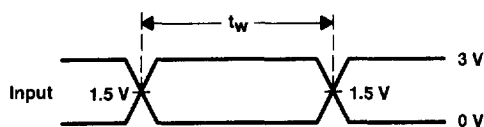
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PARAMETER MEASUREMENT INFORMATION

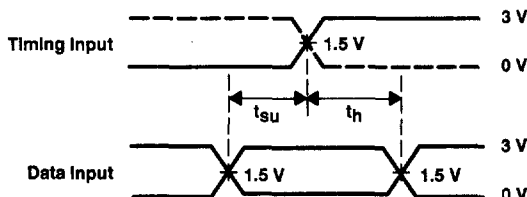


LOAD CIRCUIT FOR OUTPUTS

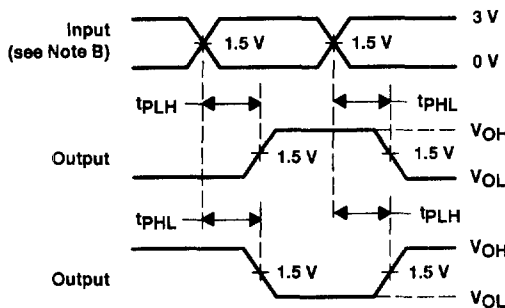
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



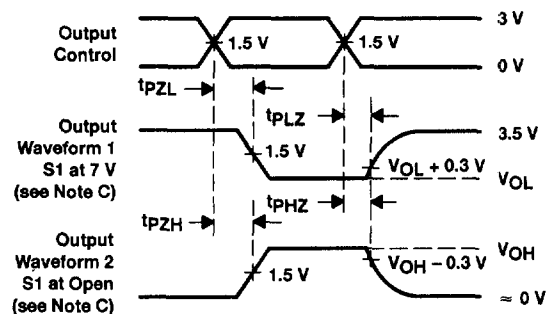
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 9. Load Circuit and Voltage Waveforms

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