

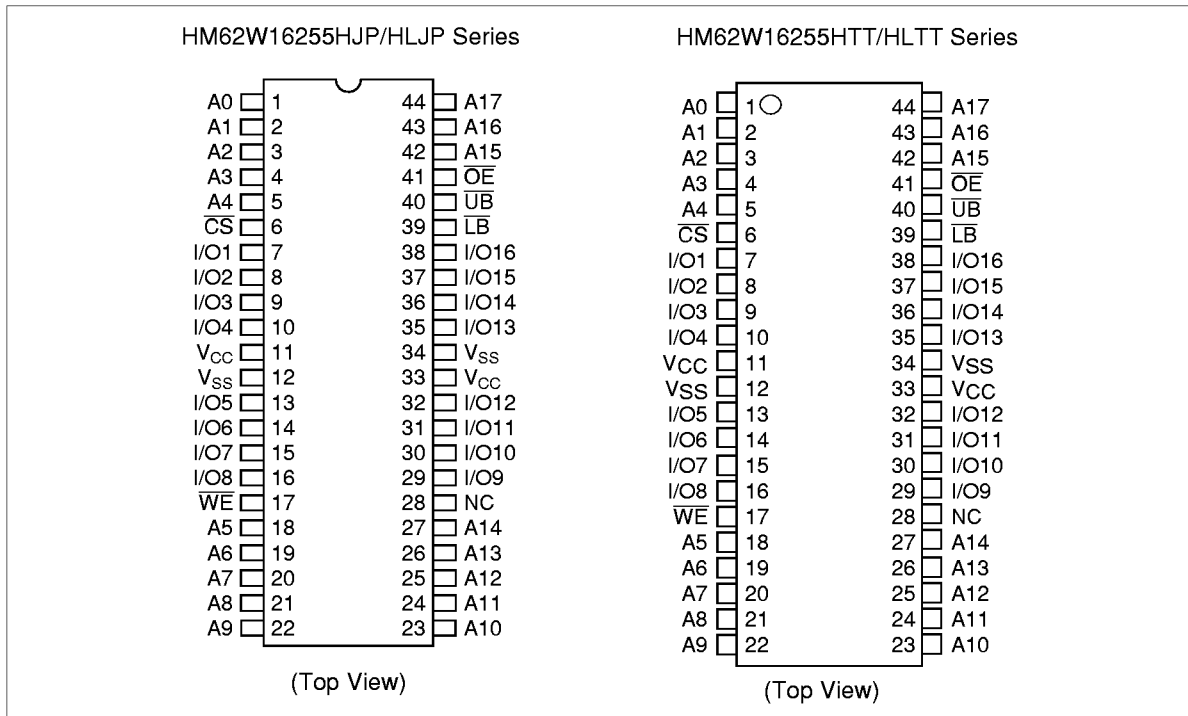


# HM62W16255H Series

## Ordering Information

Type No.	Access time	Package
HM62W16255HJP-12	12 ns	400-mil 44-pin plastic SOJ (CP-44D)
HM62W16255HJP-15	15 ns	
HM62W16255HLJP-12	12 ns	400-mil 44-pin plastic SOJ (TTP-44DE)
HM62W16255HLJP-15	15 ns	
HM62W16255HTT-12	12 ns	400-mil 44-pin plastic SOJ (TTP-44DE)
HM62W16255HTT-15	15 ns	
HM62W16255HLTT-12	12 ns	400-mil 44-pin plastic SOJ (TTP-44DE)
HM62W16255HLTT-15	15 ns	

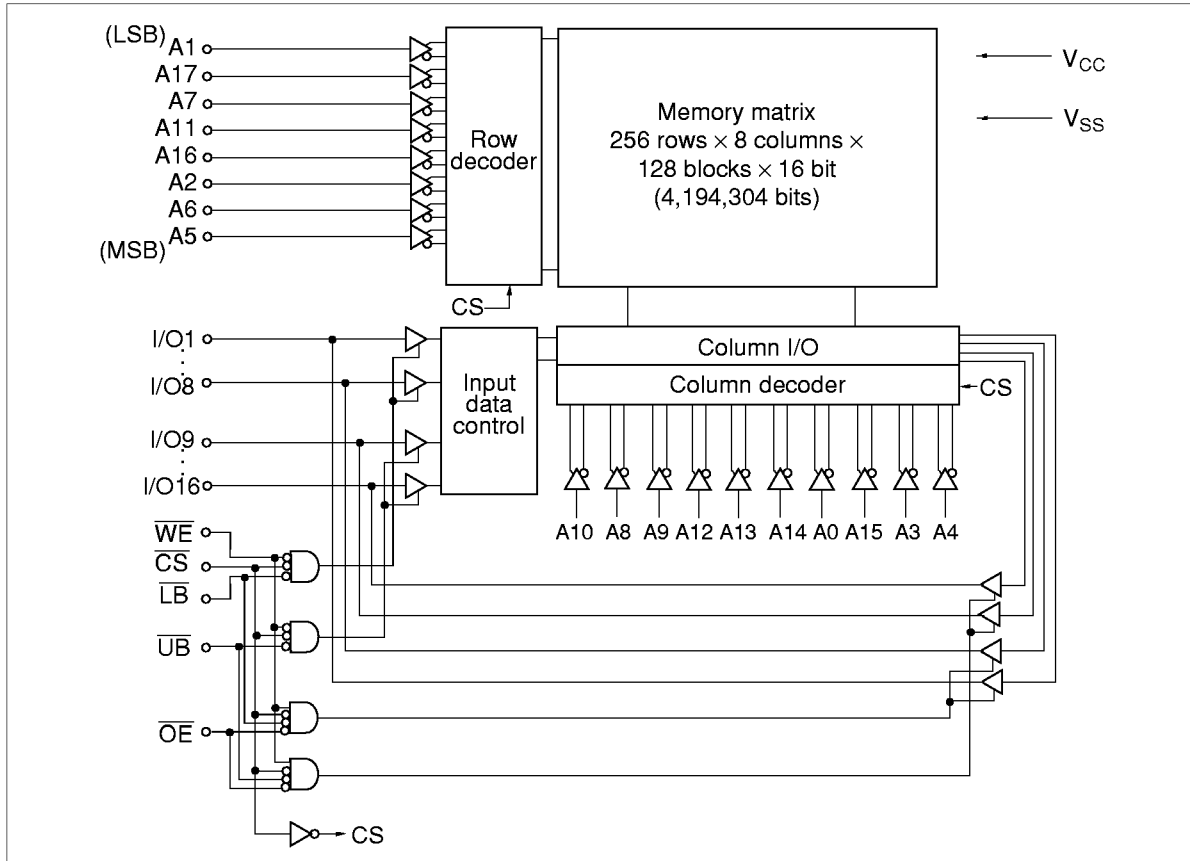
## Pin Arrangement



**Pin Description**

Pin name	Function
A0 to A17	Address input
I/O1 to I/O16	Data input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
$\overline{UB}$	Upper byte select
$\overline{LB}$	Lower byte select
$V_{CC}$	Power supply
$V_{SS}$	Ground
NC	No connection

**Block Diagram**



## HM62W16255H Series

### Operation Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	Mode	$V_{CC}$ current	I/O1–I/O8	I/O9–I/O16	Ref. cycle
H	x	x	x	x	Standby	$I_{SB}, I_{SB1}$	High-Z	High-Z	—
L	H	H	x	x	Output disable	$I_{CC}$	High-Z	High-Z	—
L	L	H	L	L	Read	$I_{CC}$	Output	Output	Read cycle
L	L	H	L	H	Lower byte read	$I_{CC}$	Output	High-Z	Read cycle
L	L	H	H	L	Upper byte read	$I_{CC}$	High-Z	Output	Read cycle
L	L	H	H	H	—	$I_{CC}$	High-Z	High-Z	—
L	x	L	L	L	Write	$I_{CC}$	Input	Input	Write cycle
L	x	L	L	H	Lower byte write	$I_{CC}$	Input	High-Z	Write cycle
L	x	L	H	L	Upper byte write	$I_{CC}$	High-Z	Input	Write cycle
L	x	L	H	H	—	$I_{CC}$	High-Z	High-Z	—

Note: x: H or L

### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to $V_{SS}$	$V_{CC}$	-0.5 to +4.6	V
Voltage on any pin relative to $V_{SS}$	$V_T$	-0.5* <sup>1</sup> to $V_{CC} + 0.5$ * <sup>2</sup>	V
Power dissipation	$P_T$	1.0	W
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	-55 to +125	°C
Storage temperature under bias	$T_{bias}$	-10 to +85	°C

Notes: 1.  $V_T$  (min) = -2.0 V for pulse width (under shoot)  $\leq 8$  ns  
 2.  $V_T$  (max) =  $V_{CC} + 2.0$  V for pulse width (over shoot)  $\leq 8$  ns

## HM62W16255H Series

### Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}^{*3}$	3.0	3.3	3.6	V
	$V_{SS}^{*4}$	0	0	0	V
Input voltage	$V_{IH}$	2.2	—	$V_{CC} + 0.5^{*2}$	V
	$V_{IL}$	$-0.5^{*1}$	—	0.8	V

- Notes: 1.  $V_{IL}$  (min) = -2.0 V for pulse width (under shoot)  $\leq 8$  ns  
 2.  $V_{IH}$  (max) =  $V_{CC} + 2.0$  V for pulse width (over shoot)  $\leq 8$  ns  
 3. The supply voltage with all  $V_{CC}$  pins must be on the same level.  
 4. The supply voltage with all  $V_{SS}$  pins must be on the same level.

### DC Characteristics (Ta = 0 to +70°C, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ , $V_{SS} = 0 \text{ V}$ )

Parameter	Symbol	Min	Typ <sup>*1</sup>	Max	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	—	2	$\mu\text{A}$	$V_{in} = V_{SS}$ to $V_{CC}$
Output leakage current <sup>*1</sup>	$ I_{LO} $	—	—	2	$\mu\text{A}$	$V_{in} = V_{SS}$ to $V_{CC}$
Operating power supply current	12 ns cycle $I_{CC}$	—	—	180	mA	Min cycle $\overline{CS} = V_{IL}$ , $I_{out} = 0 \text{ mA}$ Other inputs = $V_{IH}/V_{IL}$
		15 ns cycle $I_{CC}$	—	—		
Standby power supply current	12 ns cycle $I_{SB}$	—	—	60	mA	Min cycle, $\overline{CS} = V_{IH}$ , Other inputs = $V_{IH}/V_{IL}$
		15 ns cycle $I_{SB}$	—	—		
	$I_{SB1}$	—	0.05	5	mA	f = 0 MHz $V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2 \text{ V}$ , (1) $0 \text{ V} \leq V_{in} \leq 0.2 \text{ V}$ or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2 \text{ V}$
— <sup>*2</sup>	0.05 <sup>*2</sup>	1.0 <sup>*2</sup>				
Output voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 8 \text{ mA}$
	$V_{OH}$	2.4	—	—	V	$I_{OH} = -4 \text{ mA}$

- Note: 1. Typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_a = +25^\circ\text{C}$  and not guaranteed.  
 2. This characteristics is guaranteed only for L-version.

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## HM62W16255H Series

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**Capacitance** ( $T_a = +25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ )

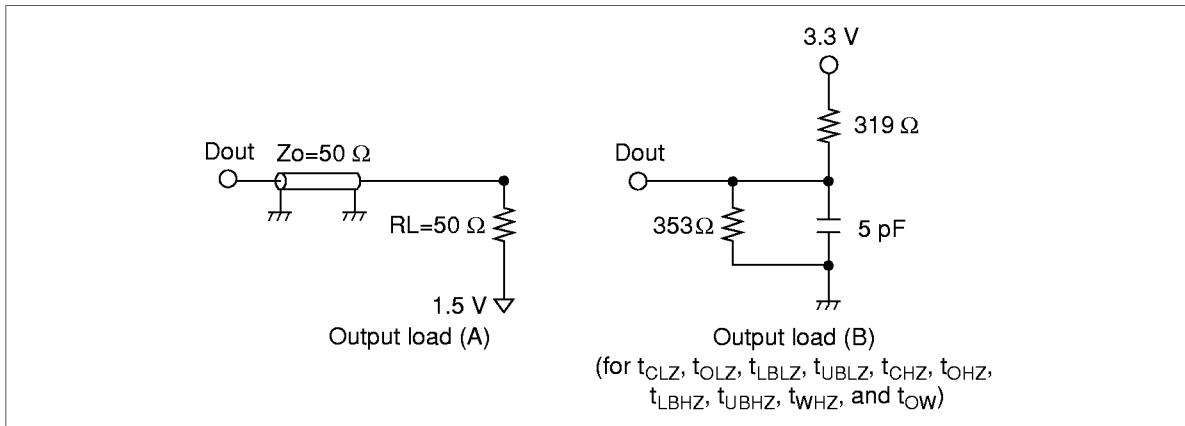
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance*1	$C_{in}$	—	—	6	pF	$V_{in} = 0\text{ V}$
Input/output capacitance*1	$C_{i/o}$	—	—	8	pF	$V_{i/o} = 0\text{ V}$

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 3.3 V ± 0.3 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: 3.0 V/0.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	HM62W16255H				Unit	Notes
		-12		-15			
		Min	Max	Min	Max		
Read cycle time	t <sub>RC</sub>	12	—	15	—	ns	
Address access time	t <sub>AA</sub>	—	12	—	15	ns	
Chip select access time	t <sub>ACS</sub>	—	12	—	15	ns	
Output enable to output valid	t <sub>OE</sub>	—	6	—	7	ns	
Byte select to output valid	t <sub>LB</sub> , t <sub>UB</sub>	—	6	—	7	ns	
Output hold from address change	t <sub>OH</sub>	3	—	3	—	ns	
Chip select to output in low-Z	t <sub>CLZ</sub>	3	—	3	—	ns	1
Output enable to output in low-Z	t <sub>OLZ</sub>	0	—	0	—	ns	1
Byte select to output in low-Z	t <sub>LBLZ</sub> , t <sub>UBLZ</sub>	0	—	0	—	ns	1
Chip deselect to output in high-Z	t <sub>CHZ</sub>	—	6	—	7	ns	1
Output disable to output in high-Z	t <sub>OHZ</sub>	—	6	—	7	ns	1
Byte deselect to output in high-Z	t <sub>LBHZ</sub> , t <sub>UBHZ</sub>	—	6	—	7	ns	1

## HM62W16255H Series

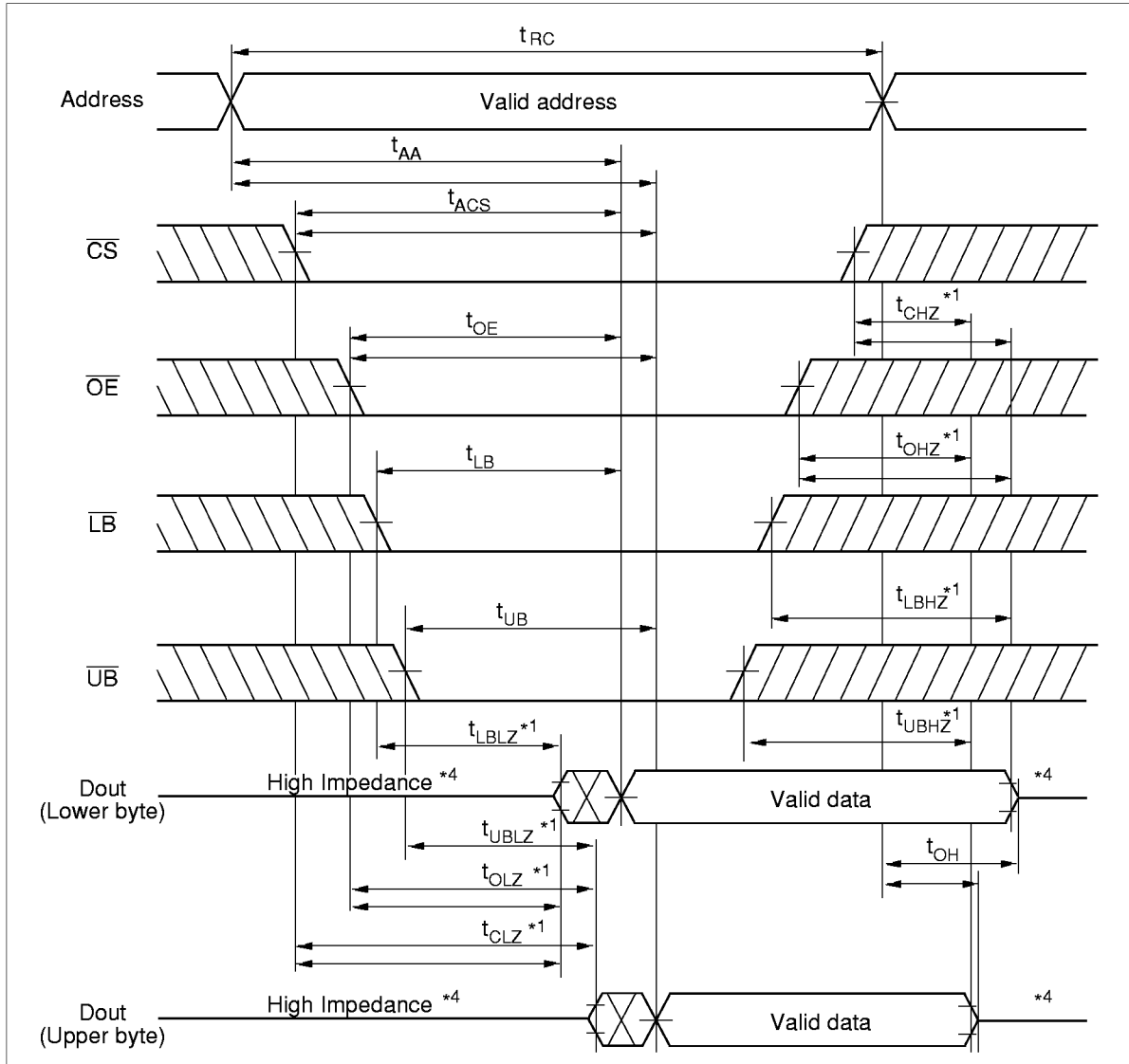
### Write Cycle

Parameter	Symbol	HM62W16255H				Unit	Notes
		-12		-15			
		Min	Max	Min	Max		
Write cycle time	$t_{WC}$	12	—	15	—	ns	
Address valid to end of write	$t_{AW}$	8	—	10	—	ns	
Chip select to end of write	$t_{CW}$	8	—	10	—	ns	8
Write pulse width	$t_{WP}$	8	—	10	—	ns	7
Byte select to end of write	$t_{LBW}, t_{UBW}$	8	—	10	—	ns	9, 10
Address setup time	$t_{AS}$	0	—	0	—	ns	5
Write recovery time	$t_{WR}$	0	—	0	—	ns	6
Data to write time overlap	$t_{DW}$	6	—	7	—	ns	
Data hold from write time	$t_{DH}$	0	—	0	—	ns	
Write disable to output in low-Z	$t_{OW}$	3	—	3	—	ns	1
Output disable to output in high-Z	$t_{OHZ}$	—	6	—	7	ns	1
Write enable to output in high-Z	$t_{WHZ}$	—	6	—	7	ns	1

- Notes:
1. Transition is measured  $\pm 200$  mV from steady voltage with Load (B). This parameter is sampled and not 100% tested.
  2. If the  $\overline{CS}$  or  $\overline{LB}$  or  $\overline{UB}$  low transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  transition, output remains a high impedance state.
  3.  $\overline{WE}$  and/or  $\overline{CS}$  must be high during address transition time.
  4. If  $\overline{CS}$ ,  $\overline{OE}$ ,  $\overline{LB}$  and  $\overline{UB}$  are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
  5.  $t_{AS}$  is measured from the latest address transition to the latest of  $\overline{CS}$ ,  $\overline{WE}$ ,  $\overline{LB}$  or  $\overline{UB}$  going low.
  6.  $t_{WR}$  is measured from the earliest of  $\overline{CS}$ ,  $\overline{WE}$ ,  $\overline{LB}$  or  $\overline{UB}$  going high to the first address transition.
  7. A write occurs during the overlap of low  $\overline{CS}$ , low  $\overline{WE}$  and low  $\overline{LB}$  or low  $\overline{UB}$ .
  8.  $t_{CW}$  is measured from the later of  $\overline{CS}$  going low to the end of write.
  9.  $t_{LBW}$  is measured from the later of  $\overline{LB}$  going low to the end of write.
  10.  $t_{UBW}$  is measured from the later of  $\overline{UB}$  going low to the end of write.

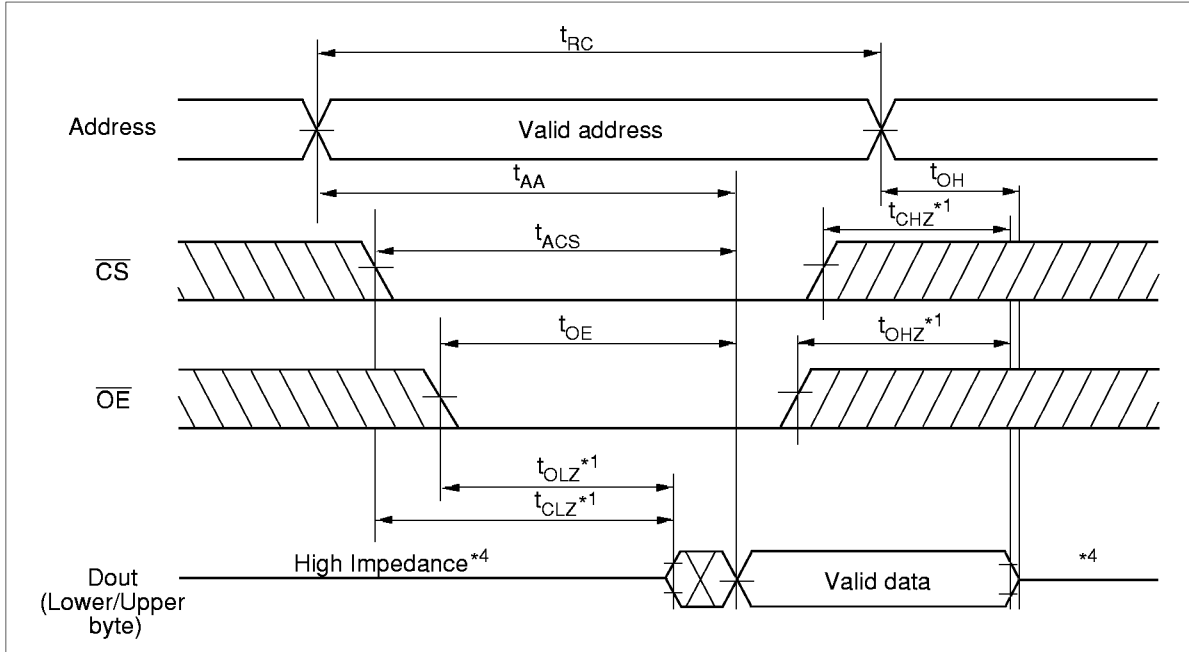
Timing Waveforms

Read Timing Waveform (1) ( $\overline{WE} = V_{IH}$ )

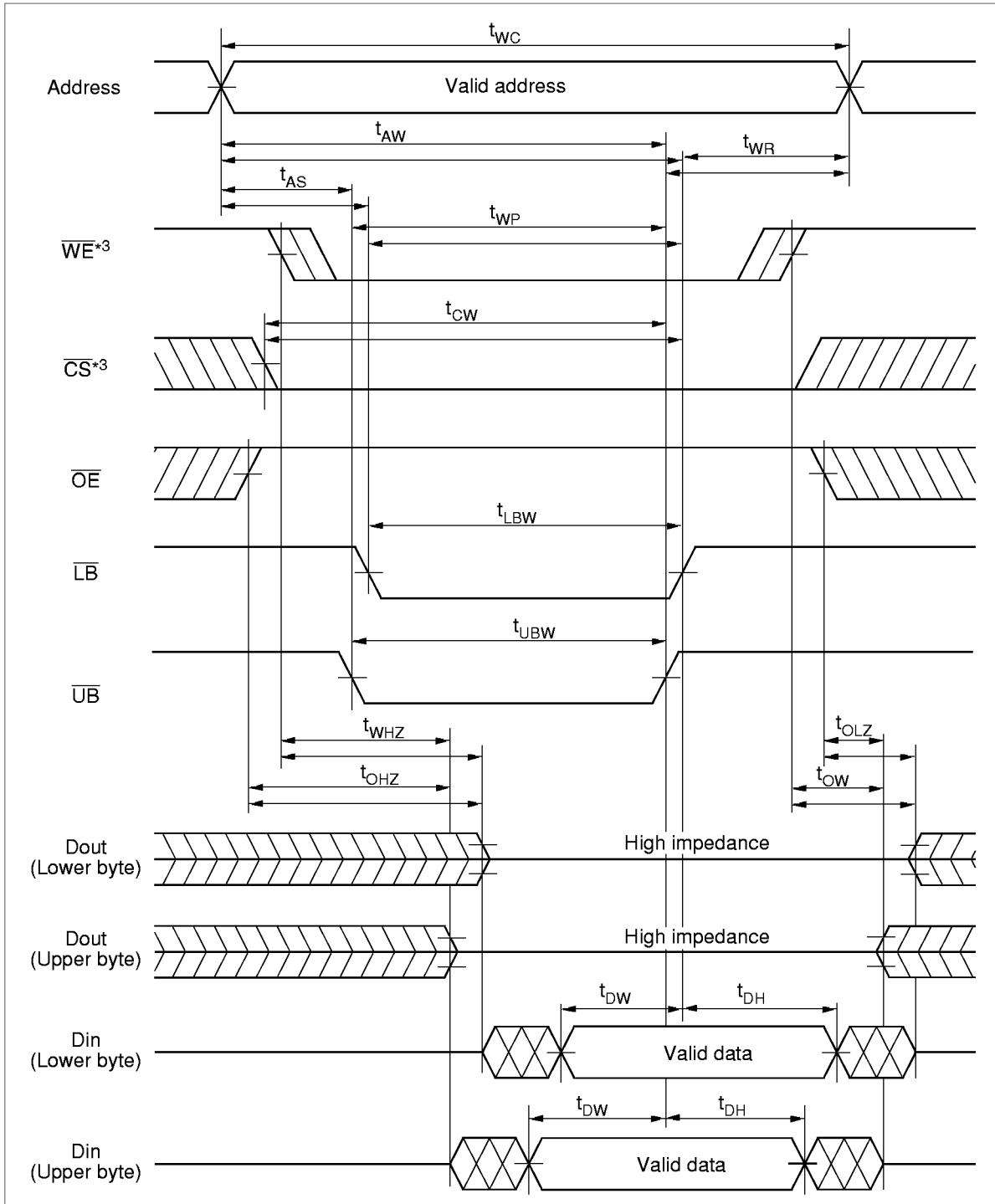


## HM62W16255H Series

Read Timing Waveform (2) ( $\overline{WE} = V_{IH}$ ,  $\overline{LB} = V_{IL}$ ,  $\overline{UB} = V_{IL}$ )

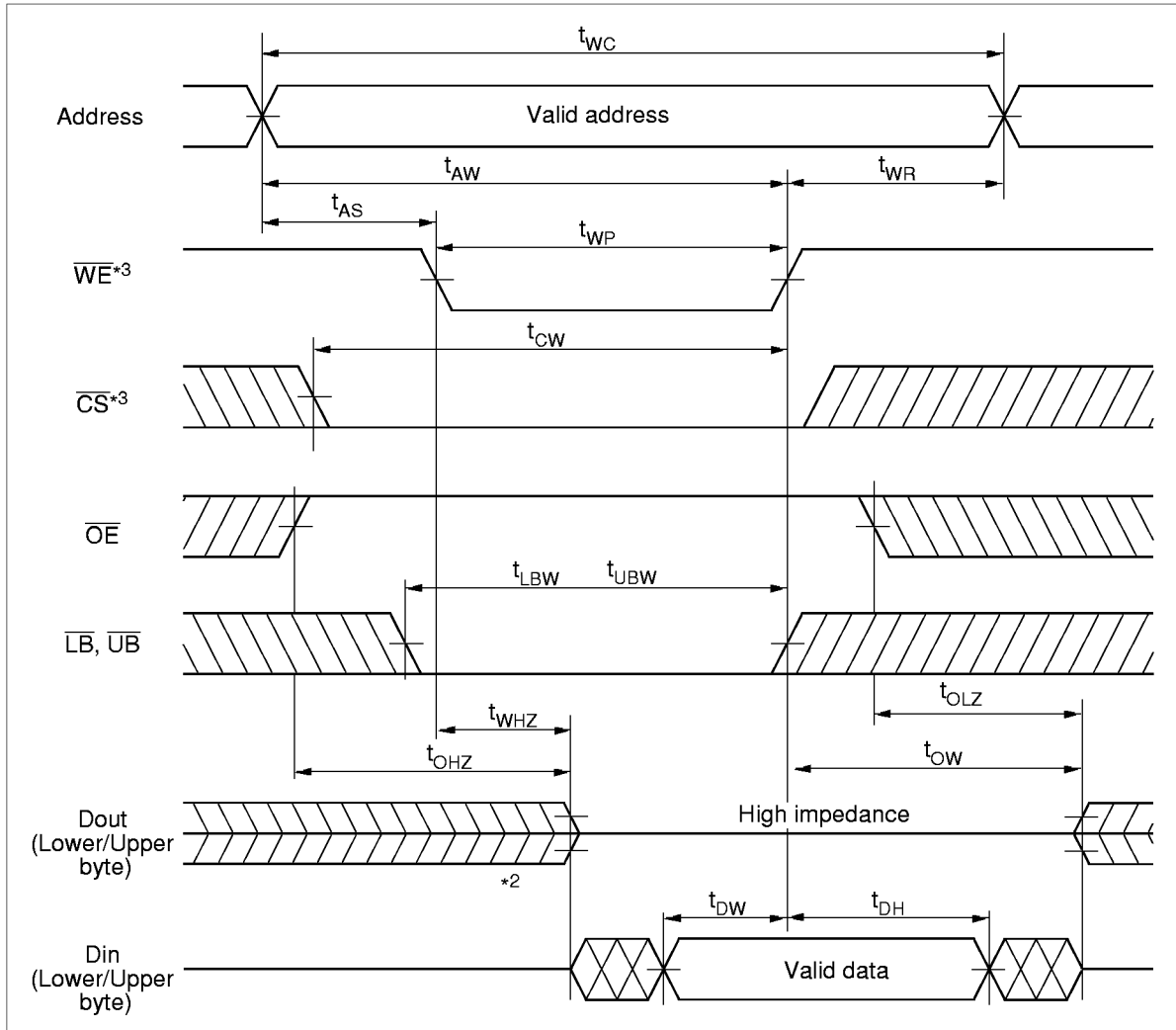


Write Timing Waveform (1) ( $\overline{\text{LB}}$ ,  $\overline{\text{UB}}$  Controlled)

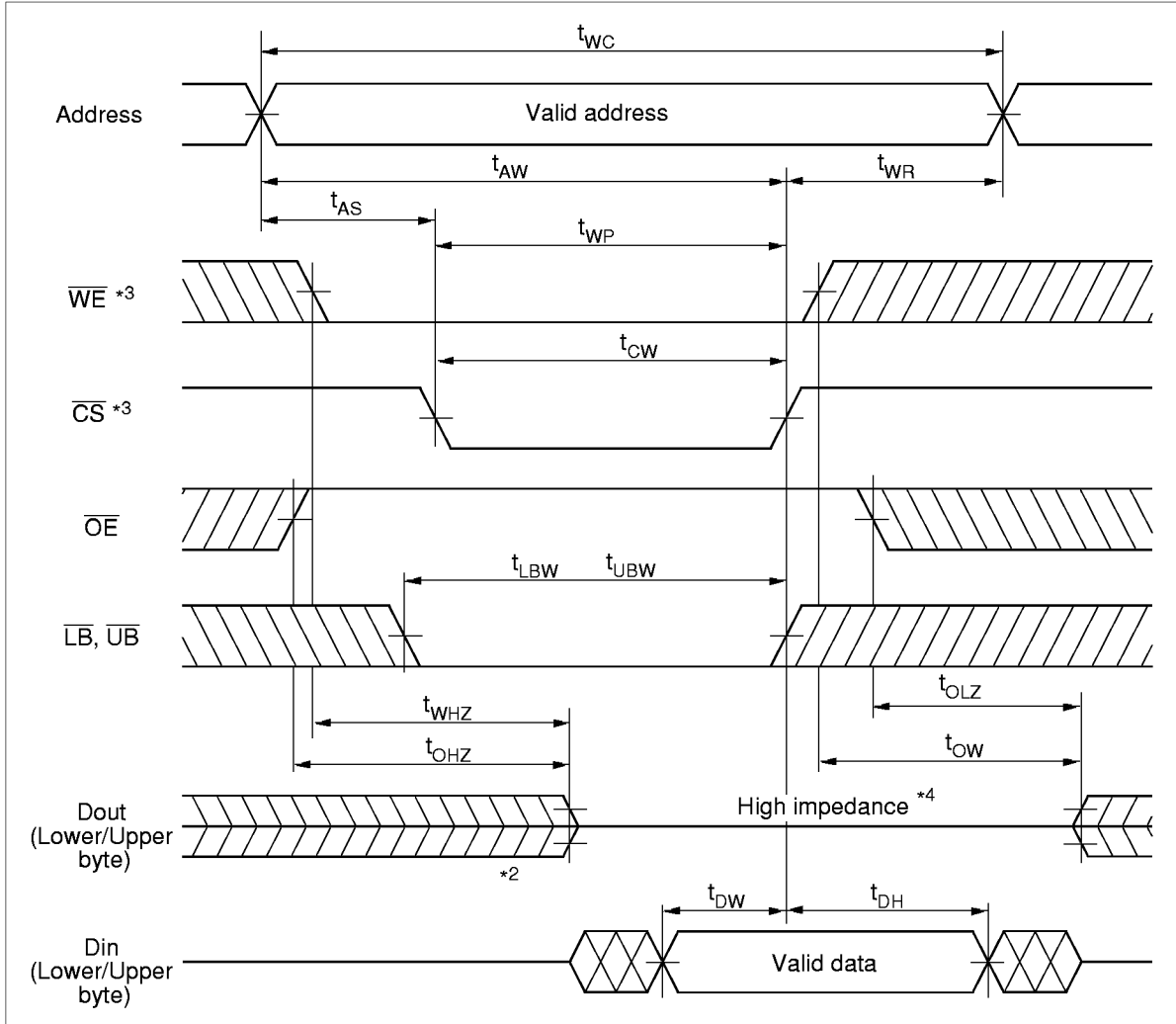


# HM62W16255H Series

## Write Timing Waveform (2) ( $\overline{WE}$ Controlled)



Write Timing Waveform (3) ( $\overline{CS}$  Controlled)



## HM62W16255H Series

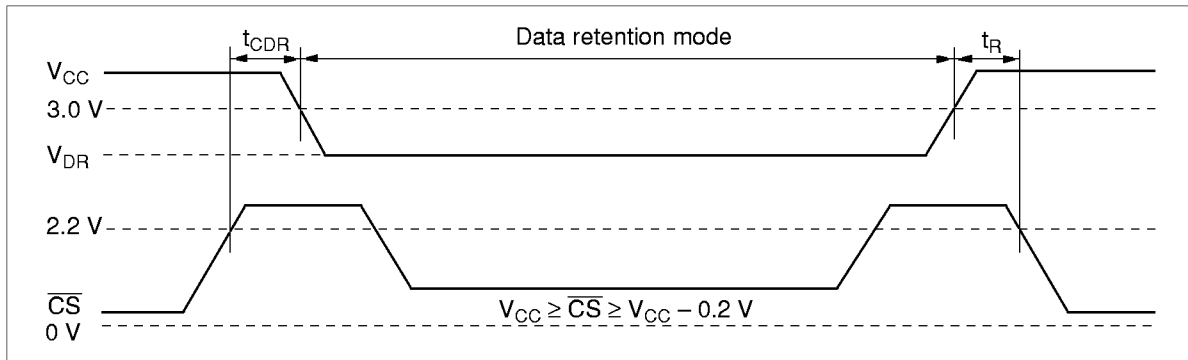
### Low $V_{CC}$ Data Retention Characteristics ( $T_a = 0$ to $+70^\circ\text{C}$ )

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ <sup>*1</sup>	Max	Unit	Test conditions
$V_{CC}$ for data retention	$V_{DR}$	2.0	—	—	V	$V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V, (1) $0$ V $\leq V_{in} \leq 0.2$ V or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2$ V
Data retention current	$I_{CCDR}$	—	40	600	$\mu\text{A}$	$V_{CC} = 3$ V $V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V, (1) $0$ V $\leq V_{in} \leq 0.2$ V or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2$ V
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveform
Operation recovery time	$t_R$	5	—	—	ms	

Note: 1. Typical values are at  $V_{CC} = 3.0$  V,  $T_a = +25^\circ\text{C}$ , and not guaranteed.

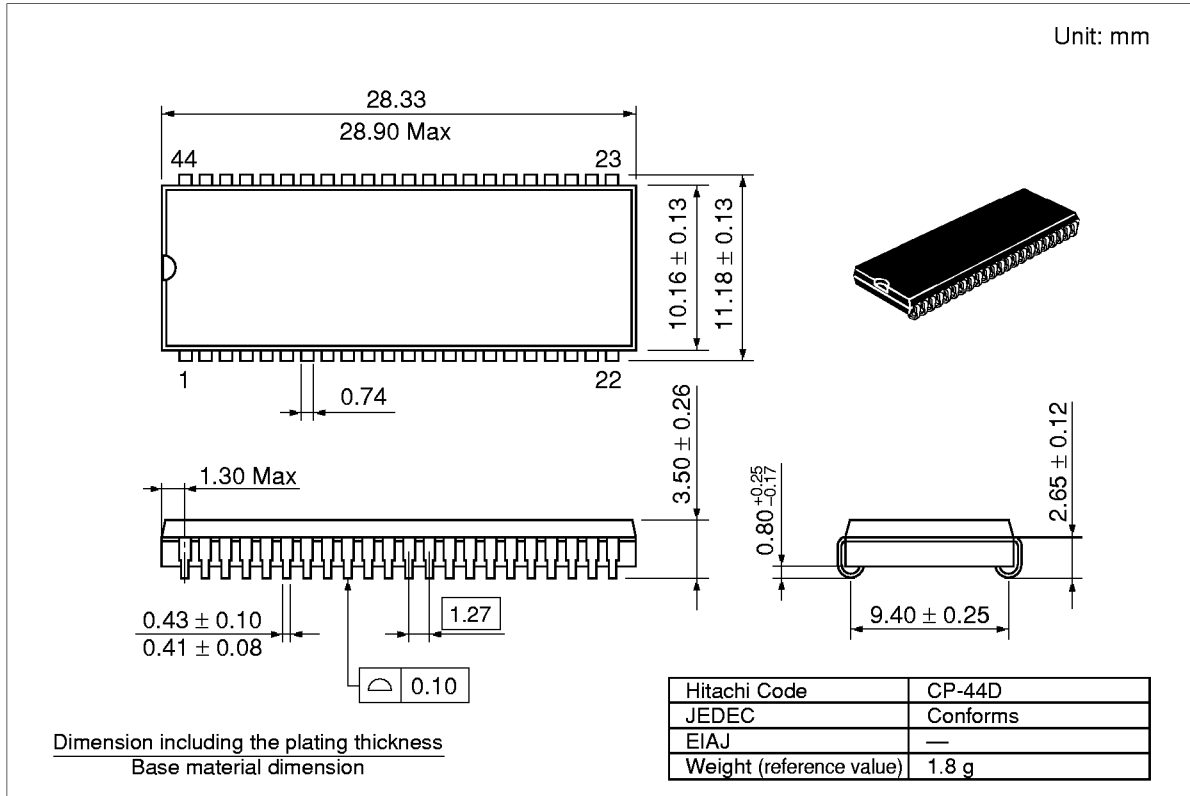
### Low $V_{CC}$ Data Retention Timing Waveform



# HM62W16255H Series

## Package Dimensions

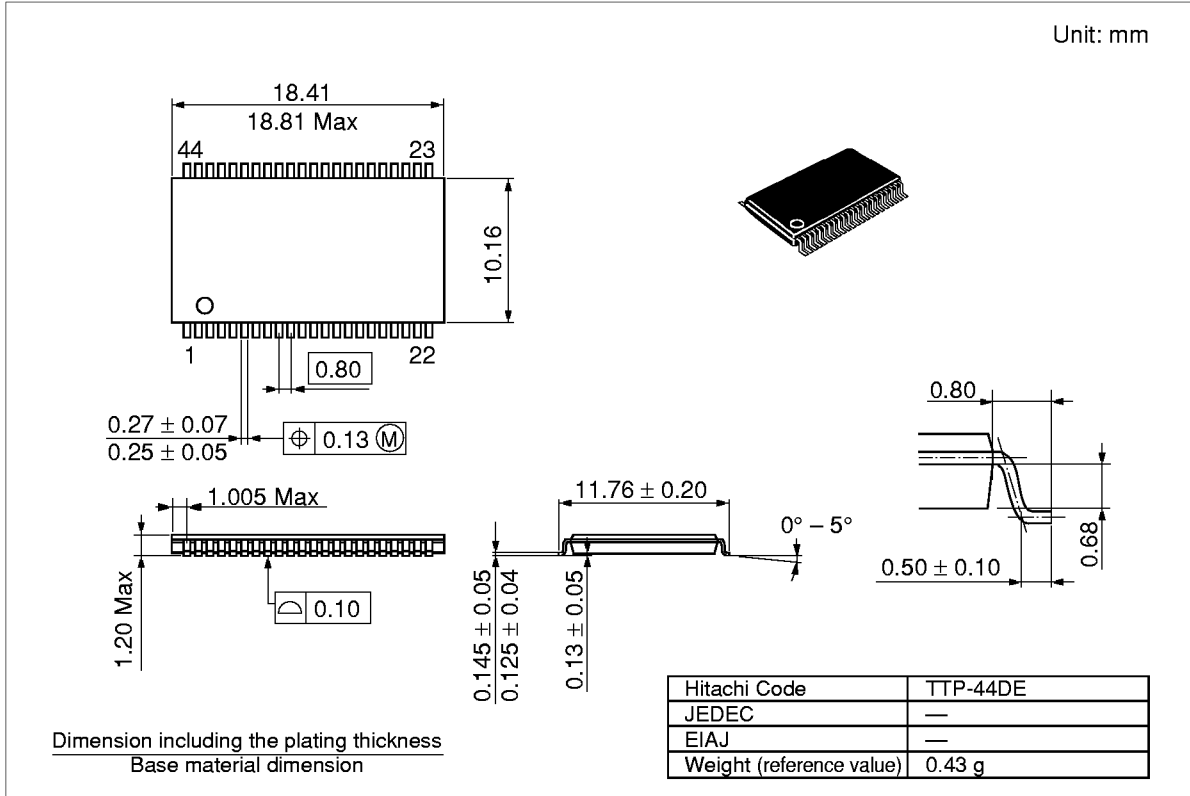
HM62W16255HJP/HLJP Series (CP-44D)



# HM62W16255H Series

## HM62W16255HTT/HLTT Series (TTP-44DE)

Unit: mm



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## HM62W16255H Series

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Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Sep. 15, 1998	Delete of HM62W16255H-10 Series Features Change of Data retention current DC Characteristics $I_{SB1}$ (typ): —/— mA to 0.05/0.05 mA Low $V_{CC}$ Data Retention Characteristics $I_{CCDR}$ : —/—/300 $\mu$ A to —/40/600 $\mu$ A		

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