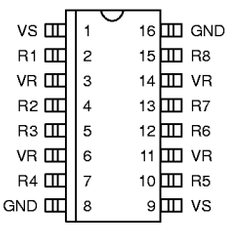
DALLAS SEMICONDUCTOR

DS2112
BTL Terminator

FEATURES

- Complies with Backplane Transceiver Logic (BTL) specifications (IEEE 1194.1–1991) and Futurebus+ specifications (IEEE 896.2–1991)
- Provides active termination for eight signal lines
- Laser–trimmed 33Ω termination resistors have 2.5% tolerance from 0°C to 70°C
- Onboard precise 2.1V (±2%) voltage regulator
- Package optimized for minimum parasitic inductance and resistance
- 16–pin (300 mil) plastic SOIC package

PIN ASSIGNMENT



16–PIN SOIC
(300 MIL)

DESCRIPTION

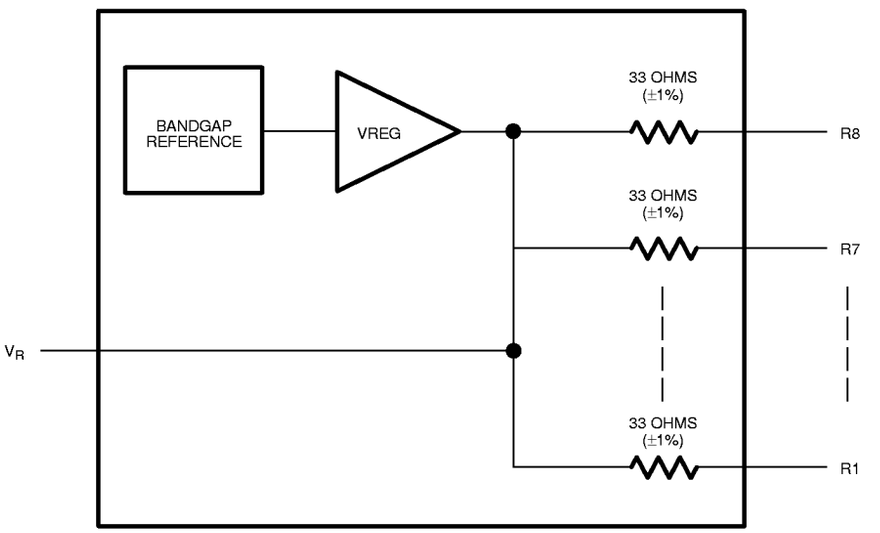
The DS2112 BTL Terminator provides active termination for Backplane Transceiver Logic (BTL) drivers and is fully compliant with IEEE 1194.1–1991, as well as the Futurebus+ specification (IEEE 896.2–1991). The DS2112 integrates a low dropout regulator and eight precision resistors into a single monolithic CMOS IC that is optimized for the high switching speeds and current required of BTL systems. The DS2112 allows the user to provide a distributed 2.1 volt supply that supports the instantaneous current required in incident wave switching while meeting the stringent ripple requirements of BTL without using a costly high speed specialized power supply.

FUNCTIONAL DESCRIPTION

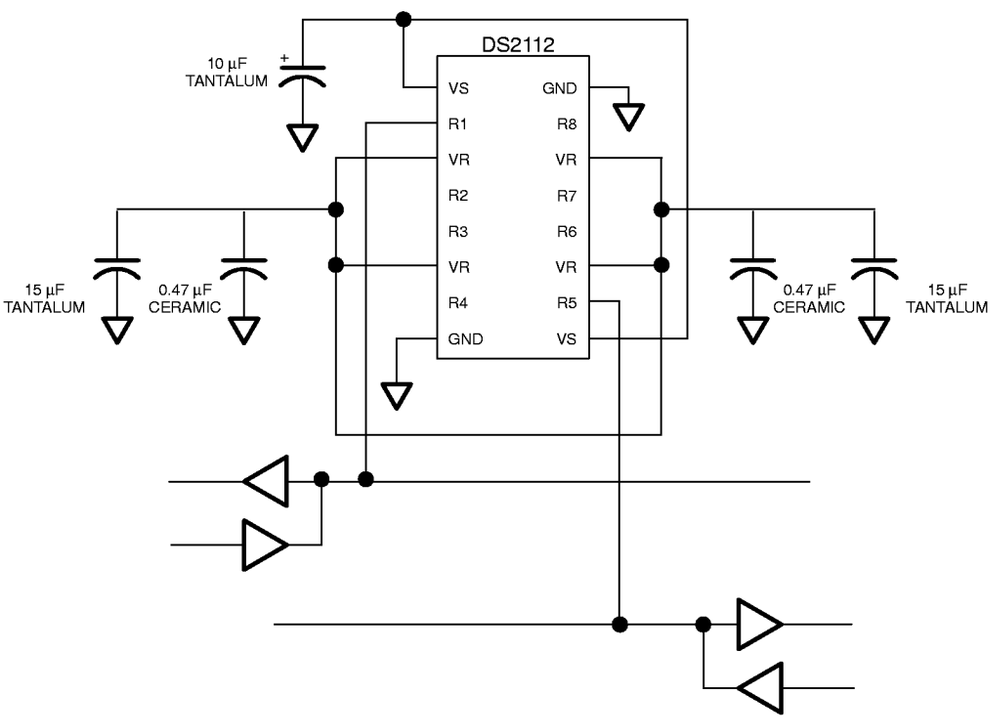
The DS2112 consists of a bandgap reference, a power amplifier, and eight precise 33Ω terminating resistors (see Figure 1). The bandgap reference produces a laser–trimmed 1.26 volt source which is amplified to 2.1 volts and fed to the unity gain power amp. The power amp is capable of sourcing 41 mA into each of the eight terminating resistors when the signal line is driven low. When the driver releases the line, the terminator will pull it back to 2.1 volts. When all lines are in the quiescent state, the DS2112 consumes about 10 mA (V_S=5.0 volts). The DS2112 can operate with supply voltages as low as 4.0 volts and meet all BTL specifications.

Due to the high switching speeds and the amount of current that can be switched, layout and bypass capacitor placement is critical to the proper operation of the DS2112's regulator. The DS2112 die, pinout and package have been optimized to reduce parasitic inductance and resistance, thereby minimizing the effects of large di/dt. The V_S pins should be connected to the backplane power supply and bypassed with a 10 μF tantalum; the two sets of V_R pins are designed to be tied together externally and bypassed. The preferred configuration would be to tie pins 3, 6, 11, and 14 together and bypass each pair locally with a 15 μF tantalum in parallel with a 0.47 μF ceramic. This optimizes the current path to the internal resistors while minimizing parasitic inductances and resistances. The traces making all connections to the DS2112 should be as short as possible. A typical configuration for one DS2112 is shown in Figure 2.

FUNCTIONAL BLOCK DIAGRAM Figure 1



TYPICAL CONFIGURATION Figure 2



PIN DESCRIPTION Table 1

PIN	SYMBOL	DESCRIPTION
1, 9	VS	**Power Supply**. Decouple with 10 µF tantalum, see Figure 2.
8, 16	GND	**Ground**. Signal ground; 0.0 volt.
3, 6, 11, 14	VR	**Reference Voltage**. Tie together and connect to bypass capacitors; see Figure 2.
2, 4, 5, 7, 10, 12, 13, 15	R	**Termination Resistor**. 33 ohm termination.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–1.0V to +7.0V
Operating Temperature	0°C to +70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_S	4.0		5.5	V	

DC CHARACTERISTICS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{TP} I_{TP}			350 15	mA mA	1, 3 1, 4
Termination Resistance	R_{TERM}	32.18	33.00	33.82	Ω	1, 2

REGULATOR CHARACTERISTICS

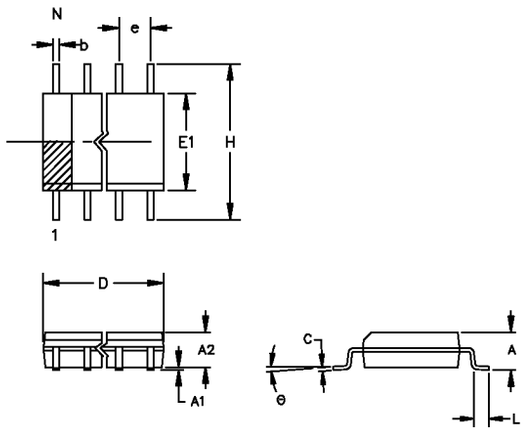
(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Voltage	V_R	2.058	2.100	2.142	V	1, 2
Load Regulation	LO_{REG}			2	%	1, 2, 5, 8
AC Ripple Voltage	V_{RIPPLE}	–50		+50	mV	1, 2, 5, 7
Regulation Time	T_{REG}			100	µs	6, 7
Input Capacitance	C_{IN}			5	pF	7

NOTES:

1. $4.0V < V_S < 5.5V$
2. 0.75V < signal lines < 2.0V
3. All signal lines = 0.75V.
4. All signal lines open.
5. R1 to R8 switching simultaneously between 1.0V and 2.0V with 2 ns rise/fall time.
6. Measured from the time V_S reaches 4.0V until V_R reaches regulation.
7. Guaranteed by design and characterization, not tested in production.
8. Production test for this device is at DC conditions.

16–PIN SOIC (300 MIL)



The chamfer on the body is optional. If it is not present, a terminal 1 identifier must be positioned so that 1/2 or more of its area is contained in the hatched zone.

PKG	16–PIN	
DIM	MIN	MAX
A IN. MM	0.094 2.38	0.105 2.68
A1 IN. MM	0.004 0.102	0.012 0.30
A2 IN. MM	0.089 2.26	0.095 2.41
b IN. MM	0.013 0.33	0.020 0.51
C IN MM	0.009 0.229	0.013 0.33
D IN. MM	0.398 10.11	0.412 10.46
e IN. MM	0.050 BSC 1.27 BSC	
E1 IN. MM	0.290 7.37	0.300 7.62
H IN MM	0.398 10.11	0.416 10.57
L IN MM	0.016 0.40	0.040 1.02
Θ	0°	8°