SMART
Modular Technologies

SM536512
August 1991
Rev 1

SM536512
2MByte (512K x 36) CMOS DRAM Module

General Description

The SM536512 is a high performance, 2-megabyte dynamic RAM module organized as 512K words by 36 bits, in a 72-pin, leadless single-in-line memory module (SIMM) package.

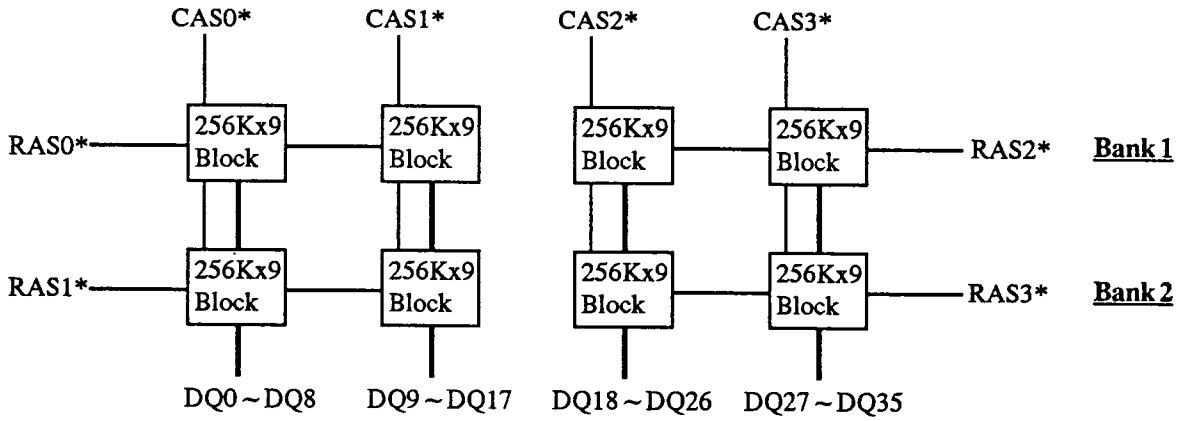
The module utilizes sixteen CMOS 256K x 4 and eight 256K x 1 dynamic RAMs in surface mount package on an epoxy laminate substrate. The 256K x 1 DRAMs are for parity. Each device is accompanied by a 0.22μf decoupling capacitor for improved noise immunity.

Control lines are provided such that byte control is possible.

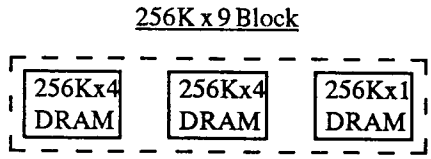
Features

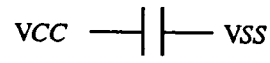
- High Density : 2Mbyte
- Fast Access Time of 70/80/100ns (max.)
- Low Power :
  5/4.25/3.54W (max.) - Active (70/80/100ns)
  0.264W (max.) - Standby (TTL)
  0.132W(max.) - Standby (CMOS)
- TTL-compatible inputs and outputs
- Separate power and ground planes to improve noise immunity
- Single power supply of 5V $\pm$ 10%
- PCB footprint of less than 1.49 sq. in. (Height:1")

Functional Diagram



A0 ~ A8 : To all devices
WE* : To all devices
OE* of all 256Kx4 devices are grounded





0.22μf to all devices

Note: All specifications of this device are subject to change without notice
"*" signifies complement

5405 Randall Place, Fremont, CA 94538 Tel: (415) 623-1231 Fax: (415) 623-1434

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Pin Name

A0 ~ A8	Address
DQ0 ~ DQ35	Data Input/Output
CAS0* ~ CAS3*	Column Address Strobe
RAS0* ~ RAS3*	Row Address Strobe
WE*	Read/Write
PD1 ~ PD4	Presence Detect
VCC	Power Supply
VSS	Ground
NC	No Connection

Presence Detect Pins

Pin	70ns	80ns	100ns
PD1	NC	NC	NC
PD2	*VSS*	*VSS*	*VSS*
PD3	*VSS*	NC	*VSS*
PD4	NC	*VSS*	*VSS*

Ordering Information

Part Number	Speed
SM536512-7	70ns
SM536512-8	80ns
SM536512-10	100ns

Pin No.	Pin Designation	Pin No.	Pin Designation
1	*VSS*	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	*VSS*
4	DQ1	40	CAS0*
5	DQ19	41	CAS2*
6	DQ2	42	CAS3*
7	DQ20	43	CAS1*
8	DQ3	44	RAS0*
9	DQ21	45	RAS1*
10	*VCC*	46	NC
11	NC	47	WE*
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	NC	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	*VCC*
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	NC	65	DQ16
30	*VCC*	66	NC
31	A8	67	PD1
32	NC	68	PD2
33	RAS3*	69	PD3
34	RAS2*	70	PD4
35	DQ26	71	NC
36	DQ8	72	*VSS*

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Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Voltage on any pin relative to VSS	VT	- 1 to +7.0	V
Power Dissipation	PT	12	W
Operating Temperature	TA	0 to +70	°C
Storage Temperature	Tstg	- 55 to +125	°C
Short Circuit Output Current	IOS	50	mA

Recommended DC Operating Conditions

(Ta = 0 to +70 °C)

Symbol	Parameter	Min	Typ	Max	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
VSS	Ground	0	0	0	V
VIH	Input High Voltage	2.4	-	6.0	V
VIL	Input Low Voltage	-1	-	0.8	V

DC Characteristics

(VCC = 5V±10%, VSS = 0V, Ta = 0 to +70 °C)

Parameter	Symbol	Test Conditions	SM536512-7		SM536512-8		SM536512-10		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current	ICC1	tRC = min.	-	924	-	772	-	644	mA	1, 2
Standby Current	ICC2	TTL Interface RAS*, CAS*=VIH, DOUT=High Z	-	48	-	48	-	48	mA	
		CMOS Interface RAS*, CAS*≥VCC - 0.2V DOUT =High Z	-	24	-	24	-	24	mA	
RAS*-Only Refresh Current	ICC3	tRC = min.	-	924	-	772	-	644	mA	2
Standby Current	ICC5	RAS*=VIH, CAS*=VIL, DOUT =Enable	-	120	-	120	-	120	mA	1
CAS*-Before-RAS* Refresh Current	ICC6	tRC = Min.	-	844	-	772	-	644	mA	1
Fast Page Mode Current	ICC7	tPC = Min.	-	744	-	692	-	672	mA	1,3

DC Characteristics (contd.)

Parameter	Symbol	Test Conditions	SM536512-7		SM536512-8		SM536512-10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Input Leakage Current	*ILI*	0V≤VIN ≤7V	-240	240	-240	240	-240	240	μA
Output Leakage Current	*ILO*	0V≤V*OUT*≤7V	-20	20	-20	20	-20	20	μA
Output High Voltage	*VOH*	High I*OUT*= -5mA	2.4	*VCC*	2.4	*VCC*	2.4	*VCC*	V
Output Low Voltage	*VOL*	Low I*OUT*=4.2mA	0	0.4	0	0.4	0	0.4	V

Notes: 1. I*CC* depends on output load condition when the device is selected, I*CC* max. is specified at the output open condition.
2. Address can be changed less than three times while RAS* = V*IL* .
3. Address can be changed once or less while CAS* = V*IH* .

Capacitance

(T*a*= +25°C, V*CC* = 5V ± 10%)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input Capacitance (Address)	*CI1*	-	123	pF	1
Input Capacitance (WE*)	*CI2*	-	170	pF	1
Input Capacitance (RAS0* ~ RAS3*)	*CI3*	-	45	pF	1
Input Capacitance (CAS0* ~ CAS3*)	*CI4*	-	24	pF	1
Output Capacitance (DQ8,17,26,35)	*CI/O1*	-	19	pF	1, 2
Output Capacitance (Remaining DQs)	*CI/O2*	-	23	pF	1, 2

Notes: 1. Capacitance is measured with Boonton Meter or effective capacitance method.
2. CAS*=V*IH* to disable D*OUT*.

AC Characteristics

(T*a* = 0 to +70 °C, V*CC* = 5.0V ± 10%, V*SS* = 0V)

Parameter	Symbol	SM536512-7		SM536512-8		SM536512-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	*tRC*	130	-	160	-	190	-	ns	
Access time from RAS*	*tRAC*	-	70	-	80	-	100	ns	3, 4
Access time from CAS*	*tCAC*	-	20	-	25	-	25	ns	3, 4, 5
Access time from column address	*tAA*	-	35	-	40	-	45	ns	3, 10
Output buffer turn-off time	*tOFF*	0	20	0	20	0	25	ns	6
Transition time (rise and fall)	*tT*	3	50	3	50	3	50	ns	2
RAS* precharge time	*tRP*	50	-	70	-	80	-	ns	
RAS* pulse width	*tRAS*	70	10000	80	10000	100	10000	ns	

AC Characteristics (contd.)

Parameter	Symbol	SM536512-7		SM536512-8		SM536512-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
RAS* hold time	*tRSH*	20	-	25	-	25	-	ns	
CAS* hold time	*tCSH*	70	-	80	-	100	-	ns	
CAS* pulse width	*tCAS*	20	10000	25	10000	25	10000	ns	
RAS* to CAS* delay time	*tRCD*	20	50	25	60	25	75	ns	4
RAS* to column address delay time	*tRAD*	15	35	20	40	20	55	ns	10
CAS* to RAS* precharge time	*tCRP*	10	-	10	-	10	-	ns	
Row address set-up time	*tASR*	0	-	0	-	0	-	ns	
Row address hold time	*tRAH*	10	-	15	-	15	-	ns	
Column address set-up time	*tASC*	0	-	0	-	0	-	ns	
Column address hold time	*tCAH*	15	-	20	-	20	-	ns	
Column address to RAS* lead time	*tRAL*	35	-	40	-	50	-	ns	
Read command set-up time	*tRCS*	0	-	0	-	0	-	ns	
Read command hold time to CAS*	*tRCH*	0	-	0	-	0	-	ns	8
Read command hold time to RAS*	*tRRH*	10	-	10	-	10	-	ns	
Write command hold time	*tWCH*	15	-	20	-	20	-	ns	
Write command pulse width	*tWP*	15	-	15	-	20	-	ns	
Write command to RAS* lead time	*tRWL*	20	-	25	-	25	-	ns	
Write command to CAS* lead time	*tCWL*	20	-	25	-	25	-	ns	
Data-in set-up time	*tDS*	0	-	0	-	0	-	ns	9
Data-in hold time	*tDH*	15	-	15	-	20	-	ns	9
Refresh period (512 cycles)	*tREF*	-	8	-	8	-	8	ns	
Write command set-up time	*tWCS*	0	-	0	-	0	-	ns	7
CAS* set-up time (CBR refresh)	*tCSR*	10	-	10	-	10	-	ns	
CAS* hold time (CBR refresh)	*tCHR*	20	-	25	-	30	-	ns	
RAS* precharge to CAS* hold time	*tRPC*	10	-	10	-	10	-	ns	
Access time from CAS* precharge	*tACP*	-	45	-	45	-	55	ns	3
Fast page mode cycle time	*tPC*	50	-	55	-	60	-	ns	
CAS* precharge time (Fast page)	*tCP*	10	-	10	-	10	-	ns	
RAS* pulse width (Fast page)	*tRASC*	-	100000	-	100000	-	100000	ns	

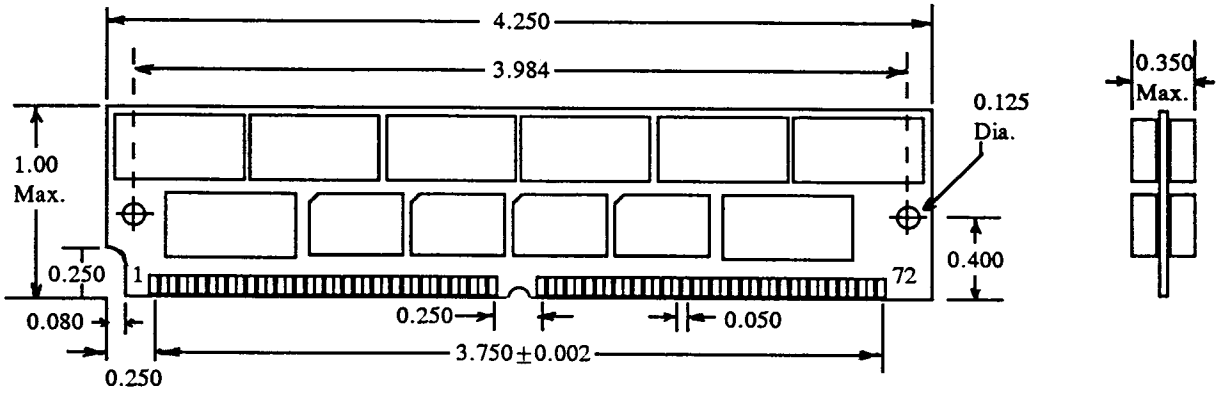
Notes:
1. An initial pause of 200μs is required after power-up followed by any eight RAS* cycles before device operation is achieved.
2. *VIH* (min) and *VIL* (max) are reference levels for measuring timing of input signals. Transition times are measured between *VIH* (min) and *VIL* (max) and are assumed to be 5ns for all inputs.
3. Measure with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the *tRCD* (max) limit ensures that *tRAC* (max) limit can be met. *tRCD* (max) is specified as a reference point only. If *tRCD* (max) is greater than the specified limit, then access time is controlled exclusively by *tCAC*.
5. Assumes that *tRCD* $\geq$ *tRCD* (max).

Notes (contd.):

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
7. tWCS is non restrictive operating parameter. It is included in the data sheet as electrical characteristic only. If tWCS > tWCS (min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the CAS* leading edge in early write cycles.
10. Operation within the tRAD (max) limit ensures that tRAC (max) can be met. tRAD (max) is specified as a reference point only. If tRAD is greater than the specified tRAD (max) limit, then access time is controlled by tAA .

Physical Dimensions

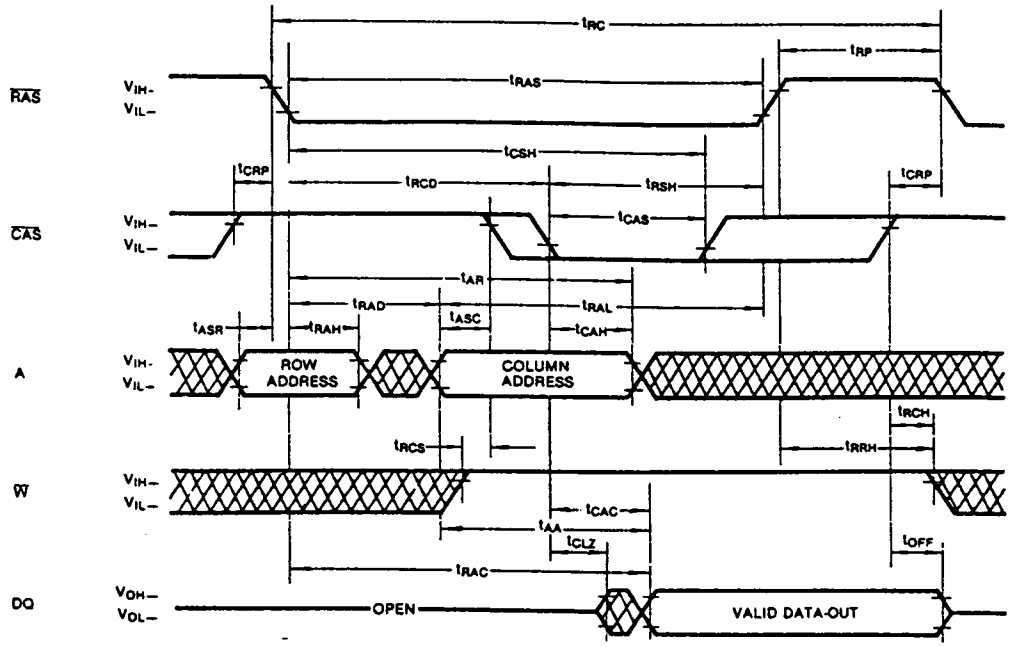
72-pin SIMM



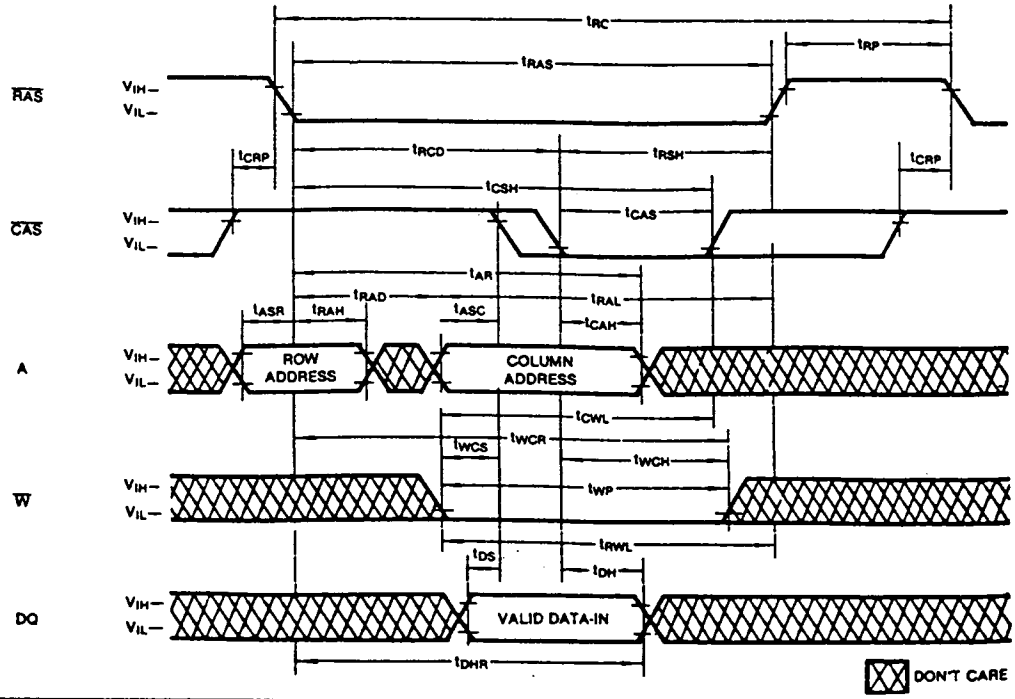
(All dimensions are in inches with a tolerance of ±0.005" unless otherwise specified)

TIMING WAVEFORMS

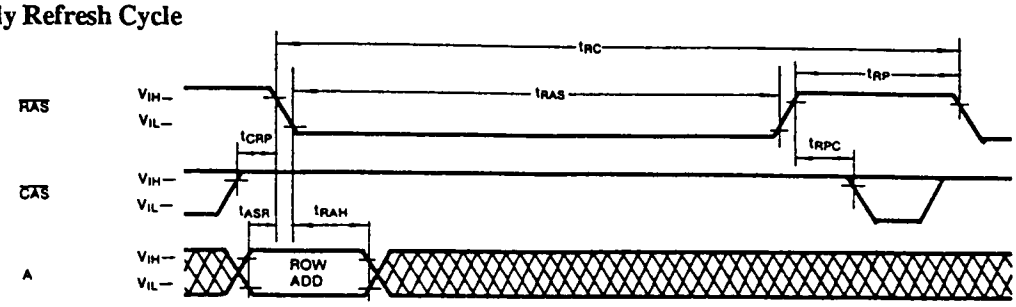
Read Cycle



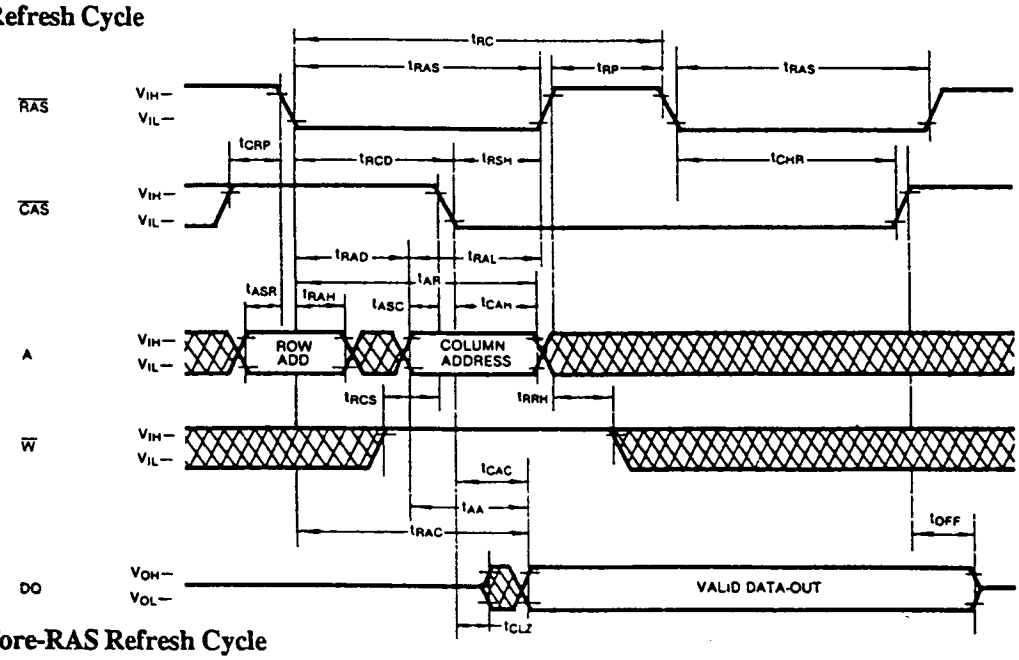
Write Cycle (Early Write)



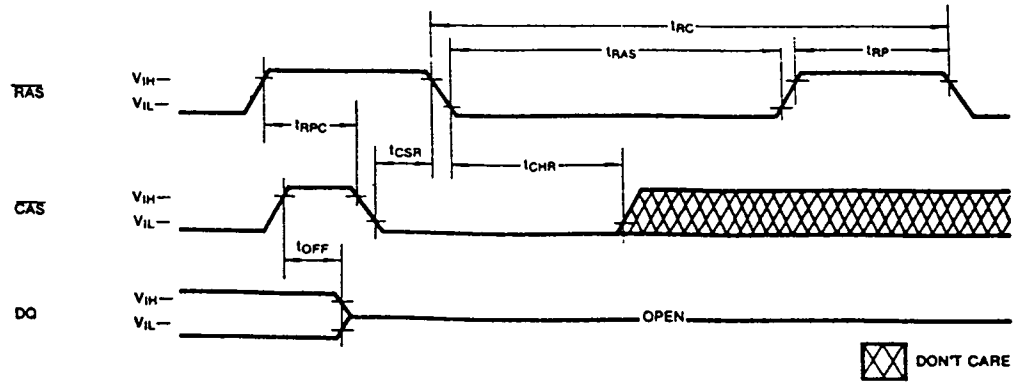
RAS Only Refresh Cycle



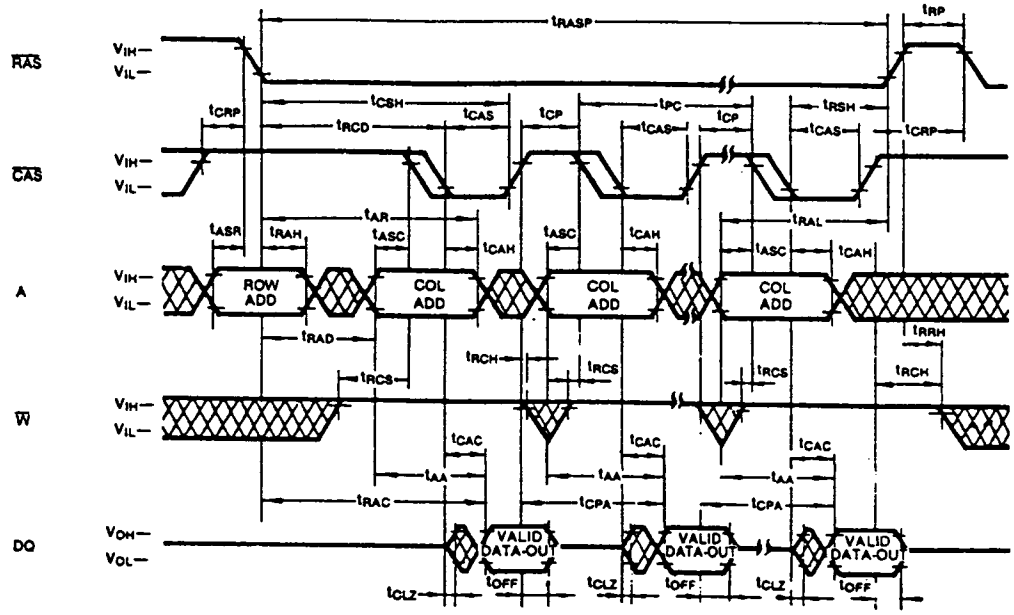
Hidden Refresh Cycle



CAS-Before-RAS Refresh Cycle



Fast Page Mode Read Cycle



Fast Page Mode Write Cycle (Early Write)