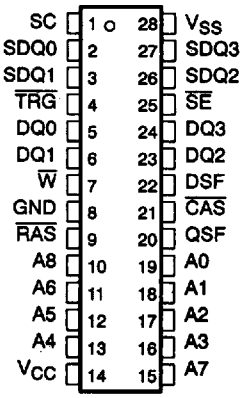
SMJ44C250
262 144 BY 4-BIT MULTIPORT VIDEO RAM

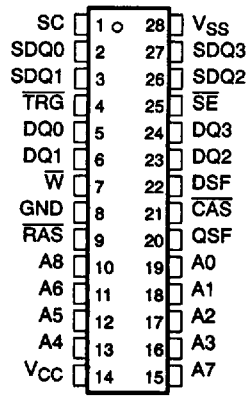
SGMS037B–JANUARY 1991–REVISED FEBRUARY 1993

- Military Operating Temperature Range . . . – 55°C to 125°C
- Processed to MIL-STD-833, Class B
- DRAM: 262 144 Words × 4 Bits
  SAM: 512 Words × 4 Bits
- Dual Port Accessibility — Simultaneous and Asynchronous Access From the DRAM and SAM Ports
- Bidirectional Data Transfer Function Between the DRAM and the Serial Data Register
- Write Per Bit Feature for Selective Write to Each RAM I/O
- Enhanced Page Mode Operation for Faster Access
- $\overline{CAS}$-before-$\overline{RAS}$ and Hidden Refresh Modes
- RAM Output Enable Allows Direct Connection of DQ and Address Lines to Simplify System Design
- Long Refresh Period . . . Every 8 ms (Max)
- Up to 33 MHz Uninterrupted Serial Data Streams
- 3-State Serial I/Os Allow Easy Multiplexing of Video Data Streams
- 512 Selectable Serial Register Starting Locations
- Texas Instruments EPIC™ CMOS Process
- Packaging Options
  - 28-pin Ceramic Side Brazed DIP (JD suffix)
  - 28-pin Ceramic Small Outline J-Leaded Chip Carrier (HJ Suffix)
- Split Serial Data Register for Simplified Realtime Register Reload

JD PACKAGE
(TOP VIEW)



HJ PACKAGE
(TOP VIEW)



PIN NOMENCLATURE

A0–A8	Address Inputs
$\overline{CAS}$	Column Enable
DQ0–DQ3	DRAM Data In-Out/Write Mask Bit
$\overline{SE}$	Serial Enable
$\overline{RAS}$	Row Enable
SC	Serial Data Clock
SDQ0–SDQ3	Serial Data In-Out
$\overline{TRG}$	Transfer Register/Q Output Enable
$\overline{W}$	Write Mask Select/Write Enable
DSF	Special Function Select
QSF	Split Register Activity Status
V_{CC}	5-V Supply
V_{SS}	Ground
GND	Ground (Important: not connected internally to V_{SS})

- **Performance Ranges:**

	ACCESS TIME ROW ADDRESS (MAX) $t_{a(R)}$	ACCESS TIME COLUMN ENABLE (MAX) $t_{a(C)}$	ACCESS TIME SERIAL DATA (MAX) $t_{a(SC)}$	ACCESS TIME SERIAL ENABLE (MAX) $t_{a(SE)}$	V_{CC} TOLERANCE
'44C250-10	100 ns	25 ns	30 ns	20 ns	±10%
'44C250-12	120 ns	30 ns	35 ns	25 ns	±10%

description

The SMJ44C250 multiport video RAM is a high speed, dual ported memory device. It consists of a dynamic random-access memory (DRAM) organized as 262 144 words of 4 bits each interfaced to a serial data register, or serial access memory (SAM), organized as 512 words of 4 bits each. The SMJ44C250 supports three basic types of operation: random access to and from the DRAM, serial access to and from the serial register, and bidirectional transfer of data between any row in the DRAM and the serial register. Except during transfer

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operations, the SMJ44C250 can be accessed simultaneously and asynchronously from the DRAM and SAM ports. During a transfer operation, the 512 columns of the DRAM are connected to the 512 positions in the serial data register. The 512 × 4 bit serial data register can be loaded from the memory row (transfer read) or else the contents of the 512 × 4 bit serial data register can be written to the memory row (transfer write).

The SMJ44C250 is equipped with several features designed to provide higher system-level bandwidth and simplify design integration on both the DRAM and SAM ports. On the DRAM port, a write mask register provides a persistent write-per-bit without repeated mask loading.

On the serial register, or SAM port, the SMJ44C250 offers a split-register transfer read (DRAM to SAM) option, which enables realtime register reload implementation for truly continuous serial data streams without critical timing requirements. The register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the memory array. This new realtime register reload implementation allows truly continuous serial data. For applications not requiring realtime register reload (for example, reloads done during CRT retrace periods), the single register mode of operation is retained to simplify design. The SAM can also be configured in input mode, accepting serial data from an external device. Once the serial register within the SAM is loaded, its contents can be transferred to the corresponding column positions in any row in memory in a single memory cycle.

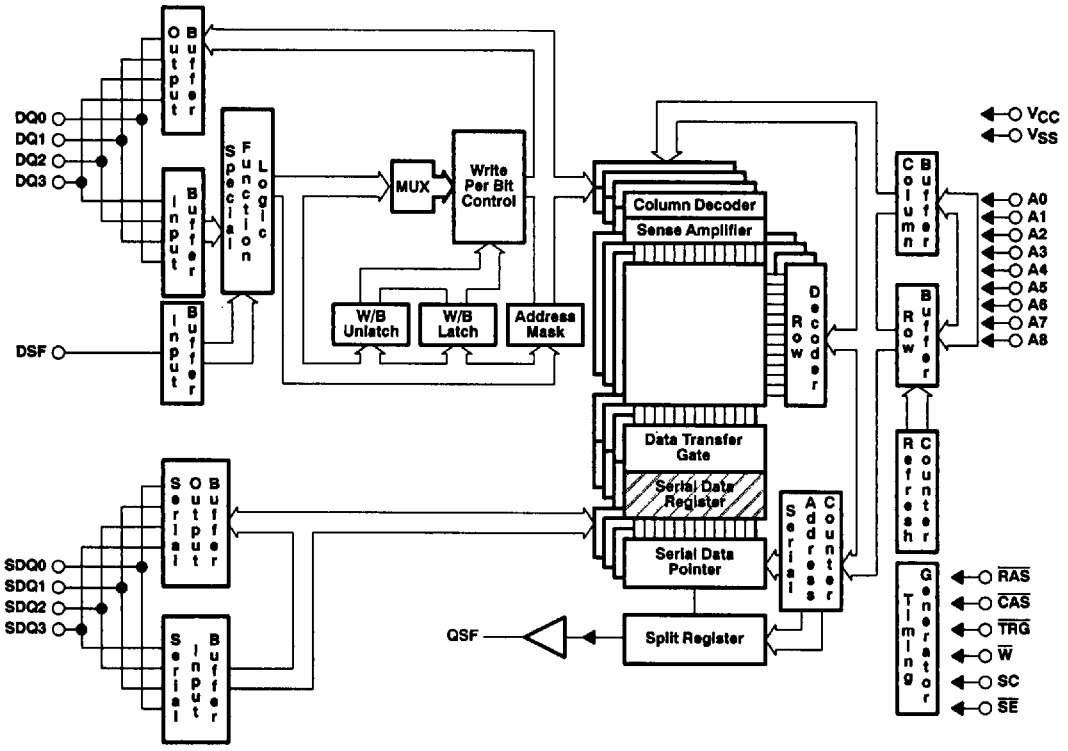
The SAM port is designed for maximum performance. Data can be input to or accessed from the SAM at serial rates up to 33 MHz. During a split-register mode of operation, internal circuitry detects when the last bit position is accessed from the active half of the register and immediately transfers control to the opposite half. A separate open-drain output, designated QSF, is included to indicate which half of the serial register is active at any given time in the split register mode.

All address lines and data-in are latched on-chip to simplify system design. All data-outs are unlatched to allow greater system flexibility.

The SMJ44C250 is offered both in a 28-pin 400-mil dual-in-line ceramic sidebrazed package (JD suffix) for through-hole row insertion, and in a 28-pin ceramic small outline J-leaded chip carrier package (HJ suffix) for surface-mount applications. The L suffix device is tested for operation from 0°C to 70°C. The M suffix device is tested for operation from – 55°C to 125°C.

The SMJ44C250 and other SMJ44C25x multiport video RAMs are supported by a broad line of video/graphic processors from Texas Instruments, including the SMJ34010 and the SMJ34020 graphics processors.

functional block diagram



Detailed Pin Description vs Operational Mode

PIN	DRAM	TRANSFER	SAM
A0–A8	Row, Column Address	Row, Tap Address	
$\overline{CAS}$	Column Enable, Output Enable	Tap Address Strobe	
DQi	DRAM Data I/O, Write Mask Bits		
DSF	Persistent Write-per-bit Enable Write-per-bit Mask Load Enable	Split Register Enable Alternate Write Transfer Enable	
$\overline{RAS}$	Row Enable	Row Enable	
$\overline{SE}$		Serial-In Mode Enable	Serial Enable
SC			Serial Clock
SDQi			Serial Data I/O
$\overline{TRG}$	Q Output Enable	Transfer Enable	
$\overline{W}$	Write Enable, Write-per-Bit Select	Transfer Write Enable	
QSF			Split Register Active Status
V_{CC}	5-V Supply (typical)		
V_{SS}	Device Ground		
GND	System Ground (Important: not connected internally to V_{SS})		

operation

random access operation

Refer to Table 1, Functional Table (page 7), for random access and transfer operations. Random access operations are denoted by the designator "R" and transfer operations are denoted by a "T."

transfer register select and DQ enable ($\overline{TRG}$)

The $\overline{TRG}$ pin selects either register or random access operation as $\overline{RAS}$ falls. For random access (DRAM) mode, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. Asserting $\overline{TRG}$ high as $\overline{RAS}$ falls causes the 512 storage elements of each data register to remain disconnected from the corresponding 512-bit lines of the memory array. (Asserting $\overline{TRG}$ low as $\overline{RAS}$ falls connects the 512-bit positions in the serial register to the bit lines and indicates that a transfer will occur between the data registers and the selected memory row. See *transfer operation* for details.)

During random access operations, $\overline{TRG}$ also functions as an output enable for the random (Q) outputs. Whenever $\overline{TRG}$ is held high, the Q outputs are in the high-impedance state to prevent an overlap between the address and DRAM data. This organization allows the connection of the address lines to the data I/O lines but prohibits the use of the early write cycle. It also allows read-modify-write cycles to be performed by providing a three-state condition to the common I/O pins so that write data can be driven onto the pins after output read data has been externally latched.

address (A0–A8)

Eighteen address bits are required to decode 1 of 262 144 storage cell locations. Nine row address bits are set up on pins A0 through A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Then the nine column address bits are set up on pins A0 through A8 and latched onto the chip on the falling edge of $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$.

$\overline{RAS}$ and $\overline{CAS}$ address strobes and device control clocks

$\overline{RAS}$ is a control input that latches the states of the row address, $\overline{W}$, $\overline{TRG}$, $\overline{SE}$, $\overline{CAS}$, and DSF onto the chip to invoke the various DRAM and transfer functions of the SMJ44C250. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is a control input that latches the states of the column address and DSF to control various DRAM and transfer functions. $\overline{CAS}$ also acts as an output enable for the DRAM output pins.

special function select (DSF)

The special function select input is latched on the falling edges of $\overline{RAS}$ and $\overline{CAS}$, similarly to an address, and serves three functions. First, during write cycles DSF invokes persistent write-per-bit operation. If $\overline{TRG}$ is high, $\overline{W}$ is low, and DSF is low on the falling edge of $\overline{RAS}$, the write mask will be reloaded with the data present on the DQ pins. If DSF is high, the mask will not be reloaded but will retain the data from the last mask reload cycle.

Second, DSF is used to change the internally stored write-per-bit mask register (or write mask) via the load write mask cycle. The data present on the DQ pins when $\overline{W}$ falls is written to the write mask rather than to the addressed memory location. See "Delayed Write Cycle Timing" and the accompanying "Write Cycle State Table" in the timing diagram section. Once the write mask is loaded, it can be used on subsequent masked write-per-bit cycles. This feature allows systems with a common address and data bus to use the write-per-bit feature, eliminating the time needed for multiplexing the write mask and input data on the data bus.

Third, the DSF pin is used to invoke the split-register transfer and serial access operation, described in the sections "transfer operation" and "serial operation".

write enable, write-per-bit enable ($\overline{W}$)

The $\overline{W}$ pin enables data to be written to the DRAM and is also used to select the DRAM write-per-bit mode of operation. A logic high level on the $\overline{W}$ input selects the read mode and logic low level selects the write mode. In an early write cycle, $\overline{W}$ is brought low before $\overline{CAS}$ and the DRAM output pins (DQ) remain in the high-impedance state for the entire cycle. During DRAM write cycles, holding $\overline{W}$ low on the falling edge of $\overline{RAS}$ will invoke the write-per-bit operation. Two modes of write-per-bit operation are supported.

Case 1. If DSF is low on the falling edge of RAS, the write mask is reloaded. Accordingly, a four-bit binary code (the write-per-bit mask) is input to the device via the random DQ pins and is latched on the falling edge of $\overline{RAS}$. The write-per-bit mask selects which of the four random I/Os are written and which are not. After $\overline{RAS}$ has latched the write mask on-chip, input data is driven onto the DQ pins and is latched on the falling edge of the later of $\overline{CAS}$ or $\overline{W}$. If a low was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will not be written to that I/O. If a high was strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data will be written to that I/O.

Case 2. If DSF is high on the falling edge of $\overline{RAS}$, the mask is not reloaded from the DQ pins but instead retains the value stored during the last write-per-bit mask reload. This mode of operation is known as persistent write-per-bit, since the write-per-bit mask is persistent over an arbitrary number of cycles.

See the corresponding timing diagrams for details. IMPORTANT: The write-per-bit operation is invoked only if $\overline{W}$ is held low on the falling edge of $\overline{RAS}$. If $\overline{W}$ is held high on the falling edge of $\overline{RAS}$, write-per-bit is not enabled and the write operation is identical to that of standard × 4 DRAMs.

data I/O (DQ0–DQ3)

DRAM data is written during a write or read-modify-write cycle. The falling edge of $\overline{W}$ strobes data into the on-chip data latches. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with data setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low. Thus, the data will be strobed in by $\overline{W}$ with data setup and hold times referenced to this signal.

The 3-state output buffers provide direct TTL compatibility (no pullup resistors required) with a fanout of two Series 74/54 TTL loads. Data-out is the same polarity as data-in. The outputs are in the high impedance (floating) state as long as $\overline{CAS}$ or $\overline{TRG}$ is held high. Data will not appear at the outputs until after both $\overline{CAS}$ and $\overline{TRG}$ have been brought low. Once the outputs are valid, they remain valid while $\overline{CAS}$ and $\overline{TRG}$ are low. $\overline{CAS}$ or $\overline{TRG}$ going high returns the outputs to a high-impedance state. In an early write cycle, the outputs are always in the high-impedance state. In a register transfer operation (memory-to-register or register-to-memory), the outputs remain in the high-impedance state for the entire cycle.

enhanced page mode

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the SMJ44C250 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

Enhanced page mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row address setup, row address hold, and address multiplex is thus eliminated, and a memory cycle time reduction of up to 3 × can be achieved, compared to minimum $\overline{RAS}$ cycle times. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and page mode cycle time used. The SMJ44C250 allows a full page (512 cycles) of information to be accessed in read, write, or read-modify-write mode during a single $\overline{RAS}$ low period using relatively conservative page mode cycle times.

During write-per-bit operations, the DQ pins are used to load the write-per-bit mask register described above under the $\overline{W}$ pin description.

refresh

A refresh operation must be performed to each row at least once every eight milliseconds to retain data. Since the output buffer is in the high-impedance state (unless $\overline{CAS}$ is applied), the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 512 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is accomplished by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$. The external row address is ignored and the refresh address is generated internally.

GND (Pin 8)

This pin is reserved for the manufacturer's test operation. It is an input and should be tied to system ground to ensure proper device operation.

IMPORTANT: GND is not connected internally to V_{SS}.

Table 1. Functional Table

TYPE†	RAS FALL					CAS FALL	ADDRESS		DQ0–DQ3		FUNCTION
	CAS	TRG	W¶	DSF	SE	DSF	RAS	CAS	RAS	CAS‡ W	
R	L	X§	X	X	X	X	X	X	X	X	CAS-before-RAS Refresh
T	H	L	L	X	L	X	Row Addr	Tap Point	X	X	Register to Memory Transfer (Transfer Write)
T	H	L	L	H	X	X	Row Addr	Tap Point	X	X	Alternate Transfer Write (Independent of SE)
T	H	L	L	L	H	X	Refresh Addr	Tap Point	X	X	Serial Write-Mode Enable (Pseudo-Transfer Write)
T	H	L	H	L	X	X	Row Addr	Tap Point	X	X	Memory to Register Transfer (Transfer Read)
T	H	L	H	H	X	X	Row Addr	Tap Point	X	X	Split Register Transfer Read (Must Reload Tap)
R	H	H	L	L	X	L	Row Addr	Col Addr	Write Mask	Valid Data	Load and Use Write Mask, Write Data to DRAM
R	H	H	L	H	X	L	Row Addr	Col Addr	X	Valid Data	Persistent Write-Per-Bit, Write Data to DRAM
R	H	H	H	L	X	L	Row Addr	Col Addr	X	Valid Data	Normal Dram Read/Write (Nonmasked)
R	H	H	H	H	X	L	Refresh Addr	X	X	Write Mask	Load Write Mask

† R = Random access operation; T = Transfer operation.
‡ DQ0–DQ3 are latched on the later of W or CAS falling edge.
§ X = Don't care.
¶ In persistent write-per-bit function, W must be high during the refresh cycles
Addr Mask = 1; write to address location enabled
Write Mask = 1; write to I/O enabled.

random port to serial port interface

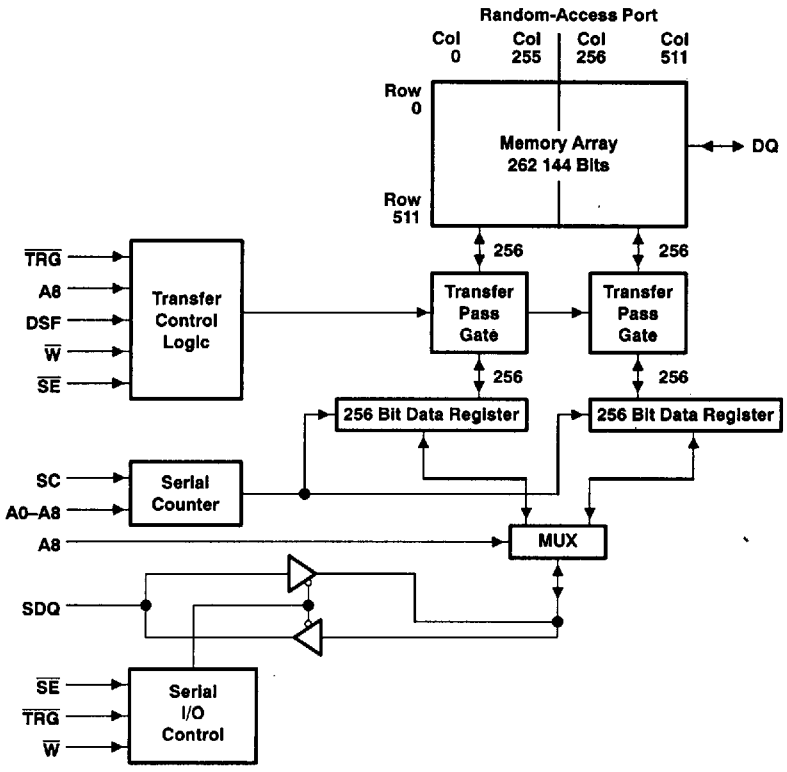


Figure 1. Block Diagram Showing One Random and One Serial I/O Interface

random-address space to serial-address space mapping

The 512 bits in each of the four data registers of the SAM are connected to the 512 column locations of each of the four random I/Os. Data can be accessed in or out of the SAM starting at any of the 512 data bit locations. This start location is selected by addresses A0 through A8 on the falling edge of $\overline{CAS}$ during any transfer cycle. The SAM is accessed starting from the selected start address, proceeding from the lowest to the highest significant bits. After the most significant bit position (511) is accessed, the serial counter wraps around such that bit 0 is accessed on the next clock pulse. The selected start address is stored and used for all subsequent transfer cycles until $\overline{CAS}$ is again brought low during any transfer cycle. Thus, the start address can be set once and $\overline{CAS}$ held high during all subsequent transfer cycles and the start address point will not change regardless of data present on A0 through A8.

split-register mode random-address to serial address-space mapping

In split-register transfer operations, the serial data register is split into halves, the low half containing bits 0–255 and the high half containing bits 256–511. When a split-register transfer cycle is performed, the tap address must be strobed in on the falling edge of $\overline{CAS}$. The most significant column address bit (A8) determines which register half will be reloaded from the memory array. The eight remaining column address bits (A0–A7) are used to select the SAM starting location for the register half selected by A8.

To insure proper operation when using the split-register read transfer feature, a non-split-register transfer must precede any split-register sequence. The serial start address must be supplied for every split-register transfer. (See Split Register Operating Sequence on page 36.)

transfer operations

As illustrated in Table 1, the SMJ44C250 supports five basic transfer modes of operation:

1. Normal Write Transfer (SAM to DRAM)
2. Alternate Write Transfer (independent of the state of $\overline{SE}$)
3. Pseudo Write Transfer (Switches serial port from serial-out mode to serial-in mode. No actual data transfer takes place between the DRAM and the SAM.)
4. Normal Read Transfer (Transfer entire contents of DRAM to SAM)
5. Split-Register Read Transfer (Divides the SAM into a high and a low half. Only one half is transferred to the SAM while the other half is read from the serial I/O port.)

NOTES: A. All transfer write operations will switch the SDQ pins into the input (write) mode. Before data can be clocked into the serial port via the SDQ pins and SC serial clock, it is necessary to switch the SDQ pins into input mode via a previous transfer write operation.
B. *Pseudo Transfer Write Mode* has the same meaning as the term "Write Mode Control Cycle" as used in some VRAM data sheets. Both modes, or control cycles, serve to switch the direction of the SDQs without an actual data transfer taking place.
C. All transfer read operations will switch the SDQ pins into the output (read) operation.
D. All transfer read operations and the pseudo transfer write operation perform a memory refresh on the selected row.

transfer register select ($\overline{TRG}$)

Transfer operations between the memory array and the data registers are invoked by bringing $\overline{TRG}$ low before $\overline{RAS}$ falls. The states of $\overline{W}$, $\overline{SE}$, and DSF, which are also latched on the falling edge of $\overline{RAS}$, determine which transfer operation will be invoked. (See Table 2.)

During read transfer cycles, $\overline{TRG}$ going high causes the addressed row of data to be transferred into the data register. Although the previous data in the data register is overwritten, the last bit of data appearing at SDQ before $\overline{TRG}$ goes high will remain valid until the first positive transition of SC after $\overline{TRG}$ goes high. The data at SDQ will then switch to new data beginning from the selected start, or *tap*, position.

transfer write enable ($\overline{W}$)

In register transfer mode, $\overline{W}$ determines whether a read or a write transfer will occur. To perform a write transfer, $\overline{W}$ and $\overline{SE}$ are held low as $\overline{RAS}$ falls. If $\overline{SE}$ is high during this transition, no transfer of data from the data register to the memory array occurs, but the SDQs are put into the input mode. The SDQs are put into input mode by use of a transfer write cycle. This allows serial data to be input into the SAM. An alternative way to perform the transfer write cycle is by holding DSF high on the falling edge of $\overline{RAS}$. In this way, the state of $\overline{SE}$ is a Don't Care as $\overline{RAS}$ falls. To perform a read transfer operation, $\overline{W}$ is held high and $\overline{SE}$ is a Don't Care as $\overline{RAS}$ falls. This cycle also puts the SDQs into the read mode, allowing serial data to be shifted out of the data register. (See Table 2.)

column enable ($\overline{CAS}$)

If $\overline{CAS}$ is brought low during a control cycle, the address present on the pins A0 through A8 will become the new register start location. If $\overline{CAS}$ is held high during a control cycle, the previous tap address will be retained from the last transfer cycle in which $\overline{CAS}$ went low to set the tap address.

addresses (A0 through A8)

Nine address bits are required to select one of the 512 possible rows involved in the transfer of data to or from the data registers. The states of A0–A8 are latched on the falling edge of $\overline{RAS}$ to select one of 512 rows for the transfer operation.

To select one of the 512 positions in the SAM from which the first serial data will be accessed, the appropriate 9-bit column address (A0–A8) must be valid when $\overline{CAS}$ falls. However, the $\overline{CAS}$ and start (tap) position need not be supplied every cycle, only when changing to a different start position.

In the split-register transfer mode, the most significant column address bit (A8) selects which half of the register will be loaded from the memory array. The remaining eight addresses (A0–A7) determine the register starting location for the register to be loaded.

special function input (DSF)

In the read transfer mode, holding DSF high on the falling edge of $\overline{RAS}$ selects the split-register mode transfer operation. This mode divides the serial data register into a high order half and a low order half; one active, and one inactive. When the cycle is initiated, a transfer occurs between the memory array and either the high half or the low half register, depending on the state of the most significant column address bit (A8) that is strobed in on the falling edge of $\overline{CAS}$. If A8 is high, the transfer is to the high half of the register. If A8 is low, the transfer is to the low half of the register. Use of the split-register mode read transfer feature allows on-the-fly read transfer operation without synchronizing $\overline{TRG}$ to the serial clock.

In the write transfer mode, holding DSF high on the falling edge of $\overline{RAS}$ permits use of an alternate mode of transfer write. This mode allows $\overline{SE}$ to be high on the falling edge of $\overline{RAS}$ without permitting a pseudo write transfer with the serial port disabled during the entire transfer write cycle.

serial access operation

Refer to Tables 2 and 3 for the following discussion on serial access operation.

serial clock (SC)

Data (SDQ) is accessed in or out of data registers on the rising edge of SC. The SMJ44C250 is designed to work with a wide range of clock duty cycles to simplify system design. Since the data registers comprising the SAM are of static design, there are no SAM refresh requirements and there is no minimum SC clock operating frequency.

serial data input/output (SDQ0–SDQ3)

SD and SQ share a common I/O pin. Data is input to the device when $\overline{SE}$ is low during write mode, and data is output from the device when $\overline{SE}$ is low during read mode. The data in the SAM will be accessed in the direction from least significant bit to most significant bit. The data registers operate modulo 512. Thus, after bit 511 is accessed, the next bits to be accessed will be bits 00, 01, 02, and so on.

serial enable ($\overline{SE}$)

The serial enable pin has two functions: first, it is latched on the falling edge of $\overline{RAS}$, with both $\overline{TRG}$ and $\overline{W}$ low to select one of the transfer functions (see Table 2). If $\overline{SE}$ is low during this transition, then a transfer write occurs. If $\overline{SE}$ is high as $\overline{RAS}$ falls and DSF is low, then a write mode control cycle is performed. The function of this cycle is to switch the SDQs from the output mode to the input mode, thus allowing data to be shifted into the data register. NOTE: All transfer read and serial mode enable (pseudo transfer write) operations will perform a memory refresh operation on the selected row.

Second, during serial access operations, $\overline{SE}$ is used as an SDQ enable/disable. In the write mode, $\overline{SE}$ is used as an input enable. $\overline{SE}$ high disables the input and $\overline{SE}$ low enables the input. To take the device out of the write mode and into the read mode, a transfer read cycle must be performed. The read mode allows data to be accessed from the data register. While in the read mode, $\overline{SE}$ high disables the output and $\overline{SE}$ low enables the output.

IMPORTANT: While $\overline{SE}$ is held high, the serial clock is NOT disabled. Thus, external SC pulses will increment the internal serial address counter regardless of the state of $\overline{SE}$. This ungated serial clock scheme minimizes access time of serial output from $\overline{SE}$ low since the serial clock input buffer and the serial address counter are not disabled by $\overline{SE}$.

QSF active status output

QSF is an open-drain output pin. During the split register mode of serial access operation, QSF indicates which half of the serial register in the SAM is being accessed. If QSF is low, then the serial address pointer is accessing the low (least significant) 256 bits of the SAM. If QSF is high, then the pointer is accessing the higher (most significant) 256 bits of the SAM.

QSF changes state upon crossing the boundary between the two register halves. When the SAM is not operating in split-register mode, the QSF output remains in the high-impedance state.

QSF is designed as an open drain output to allow OR-type of QSF outputs from several chips. Thus, an external pullup resistor is required for the zero-to-one transition on QSF, and the output rise time is determined by the load-capacitance and the value of the pullup resistor. The specification for QSF switching time assumes a pullup resistor of 820 Ω and a load capacitance of 30 pF illustrated as follows.

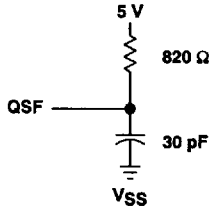


Figure 2. QSF Load Circuit

Table 2. Transfer Operation Logic

$\overline{TRG}$	$\overline{W}$	$\overline{SE}$	DSF	MODE
L	L	L	X	Register to memory (write) transfer, serial write mode enable
L	L	X	H	Alternate register to memory transfer
L	L	H	L	Serial write mode enable (pseudo write transfer)
L	H	X	L	Memory to register (read) transfer
L	H	X	H	Split-register read transfer

NOTE: Above logic states are assumed valid on the falling edge of $\overline{RAS}$.

Table 3. Serial Operation Logic

LAST TRANSFER CYCLE	$\overline{SE}$	SDQ
Alternate register to memory	H	Input Disabled
Serial write mode enable†	L	Input Enabled
Serial write mode enable†	H	Input Disabled
Memory to register	L	Output Enabled
Memory to register	H	Hi-Z

† Pseudo transfer write.

power up

To achieve proper device operation, an initial pause of 200 µs is required after power up, followed by a minimum of eight $\overline{RAS}$ cycles or eight $\overline{CAS}$-before-$\overline{RAS}$ cycles, a memory-to-register transfer cycle, and two SC cycles.

absolute maximum ratings over operating temperature (unless otherwise noted)†

Input voltage on any pin except DQ and SDQ (see Note 1) ..... −1 V to 7 V
Input voltage on DQ and SDQ (see Note 1) ..... −1 V to V_{CC} + 1
Supply voltage range on V_{CC} (see Note 1) ..... 0 V to 7 V
Short circuit output current (per output) ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range:
SMJ44C250, L suffix ..... 0°C to70°C
SMJ44C250, M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage		2.9		V_{CC} + 1	V
V_{IL}	Low-level input voltage (see Note 2)		−1		0.6	V
T_A	Operating free-air temperature	L suffix	0			°C
		M suffix	−55			
T_C	Operating case temperature	L suffix			70	°C
		M suffix			125	

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High level output voltage	I_{OH} = – 5 mA	2.4		V
V_{OL}	Low level output voltage (see Note 4)	I_{OL} = 4.2 mA		0.4	V
I_I	Input leakage current	V_I = 0 to 5.8 V, V_{CC} = 5 V, All other pins open		±1.0	µA
I_O	Output leakage current (see Note 3)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V		±10	µA

PARAMETER			SAM PORT	'44C250-10		'44C250-12		UNIT
				MIN	MAX	MIN	MAX	
I_{CC1} I_{CC1A}	Operation current $t_{c(RW)}$ = Minimum $t_{c(SC)}$ = Minimum	(see Note 5)	Standby		100		90	mA
			Active		110		100	
I_{CC2} I_{CC2A}	Standby current, All clocks = V_{CC} $t_{c(SC)}$ = Minimum		Standby		15		15	
			Active		35		35	
I_{CC3} I_{CC3A}	$\overline{RAS}$-only refresh current, $t_{c(RW)}$ = Minimum $t_{c(SC)}$ = Minimum		Standby		100		90	
			Active		110		100	
I_{CC4} I_{CC4A}	Page mode current, $t_{c(P)}$ = Minimum $t_{c(SC)}$ = Minimum		Standby		65		60	
			Active		70		65	
I_{CC5} I_{CC5A}	$\overline{CAS}$-before-$\overline{RAS}$ current, $t_{c(RW)}$ = Minimum $t_{c(SC)}$ = Minimum		Standby		90		80	
			Active		110		100	
I_{CC6} I_{CC6A}	Data transfer current, $t_{c(RW)}$ = Minimum $t_{c(SC)}$ = Minimum		Standby		100		90	
			Active		110		100	

NOTES: 3. $\overline{SE}$ is disabled for SDQ output leakage tests.

4. The SMJ44C250 1-megabit video RAM may exhibit simultaneous switching noise as described in Texas Instruments *Advanced CMOS Logic Designer's Handbook*. This phenomenon exhibits itself upon the DQ pins when the SDQ pins are switched and upon the SDQ pins when DQ pins are switched. This may cause the V_{OL} and V_{OH} to exceed the data book limit for a short period of time, depending upon output loading and temperature. Care should be taken to provide proper termination, decoupling, and layout of the device to minimize simultaneous switching effects.

5. I_{CC} (standby) vs I_{CCA} (active) denotes the following:
I_{CC} (standby) denotes that the SAM port is inactive (standby) and the DRAM port is active (except for I_{CC2}).
I_{CCA} (active) denotes that the SAM port is active and the DRAM port is active (except for I_{CC2}).
I_{CC} is measured with no load on DQ or SDQ pins.

capacitance over recommended ranges of supply voltage and operating temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7	pF
$C_{o(O)}$	Output capacitance, SDQ and DQ		8	pF
$C_{o(QSF)}$	Output capacitance, QSF		14	pF

NOTE 6: Capacitance is sampled only at initial design and after any major change. Samples are tested at 0 V and 25°C with a 1 MHz signal applied to the pin under test. All other pins are open.

switching characteristics over recommended ranges of supply voltage and operating temperature (see Note 7)

NO.	PARAMETER		TEST CONDITIONS	ALT. SYMBOL	'44C250-10		'44C250-12		UNIT
					MIN	MAX	MIN	MAX	
1	$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{d(RLCL)}$ = MAX	t_{CAC}		25		30	ns
2	$t_{a(CA)}$	Access time from column address	$t_{d(RLCL)}$ = MAX	t_{CAA}		50		60	ns
3	$t_{a(CP)}$	Access time from $\overline{CAS}$ high	$t_{d(RLCL)}$ = MIN	t_{CAP}		55		65	ns
4	$t_{a(R)}$	Access time from $\overline{RAS}$	$t_{d(RLCL)}$ = MIN	t_{RAC}		100		120	ns
5	$t_{a(G)}$	Access time of Q from $\overline{TRG}$ low		t_{OEA}		25		30	ns
6	$t_{a(SQ)}$	Access time of SQ from SC high	C_L = 30 pF	t_{SCA}		30		35	ns
7	$t_{a(SE)}$	Access time of SQ from $\overline{SE}$ low	C_L = 30 pF	t_{SEA}		20		25	ns
8	$t_{a(QSF)}$	Access time of QSF from SC low	C_L = 30 pF			60		60	ns
9	$t_{dis(CH)}$	Random output disable time from $\overline{CAS}$ high (see Note 8)	C_L = 80 pF	t_{OFF}	0	20	0	20	ns
10	$t_{dis(G)}$	Random output disable time from $\overline{TRG}$ high (see Note 8)	C_L = 80 pF	t_{OEZ}	0	20	0	20	ns
11	$t_{dis(SE)}$	Serial output disable time from $\overline{SE}$ high (see Note 8)	C_L = 30 pF	t_{SEZ}	0	20	0	20	ns

NOTES: 7. Switching times assume C_L = 100 pF unless otherwise noted (see Figure 3).
8. Disable times are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating temperature†

NO.	PARAMETER		ALT. SYMBOL	'44C250-10		'44C250-12		UNIT
				MIN	MAX	MIN	MAX	
12	$t_{c(rd)}$	Read cycle time (see Note 9)	t_{RC}	190		220		ns
13	$t_{c(W)}$	Write cycle time	t_{WC}	190		220		ns
14	$t_{c(rdW)}$	Read-modify-write cycle time	t_{RWC}	250		290		ns
15	$t_{c(P)}$	Page-mode read, write cycle time	t_{PC}	60		70		ns
16	$t_{c(RDWP)}$	Page-mode read-modify-write cycle time	t_{RWC}	105		125		ns
17	$t_{c(TRD)}$	Transfer read cycle time	t_{RC}	190		220		ns
18	$t_{c(TW)}$	Transfer write cycle time	t_{WC}	190		220		ns
19	$t_{c(SC)}$	Serial clock cycle time (see Note 10)	t_{SCC}	30		35		ns
20	$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	20		30		ns
21	$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 11)	t_{CAS}	25	75 000	30	75 000	ns
22	$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	80		90		ns
23	$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 12)	t_{RAS}	100	75 000	120	75 000	ns
24	$t_{w(WL)}$	Pulse duration, $\overline{W}$ low	t_{WP}	25		25		ns
25	$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		25		30		ns
26	$t_{w(SCH)}$	Pulse duration, SC high	t_{SC}	10		12		ns
27	$t_{w(SCL)}$	Pulse duration, SC low	t_{SCP}	10		12		ns
28	$t_{su(CA)}$	Column address setup time	t_{ASC}	0		0		ns
29	$t_{su(SFC)}$	DSF setup time before $\overline{CAS}$ low		0		0		ns
30	$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
31	$t_{su(WMR)}$	$\overline{W}$ setup time before $\overline{RAS}$ low	t_{WSR}	0		0		ns
32	$t_{su(DQR)}$	DQ setup time before $\overline{RAS}$ low (write mask operation)	t_{MS}	0		0		ns
33	$t_{su(TRG)}$	$\overline{TRG}$ setup time before $\overline{RAS}$ low	t_{TLS}	0		0		ns
34	$t_{su(SE)}$	$\overline{SE}$ setup time before $\overline{RAS}$ low (see Note 13)	t_{ESR}	0		0		ns
35	$t_{su(SFR)}$	DSF setup time before $\overline{RAS}$ low		0		0		ns
36	$t_{su(DCL)}$	Data setup time before $\overline{CAS}$ low	t_{DSC}	0		0		ns
37	$t_{su(DWL)}$	Data setup time before $\overline{W}$ low	t_{DSW}	0		0		ns
38	$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		ns
39	$t_{su(WCL)}$	Early write command setup time before $\overline{CAS}$ low	t_{WCS}	−5		−5		ns
40	$t_{su(WCH)}$	Write setup time before $\overline{CAS}$ high	t_{CWL}	25		30		ns
41	$t_{su(WRH)}$	Write setup time before $\overline{RAS}$ high	t_{RWL}	25		30		ns
42	$t_{su(SDS)}$	SD setup time before SC high	t_{SDS}	3		3		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 9. All cycle times assume t_t = 5 ns.
10. When the odd tap is used (tap address can be 0–511, and odd taps are 1,3,5, etc.), the cycle time for SC in the first serial data out cycle needs to be 70 ns minimum.
11. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$).
12. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).
13. Register to memory (write) transfer cycles only.

timing requirements over recommended ranges of supply voltage and operating temperature (continued)†

NO.	PARAMETER		ALT. SYMBOL	'44C250-10		'44C250-12		UNIT
				MIN	MAX	MIN	MAX	
43	$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	20		20		ns
44	$t_{h(SFC)}$	DSF hold time after $\overline{CAS}$ low		20		20		ns
45	$t_{h(RA)}$	Row address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		ns
46	$t_{h(TRG)}$	$\overline{TRG}$ hold time after $\overline{RAS}$ low	t_{TLH}	15		15		ns
47	$t_{h(SE)}$	$\overline{SE}$ hold time after $\overline{RAS}$ low (see Note 13)	t_{REH}	15		15		ns
48	$t_{h(RWM)}$	$\overline{W}$ hold time after $\overline{RAS}$ low	t_{RWH}	15		15		ns
49	$t_{h(RDQ)}$	DQ hold time after $\overline{RAS}$ low (write mask operation)	t_{MH}	15		15		ns
50	$t_{h(SFR)}$	DSF hold time after $\overline{RAS}$ low		15		15		ns
51	$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low (see Note 14)	t_{AR}	45		45		ns
52	$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	20		25		ns
53	$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 14)	t_{DHR}	45		50		ns
54	$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	20		25		ns
55	$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ (see Note 15)	t_{RCH}	0		0		ns
56	$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ (see Note 15)	t_{RRH}	10		10		ns
57	$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low	t_{WCH}	30		35		ns
58	$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 14)	t_{WCR}	50		55		ns
59	$t_{h(WLG)}$	$\overline{TRG}$ hold time after $\overline{W}$ low (see Note 20)	t_{WCR}	25		30		ns
60	$t_{h(SDS)}$	SD hold time after SC high	t_{SDH}	5		5		ns
61	$t_{h(SHSQ)}$	SQ hold time after SC high	t_{SOH}	5		5		ns
62	$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		ns
63	$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
64	$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	25		30		ns
65	$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Notes 16 and 17)	t_{CWD}	55		65		ns
66	$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 18)	t_{RCD}	25	75	25	90	ns
67	$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	50		60		ns
68	$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 16)	t_{RWD}	130		155		ns
69	$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 16)	t_{AWD}	85		100		ns
70	$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 19)	t_{CHR}	25		25		ns
71	$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 19)	t_{CSR}	10		10		ns
72	$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 19)	t_{RPC}	10		10		ns
73	$t_{d(CLGH)}$	Delay time, $\overline{CAS}$ low to $\overline{TRG}$ high	t_{CTH}	25		30		ns
74	$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ (see Note 16)		25		30		ns
75	$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high	t_{RTH}	90		95		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 13. Register to memory (write) transfer cycles only.
14. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
15. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
16. Read-modify-write operation only.
17. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.
18. Maximum value specified only to assure $\overline{RAS}$ access time.
19. $\overline{CAS}$-before-$\overline{RAS}$ refresh operation only.
20. Output enable controlled write. Outputs remain in the high-impedance state for the entire cycle.

timing requirements over recommended ranges of supply voltage and operating temperature (concluded)†

NO.	PARAMETER		ALT. SYMBOL	'44C250-10		'44C250-12		UNIT
				MIN	MAX	MIN	MAX	
76	$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 21)	t_{RSD}	130		140		ns
77	$t_{d(CLSH)}$	Delay time, $\overline{CAS}$ low to first SC high after $\overline{TRG}$ high (see Note 21)	t_{CSD}	40		45		ns
78	$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high (see Notes 21 and 22)	t_{TSL}	15		20		ns
79	$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see Note 21)	t_{TRD}	−10		−10		ns
80	$t_{d(SCRL)}$	Delay time, SC high to $\overline{RAS}$ (see Notes 13 and 21)	t_{SRS}	10		20		ns
81	$t_{d(SCSE)}$	Delay time, SC high to $\overline{SE}$ high in serial input mode		20		20		ns
82	$t_{d(RHSC)}$	Delay time, $\overline{RAS}$ high to SC high (see Note 13)	t_{SRD}	25		30		ns
83	$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 24)	t_{TRP}	$t_{w(RH)}$		$t_{w(RH)}$		ns
84	$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 24)	t_{TSD}	35		40		ns
85	$t_{d(SESC)}$	Delay time, $\overline{SE}$ low to SC high (see Note 25)	t_{SWS}	10		15		ns
86	$t_{d(RHMS)}$	Delay time, $\overline{RAS}$ high to last (most significant) rising edge of SC before boundary switch during split read transfer cycles		25		30		ns
87	$t_{d(TPRL)}$	Delay time, first (TAP) rising edge of SC after boundary switch to $\overline{RAS}$ low during split read transfer cycles		20		25		ns
88	$t_{rf(MA)}$	Refresh time interval, memory	t_{REF}		8		8	ms

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 13. Register to memory (write) transfer cycles only.
21. Memory to register (read) transfer cycles only.
22. In a transfer read cycle, the state of SC when $\overline{TRG}$ rises is a Don't Care condition. However, to assure proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{TRG}$ goes high.
23. In a transfer write cycle, the state of SC when $\overline{RAS}$ falls is a Don't Care condition. However, to assure proper sequencing of the internal clock circuitry, there can be no positive transitions of SC for at least 10 ns prior to when $\overline{RAS}$ goes low.
24. Memory to register (read) and register to memory (write) transfer cycles only.
25. Serial data-in cycles only.
26. System transition times (rise and fall) are to be a minimum of 3 ns and a maximum of 50 ns.

PARAMETER MEASUREMENT INFORMATION

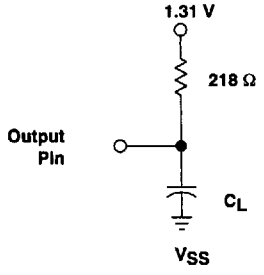


Figure 3. Load Circuit

PARAMETER MEASUREMENT INFORMATION

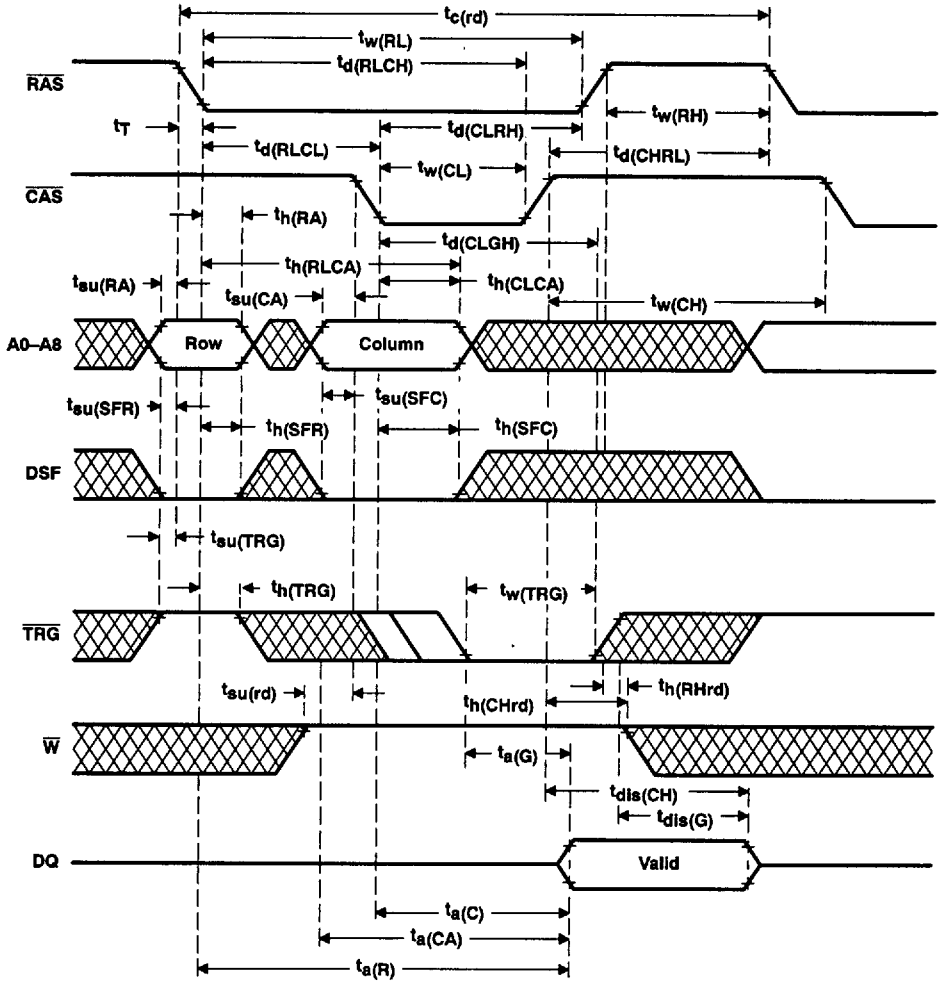
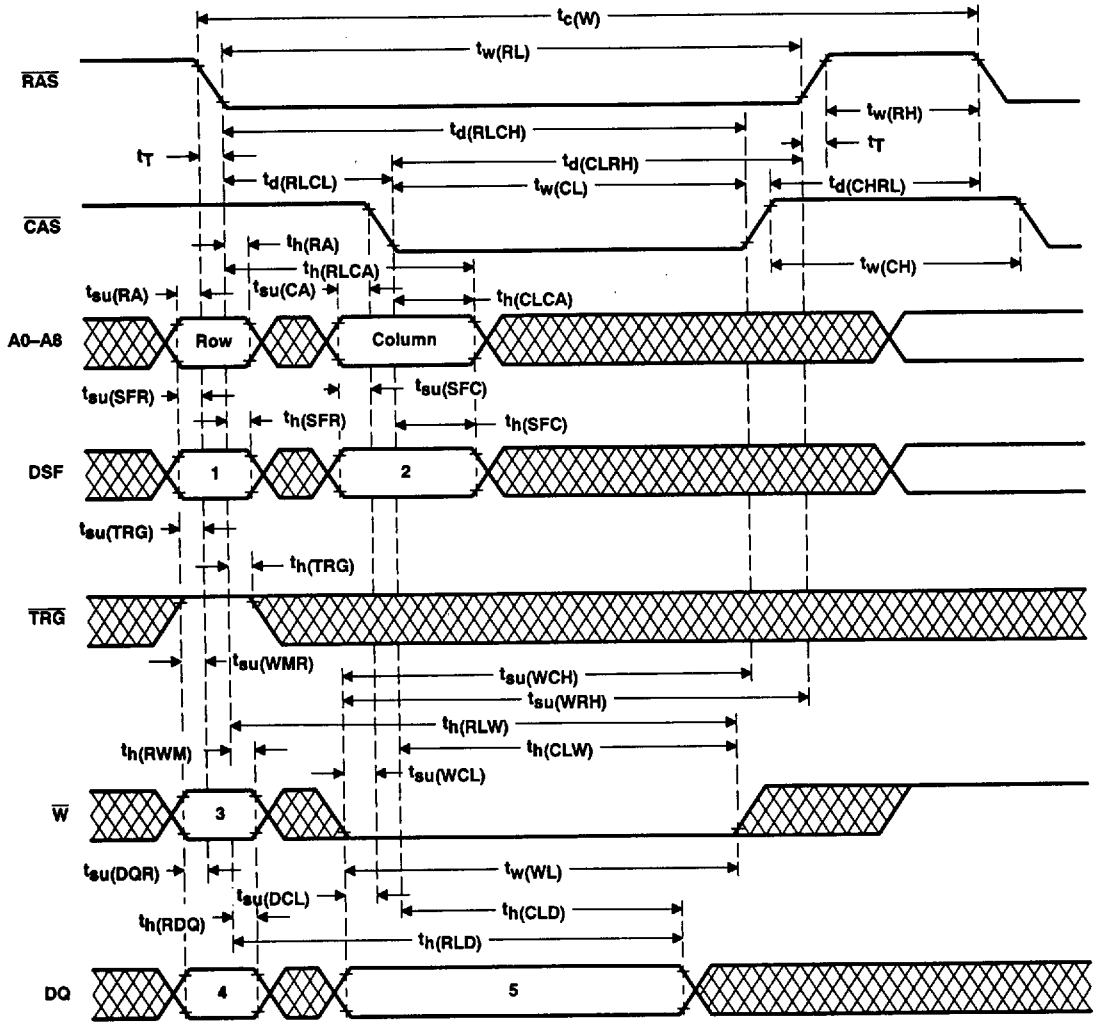


Figure 4. Read Cycle Timing

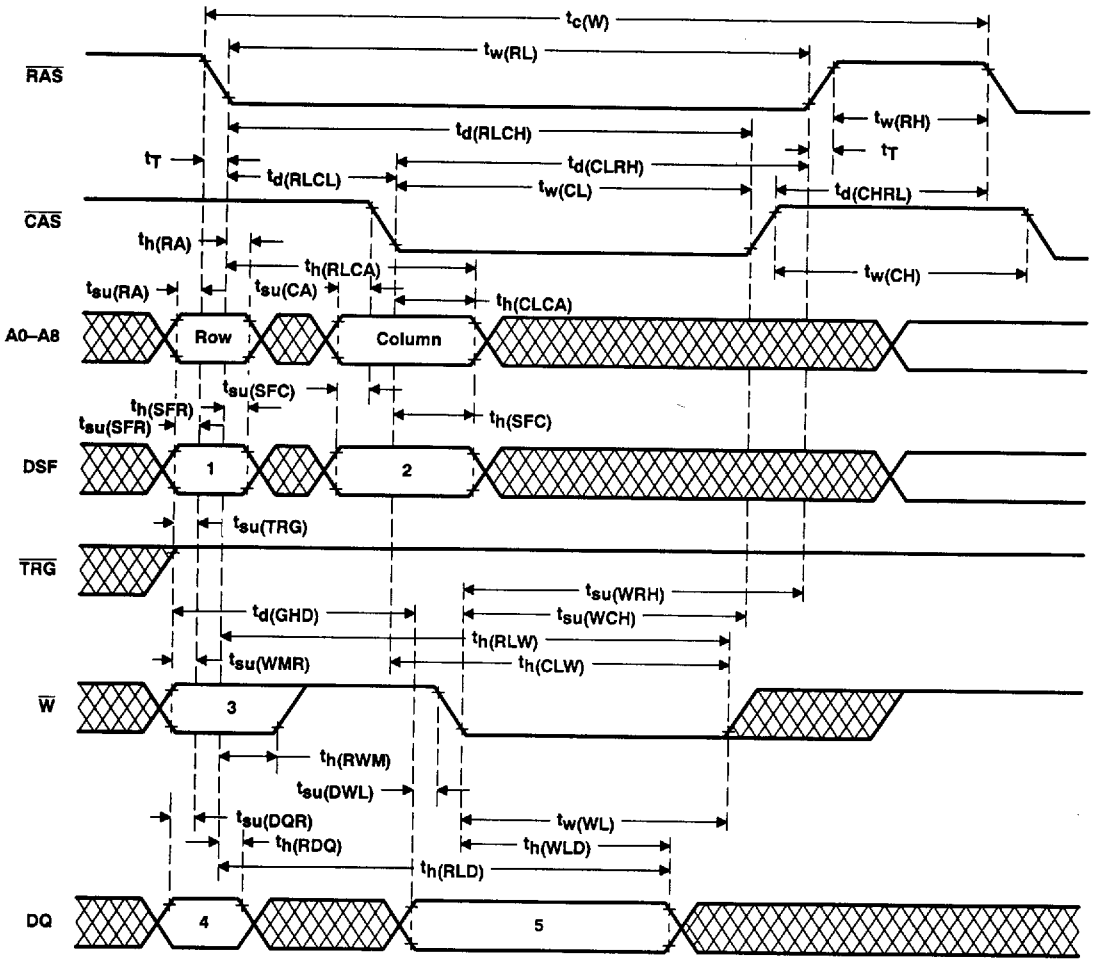
PARAMETER MEASUREMENT INFORMATION



NOTE A: See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

Figure 5. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

Figure 6. Delayed Write Cycle Timing

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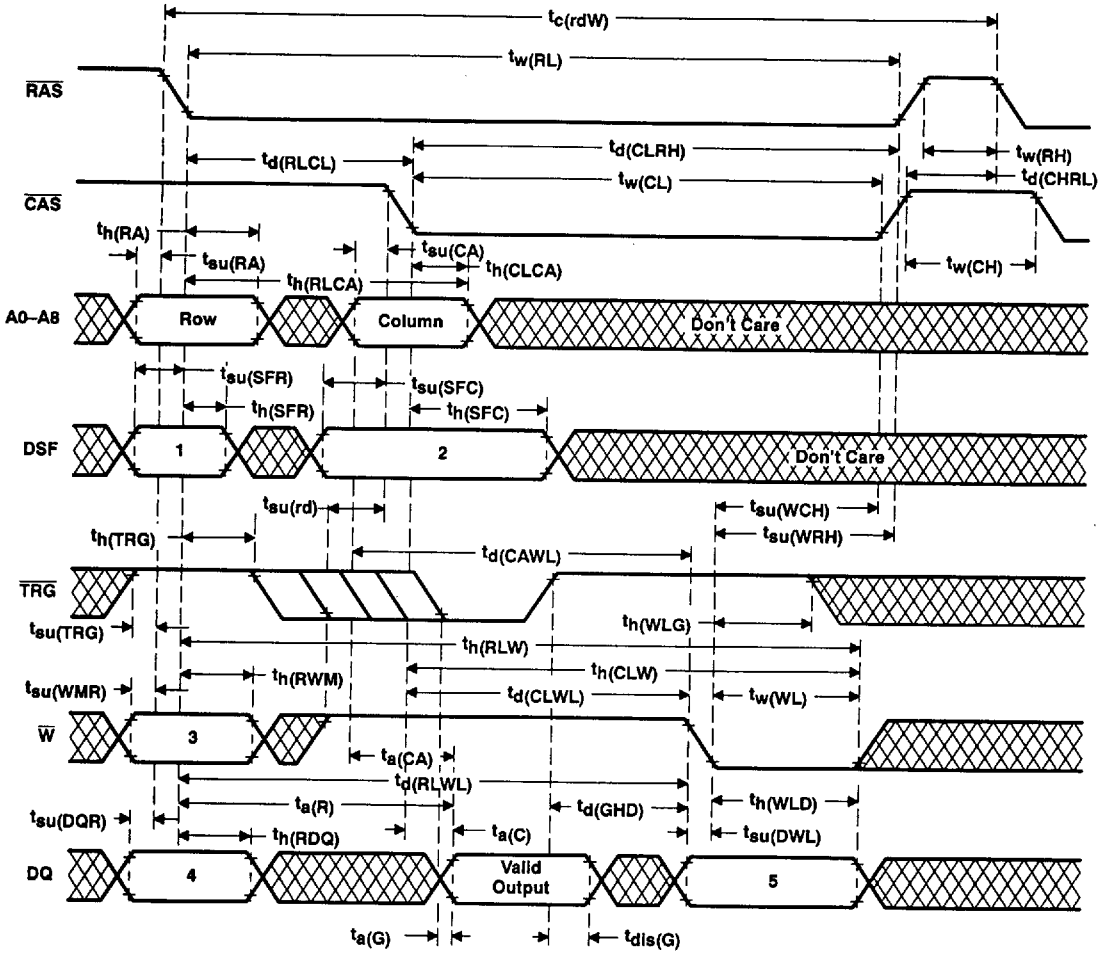
PARAMETER MEASUREMENT INFORMATION

write cycle state table

CYCLE	STATE				
	1	2	3	4	5
Write mask load/use write DQs to I/Os	L	L	L	Write Mask	Valid Data
Use previous write mask, write DQs to I/Os	H	L	L	Don't Care	Valid Data
Load write mask on later of $\overline{W}$ fall and $\overline{CAS}$ fall	H	L	H	Don't Care	Write Mask
Normal early or late write operation	L	L	H	Don't Care	Valid Data

PARAMETER MEASUREMENT INFORMATION



NOTE A: See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5". Same logic as delayed write cycle.

Figure 7. Read-Write/Read-Modify-Write Cycle Timing

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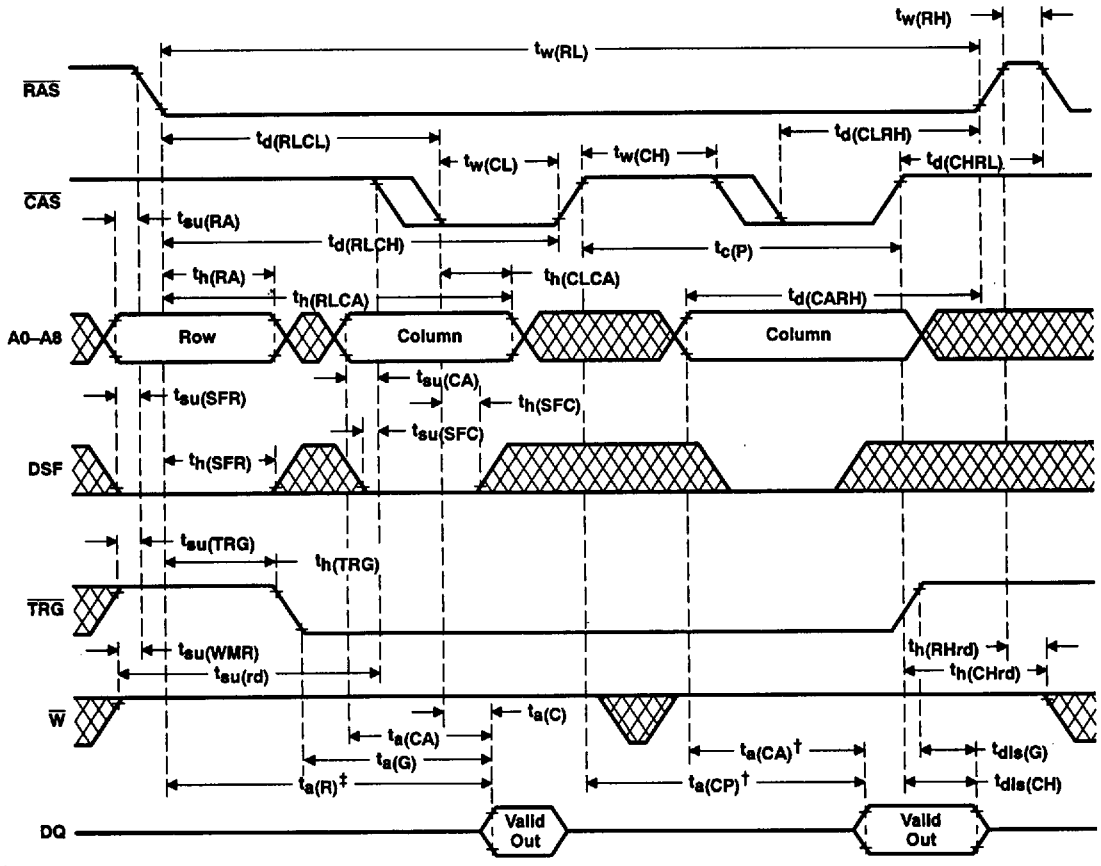
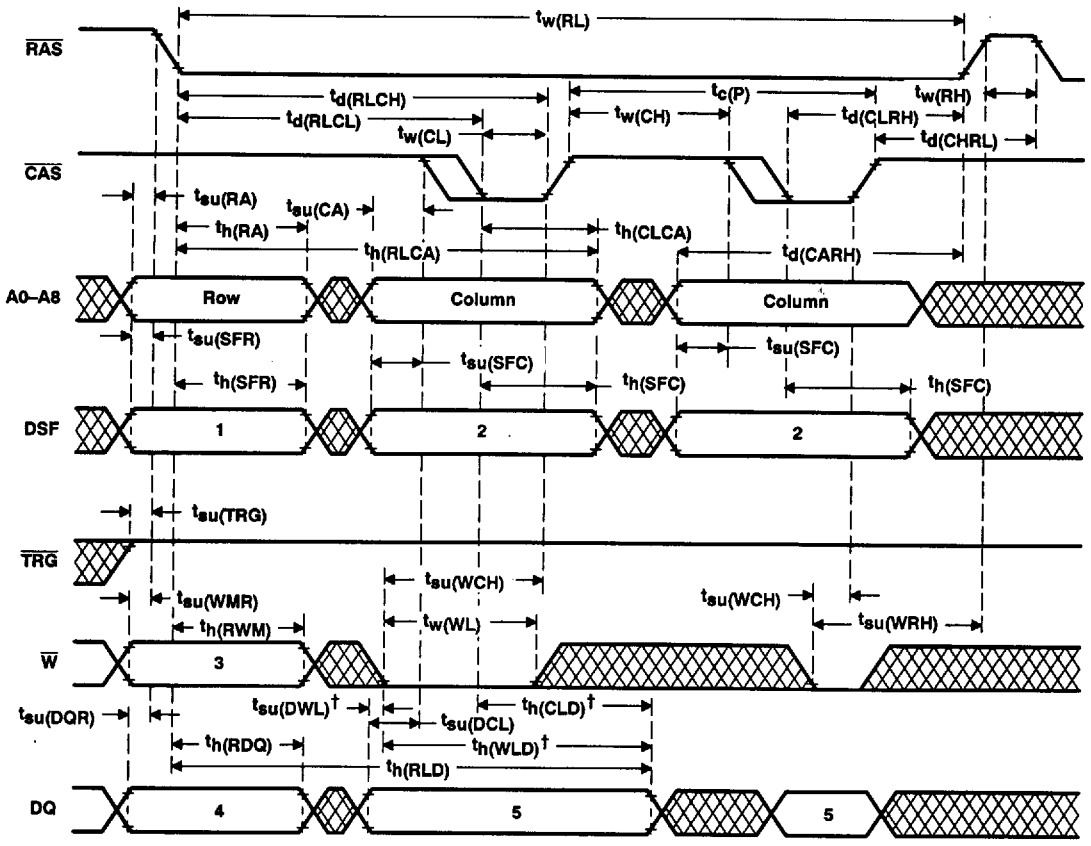
PARAMETER MEASUREMENT INFORMATION



† Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
‡ Output may go from high-impedance state to an invalid data state prior to the specified access time.
NOTE A: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edge of $\overline{RAS}$ and $\overline{CAS}$ to select the desired write mode (normal, block write, etc.).

Figure 8. Enhanced Page-Mode Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION



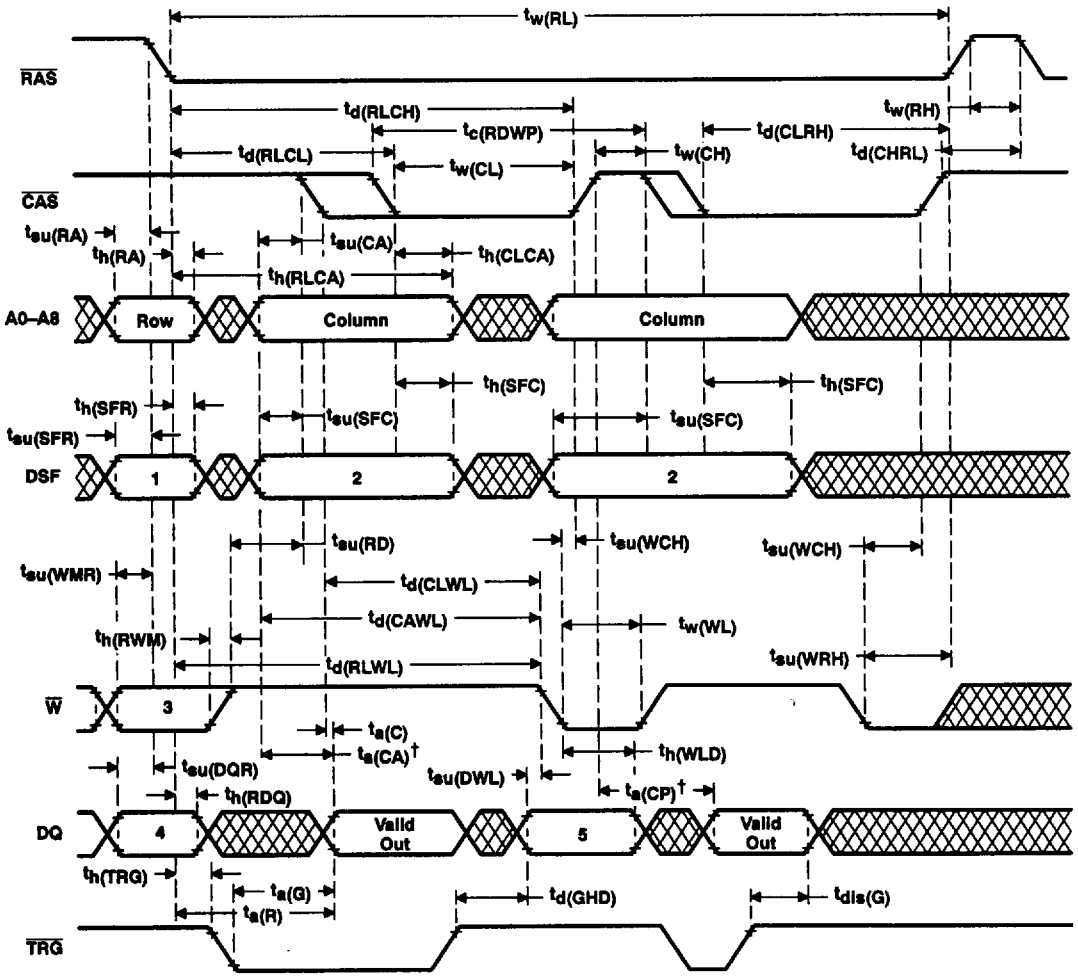
† Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

NOTES: A. See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

B. A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used, to assure page-mode cycle time. If the early write cycle timing is used, the state of $\overline{TRG}$ is a Don't Care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

Figure 9. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† Output may go from the high-impedance state to an invalid data state prior to the specified access time.

NOTES: A. See "Write Cycle State Table" for the logic state of "1", "2", "3", "4", and "5".

B. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

Figure 10. Enhanced Page-Mode Read-Modify-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

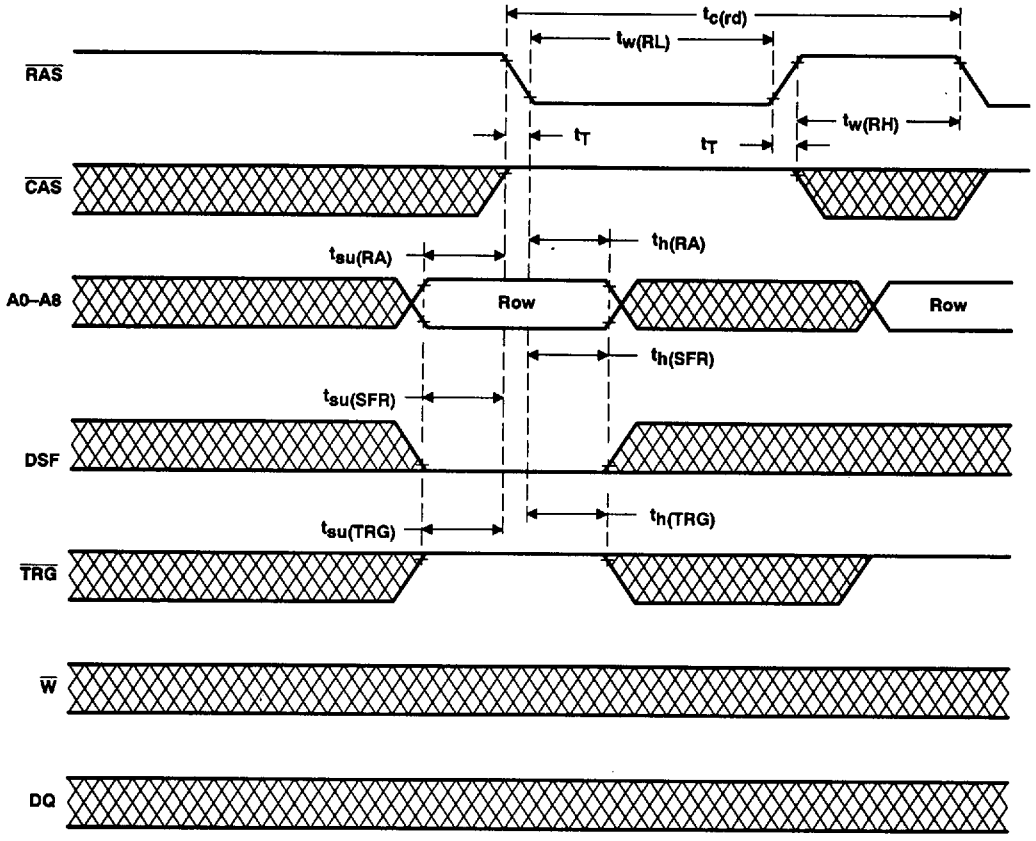


Figure 11. $\overline{RAS}$-Only Refresh Timing

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PARAMETER MEASUREMENT INFORMATION

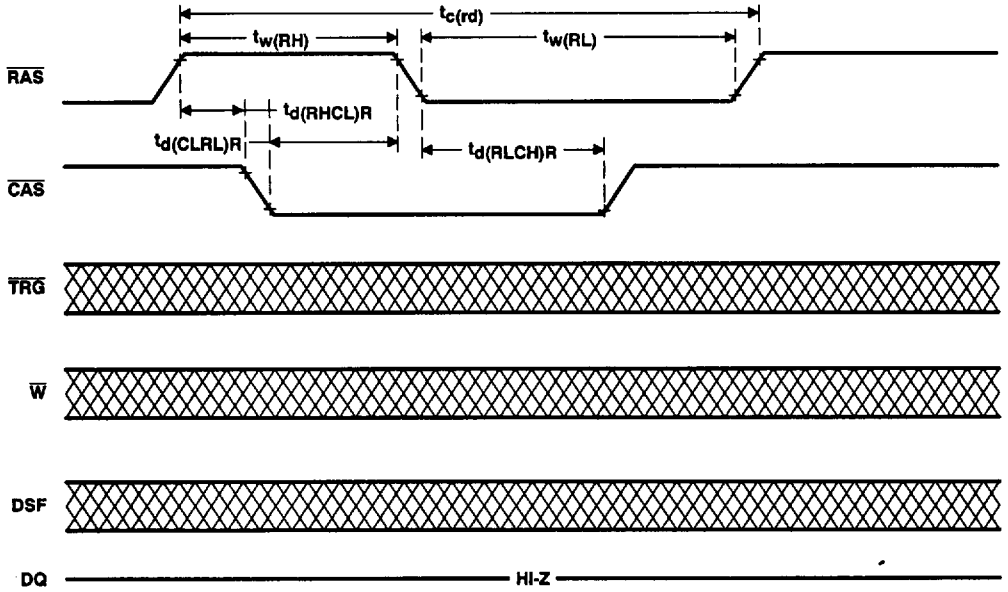


Figure 12. $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh

PARAMETER MEASUREMENT INFORMATION

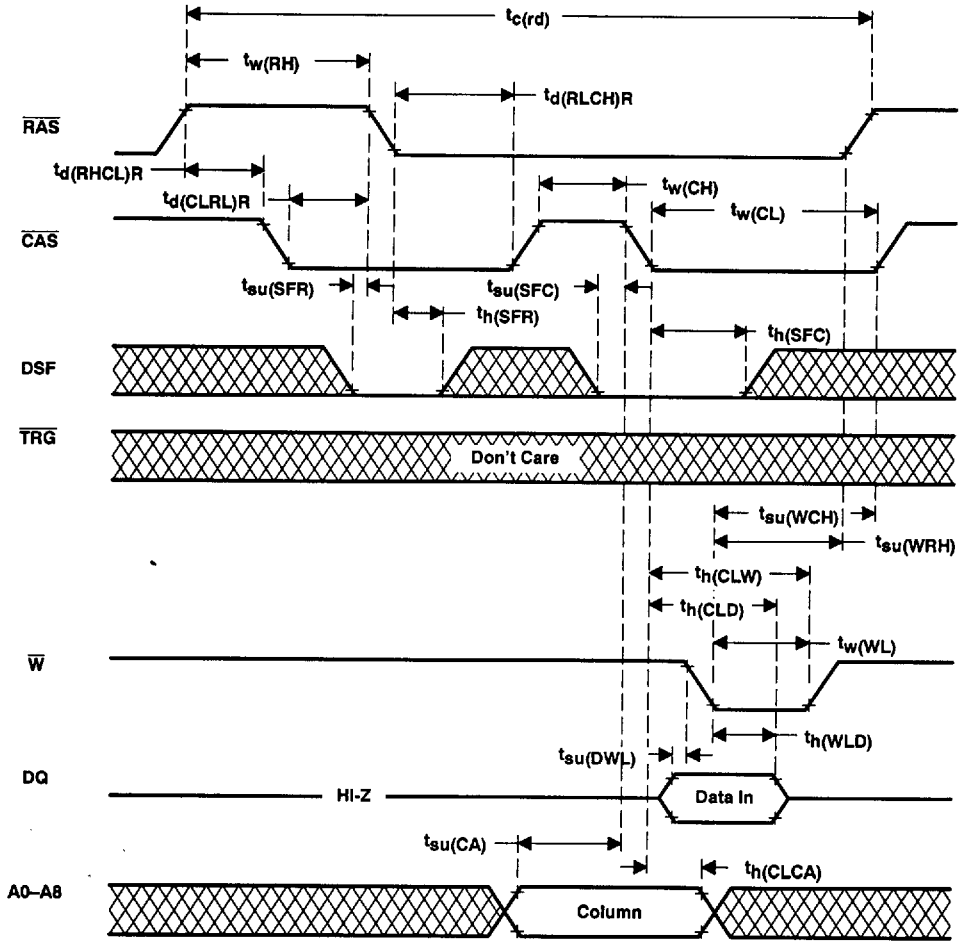


Figure 13. $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Timing

PARAMETER MEASUREMENT INFORMATION

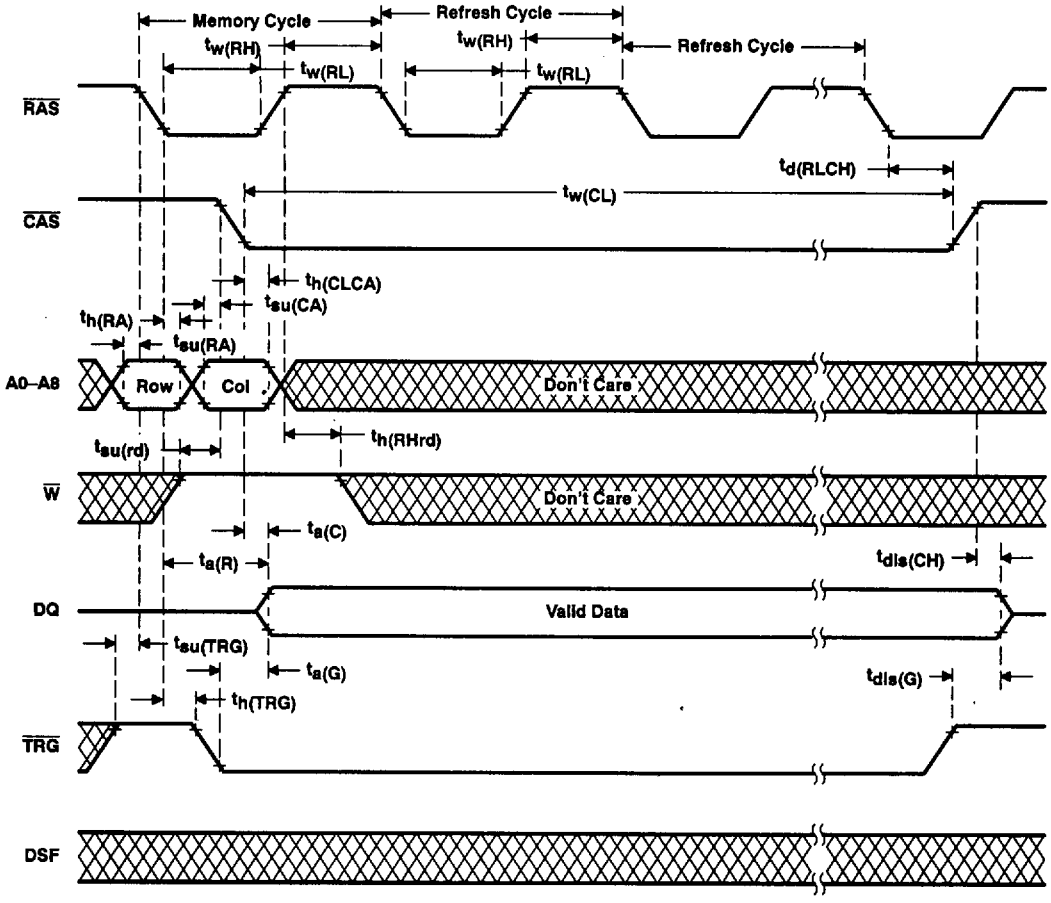
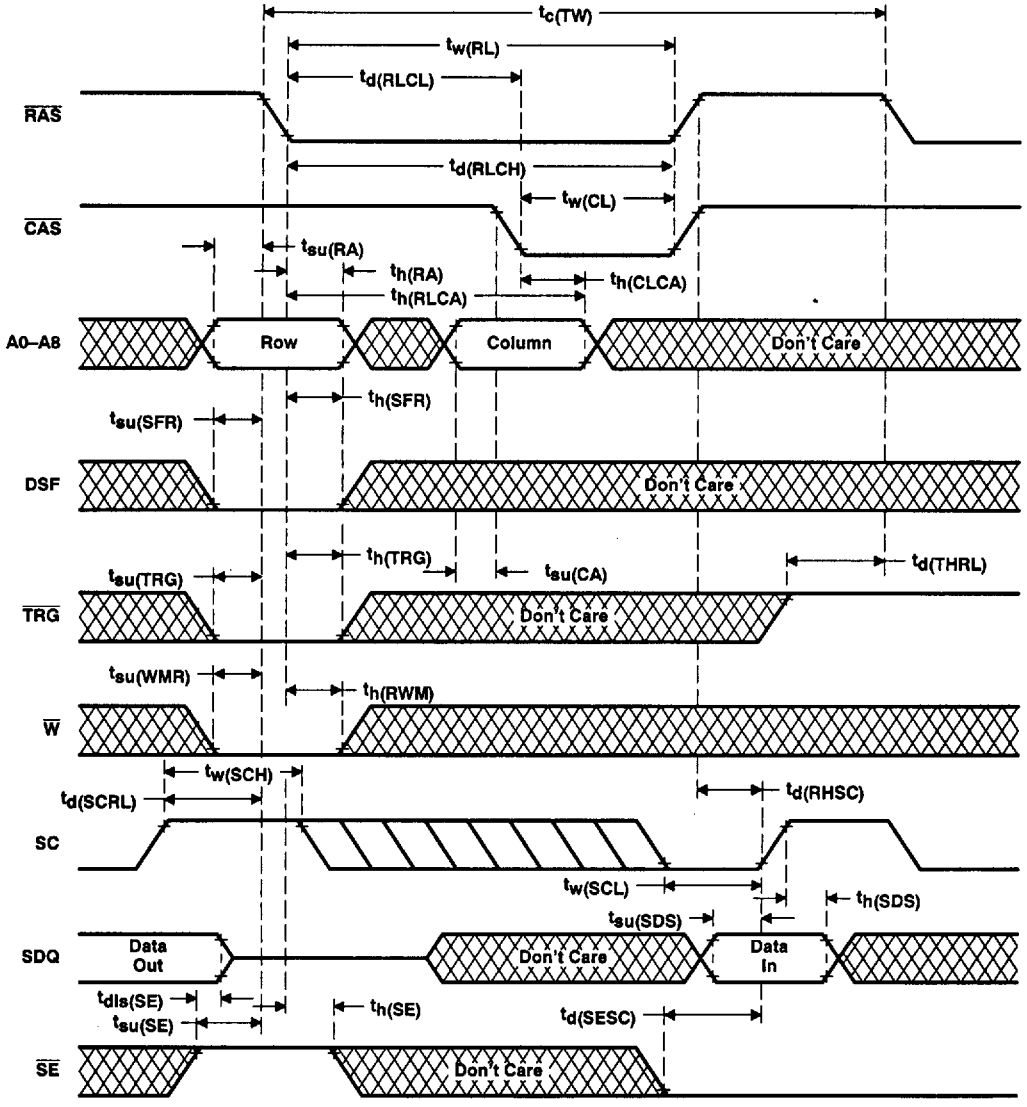


Figure 14. Hidden Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION

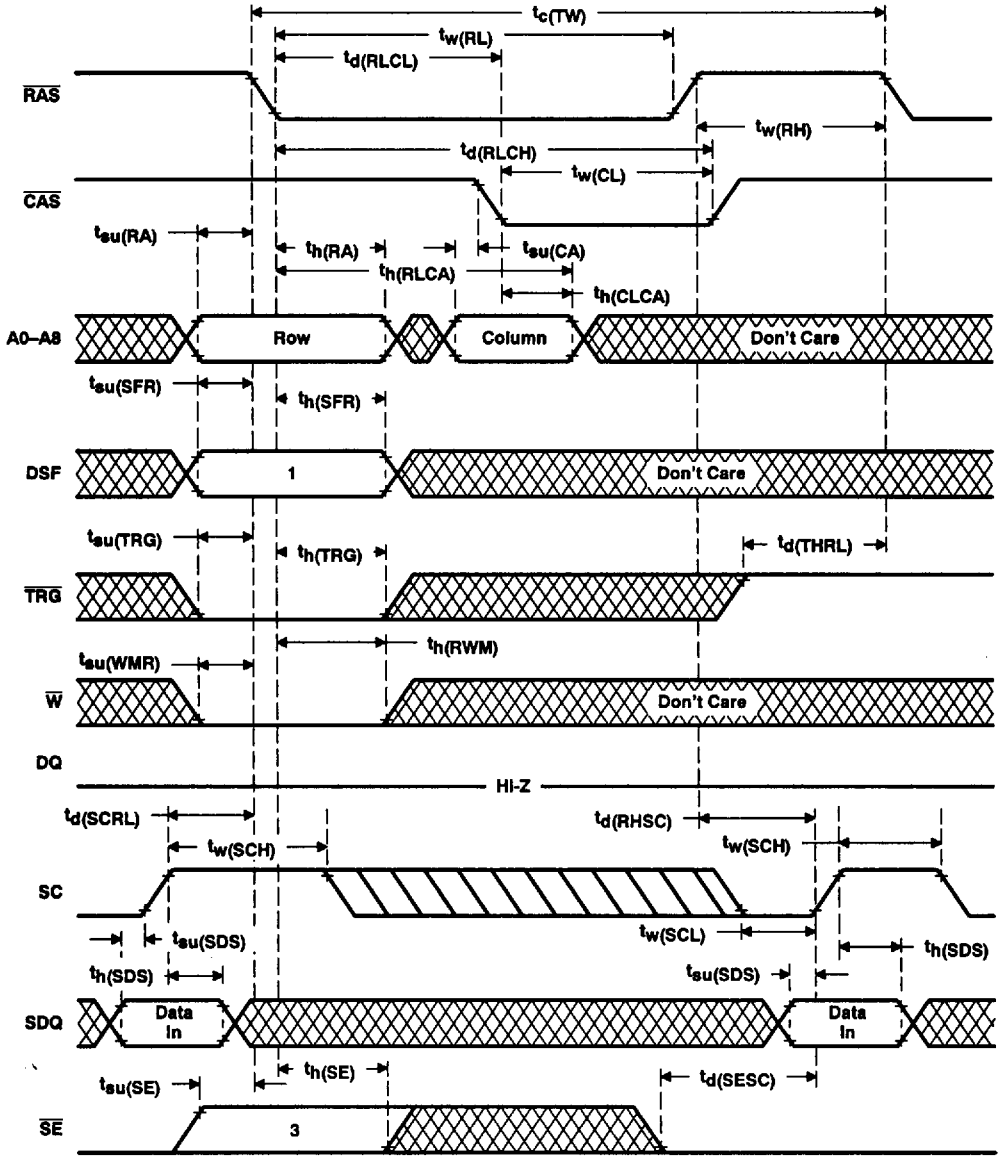
The write-mode control cycle is used to change the SDQs from the output mode to the input mode. This allows serial data to be written into the data register. The diagram below assumes that the device was originally in the serial read mode.



NOTES: A. Random-mode Q outputs remain in the high-impedance state for the entire write-mode control.
B. $\overline{SE}$ must be high as $\overline{RAS}$ falls in order to perform a write-mode control cycle.

Figure 15. Write-Mode Control Pseudo Write Transfer Timing

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Random mode Q outputs remain in the high-impedance state for the entire data register to memory transfer cycle. This cycle is used to transfer data from the data register to the memory array. Every one of the 512 locations in each data register is written into the corresponding 512 columns of the selected row. Data in the data register may proceed from a serial shift-in or from a parallel load from one of the memory array rows. The above diagram assumes that the device is in the serial write mode (i.e., SD is enabled by a previous write mode control cycle, thus allowing data to be shifted-in).

B. See "Register Transfer Function Table" for logic state of "1" and "3".

C. Successive transfer writes can be performed without serial clocks for applications requiring fast memory array clears.

Figure 16. Data Register to Memory Timing, Serial Input Enabled

PARAMETER MEASUREMENT INFORMATION

register transfer function table

FUNCTION	$\overline{RAS}$ FALL			
	$\overline{TRG}$	$\overline{W}$	DSF (1)	$\overline{SE}$ (3)
Register to memory transfer	L	L	X	L
Register to memory transfer, alternate transfer write	L	L	H	X
Pseudo-transfer SDQ control, serial input enabled	L	L	L	H
Memory to register transfer	L	H	L	X
Split-register transfer	L	H	H	X

PARAMETER MEASUREMENT INFORMATION

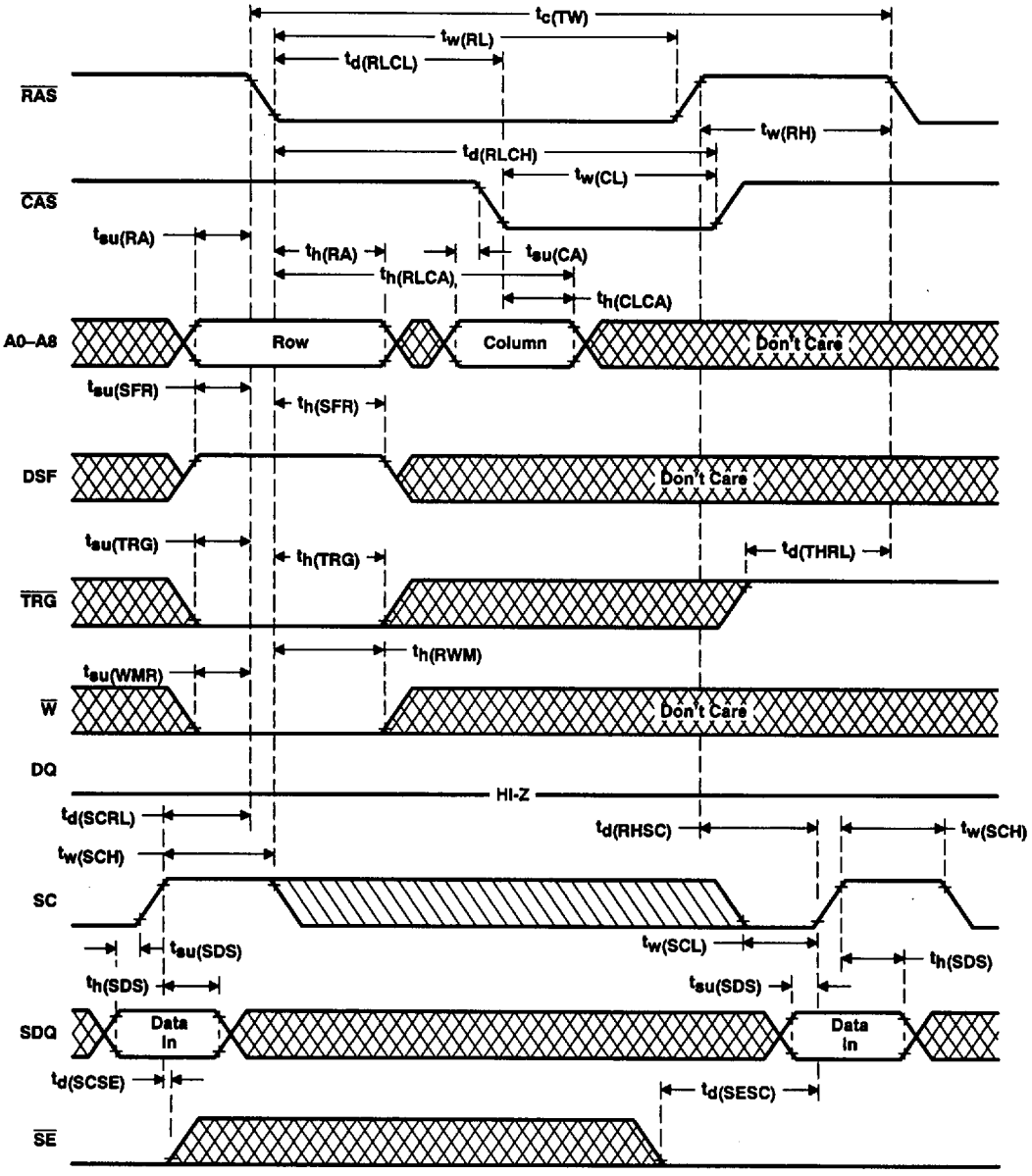
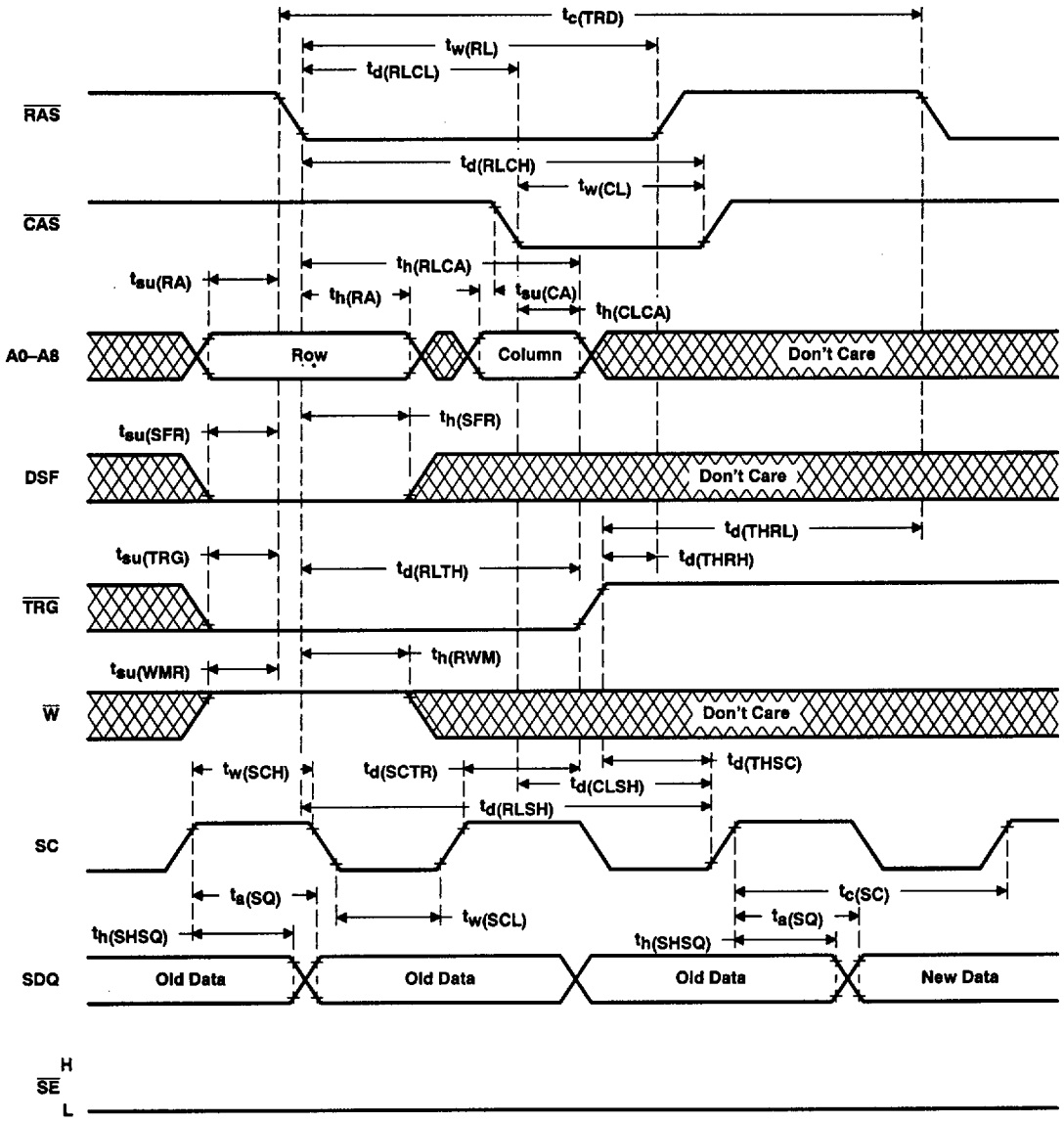


Figure 17. Alternate Data Register to Memory Timing

PARAMETER MEASUREMENT INFORMATION

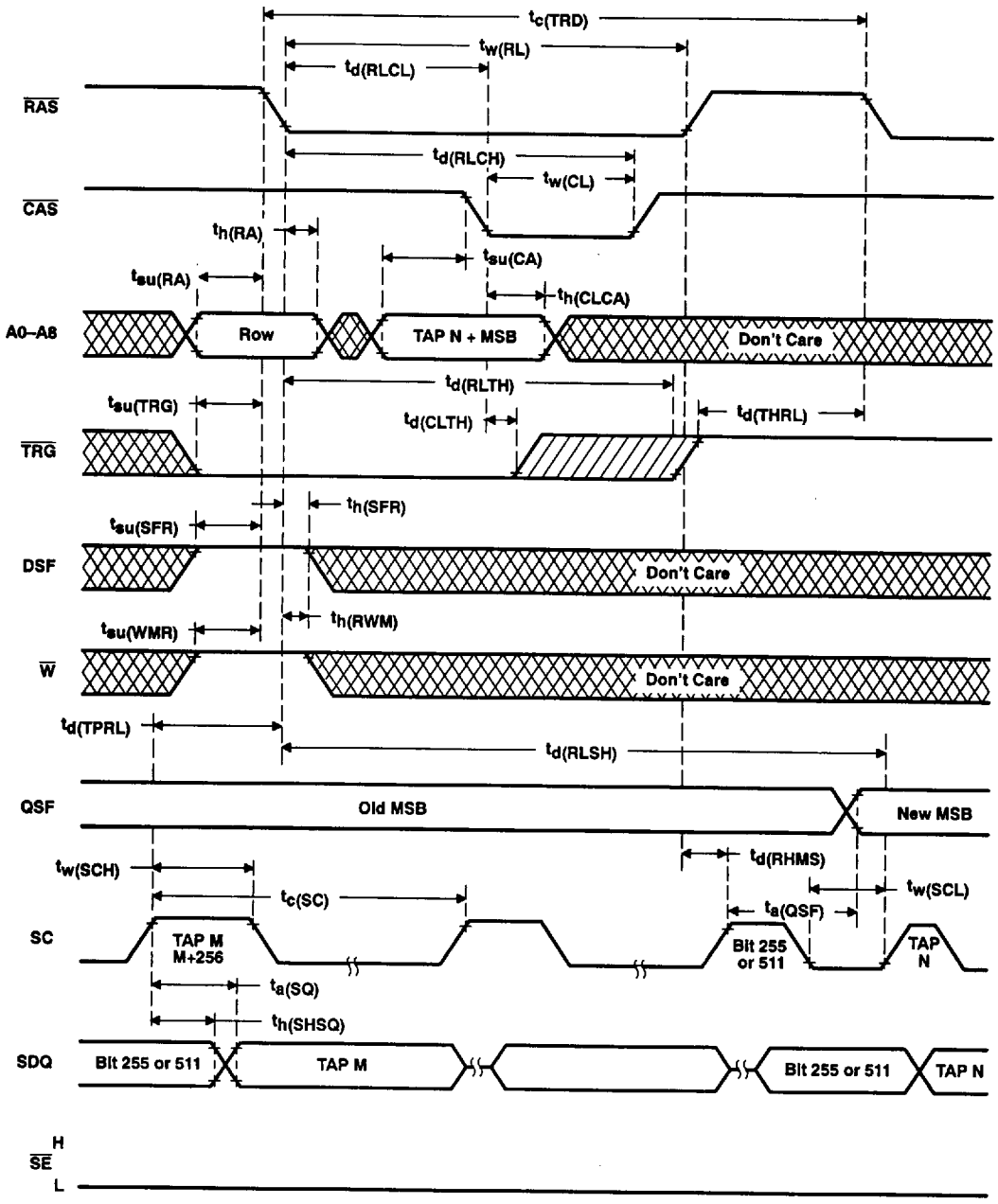


NOTES: A. Random mode (Q outputs) remain in the high-impedance state for the entire memory to data register transfer cycle. The memory to data register transfer cycle is used to load the data registers in parallel from the memory array. The 512 locations in each data register are written into from the 512 corresponding columns of the selected row. The data that is transferred into the data registers may be either shifted out or transferred back into another row.

B. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., the SQ is enabled), thus allowing data to be shifted out of the registers. Also, the first bit to be read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

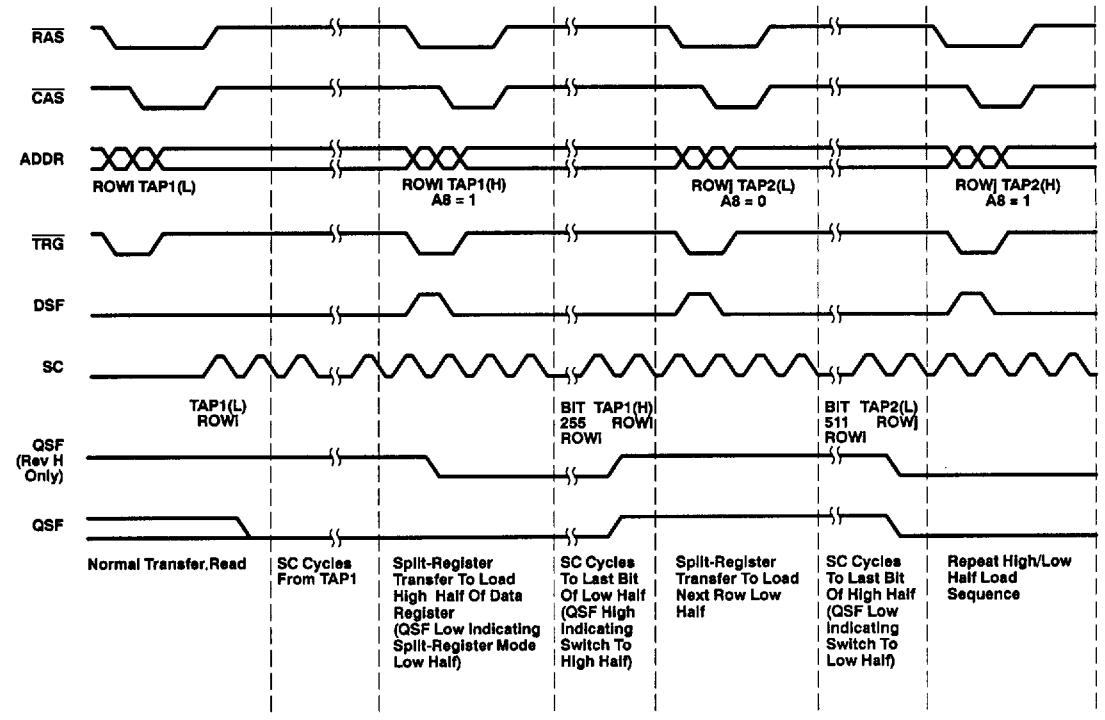
Figure 18. Memory to Data Register Transfer Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: There must be a minimum of two SC clocks cycle between any two split-register reload cycles, and a minimum of one SC clock cycle between a transfer read cycle and a split-register cycle.

Figure 19. Split-Register Mode Read Transfer Timing



NOTES: A. In the split-register mode, data can be transferred from different rows to the low and high halves of the data register.
B. When enabling or disabling the split-register mode, $t_{a(QSF)}$ is measured from $\overline{RAS}$ low in the transfer cycle.

Figure 20. Split-Register Operating Sequence

application notes

1. In order to achieve proper split-register operation, a normal read transfer followed by a minimum of one serial clock cycle should be performed before the first split-register transfer cycle. This is necessary to initialize the data register and the starting tap location. Serial access can then begin after the normal transfer cycle.
2. A split-register transfer into the inactive half is not allowed until $t_{d(TPRL)}$ is met. $t_{d(TPRL)}$ is the minimum delay time between the rising edge of the serial clock (SC) of the previously loaded tap point and the falling edge of $\overline{RAS}$ of the split-register transfer cycle into the inactive half.
3. After $t_{d(TPRL)}$ is met, the split-register transfer into the inactive half must also satisfy the $t_{d(RHMS)}$ condition. $t_{d(RHMS)}$ is the minimum delay time between the rising edge of $\overline{RAS}$ of the split-register transfer cycle into the inactive half and the rising edge of the last serial clock (SC 255 or 511) of the active half.

PARAMETER MEASUREMENT INFORMATION

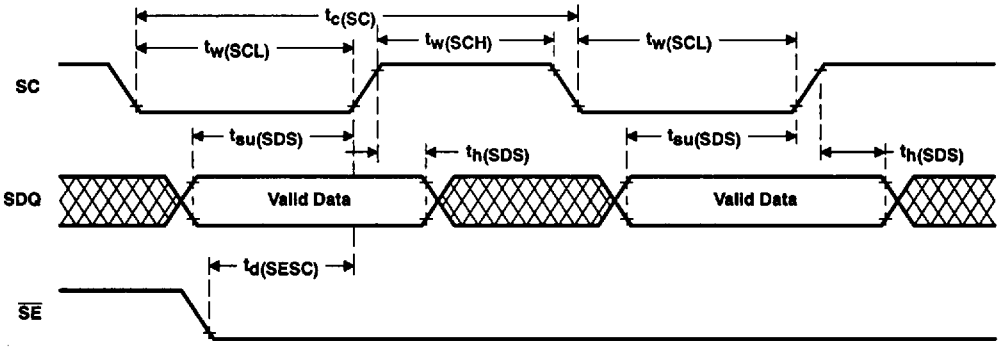
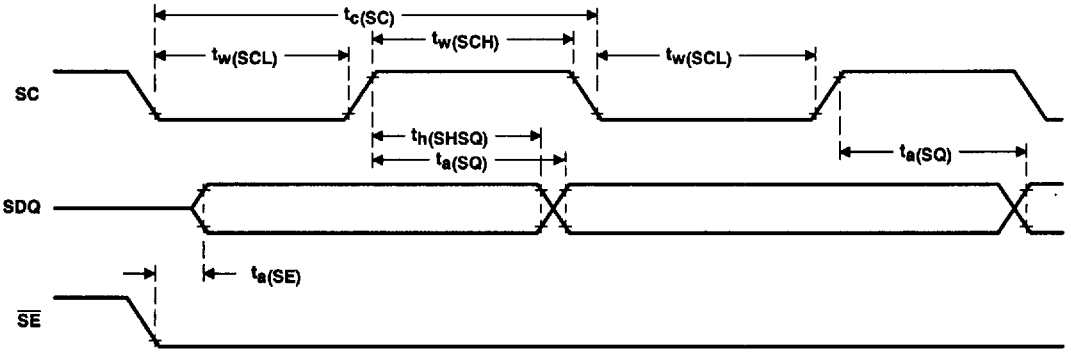


Figure 21. Serial Data-In Timing

The serial data-in cycle (SD) is used to input serial data into the data registers. Before data can be written into the data registers via SD, the device must be put into the write mode by performing a write mode control, or transfer write cycle. Transfer write cycles occurring between the write mode control cycle and the subsequent writing of data will not take the device out of the write mode. However, a transfer read cycle during that time will take the device out of the write mode and put it into the read mode, thus disabling the input of data. Data will be written starting at the location specified by the input address loaded on the previous transfer cycle.

While accessing data in the serial data registers, the state of $\overline{TRG}$ is a Don't Care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low to prevent data transfers between memory and data registers.



NOTE A: When the odd tap is used (tap addresses can be 0–511, and odd taps are 1,3,5 ... etc.), the cycle time for SC in the first serial data out cycle needs to be 70 ns minimum.

Figure 22. Serial Data-Out Timing

The serial data-out (SQ) cycle is used to read data out of the data registers. Before data can be read via SQ, the device must be put into the read mode by performing a transfer read cycle. Transfer write cycles occurring between the transfer read cycle and the subsequent shifting out of data will not take the device out of the read mode. But a write mode control cycle at that time will take the device out of the read mode and put it in the write mode, thus not allowing the reading of data.

While accessing data in the serial data registers, the state of $\overline{TRG}$ is a Don't Care as long as $\overline{TRG}$ is held high when $\overline{RAS}$ goes low to prevent data transfers between memory and data registers.