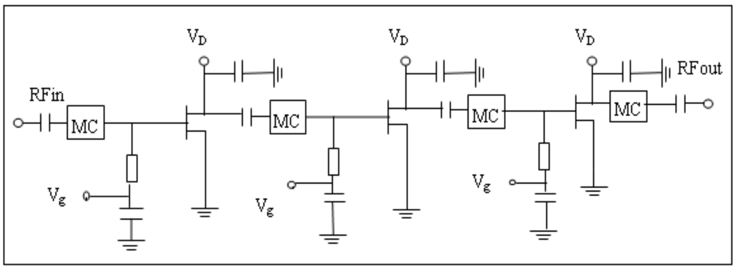
Function Diagram



Feature

- Frequency ：32GHz～38GHz
- Power Gain：18dB
- Psat：33dBm
- PAE：20%
- +22V@0.35A(quiescent)
- Dimension ：3.20mm×1.30mm×0.10mm

DC Electrical Specification（T_A = +25℃）

Parameter	Min	Typical	Max	Unit
Vd	-1.2	-1.5	-1.8	V
Vg	18	22	24	V
Id	0.30	0.35	0.38	A
Idd		0.40	0.45	A
Ig		0.01	0.02	mA
Igg		0.01	0.06	mA

Microwave Electrical Specification（T_A = +25℃，Vd = +22V，Vg = -1.5V）

Parameter	Min	Typical	Max	Unit
f	32～38			GHz
Psat	32	33		dBm
Gp	17	18		dB
∆Gp			±1	dB
PAE	18	20		%
Gain	21	23	25	dB
∆Gain			±2	dB
VSWR(in)		2.0	2.2	-

Note ：1）The mmic should be 100% DC and RF tested on chip.

2）Test Condition：Vd=+22V，Vg=-1.5V，P_{in}=15dBm，CW；

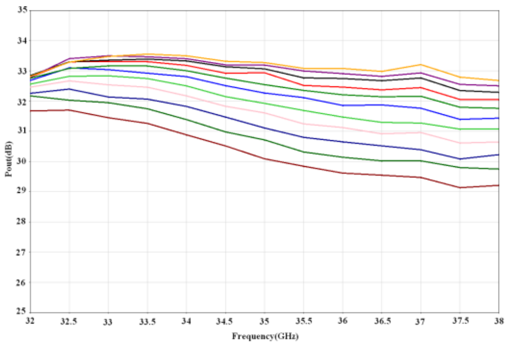
3）Thermal Values:1.2℃/W（test condition：pulse Width:100μs，duty cycle:10%，thermal dissipation18W，environment temperature 70℃）

Max Limited Values

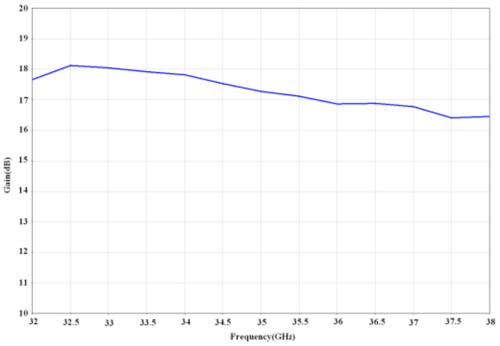
Parameter	Symbol	Values
Max Drain Voltage	Vd	+40V
Max Gate Voltage	Vg	-6V
Max Pin（CW）	P_p	+20dBm
Storage Temperature	T_{STG}	-65℃～+150℃
Max Operation Channel Temperature	T_{op}	+200℃
Load Impedance Mismatch (anti-burn)	Z_0	6：1

Typical Test Curves（Vd=+22V，Vg=-1.5V，CW）

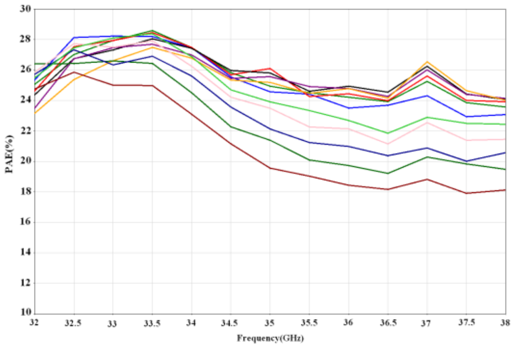
Pout vs. Pin（P_{in}=10dBm～20dBm）



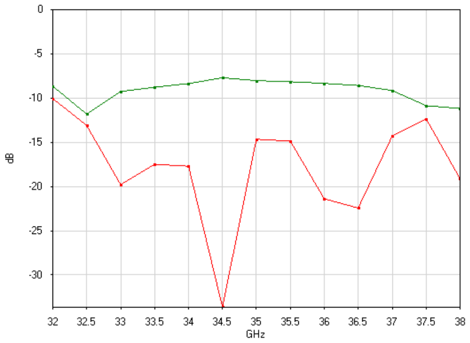
Power Gain vs. Frequency（P_{in}=11dBm）



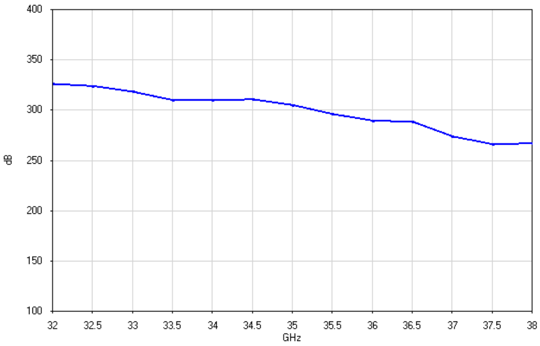
Efficiency vs. Pin（P_{in}=16dBm～30 dBm）



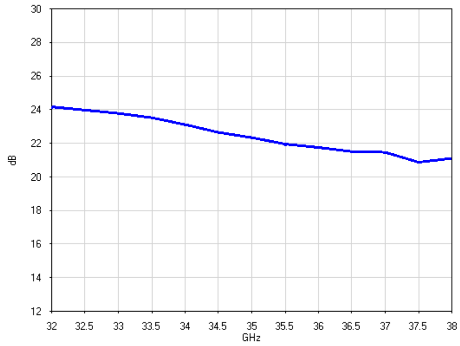
VSWRin/out vs. Frequency（P_{in}=-10dBm）



Dynamic Id vs. Frequency



Linary Gain vs. Frequency



Outline and Pad Definition

symbol	Values （mm）		
	Min	Nominal	Max
L	3.01	3.11	3.21
W	1.11	1.21	1.31

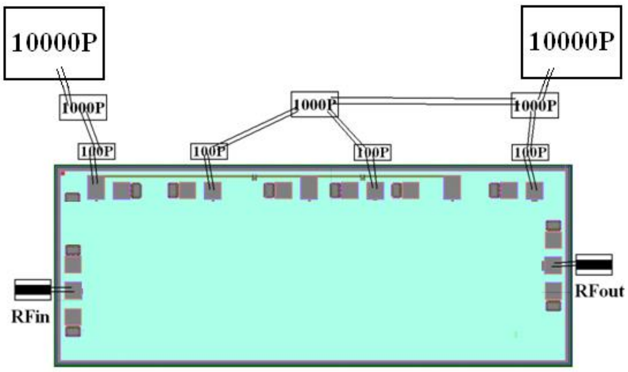
Table 1

PAD	Function	Dimension µm	Location	
			X µm	Y µm
1	Microwave Signal Pin	100×100	115	455
2	Microwave Signal Pout	100×100	3000	605
3	Three-level drain bias bond pad	100×100	2880	1055
4	Three-level gate bias bond pad	100×140	2390	1075
5	Two-level drain bias bond pad	100×100	1930	1055
6	Two-level gate bias bond pad	100×140	1535	1075
7	One-level drain bias bond pad	100×100	955	1055
8	One-level gate bias bond pad	100×140	255	1075

Note 1: Figure 1 uses the lower left corner of the chip as the origin, and the horizontal direction is the chip input to output direction as the x-axis and the vertical direction as the y-axis.

Note 2: The coordinate position of the bonding area in the table is based on the nominal value of the chip size, and the coordinates of the bonding area are the coordinates of the center point of the bonding area.

Assembly Diagram



Note: 1) The capacitance value of the external capacitor is C1=100pF, C2=1000pF. It is recommended to use a single-layer ceramic capacitor. C1 should be as close as possible to the chip and should not exceed 750µm.

2) Ku-band and below power circuit microstrip lines can use 200µm ~ 300µm thick ceramic sintered on the carrier to simplify the assembly process. Ku-band and above 125µm ~ 250µm low-loss low-dielectric material microstrip lines are bonded/sintered on the carrier to reduce the transmission loss, and the input/output bond wire length is controlled within 350µm±150µm.

Attention

1) The monolithic circuit needs to be stored in a dry and clean N2 environment;

2) The chip substrate material 6H-SiC is very brittle and must be used carefully so as not to damage the chip;

3) There is no insulating protective layer on the surface of the chip. Please pay attention to the cleanliness of the assembly environment to avoid excessive contamination of the surface.

4) The thermal expansion coefficient of the carrier should be close to that of 6H-SiC, and the coefficient of thermal expansion of the wire is 4.2×10-6/℃. CuMoCu or CuMo or CuW is the recommended carrier material.

5) Please avoid voids between the chip and the carrier during assembly and ensure good heat dissipation of the case and the carrier.

6) It is recommended to use gold-tin solder for sintering, Au:Sn=80%:20%, sintering temperature does not exceed 300℃, and the time is not longer than 30 seconds. The sintering process avoids rapid temperature changes and requires gradual temperature rise and fall;

7) It is recommended to use 25µm to 30µm diameter gold wire, the bonding table chassis temperature does not exceed 250 ℃, the bonding time is as short as possible, the bonding process to avoid rapid temperature changes;

8) When the power is applied, first increase the gate pressure and then add the leakage pressure. When the power goes off, drop the pressure before lowering the gate voltage;

9) The input and output of the chip has a blocking capacitor, but the input has a short circuit to DC;

10) Please pay attention to anti-static electricity during the use and assembly of the chip, wear a grounded anti-static bracelet, and ground the bonding and bonding station well;

11) Available QF087 type cermet package products;

12) Please contact the supplier if you have any problems.