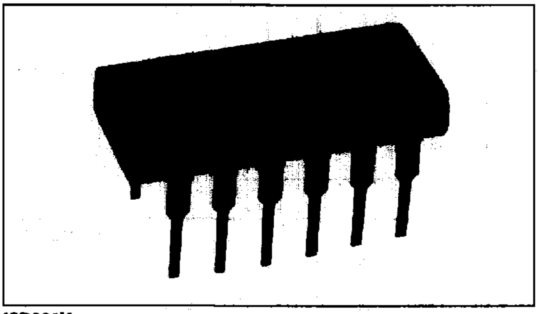
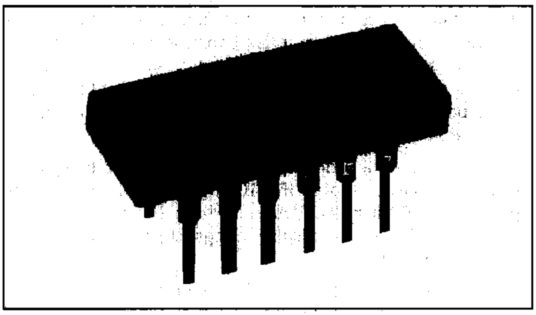
SIEMENS

RED ISD2010/2310
YELLOW ISD2011/2311/2351
HIGH EFFICIENCY RED ISD2012/2312/2352
HIGH EFFICIENCY GREEN ISD2013/2313/2353

4-Character 5x7 Dot Matrix
Serial Input Alphanumeric Industrial Display
Sunlight Viewable: ISD235X



ISD201X



ISD231X/235X

FEATURES

- **Four Dot Matrix Characters**
- **Character Height**
  ISD201X—0.150"
  ISD231X/235X—0.200"
- **ISD201X/231X, Four Colors: Red, Yellow, High Efficiency Red, High Efficiency Green**
- **ISD235X, Three Colors: Yellow, High Efficiency Red, High Efficiency Green**
- **Wide Viewing Angle**
- **Built-in CMOS Shift Registers with Constant Current LED Row Drivers**
- **Shift Registers Allow Custom Fonts**
- **Easily Cascaded for Multiple Displays**
- **TTL Compatible**
- **End Stackable**
- **Operating Temperature Range: –55°C to +100°C**
- **Categorized for Luminous Intensity**
- **Ceramic Package, Hermetically Sealed Flat Glass Window**

DESCRIPTION

The ISD201X/231X/235X are four digit 5x7 dot matrix serial input alphanumeric displays. The displays are available in red, yellow, high efficiency red, or high efficiency green. The package is a standard twelve-pin hermetic DIP with glass lens. The display can be stacked horizontally or vertically to form messages of any length.

These displays have two fourteen-bit CMOS shift registers with built-in row drivers. These shift registers drive twenty-eight rows and enable the design of customized fonts. Cascading multiple displays is possible because of the Data In and Data Out pins. Data In and Out are easily input with the clock signal and displayed in parallel on the row drivers. Data Out represents the output of the 7th bit of digit number four shift register. The shift register is level triggered. The like columns of each character in a display cluster are tied to a single pin (see Block Diagram). High true data in the shift register enables the output current mirror driver stage associated with each row of LEDs in the 5x7 diode array.

The TTL compatible V_B input may either be tied to V_{CC} for maximum display intensity or pulse width modulated to achieve intensity control and reduce power consumption.

DESCRIPTION (continued)

In the normal mode of operation, input data for digit four, column one is loaded into the seven on-board shift register locations one through seven. Column one data for digits 3, 2, and 1 is shifted into the display shift register locations. Then column one input is enabled for an appropriate period of time, T. A similar process is repeated for columns 2, 3, 4, and 5. If the decode time and load data time into the shift register is t, then with five columns, each column of the display is operating at a duty factor of:

$$DF = \frac{T}{5(T+t)}$$

T+t, allotted to each display column, is generally chosen to provide the maximum duty factor consistent with the minimum refresh rate necessary to achieve a flicker free display. For most strobed display systems, each column of the display should be refreshed (turned on) at a minimum rate of 100 times per second.

With columns to be addressed, this refresh rate then gives a value for the time T+t of: 1/[5x(100)]=2 msec. If the device is operated at 5.0 MHz clock rate maximum, it is possible to maintain t<<T. For short display strings, the duty factor will then approach 20%.

See Appnote 44 for application information and Appnotes 18, 19, 22, 23 for additional information.

Maximum Ratings

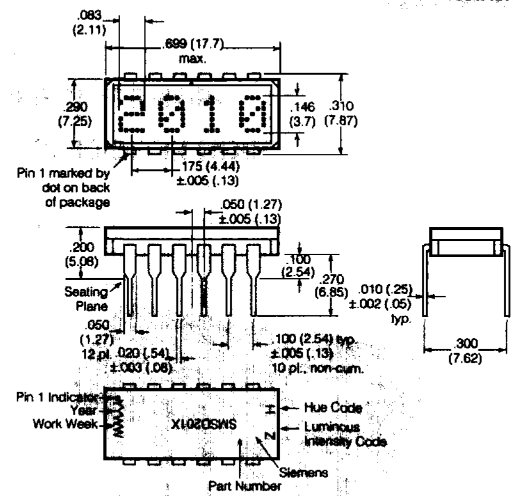
Supply Voltage V_{CC} to GND .... –0.5 V to +7.0 V
Inputs, Data Out and V_B .... –0.5 V to V_{CC} +0.5 V
Column Input Voltage, V_{COL} .... –0.5 V to +6.0 V
Operating Temperature Range .... –55°C to +100°C
Storage Temperature Range .... –65°C to +125°C
Maximum Solder Temperature, 0.063" (1.59 mm)
below Seating Plane, t<5 sec .... 260°C
Maximum Allowable Power Dissipation, T_A=25°C [2]
ISD2010 .... 0.91 W
ISD2011/2/3 .... 0.86 W
ISD231X .... 1.1 W
ISD235X .... 1.35 W

Notes:

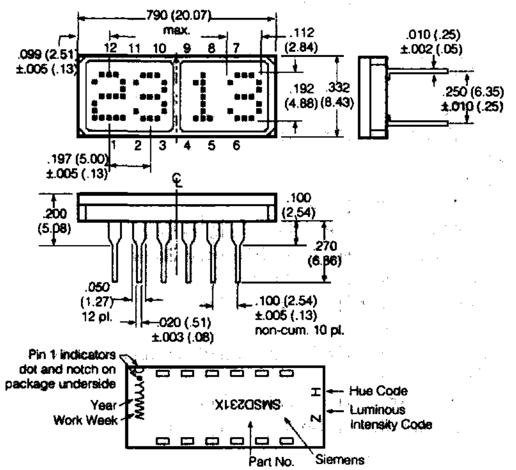
1) Operation above +100 °C ambient is possible if the following conditions are met. The junction should not exceed T_J=125 °C and the case temperature (as measured at pin 1 or the back of the display) should not exceed TC=100 °C.

2) Maximum allowable dissipation is derived from V_{CC}=5.25 V, V_B=2.4 V, V_{COL}=3.5 V 20 LEDs on per character, 20% DF.

Dimensions in Inches (mm) **ISD210X**

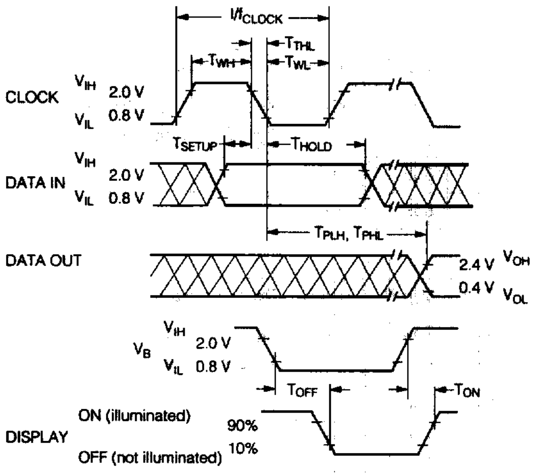


ISD231X/235X



Pin	Function	Pin	Function
1	Column 1	7	Data Out
2	Column 2	8	V_B
3	Column 3	9	V_{CC}
4	Column 4	10	Clock
5	Column 5	11	Ground
6	No connection	12	Data In

Figure 6. Timing characteristics



AC electrical characteristics

(V_{CC}=4.75 to 5.25 V, T_A=–55°C to 100°C)

Symbol	Description	Min.	Typ.	Max.[1]	Units	Fig.
T_{SETUP}	Setup Time	50	10		ns	1
T_{HOLD}	Hold Time	25	20		ns	1
T_{WL}	Clock Width Low	75	45		ns	1
T_{WH}	Clock Width High	75	45		ns	1
$F_{(CLK)}$	Clock Frequency			5	MHz	1
T_{THL} T_{TLH}	Clock Transition Time		75	200	ns	1
T_{PHL} T_{PLH}	Propagation Delay Clock to Data Out		50	125	ns	1

Notes:

1) All typical values specified at V_{CC}=5.0 V and T_A=25 °C unless otherwise noted.

2) V_B Pulse Width Frequency—50 KHz (max.)

Figure 7. Maximum allowable power dissipation vs. temperature, ISD201X

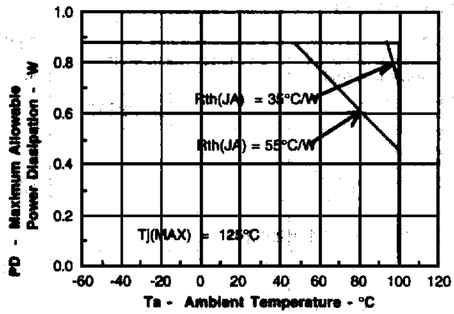


Figure 8. Maximum allowable power dissipation vs. temperature, ISD231X

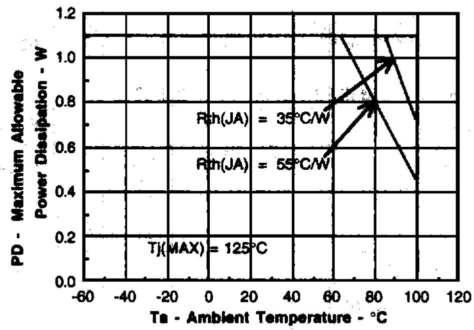
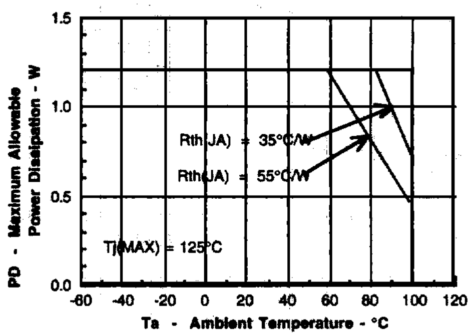


Figure 9. Maximum allowable power dissipation vs. temperature, ISD235X



Optical Characteristics

Red ISD2010, ISD2310

Description		Symbol	Min.	Typ.[4]	Units	Test Conditions
Peak Luminous Intensity per LED [1,3] (Character Average)	ISD2010	I_{VPEAK}	105	200	µcd	V_{CC}=5.0 V, V_{COL}=3.5 V T_J=25°C[5], V_B=2.4 V
	ISD2310		220	370		
Peak Wavelength		λ_{VPEAK}		655	nm	
Dominant Wavelength[2]		λ_D		639	nm	

Yellow ISD2011, IDS2311, ISD2351

Description		Symbol	Min.	Typ.[4]	Units	Test Conditions
Peak Luminous Intensity per LED [1,3] (Character Average)	ISD2011	I_{VPEAK}	400	750	µcd	V_{CC}=5.0 V, V_{COL}=3.5 V T_J=25°C[5], V_B=2.4 V
	ISD2311		650	1140		
	ISD2351		2400	3400		
Peak Wavelength		λ_{VPEAK}		655	nm	
Dominant Wavelength[2]		λ_D		639	nm	

High Efficiency Red IDS2012, ISD2312, IDS2352

Description		Symbol	Min.	Typ.[4]	Units	Test Conditions
Peak Luminous Intensity per LED [1,3] (Character Average)	ISD2012	I_{VPEAK}	400	1430	µcd	V_{CC}=5.0 V, V_{COL}=3.5 V T_J=25°C[5], V_B=2.4 V
	ISD2312		650	1430		
	ISD2352		853	2500		
Peak Wavelength		λ_{VPEAK}		655	nm	
Dominant Wavelength[2]		λ_D		639	nm	

High Efficiency Green IDS2013, ISD2313, IDS2353

Description		Symbol	Min.	Typ.[4]	Units	Test Conditions
Peak Luminous Intensity per LED [1,3] (Character Average)	ISD2013	I_{VPEAK}	850	1550	µcd	V_{CC}=5.0 V, V_{COL}=3.5 V T_J=25°C[5], V_B=2.4 V
	ISD2313		1280	2410		
	ISD2353		2400	3000		
Peak Wavelength		λ_{VPEAK}		655	nm	
Dominant Wavelength[2]		λ_D		639	nm	

Notes:

1) The displays are categorized for luminous intensity with the intensity category designated by a letter code on the bottom of the package.

2) Dominant wavelength (λ_D) is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

3) The luminous sterance of the LED may be calculated using the following relationships:
L_V (cd/m^2) = I_V (Candela)/A (Meter)^2
L_V (Footlamberts) = πI_V (Candela)/A (Foot)^2
A=5.3x10^{-8} m^2 = 5.8x10^{-7} (Foot)^2

4) All typical values specified at V_{CC}=5.0 V and T_A=25 °C unless otherwise noted.

5) The luminous intensity is measured at T_A=T_J=25 °C. No time is allowed for the device to warm up prior to measurement.

Recommended operating conditions
(Guaranteed over operating temperature range)

Parameter	Symbol	Min.	Nom.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Data Out Current, Low State	I_{OL}				mA
Data Out Current, High State	I_{OH}				mA
Column Input Voltage, Column On [1]	V_{COL}	2.75		3.5	V
Setup Time	T_{SETUP}	70	45		ns
Hold Time	T_{HOLD}	30			ns
Width of Clock	$T_{W(CLK)}$	75			ns
Clock Frequency	T_{CLK}			5	MHz
Clock Transition Time	T_{THL}			200	ns
Free Air Operating Temperature Range	T_A	–55		+100	°C

Note:
1) See Figures 5, 6 and 7: Peak column current versus column voltage

Figure 10. Peak column current vs. column voltage, ISD201X

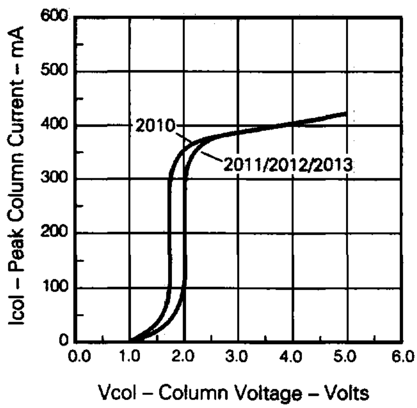


Figure 12. Peak column current vs. column voltage, ISD235X

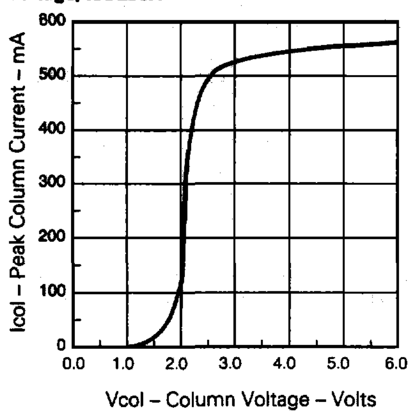
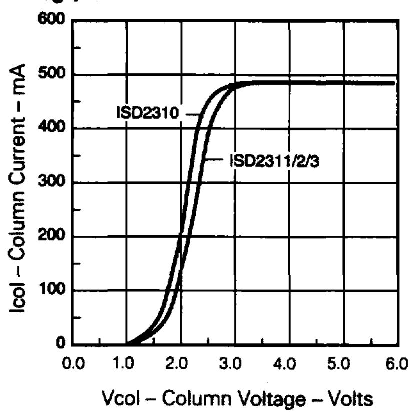


Figure 11. Peak column current vs. column voltage, ISD231X



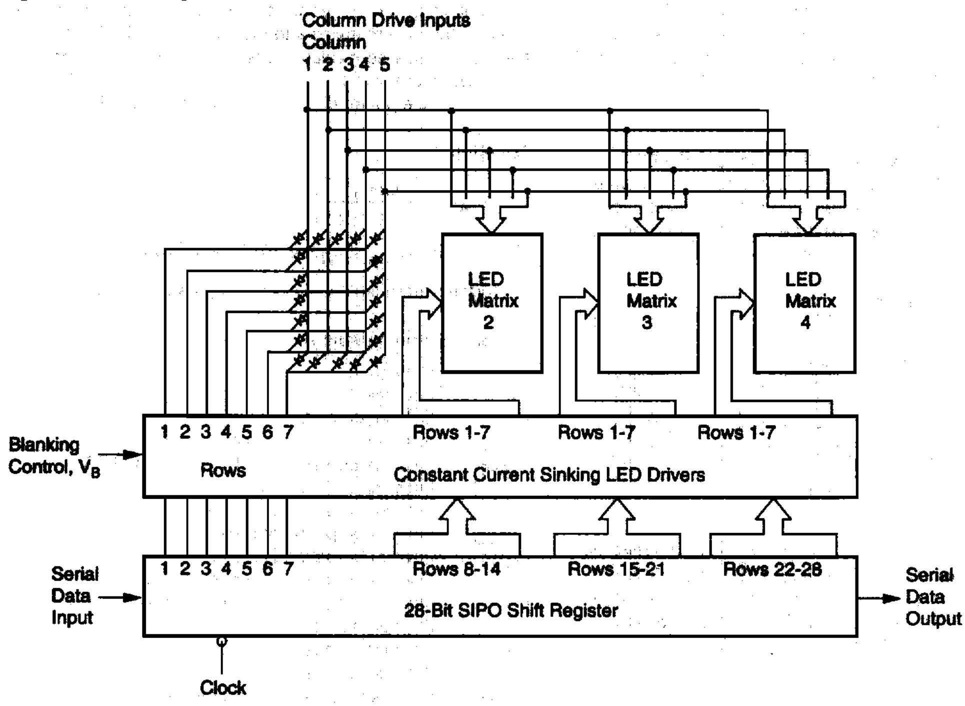
Electrical characteristics (–55°C to +100°C, unless otherwise specified)

Description	Symbol	Min.	Typ.[1]	Max.	Units	Test Conditions	
Supply Current (quiescent)	I_{CC}			5.0	mA	V_B=0.4 V	V_{CC}=5.25 V V_{CLK}=V_{DATA}=2.4 V All SR Stages=Logical 1
				5.0		V_B=2.4 V	
Supply Current (operating)	I_{CC}			10	mA	F_{CLK}=5 MHz	
Column Current at Any Column Input[2]	I_{COL}			10	µA	V_B=0.4 V	V_{CC}=5.25 V V_{COL}=3.5 V All SR Stages=Logical 1
Column Current at Any Column Input[2] ISD2010 red ISD2011/2/3: yellow, HER, green ISD231X: red, yellow, HER, green ISD235X: yellow, HER, green	I_{COL}		 350 335 380 550	 435 410 520 650	mA		
V_B, Clock or Data Input Threshold Low	V_{IL}			0.8	V	V_{CC}=4.75 V–5.25 V	
V_B, Clock or Data Input Threshold High	V_{IH}	2.0			V		
Data Out Voltage	V_{OH}	2.4	3.6		V	I_{OH}=0.5 mA	V_{CC}=5.25 V I_{COL}=0 mA
	V_{OL}					I_{OL}=1.6 mA	
Input Current Logical 0, V_B only	I_{IL}	–30	–110	–300	µA	V_{CC}=4.75 V–5.25 V, V_{IL}=0.8 V	
Input Current Logical 0, Data, Clock	I_{IL}						
Power Dissipation per Package ISD201X ISD231X ISD235X	PD	 0.44 0.52 0.74			W	V_{CC}=5.0 V, V_{COL}=3.5 V, 17.5% DF 15 LEDs on per character, V_B=2.4 V	
Thermal Resistance IC, Junction-to-Pin ISD201X ISD231X ISD235X	$R\theta_{J\text{-}PIN}$		 30 20 25		°C/W/ Device		

Notes:

1) All typical values specified at V_{CC}=5.0 V and T_A=25 °C unless otherwise noted.
2) See Figures 5, 6 and 7: Peak column current versus column voltage

Figure 13. Block diagram



Contrast enhancement filters for sunlight readability

Display Color	Filter Color	Marks Polarized Corp.*	Optical Characteristics of Filter
Red, HER	Red	MPC 20-15C	25% at 635 nm, Circular Polarizer
Yellow	Amber	MPC 30-25C	25% at 583 nm, Circular Polarizer
Green	Yellow/Green	MPC 50-122C	22% at 568 nm, Circular Polarizer
Multiple Colors High Ambient Light	Neutral Gray	MPC 80-10C	10% Neutral, Circular Polarizer
Multiple Colors	Neutral Gray	MPC 80-37C	37% Neutral, Circular Polarizer

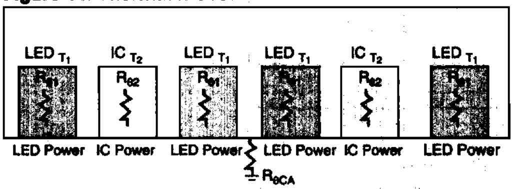
* Marks Polarized Corp.
25-B Jefryn Blvd. W.
Deer Park, NY 11729
516/242-1300
FAX 516/242-1347
Marks Polarized Corp. manufactures
to MIL-1-45208 inspection system.

The small alphanumeric displays are hybrid LED and CMOS assemblies that are designed for reliable operation in commercial and industrial environments. Optimum reliability and optical performance will result when the junction temperature of the LEDs and CMOS ICs are kept as low as possible.

Thermal Modeling

ISD displays consist of two driver ICs and four 5x7 LED matrixes. A thermal model of the display is shown in Figure 9. It illustrates that the junction temperature of the semiconductor = junction self heating + the case temperature rise + the ambient temperature. Equation 1 shows this relationship.

Figure 14. Thermal model



See Equation 1 below.

The junction rise within the LED is the product of the thermal impedance of an individual LED (37°C/W, DF=20%, F=200 Hz), times the forward voltage, $V_{F(LED)}$, and forward current I_F(LED), of 13 – 14.5 mA. This rise averages $T_{J(LED)}$=1°C. The Table below shows the $V_{F(LED)}$ for the respective displays.

Model Number	VF		
	Min.	**Typ.**	**Max.**
ISD2010 ISD2310	1.6	1.7	2.0
ISD2011/2/3 ISD2311/2/3 ISD2351/2/3	1.9	2.2	3.0

The junction rise within the LED driver IC is the combination of the power dissipated by the IC quiescent current and the 28 row driver current sinks. The IC junction rise is given in Equation 2.

A thermal resistance of 28°C/W results in a typical junction rise of 6°C.

See Equation 2 below.

For ease of calculations the maximum allowable electrical operating condition is dependent upon the aggregate thermal resistance of the LED matrixes and the two driver ICs. All of the thermal management calculations are based upon the parallel combination of these two networks which is 15°C/W. Maximum allowable power dissipation is given in Equation 3.

Equation 3.

$$P_{DISPLAY} = \frac{T_{J(MAX)} - T_A}{R_{\theta JC} + R_{\theta CA}}$$

$$P_{DISPLAY} = 5V_{COL}\, I_{COL}\,(n/35)\,DF + V_{CC}\, I_{CC}$$

For further reference see Figures 2, 3, 4 and 11 – 23.

Key to equation symbols

DF	Duty factor
I_{CC}	Quiescent IC current
I_{COL}	Column current
n	Number of LEDs on in a 5x7 array
P_{CASE}	Package power dissipation excluding LED under consideration
P_{COL}	Power dissipation of a column
$P_{DISPLAY}$	Power dissipation of the display
P_{LED}	Power dissipation of a LED
$R_{\theta CA}$	Thermal resistance case to ambient
$R_{\theta JC}$	Thermal resistance junction to case
T_A	Ambient temperature
$T_{J(IC)}$	Junction temperature of an IC
$T_{J(LED)}$	Junction temperature of a LED
$T_{J(MAX)}$	Maximum junction temperature
V_{CC}	IC voltage
V_{COL}	Column voltage
$V_{F(LED)}$	Forward voltage of LED
$Z_{\theta JC}$	Thermal impedance junction to case

Optical Considerations

The light output of the LEDs is inversely related to the LED diode's junction temperature as shown in Figure 10. For optimum light output, keep the thermal resistance of the socket or PC board as low as possible.

Equation 1.

$$T_{J(LED)} = P_{LED}\, Z_{\theta JC} + P_{CASE}\,(R_{\theta JC} + R_{\theta CA}) + T_A$$

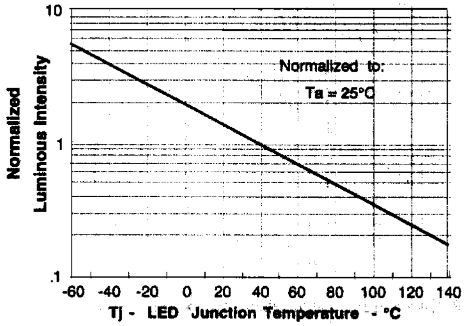
$$T_{J(LED)} = [(I_{COL}/28)\, V_{F(LED)}\, Z_{\theta JC}] + [(n/35)\, I_{COL}\, DF(5V_{COL}) + V_{CC}\, I_{CC}] \cdot [R_{\theta JC} + R_{\theta CA}] + T_A$$

Equation 2.

$$T_{J(IC)} = P_{COL}(R_{\theta JC} + R_{\theta CA}) + T_A$$

$$T_{J(IC)} = [5(V_{COL} - V_{F(LED)}) \cdot (I_{COL}/2) \cdot (n/35)DF + V_{CC} \cdot I_{CC}] \cdot [R_{\theta JC} + R_{\theta CA}] + T_A$$

Figure 15. Normalized luminous intensity vs. junction temperature



When mounted in a 10°C/W socket and operated at Absolute Maximum Electrical conditions, the display will show an LED junction rise of 17°C. If T_A=40°C, then the LED's T_J will be 57°C. Under these conditions Figure 11 shows that the IV will be 75% of its 25°C value.

Figure 16. Max. LED junction temperature vs. socket thermal resistance

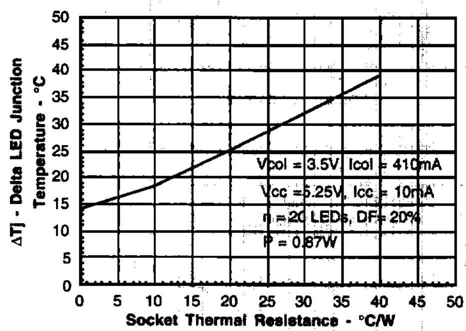


Figure 17. Max. package power dissipation, ISD201X

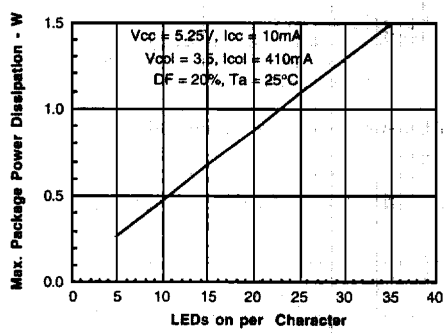


Figure 18. Max. package power dissipation, ISD231X

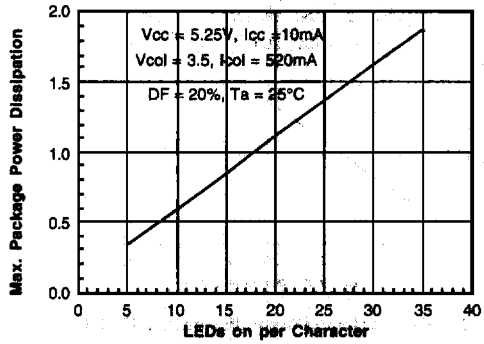


Figure 19. Max. package power dissipation, ISD235X

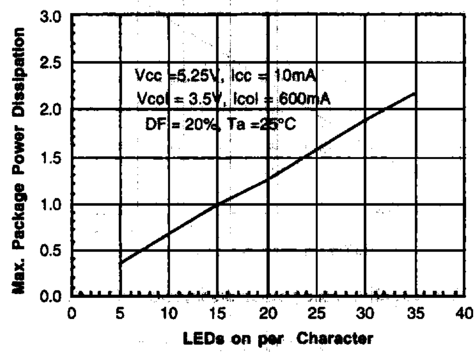


Figure 20. Package power dissipation, ISD201X

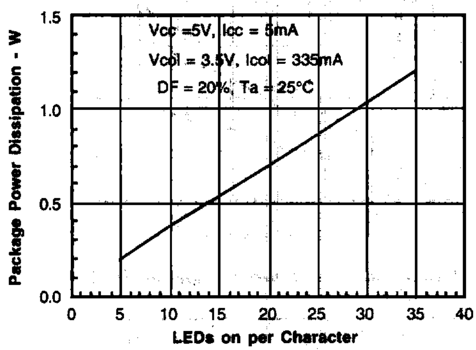


Figure 21. Max. package power dissipation, ISD231X

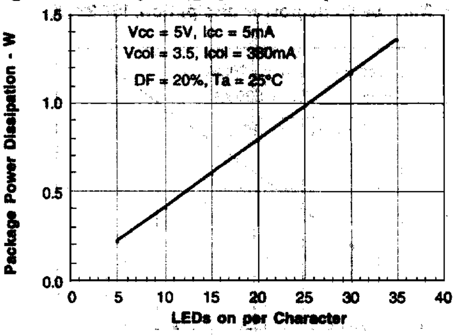


Figure 22. Max. package power dissipation, ISD235X

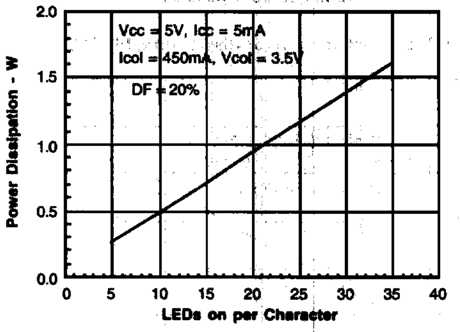


Figure 23. Max. character power dissipation, ISD201X

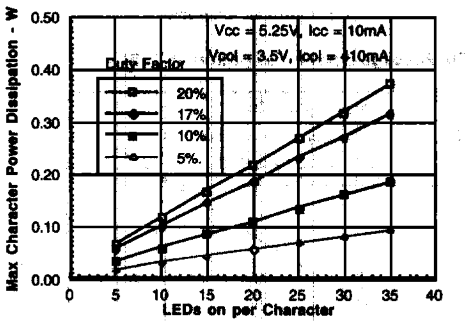


Figure 24. Max. character power dissipation, ISD231X

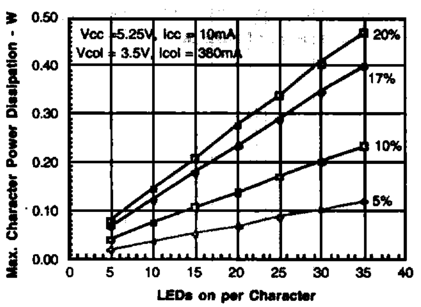


Figure 25. Max. character power dissipation, ISD235X

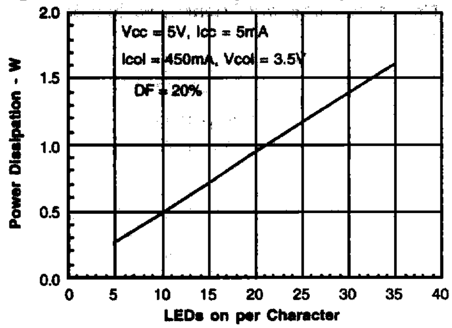


Figure 26. Character power dissipation, ISD201X

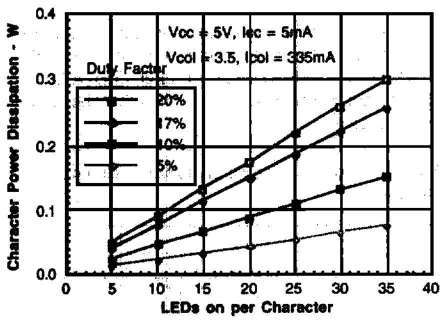


Figure 27. Character power dissipation, ISD231X

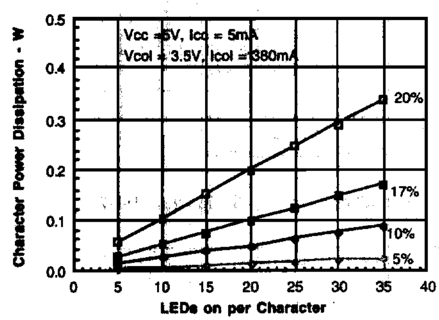


Figure 28. Character power dissipation, ISD235X