PIONEER
SEMICONDUCTOR CORPORATION

PI4C4301

High Performance Single Chip Ethernet Controller

Product Features:

- Compatible with IEEE 802.3 specification
- Interface with 16-bit ISA bus or 8-bit ISA bus
- Buffer ring memory management
- Supports physical, multicast and broadcast address filtering
- On-chip EEPROM interface logic for switchless NIC
- 3 levels of loopback test
- ISA bus interface logic integrated on-chip
- Supports both NE1000 and NE2000 operations
- 128-pin PQFP package

1.0 GENERAL DESCRIPTION

The PI4C4301 is a high performance single chip Ethernet controller with all the ISA bus interface logic integrated on chip. It is designed specially for the implementation of a switchless and jumperless Ethernet Network Interface Controller (NIC). It contains proprietary protocol circuits that handle the functions of IEEE 802.3 standard and host interface. The PI4C4301 can interface directly to AMD's Am7992 SIA, NS's DP82910 SNI, AT&T's T7213 DISC, and Level 1's 901.

A system diagram that demonstrates the application of the Pioneer Semiconductor's Ethernet Controller is shown in Figure 1.

2.0 FUNCTIONAL DESCRIPTION

The Pioneer Semiconductor's PI4C4301 Ethernet Controller consists of several major logic blocks. The cores of which is the protocol engine that implements all of the transmit and receive logic as specified in the IEEE 802.3 MAC protocol. To enable transparent interface to the ISA bus it has integrated the bus interface logic on chip. User stores station ID and configuration data in the EEPROM. The PI4C4301 also has all of the EEPROM programming logic built-in to make switchless and jumperless NIC painless. A detail block diagram is shown in Figure 2.

Transmit and Receive Frame Structure

Table 1 shows the fields of a frame: the preamble, Start Frame Delimiter (SFD), the addresses of the frame's source and destination, a length field to indicate the length of the LLC (Logical Link Control) data to be transmitted and the frame check sequence field (FCS).

Table 1. Fields of a Frame

Preamble	7 bytes
SFD	1 bytes
Destination Address	6 bytes
Source Address	6 bytes
Length	2 bytes
LLC Data	
Frame Check Sequence	4 bytes

Preamble Field. The preamble field is a 7-bytes field. The PLS (Physical Signaling) circuitry uses this bit pattern to reach its steady-state synchronization with the received frame timing.

Start Frame Delimiter (SFD). The SFD field is the sequence 10101011. It immediately follows the preamble pattern and indicates the beginning of a frame.

Destination Address Field. The Destination Address field specifies the station or stations for which the frame is intended.

Source Address Field. The Source Address field specifies the station sending the frame. NIC does not interpret this field.

Length Field. The length field is a 2-byte field. It is not interpreted by the NIC.

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Data Field. The data field contains a sequence of up to 1518 bytes of data. The NIC will accept packet less than 64 bytes if NIC set the Accept Runts (AR) bit in the Receive Configuration Register.

Frame Check Sequence Field. The FCS is a 32-bit CRC (Cycle Redundancy Code). NIC calculates the CRC and appends it to a packet during transmission. The NIC checks this code during reception to detect errors. The CRC value is computed as a function of the contents of all the fields except preamble, SFD, and FCS. The CRC encoding is defined by the following generating polynomial.

$$G(X) = X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^{8} + X^{7} + X^{5} + X^{4} + X^{2} + X + 1$$

Figure 1. System Diagram

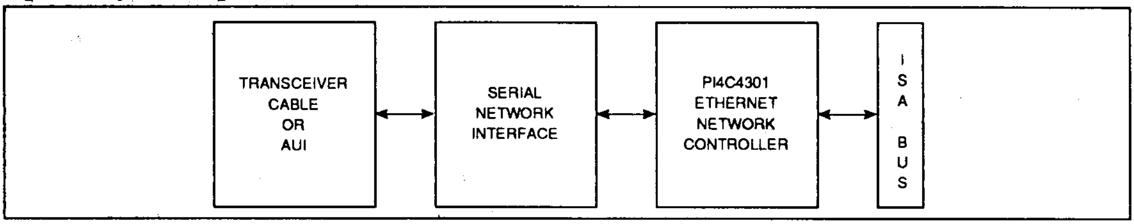
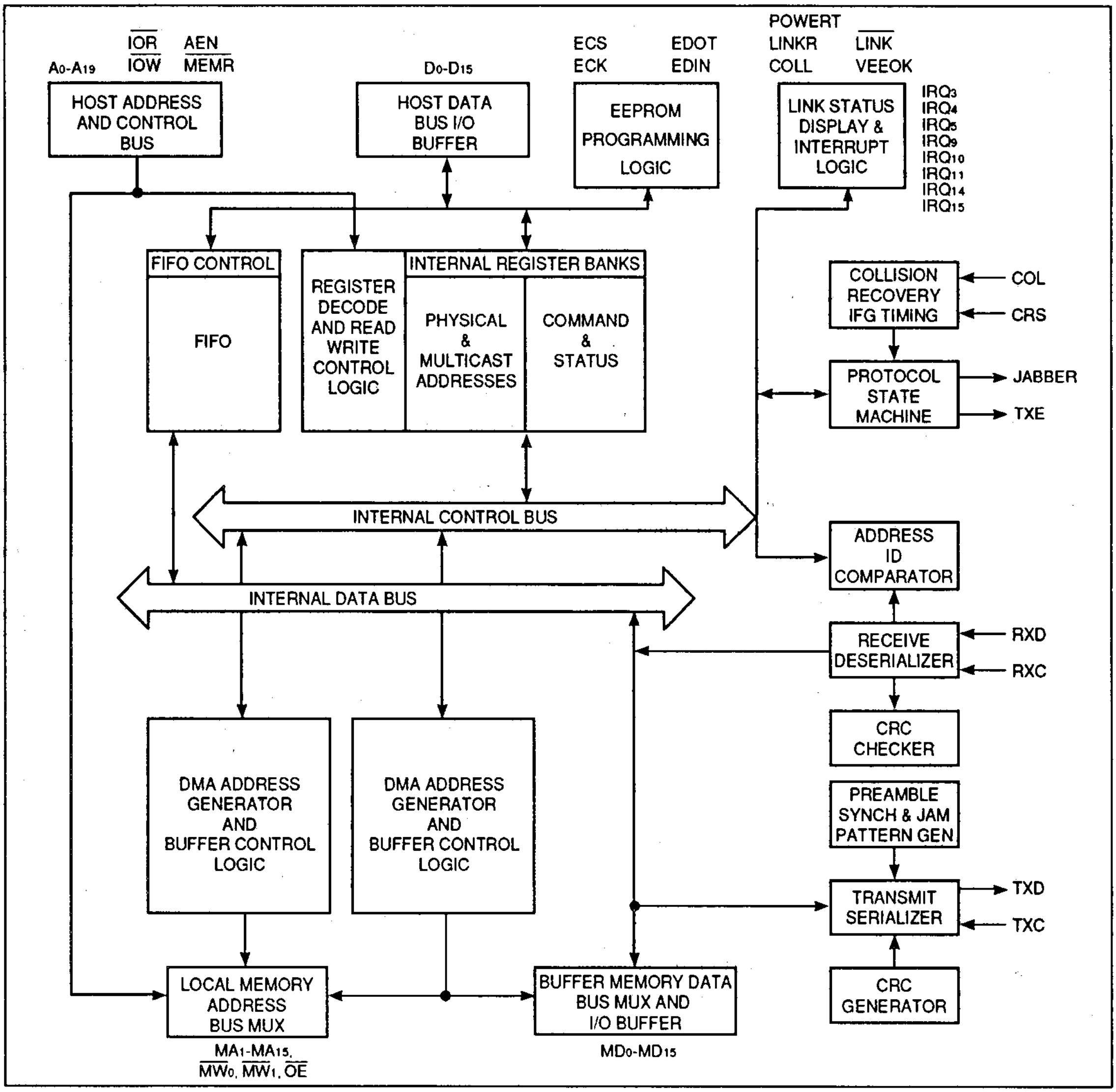


Figure 2. Block Diagram



Transmit Serializer

The transmit serializer fetches data from the RAM buffer and converts them into serial form. The NIC initiates a transmit operation after a 9.6 μsec line idle time period (interframe gap). RAM data is preceded by 62 bits of 1,0 preamble and a 1,1 synchronous pattern. After the last bit of the packet is sent, the 32-bit FCS field is shifted out of the CRC generator and appends to the transmit bit stream. When collision occurs, the preamble and synch generator would generate a 32-bit JAM pattern of all ones.

CRC Generator and Checker

Receive CRC checker generates a CRC field from the incoming packet. CRC computation includes address, data, and CRC fields of the packet. It does not include the preamble and the SFD. Local CRC is compared to incoming CRC during reception.

Transmit CRC circuit generates CRC serially and appends it to each outgoing packet. CRC is clocked out, most significant bit first, which is different from the address and data field.

Receive Deserializer

Receive deserializer is activated by the Carrier Sense signal. Incoming data (RXD) bit stream is clocked into a serial-to-parallel converter circuit lsb (least significant bit) first by the receive clock (RXC) while the receive CRC logic generates a CRC field. The CRC is compared serially with the incoming CRC. Both RXD and RXC come from an external Manchester decoder. When an octet is completely shifted into the receive serializer, parallel data is loaded into a receive register. Byte alignment is determined by a 'synch' circuit which detects the SFD.

Address ID Comparator

Destination address is compared to a 6-byte station address stored in the internal registers. If all bits match or if promiscuous mode is enabled, the packet is received. If the packet's destination is a group address, it will be received when group address reception is enabled.

The NIC filters multicast addresses using a standard hashing algorithm that maps all multicast addresses into a 6-bit value. The destination addresses are fed through the CRC generator and as the last bit of the destination address enters the generator, the six most significant bits in the generator are latched. These bits are decoded to index a unique filter bit (FB0-FB63) of multicast registers (MAR0-MAR7). If the Filter Bit Select is set, the multicast packet is accepted. Broadcast packets are received when the Broadcast enable bit is active.

If the address is rejected, the receive deserializer is cleared and the first four bytes are written into buffer memory. However, when Overwrite occurs, none of the packets will be stored in buffer memory. Buffering of the packet begins if the address is accepted.

Protocol State Machine

A sequential state machine is installed in the NIC to handle the transmission protocol. It controls transmit sequence, JAM pattern generation, interframe gap (line idle detection), pseudo-random generator, and backoff scheme when collision occurs.

DMA Address Generator, RAM Data Register, Address Bus Arbitrator and FIFO Logic

Instead of placing the FIFO circuit between line interface and buffer RAM, the NIC installs a FIFO between host interface and buffer RAM. When reception is in progress, the DMA requests RAM bus every 16 data bits (1.6 μsec). The cycle for RAM access is 200 nsec. During every cycle, the access right of the next 200 nsec is decided by the internal bus arbitration circuit.

RAM Data Register is the only 16-bit register in the NIC. Host reads buffer RAM data by reading this register. After the Remote Start Address Registers (RSAR0, RSAR1) and the Remote DMA command bits (RD0, RD1) are set, local DMA address generator is able to generate address and fetch the addressed data from RAM, fill them into FIFO until FIFO is full. DMA control circuit will fill FIFO with RAM data any time a word is fetched by host.

Similarly, the host stores data to RAM by writing them into RAM Data Register. Data are filled into FIFO and entered into RAM addressed by Current Remote DMA address (CRDA0 and CRDA1).

Address Decoder and Register Banks

Address lines are decoded in accordance with the contents of the EEPROM. A15 to A5 are used to select the chip while A4 to A0 are used to select NIC internal registers. A19 to A16 are ignored for host IO operations. Detail descriptions of the internal registers are covered in the later sections.

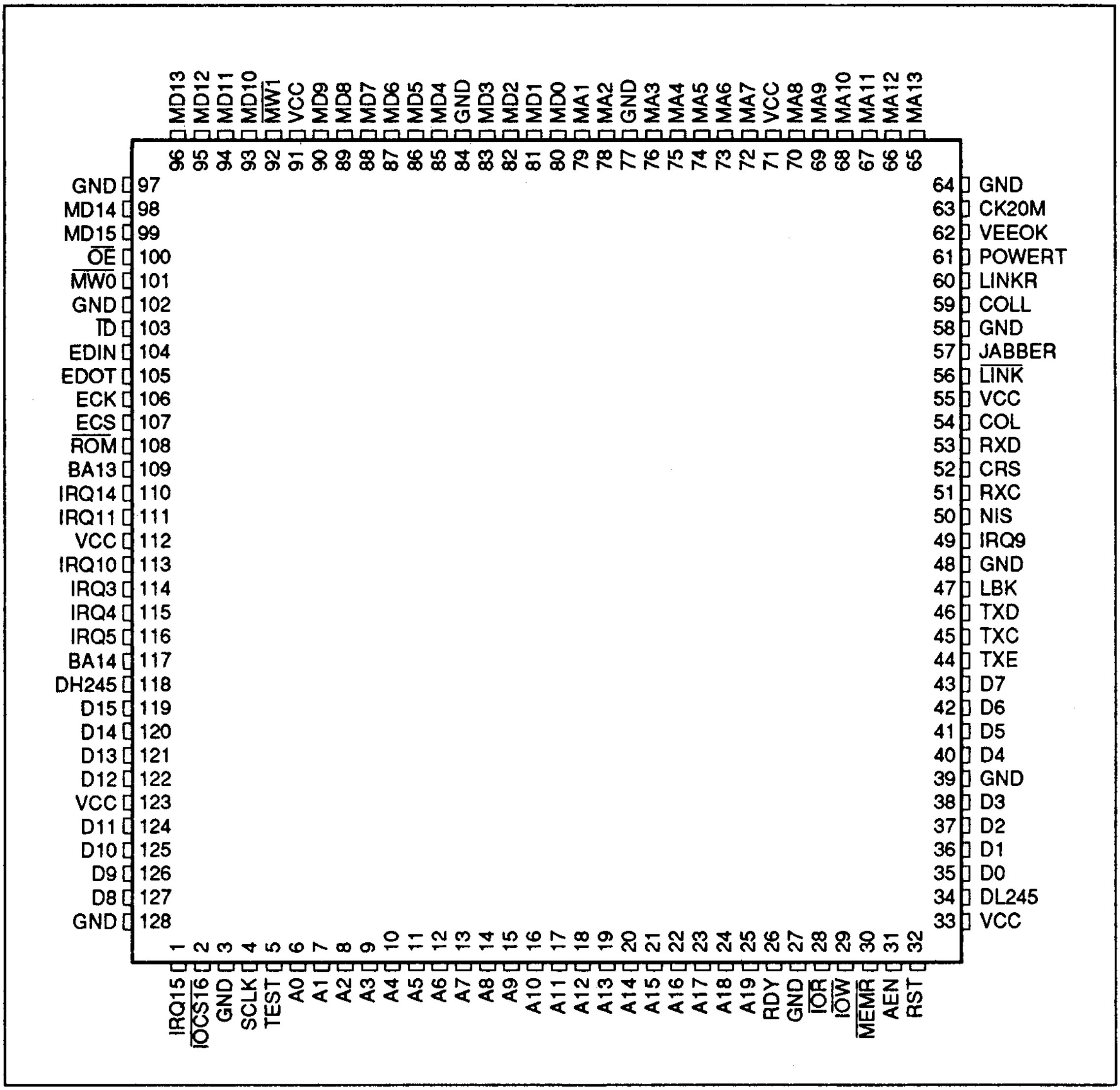
EEPROM Logic

The NIC interfaces to a 1024-bit EEPROM (NMC93C46 or equivalent). Data stored in EEPROM includes physical address ID, ROM base address, IO base address, and IRQ channel selection. Upon power on, all essential data stored in EEPROM will be shifted into the Configuration Registers. The host can access EEPROM through the IO port offset 1EH at any time. However, to change the contents of the Configuration Register with new EEPROM data, it is necessary to reset the NIC and down load the update data. Detail definition for the data in the EEPROM as well as programming procedure can be found in the appendix.

Line Status Display Drivers Functions

The NIC provides LED drivers to display line status. This is an essential function for twisted-pair serial interface diagnostic. Driver pins are connected to LEDs through a serial 470 ohm resistor to VCC. The description for the different LED indicators are detailed in the pin description section.

3.0 PIN CONNECTION DIAGRAM



4.0 PIN DESCRIPTIONS

Host Interface Pins

Symbol	Function	Description
A19-A0	I	Address 19 to 0: Should connect directly to the ISA bus address line slot. They are used to access the NIC's internal registers or to specify the BIOS ROM location.
AEN	I	Address Enable: Should connect directly to ISA bus AEN slot. AEN=1 indicates DMA bus cycles, AEN=0 indicates NIC internal registers or ROM access cycles.
D15-D0	I/O	Bi-directional Data bus, Data 15 to 0: Drives the ISA host data bus through TTL bus transceivers (74LS245) to meet the sinking and sourcing current requirements. Host accesses the NIC and BIOS ROM through these lines.
DL245, DH245	O	Data Bus Transceiver Direction Control: Used to control the external data bus transceiver directions. DL245 controls D7 to D0, DH245 controls D15 to D8. They become low when host is reading the NIC registers or accessing the ROM .
$\overline{IOW}$	I	IO write, active low signal: When it is asserted, it enables host to write to NIC internal registers.
$\overline{IOR}$	I	IO read, active low signal: When it is asserted, it enables host to read NIC's internal registers.
$\overline{MEMR}$	I	Memory Read, active low signal: Enable host to read ROM when active.
RDY	O	Ready: Three-state output, drive high to lengthen the current bus cycle when host is accessing RAM data registers, Command Register or Remote Start register.
IRQ3, IRQ4, IRQ5, IRQ9, IRQ10, IRQ11 IRQ14, IRQ15	IO	Interrupt Request: Should be connected to IRQ slot directly. The interrupt channel selection is stored in the EEPROM and down loads the NIC configuration registers on initialization. They can be set either to shared mode (compatible to Family-1 computers) or unshared mode. Note IRQ15 is always unshared.
$\overline{IOCS16}$	O	Sixteen-Bit IO mode: Active low, when asserted indicates host accessing 16-bit wide RAM data port. It is a three-state output to allow sharing.
$\overline{ROM}$	O	ROM enable: Active low, driven low when host accesses the ROM addressed space.
BA14	O	Boot ROM Address Pin: BA14 and 245 GHz share the same pin.
$\overline{ID}$	I	ID: There are two ways to get the node address: First is to use an EEPROM, in which case this pin should not be connected. The second way is to get the ID programmed in EEPROM using this as a read control pin.
RST	I	Hardware Reset: Active high, when it is asserted, it will reset all NIC internal register to their default states.

RAM Interface Pins

Symbol	Function	Description
MA13-MA1	O	Buffer RAM Address Bus: Address 13 to 0, used to access locations of the local RAM buffer.
MD15-MD0	IO	Bi-directional Buffer RAM Data Bus.
$\overline{OE}$	O	Output Enable: Active low enables RAM data output ports. When high, drives the RAM data bus into high impedance state.
$\overline{MW0}$, $\overline{MW1}$	O	Write Enable: Active low, when asserted enable RAM to receive data from RAM data bus. $\overline{MW0}$ controls MD7-MD0: $\overline{MW1}$ controls MD15-MD8.

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4.0 PIN DESCRIPTIONS (continued)

Network Interface Pins

Symbol	Function	Description
TXE	O	Transmit Enable: This is an active high signal. It is driven high when the first bit of the packet is valid on TXD and deasserted after the last bit of the packet is clocked out of TXD. It is connected directly to the corresponding pin in a SNI (Serial Network Interface) chip.
TXD	O	Transmit Data: Serial NRZ Data Output .
TXC	I	Transmit Clock: This clock is used to provide timing for internal operation of the transmit logic.
CRS	I	Carrier Sense: This signal is active high. It is asserted by the Serial Network Interface to indicate to the NIC that carrier is present.
RXD	I	Receive Data: Serial NRZ data received from the SNI. Data is clocked into the NIC on the rising edge of RXC.
RXC	I	Receive Clock: Clock signal recovered from the received preamble data stream, used to resynchronize received data into the NIC.
COL	I	Collision Detect: It becomes active when a collision has been detected. It is monitored during transmission after preamble and synch have been transmitted. It is monitored for CD heartbeat at the end of transmission.
LBK	O	Loop back: It is set to high to indicate the NIC is programmed to the loop back mode.
NIS	O	Network Interface Select: It informs external transceiver the selection of media. Set high to select twisted-pair interface. Set low to select 10BASE2 thin cable interface. Loop back mode is selected when it is in high impedance state.
CK20M		System Clock: Twenty MHz 50% clock.

EEPROM Interface Pins

Symbol	Function	Description
ECS	IO	EEPROM Chip Select: Active High when asserted enable programming of EEPROM.
ECK	IO	EEPROM Clock: Serial data clock to clock data in or clock out of the serial EEPROM.
EDOT	O	EEPROM Data out pin, connect to the DI pin of EEPROM.
EDIN	I	Serial Data input pin from the EEPROM DO pin.

4.0 PIN DESCRIPTIONS (continued)

EEPROM Interface Pins

Symbol	Function	Description
POWERT	O	Power and Transmit operation indicator. It is normally low after power on. When a packet is being transmitted, it will go high for a period of time preset in the EEPROM and also blinks at a preset frequency during transmit.
LINKR	O	Link Receive: As NIC receive LINK signal, it is pulled low. It is pulled high when Carrier Sense signal is active.
COLL	O	Collision: It is pulled low when collision occurs.
JABBER	O	Jabber: This signal goes low when the NIC attempts to transmit a packet longer than 50 msec. It will return high when JABBER is released.
$\overline{\text{LINK}}$	I	Diagnostic pin from SNI to indicate that the SNI's connection to the network media is good.
VEEOK	I	Diagnostic Pin to help monitoring the VEE pin of the transceiver.
TEST	I	Test Pin must connected to ground.

Power and Clock Pins

Symbol	Function	Description
VCC	Power	+5 volt
GND	Ground	0 volt chip ground
SCLK	I	System clock

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5.0 PACKET RECEPTION AND TRANSMISSION

The Protocol State Machine controls packet reception and transmission. The transmit and receive circuits are enabled by setting the START and clearing the STOP bits in the Command Register. Until enabled, the serial interface sections ignore incoming packets and requests to send out packets.

If STOP is set while these sections are operational, the chip will complete the handling of the current packet and then go to a soft reset condition ignoring incoming packets and requests for transmission. The transmitter will finish all retransmissions of a colliding packet prior to heeding the STOP command. When both sections are stopped, the RST bit in the Interrupt Status Register will be set. It should be noted that the DMA controllers may remain active while STOP is set.

Packet Reception

IEEE 802.3 packets consist of these fields: preamble, SFD, DA, SA, data, and CRC.

Reception

The preamble field is used to train the external Manchester decoder and to detect carrier. If Carrier Sense (CRS) is true, preamble passes through the receive deserializer which discards it while searching for the consecutive '1' bits, Start-Frame-Delimiter (SFD) symbol. Instead of using a FIFO for TX and RX, the PI4C4301 uses an 8-bit deserializer and a 16-bit wide buffer. The receive local DMA is always available unless the NIC is in monitor mode or it finds some condition to make it abort (i.e., address does not match, CRC error, etc.). While the destination address (DA field) is being checked for recognition, the receive local DMA is disabled. If the packet is accepted, the local DMA is enabled and starts transferring data to memory. On the contrary, the receive unit clears out the deserializer, stops filling it, and waits for the start of the next packet. The source address and data fields are passed to buffer memory. In some protocols, the first two bytes of the data field denote a packet length. These bytes are not interpreted by the controller and treated as ordinary data.

End of packet

Upon loss of carrier sense, dribble clocks (receive clocks that occur after the loss of carrier) on the RXC pin flush the remainder of the received packet through the deserializer and CRC checker. The CRC of all complete octets received is computed and compared to the CRC at the end of the packet. The status of this comparison is recorded in the Receive Status Register. The CRC from each received packet is sent to memory with the packet via local DMA and is included in the byte count posted in the buffer header.

The deserializer counts the number of bits left over after the last complete octet. If that number is greater than six, a packet alignment error is reported.

If the receive unit detects errors in the packet, it may abort reception depending on the configuration of the Save Errored Packets (SEP) and Accept Runt Packets (ARP) bits of the Receive Configuration Register. If reception is aborted, the DMA controller stops sending bytes to the buffer, the receive unit clears out the deserializer, the Receive Status Register (RSR) and the Interrupt Status Register (ISR) are updated, and the receive unit waits for the next packet to begin.

The received packet length must be less than 1518 bytes including DA, SA, data, and CRC to comply with IEEE 802.3 specification. In addition, the buffer ring must have enough space to buffer the entire packet with a 4-byte header. Receiver interrupts (RXE, PRX) are posted after the packet has been completely transferred to memory. If DMA aborts, these interrupts are not set for the current packet. If set previously, they remain unchanged. Packets shorter than 64 bytes will be received only when the Accept Runts bit is enabled.

Packet Transmission

Initialization for Transmission

Packets to be transmitted are built in the buffer memory by the host. These packets must include the DA, SA, and data fields.

The transmit unit requests the packet from the local DMA unit when the TXP bit is set by the host. The TPSR , TBCR0, and TBCR1 registers must be properly programmed prior to setting TXP. Once set by the host, TXP can be cleared only by the transmitter upon completion of an attempted transmission.

Transmission Process

Transmission local DMA fills the transmission serializer and waits until the media is ready for transmission. It generates 62 bits of preamble and the 1 byte SFD pattern. The content of the transmit buffer, the preamble and SFD are then serialized and shifts bits to the TXD output pin while CRC is being computed. When the last byte is transmitted, CRC calculation stops and the CRC is appended serially to the packets with the most significant bit first.

6.0 DMA AND BUFFER MANAGEMENT

There are two DMA modes in the PI4C4301. Remote DMA controls the data between host and RAM. Local DMA manages the data transfer between buffer and the network.

Receive Buffer Management

The DMA buffer management logic is responsible for linking, recovering and recirculating of buffers. The local memory is organized as a logical ring structure consisting of a series of contiguous fixed length buffers. Each buffer is 256 bytes long. Two static registers (PAGE START, PAGE STOP) and two working registers (CURRENT PAGE, BOUNDARY POINTER) are defined to support these buffer management functions.

The Page Start and Page Stop registers must be properly set before local DMA initialize its transfer operation. These two registers should have been programmed to reserve a portion of the 64K memory locations for the receive buffer. The PSTART address points to the beginning of the buffer page and PSTOP points to the end of the page. When the DMA address reaches the PSTOP, it is reset to the PSTART. Thus the receive buffer behaves like a logical ring. The Current Page Register contains the address of the first buffer used to store an incoming packet. It serves like a write pointer for the receive DMA operation. To prevent received packet from over-writing unread packets, DMA logic stops writing frame data into the buffer when its address equals the address value as programmed in the Boundary Pointer Register. The Boundary Pointer Register points to the first unread packet. The buffer ring organization is illustrated in Figure 3.

Buffer Linking

The DMA performs a forward link to the next buffer to store packets longer than 256 bytes. Before the buffer management logic links the next buffer, it will carry out two checks. It will check if it has reached the end of the page (DMA address equals to Page Stop Address). If it does, it will reset to the beginning of the page. It will also check to see if this buffer is free by comparing its address with the address pointed to by the BOUNDARY POINTER. If the two values are equal, it aborts reception to prevent over-writing of unread data. It will use the next buffer only when the DMA address equals to neither the PSTOP nor Boundary Pointer address. Figure 4 illustrates the operations of this linin operation.

Buffer Recovery and Normal Reception Termination

If a packet is rejected due to CRC, Frame Alignment or other protocol errors, the DMA is reset back to the first buffer page used to store the packet. thus recovering all buffers that it has used to store the rejected packet. If the reception is successful, the DMA logic will store the packet header at the beginning of the first buffer used to store the packet (pointed to by the Current Page Register). The header consists of receive-status, received-byte-count and next buffer address. It then initializes the Current Page Register to the next available buffer in the ring.

Buffer Recirculation

When a packet is removed (read) from the buffer by the host, the Boundary Pointer address is advanced to free up additional buffers for reception.

Figure 3. Buffer Ring Organization

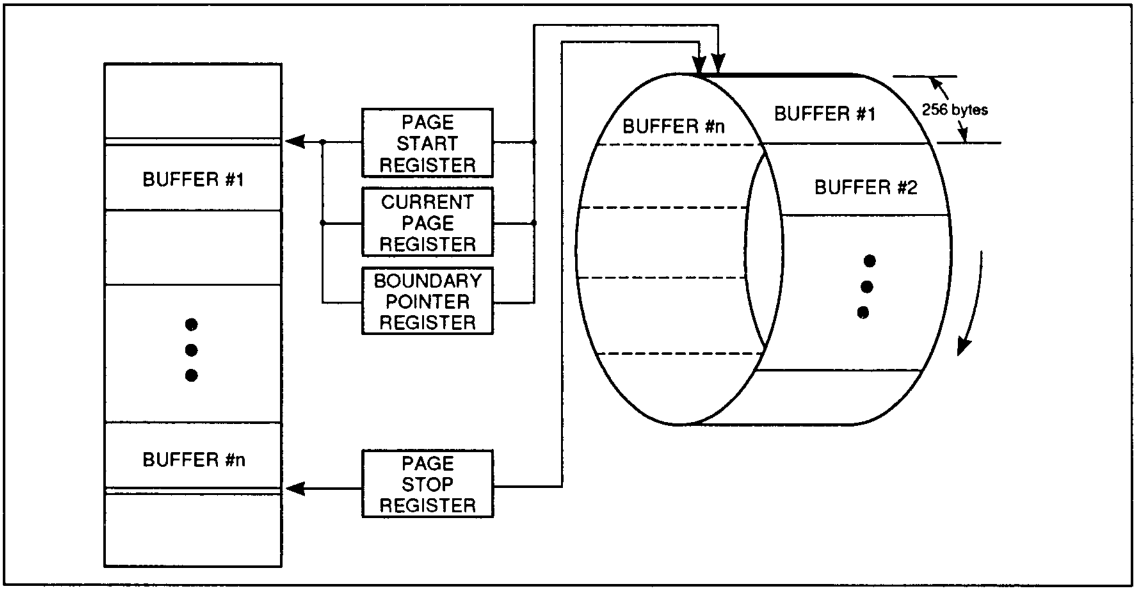
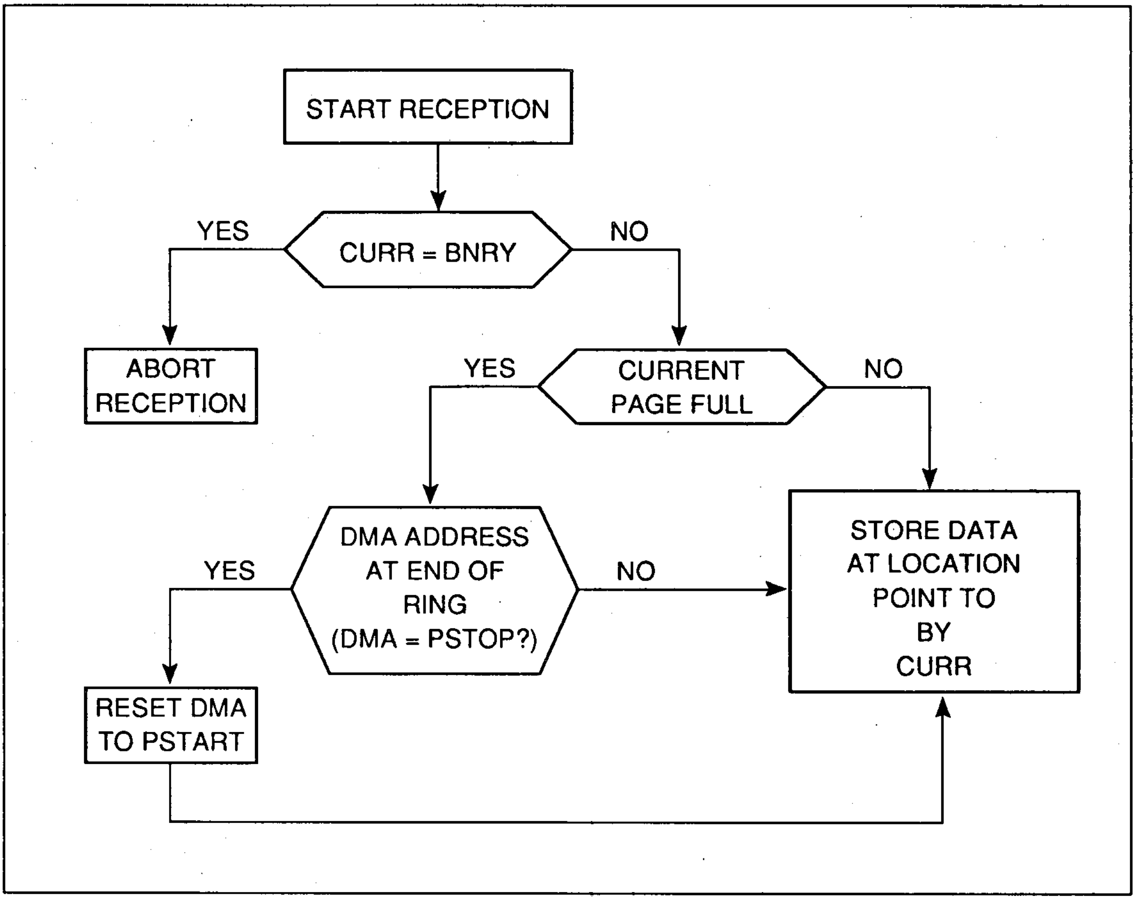


Figure 4. Buffer Linking Operation



Remote DMA Operation

Remote DMA Write

The Remote DMA can be programmed to operate in "write" mode via the command register. In this, it moves a block of data from a host I/O port (offset 10H). The block of data may be more or less than one packet. The destination starts at the value written into the RSAR0 and RSAR1 registers. The number of bytes to be transferred is programmed into the RBCR0 and RBCR1 registers.

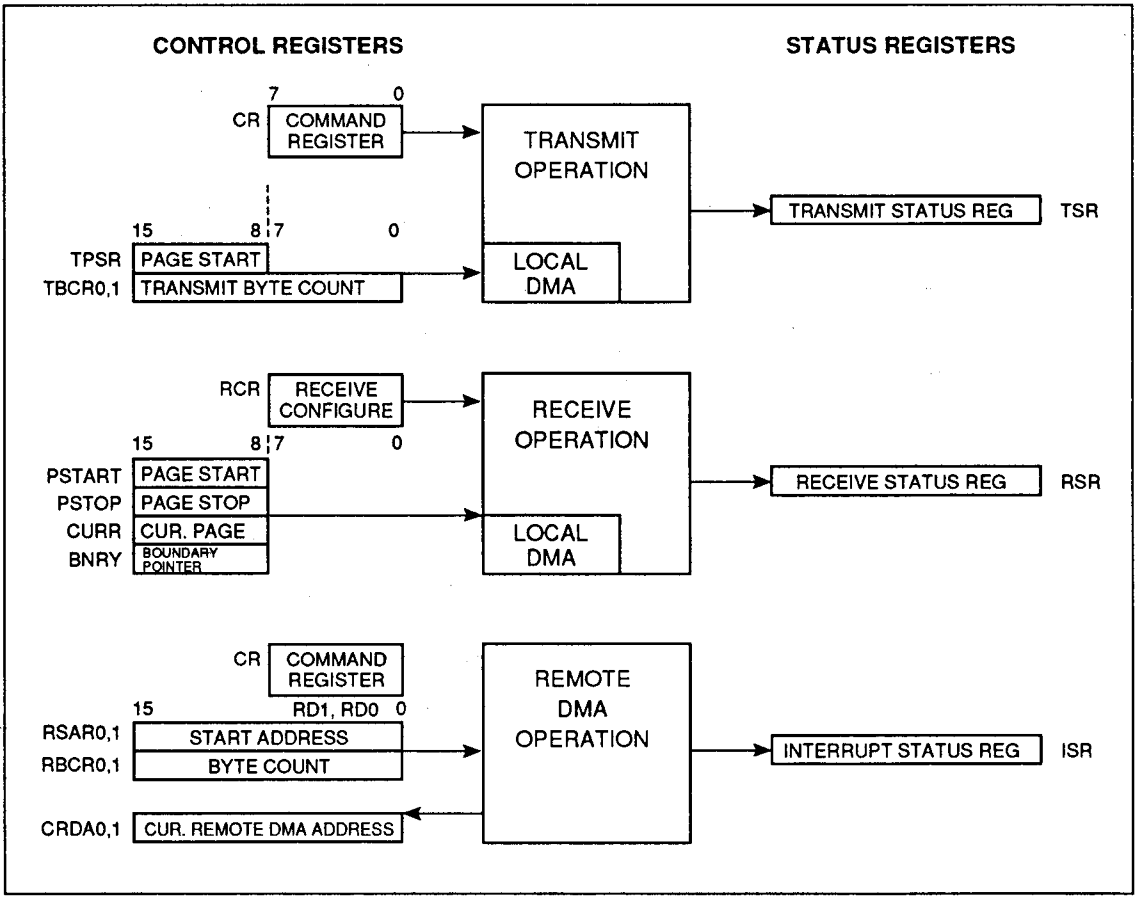
When the transfer count is satisfied, completion status is posted in the Command Register and the Interrupt Status Register. The transfer cannot be resumed once aborted but it can be restarted by setting the appropriate bit in the command register.

Remote DMA Read

The remote DMA read operation is similar to the write operation except that it transfers data from buffer memory to host I/O port. The host's read strobe to the port is monitored to indicate when the transfer has been completed and another transfer can be initiated. To utilize this mode, the host must know the starting location and the length of data that needs to be transferred. Adapter architecture that does not allow direct host access to buffer memory may not be able to utilize this mode efficiently.

Figure 5 summarizes the functions of the control and status for DMA operations.

Figure 5. Control and Status Registers Overview



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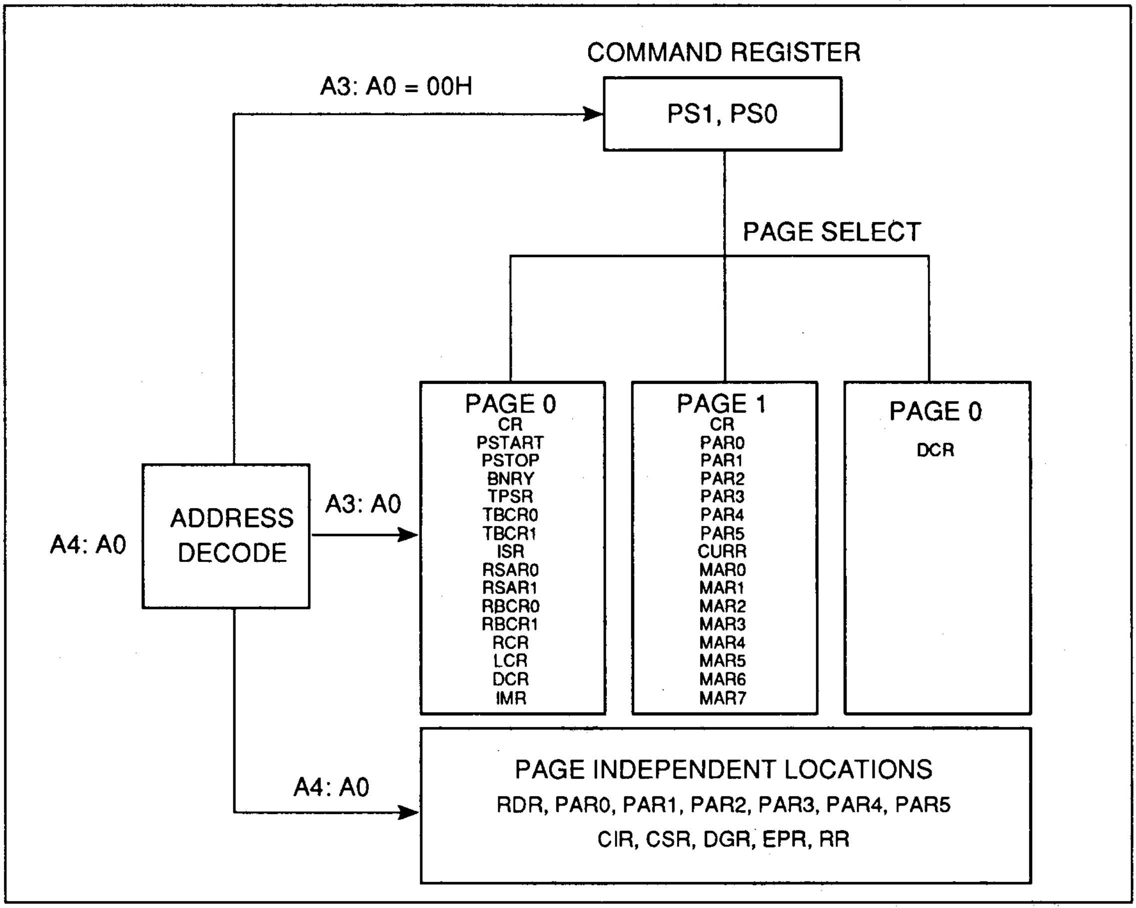
7.0 REGISTER DESCRIPTION

Internal Register Overview

The NIC contains 32 IO address spaces. IO address offset 00H to 0FH contains two pages. All IO ports except RAM Data Registers (offset 10H) are 8-bit wide. Page is selected by Command Register bits PS0 and PS1. A0 to A3 are used to address registers within the page. An overview of these registers organization is shown in Figure 6.

Figure 6. Register Addressing Overview



Register Address Assignments

Page 0 (PS1=0, PS0=0)

A0:A3	READ		WRITE	
00H	Command Register	CR	Command Register	CR
01H	—		Page Start Register	PSTART
02H	—		Page Stop Register	PSTOP
03H	Boundary Pointer	BNRY	Boundary Pointer	BNRY
04H	Transmit Status Register	TSR	Transmit Status Register	TPSR
05H	Number of Collision Register	NCR	Transmit Byte Count Register 0	TBCR0
06H	—		Transmit Byte Count Register 1	TBCR1
07H	Interrupt Status Register	ISR	Interrupt Status Register	ISR
08H	Current Remote DMA Address 0	CRDA0	Remote Start Address 0	RSAR0
09H	Current Remote DMA Address 1	CRDA1	Remote Start Address 1	RSAR1
0AH	Same as 07H		Remote Byte Count Register 0	RBCR0
0BH			Remote Byte Count Register 1	RBCR1
0CH	Receive Status Register	RSR	Receive Configuration Register	RCR
0DH			Transmit Configuration Register	TCR
0EH			Data Configuration Register	DCR
0FH			Interrupt Mask Register	IMR

Page 1 (PS1=1, PS0=1)

A0:A3	READ		WRITE	
00H	Command Register	CR	Command Register	CR
01H	Physical Address Register 0	PAR0	Physical Address Register 0	PAR0
02H	Physical Address Register 1	PAR1	Physical Address Register 1	PAR1
03H	Physical Address Register 2	PAR2	Physical Address Register 2	PAR2
04H	Physical Address Register 3	PAR3	Physical Address Register 3	PAR3
05H	Physical Address Register 4	PAR4	Physical Address Register 4	PAR4
06H	Physical Address Register 5	PAR5	Physical Address Register 5	PAR5
07H	Current Page Register	CURR	Current Page Register	CURR
08H	Multicast Address Register 0	MAR0	Multicast Address Register 0	MAR0
09H	Multicast Address Register 1	MAR1	Multicast Address Register 1	MAR1
0AH	Multicast Address Register 2	MAR2	Multicast Address Register 2	MAR2
0BH	Multicast Address Register 3	MAR3	Multicast Address Register 3	MAR3
0CH	Multicast Address Register 4	MAR4	Multicast Address Register 4	MAR4
0DH	Multicast Address Register 5	MAR5	Multicast Address Register 5	MAR5
0EH	Multicast Address Register 6	MAR6	Multicast Address Register 6	MAR6
0FH	Multicast Address Register 7	MAR7	Multicast Address Register 7	MAR7

Register Address Assignments (continued)

Page 2 (PS1=0, PS0=0)

A0:A3	READ		WRITE
0EH	Data Configuration Register	DCR	

Page Independent Register Assignments

A0:A4	READ		WRITE	
10H	RAM Data Register	RDR	RAM Data Register	RDR
14H	Physical Address Register 0	PAR0		
15H	Physical Address Register 1	PAR1		
16H	Physical Address Register 2	PAR2		
17H	Physical Address Register 3	PAR3		
18H	Physical Address Register 4	PAR4		
19H	Physical Address Register 5	PAR5		
1AH	Card ID Register	CIR		
1BH	Check Sum Register	CSR		
1DH	Diagnostic Register	DGR		
1EH	EEPROM Register	EPR	EEPROM Register	
1FH	Reset Register	RR		

Internal Register Detail Usage Description

Command Register (CR) 00H Read/Write

Command Register is used to initialize the NIC, start transmission, control DMA, and switch register pages. Detail function of each register bit is summarized in the following:

D7	D6	D5	D4	D3	D2	D1	D0
PS1	PS0	RD2	RD1	RD0	TXP	STA	STP

Bit	Symbol	Description
D7,D6	PS1,PS0	Page Select: These bits select which register page is to be accessed with A0-A4. PS1 PS0 0 0 Select Page Register 0 0 1 Select Page Register 1 1 0 Select Page Register 2 1 1 Reserved
D5,D4,D3	RD2,RD1,RD0	Remote DMA Command: These bits control Remote DMA cooperation's. RD2 RD1 RD0 0 0 0 Not allowed 0 0 1 Remote Read 0 1 0 Remote Write 1 X X Abort or Remote DMA complete Note: RD2 when set to 1 will abort any Remote DMA in progress. Software should clear the Remote Byte Count Registers and restore the starting address if the Remote DMA is aborted.
D2	TXP	Transmit Packet: This bit will initiate transmission when set. For proper operation the Transmit Byte Count and Transmit Page Start registers should have been programmed.
D1	STA	Start: This bit is powered up low and set high to activate the NIC after either power up or hardware/software reset.
D0	STP	Stop: Power up high. Set high with software to take the NIC off-line and stop packet reception or transmission. Any reception or transmission in progress will continue to completion before entering this reset state. To exit reset, STP must be set low and STA high.

Interrupt Status Register (ISR) 07H Read/Write

Interrupt Status Register: Allows the driver to determine the sources of interrupt. Pending interrupt can be cleared by writing '1' to the corresponding ISR bit. IRQx signals connected to the slot will be set high as long as any of unmasked bit is set.

D7	D6	D5	D4	D3	D2	D1	D0
RST	RDC	Reserved	Reserved	TXE	RXE	PTX	PRX

Bit	Symbol	Description
D7	RST	Reset Status: Set when NIC is reset and clear when STA command is issued to the Command Register.
D6	RDC	Remote DMA Complete: This bit is set when Remote DMA operation is completed.
D5,D4		Reserved
D3	TXE	Transmit Error: Set when 16 attempts to transmit a packet fails due to repeat collision.
D2	RXE	Receive Error: Set to indicate received packet has CRC or frame alignment error.
D1	PTX	Packet Transmitted: Set to indicate a packet is transmitted successfully.

Interrupt Mask Register (IMR) 0FH Write

Interrupt Mask Register is used to mask out certain interrupt sources selectively. Mask bits that are '1' allow the corresponding interrupts to cause an'IRQ', and '0' blocks their interrupt source.

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	RDCE	Reserved	Reserved	TXEE	RXEE	PTXE	PRXE

Bit	Symbol	Description
D7		Reserved
D6	RDCE	Remote DMA Complete Interrupt Enable
D5,D4		Reserved
D3	TXEE	Transmit Error Interrupt Enable
D2	RXEE	Receive Error Interrupt Enable
D1	PTXE	Packet Transmitted Interrupt Enable
D0	PRXE	Packet Received Interrupt Enable

Data Configuration Register (DCR) 0FH Write

This register is used to program the NIC for 8-bit or 16-bit memory interface.

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	WTS

Bit	Symbol	Description
D7		Reserved
D6		Reserved
D5		Reserved
D4		Reserved
D3		Reserved
D2		Reserved
D1		Reserved
D0	WTS	Word Transfer Select: WTS=0: Select byte wide memory access WTS=1: Select word wide memory access

Loop-back Control Register (LCR) 0DH Write

Loop back Control register defines the mode of loop back test.

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	Reserved	Reserved	LB1	LB0	Reserved

Bit	Symbol	Description
D7		Reserved
D6		Reserved
D5		Reserved
D4		Reserved
D3		Reserved
D2,D1	LB1,LB0	Loop back test Mode Select: LB1 LB0 0 0 Normal operation, default to operation at power on 0 1 Internal Loop back inside NIC 1 0 External Loop back 1 1 External Loop back
D0		Reserved

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Transmit Status Register (TSR) 04H Read

Transmit Status Register reports events occurred on the line during transmission. Before transmission all bits are cleared and set as need for correct operation.

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	CDH	Reserved	Reserved	ABT	COL	Reserved	PTX

Bit	Symbol	Description
D7		Reserved
D6	CDH	CD Heartbeat: This bit will be set if NIC fails to detect CD Heartbeat signal. The "heartbeat" signal is sent from the MAU (Ethernet transceiver) to the station that confirms that MAU collision signaling is working and connected to the station. CD Heartbeat shall commence during the first 6.4 µsec of the interframe gap following a transmission.
D5,D4		Reserved
D3	ABT	Transmit Abort: Set this bit when NIC aborts transmission of a packet suffering excessive collisions (16 unsuccessfully attempts)
D2	COL	Transmit Collided: This bit is set if the packet collided at least once with another packet on the network.
D1		Reserved
D0	PTX	Packet Transmitted: When set indicates packet has been transmitted successfully .

Receive Configuration Register (RCR) 0CH Write

This register defines the optional operation of the NIC during the packet reception. It controls address recognition and the acceptance of abnormal packets.

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	MON	PRO	AM	AB	AR	SEP

Bit	Symbol	Description
D7		Reserved
D6		Reserved
D5	MON	Monitor Mode: When this bit is set, NIC enters the monitor mode and enables the NIC to check addresses and CRC on imcoming packets without buffering them to the RAM . MON=0: Packets buffered to memory MON=1: Packets checked but not buffered to memory
D4	PRO	Promiscuous Mode: Set this bit high to enable acceptance of all packets.
D3	AM	Accept Multicast: Setting this bit high will enable reception of all packets destined to multicast addresses.
D2	AB	Accept Broadcast: Setting this bit enables reception of broadcast address.
D1	AR	Accept Runt Packets: Setting this bit directs the NIC to store packets shorter than 64 bytes.
D0	SEP	Same Errored Packets: Setting this bit directs the NIC to store packets with CRC or packet alignment errors .

Receive Status Register (RSR) 0CH Read

This register reports the status of new received packets. It categorizes errors that are detected and reports on the type of address recognized. All bits are cleared at the start of reception except the DIS (Receive Disable) bit.

D7	D6	D5	D4	D3	D2	D1	D0
DFR	DIS	PHY	MON	Reserved	FAE	CRC	PRX

Bit	Symbol	Description
D7	DFR	Deferring: Set when both CRS and COL are high. If MAU has asserted COL as a result of jabber, this bit will stay set to indicate a jabber condition.
D6	DIS	Receiver Disable: Set when the receiver is in monitor mode. Cleared when leaving this mode.
D5	PHY	Physical/Multicast Address: Set when the NIC is programmed to receive physical and multicast addresses. Reset when the NIC is requested to receive physical address only.
D4	MON	Monitor Mode: Set to indicate NIC is in monitor mode. Packet received is not buffered to memory.
D3		Reserved
D2	FAE	Packet Alignment Error: Indicates the incoming packet did not end on a byte boundary.
D1	CRC	CRC Error: Indicates packet's computed CRC fails to match with the CRC appended to the end of packet.

DMA Registers

Transmit DMA register

Transmit Page Start Register (TPSR) 04H Write

TPSR specifies the RAM page address to be transmitted. Packet transmitted is always from the beginning of a page.

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

9

Transmit Byte Count Register 0, 1 (TBCR0, TBCR1) 05H,06H Write

TBCR0 and TBCR1 indicate the byte count of the packet to be transmitted. They include address field, length field and data field. The maximum allowable length is 64K bytes.

TBCR1

D7	D6	D5	D4	D3	D2	D1	D0
L15	L14	L13	L12	L11	L10	L9	L8

TBCR0

D7	D6	D5	D4	D3	D2	D1	D0
L7	L6	L5	L4	L3	L2	L1	L0

Local DMA Receive Registers

Page Start and Page Stop Registers (PSTART,PSTOP) 01H,02H in register page 0 Write

PSTART and PSTOP set thee page range for local DMA operation.

PSTART or PSTOP

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

Boundary Register (BNRY) 03H page 0 Write

BNRY Register is used to prevent overflow in the receive ring buffer. Local DMA controller compares the contents of BNRY to the next buffer address. If they match, the local DMA operation will be aborted.

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

Current Page Register (CURR) 0AH in page 0 Read Only, 07H page 1 Read/Write.

D7	D6	D5	D4	D3	D2	D1	D1
A15	A14	A13	A12	A11	A10	A9	A8

Remote DMA Registers

Remote Start Address Register (RSAR0,RSAR1) 08H,09H Write

These two registers point to the starting address of the memory block to be transferred to or from host.

RSAR1

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

RSAR0

D7	D6	D5	D4	D3	D2	D1	D0
A7	A6	A5	A4	D7	D6	A1	A0

Remote Byte Count Register (RBCR0,RBCR1) 0BH, 0CH Write

RBCR0 and RBCR1 indicate the byte count to transferred through remote DMA.

RBCR1

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

RBCR0

D7	D6	D5	D4	D3	D2	D1	D0
A7	A6	A5	A4	D7	D6	A1	A0

Current Remote DMA Address (CRDA0,CRDA1) 08H,09H Read

CRDA0 and CRDA1 contain the current address of the Remote DMA.

CRDA1

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

CRDA0

D7	D6	D5	D4	D3	D2	D1	D0
A7	A6	A5	A4	A3	A2	A1	A0

RAM Data Register (RDR) 10H Read/Write

RDR is a 16-bit wide register. Host fetches data from or stores data to the RAM through this register. Remote DMA controller is responsible for the data moving between RAM and this port.

RDR

D15	D14	D13	D12	D11	D10	D9	D8
RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8

D7	D6	D5	D4	D3	D2	D1	D0
RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

Physical Address Register (PAR0-PAR5)

Page 0: 14H-19H Read
Page 1: 01H-07H Read/Write

The offset 10H and 14H to 1FH do not belong to any page. Upon power-on, PAR0 to PAR5 in EEPROM are shifted to 14H to 19H and page 1, 01H to 07H at the same time. The NIC can handle both NE1000 and NE2000.

9

PAR0

D7	D6	D5	D4	D3	D2	D1	D0
DA7	DA6	DA5	DA3	DA2	DA1	DA1	DA0

PAR1

D7	D6	D5	D4	D3	D2	D1	D0
DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8

PAR2

D7	D6	D5	D4	D3	D2	D1	D0
DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16

PAR3

D7	D6	D5	D4	D3	D2	D1	D0
DA31	DA30	DA29	DA28	DA27	DA26	DA25	DA24

PAR4

D7	D6	D5	D4	D3	D2	D1	D0
DA39	DA38	DA37	DA36	DA35	DA34	DA33	DA32

PAR5

D7	D6	D5	D4	D3	D2	D1	D0
DA47	DA46	DA45	DA44	DA43	DA42	DA41	DA40

Destination Address Data Format

P/S DA0...DA47...

Multicast Address Register (MAR0-MAR7)
Page 1, 08H-0FH Read/Write

MAR0

D7	D6	D5	D4	D3	D2	D1	D0
FB7	FB6	FB5	FB4	FB3	FB2	FB1	FB0

MAR1

D7	D6	D5	D4	D3	D2	D1	D0
FB15	FB14	FB13	FB12	FB11	FB10	FB9	FB8

MAR2

D7	D6	D5	D4	D3	D2	D1	D0
FB23	FB22	FB21	FB20	FB19	FB18	FB17	FB16

MAR3

D7	D6	D5	D4	D3	D2	D1	D0
FB31	FB30	FB29	FB28	FB27	FB26	FB25	FB24

MAR4

D7	D6	D5	D4	D3	D2	D1	D0
FB39	FB38	FB37	FB36	FB35	FB34	FB33	FB32

MAR5

D7	D6	D5	D4	D3	D2	D1	D0
FB47	FB46	FB45	FB44	FB43	FB42	FB41	FB40

MAR6

D7	D6	D5	D4	D3	D2	D1	D0
FB55	FB54	FB53	FB52	FB51	FB50	FB49	FB48

MAR7

D7	D6	D5	D4	D3	D2	D1	D0
FB63	FB62	FB61	FB60	FB59	FB58	FB57	FB56

Card ID Register (CIR) 1AH Read

CIR contains the card ID down loaded from the EEPROM.

CIR

D7	D6	D5	D4	D3	D2	D1	D0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Check Sum Register (SR) 1BH Read

The summation of data in registers offset 14H to 1AH, and in this register, should be FFH to indicate a valid signature of NIC.

SR

D7	D6	D5	D4	D3	D2	D1	D0
SUM7	SUM6	SUM5	SUM4	SUM3	SUM2	SUM1	SUM0

Diagnostic Register (DGR) 1DH Read

This register provides the diagnostic status of the following signals: NIC, LB, LNK, COLL, TCOK, CK20M and VEE.

DGR

D7	D6	D5	D4	D3	D2	D1	D0
NIS	LB	LNK	COLL	Reserved	TCOK	CK20M	VEE

Bit	Symbol	Description
D7	NIS	This bit when set to '1' indicates T7213 is in the twisted-pair mode. It is also reflected from the setup configuration register "NIS" bit that loads from EEPROM.
D6	LB	This bit when set to '1' indicates that T7213 is in the loopback mode.
D5	LNK	This bit reflects the real-time status of the LINK pin from the serial network interface device.
D4	COLL	This bit reflects the real-time status of the COLL pin from the external serial network interface circuit.
D3		Reserved
D2	TCOK	This bit when high indicates that the transmission clock TXC from the external SNI is in good condition.
D1	CK20M	When high indicates the CK20M clock is in good condition.
D0	VEE	Active low indicates that the DC-DC converter is in good condition. It has the status as the VEEOK pin from DC-DC detector circuit.

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EEPROM Programming Register (EPR) 1EH Read/Write

EPR is used to read or write serial EEPROM. Strict programming rules should be obeyed to avoid losing EEPROM programmed data. Detail programming method and usage are outlined in the appendix.

EPR — Read

D7	D6	D5	D4	D3	D2	D1	D0
12.8µ	EEPRM	RCL	ASIC	ECS	ECK	EDOT	EDIN

EPR — Write

D7	D6	D5	D4	D3	D2	D1	D0
—	—	RCL	ASIC	ECS	ECK	EDOT	ADOT

Bit	Symbol	Description
D7	12.8µ	This is a 12.8 µsec time period square wave signal. It can be used as a time reference when programming EEPROM.
D6	EEPM	This bit is active high. When it is set, it indicates that EEPROM is loading data to the NIC setup registers. EEPM active will disable ASIC function.
D5	RCL	Recall function: In normal operation, this bit will be low. A high-to-low transition will cause data to be reloaded from EEPROM to the setup registers. This bit can be read back from the same IO port.
D4	ASIC	When programming EEPROM, this bit must be set to low. Set the bit high to modify the setup register and program setup register using ECS, ECK, and ADOT. This bit can be read back from the same IO port.
D3	ECS	EEPROM chip select. This active high bit controls the ECS pin of EEPROM directly and can be read back from the same IO port.
D2	ECK	EEPROM clock: It is used to clock data in and out of the EEPROM. It controls the ECK pin of the EEPROM and can be read back from the same IO port.
D1	EDOT	Data Out: Serial data out to EEPROM via EDOT pin and can be read back from the same IO port.
D0	EDIN (read)	Data in: Serial data in via EDIN pin from EEPROM DO pin.
	ADOT (write)	Data out to ASIC setup registers. With ASIC pin set to high, the serial data from ADOT will be written to the setup registers to cooperate with ECS and ECK signals.

Reset Register (RR) 1FH Read

Reading this register will cause a software reset. Data in this register is meaningless.

8.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Power Supply Voltage	GND – 0.3V to 7.0V
Input Voltage	GND – 0.3V to Vcc + 0.5V
Output Voltage	GND – 0.3V to Vcc + 0.5V
Output Current	±24 mA
Power Dissipation	200 mW
Power Supply Current	±40 mA
Storage Temperature	–65°C to +150°C

NOTE:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

	Min.	Typ.	Max.
Power Supply Voltage	4.5V	5.0V	5.5V
Input Voltage	GND		Vcc
Operating Temperature	0°C		70°C

NOTE:
Any changes in Power Supply Min/Max voltage and Min/Max operating temperature will cause changes in D.C. and A.C. parameters. Consult Pioneer Semiconductor for the impact of these changes.

D.C. Electrical Characteristics (on Recommended Operating Conditions)

Symbol	Description	Test Conditions	Min.	Typ	Max.	Units
I_{DDS}	Static Current	V_{IN} = Vcc or GND, Vcc = Max, I_{OH} = I_{OL} = 0			200	μA
I_L	Input Leakage Current	V_{IH} = Vcc, V_{IL} = GND, Vcc = Max	–1		1	μA
V_{IH1}	Input HIGH Voltage	Vcc = Max	3.5			V
V_{IL1}	Input LOW Voltage	Vcc = Min			1.0	V
V_{IH2}	Input HIGH Voltage	Vcc = Max	2.0			V
V_{IL2}	Input LOW Voltage	Vcc = Min			0.8	V
V_{T1+}	Trigger HIGH Voltage	Vcc = 5.0V (LIN + STB)			4.0	V
V_{T1-}	Trigger LOW Voltage	Vcc = 5.0V (LIN + STB)	0.8			V
V_{H1}	Hysteresis	Vcc = 5.0V (LIN + STB)	0.3			V
V_{T2+}	Trigger HIGH Voltage	Vcc = 5.0V (LIN + STBT)			3.0	V
V_{T2-}	Trigger LOW Voltage	Vcc = 5.0V (LIN + STBT)	0.6			V
V_{H2}	Hysteresis	Vcc = 5.0V (LIN + STBT)	0.1			V
R_{PU1}	Pull Up Resistor	Vcc = 5.0V	50		500	KΩ
R_{PD1}	Pull Down Resistor	Vcc = 5.0V	50		500	KΩ
V_{OH1}	Output HIGH Voltage	Vcc = Min, I_{OH} = –1 mA	Vcc–0.4			V
V_{OL1}	Output LOW Voltage	Vcc = Min., I_{OL} = 2 mA			Vss+0.4	V
V_{OH2}	Output HIGH Voltage	Vcc = Min, I_{OH} = –3 mA	Vcc–0.4			V
V_{OL2}	Output LOW Voltage	Vcc = Min., I_{OL} = 6 mA			Vss+ 0.4	V
V_{OH3}	Output HIGH Voltage	Vcc = Min, I_{OH} = –6 mA	Vcc–0.4			V
V_{OL3}	Output LOW Voltage	Vcc = Min., I_{OL} = 12 mA			Vss+0.4	V
V_{OH4}	Output HIGH Voltage	Vcc = Min, I_{OH} = –12 mA	Vcc–0.4			V
V_{OL4}	Output LOW Voltage	Vcc = Min., I_{OL} = 24 mA			Vss+0.4	V
V_{OZ}	Offstate Leakage	Vcc = Max, V_{OH} = Vcc, V_{OL} = GND	–1		1	μA

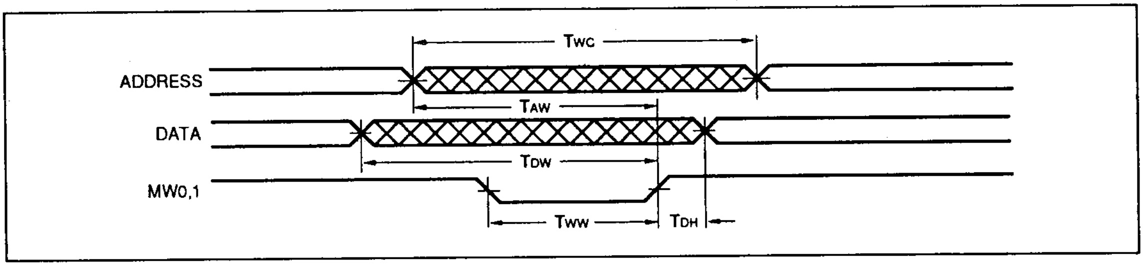
NOTE: All output drives are of type V_{OL2} and V_{OH2} except the following: RDY and $\overline{IOCS16}$ of type V_{OL4} and V_{OH4}; POWERT, LINKR, COLL, JABBER are type V_{OL3} and V_{OH3}.

9.0 SWITCHING TIMING AND AC CHARACTERISTICS

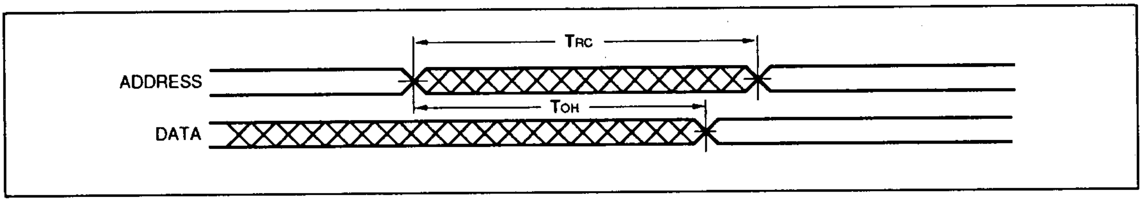
MEMORY

Symbol	Parameter	Min	Max	Unit
T_{RC}	Read cycle time	200	—	ns
T_{OH}	Output hold from address change	150	—	ns
T_{WC}	Write cycle time	200	—	ns
T_{AW}	Address valid to end of write	152	—	ns
T_{WW}	Memory write width	104	—	ns
T_{DW}	Data to write time overlap	153	—	ns
T_{DH}	Data hold from write time	47	—	ns
T_{RD}	$\overline{\text{MEMR}}$ to $\overline{\text{ROM}}$ delay time	3	—	ns

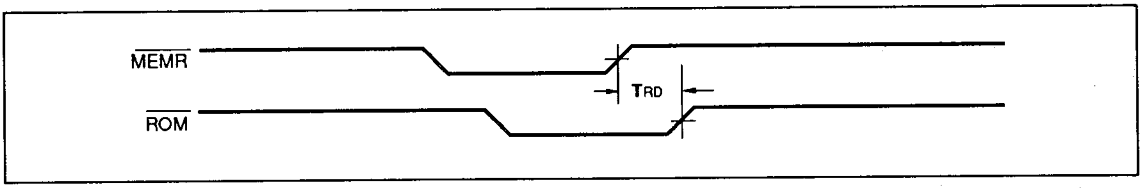
RAM WRITE Cycle Waveform



RAM READ Cycle Waveform



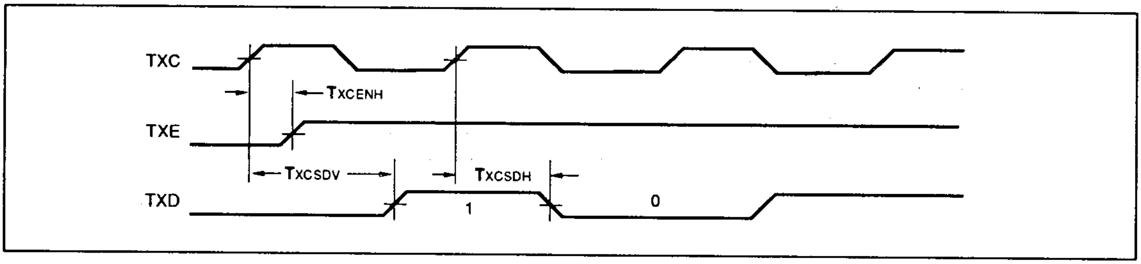
ROM READ Cycle Waveform



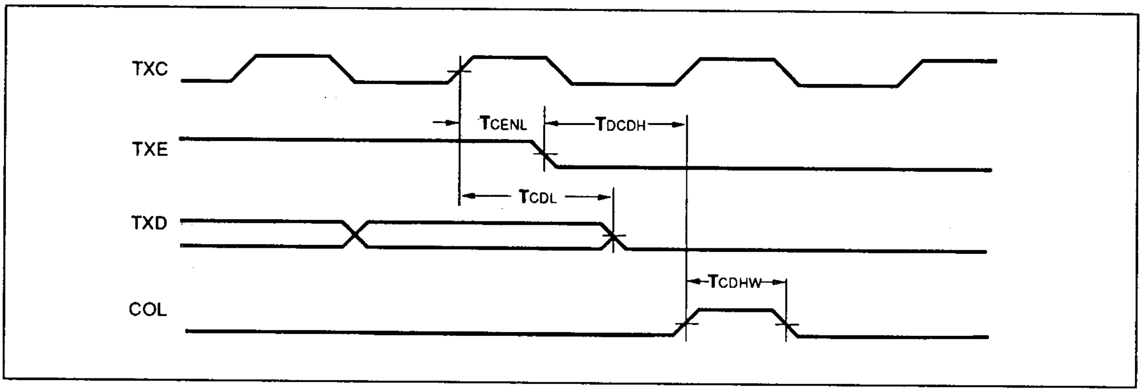
TRANSMIT

Symbol	Parameter	Min	Max	Unit
TXCENH	TXC to TXE high	—	39	ns
TXCSDV	TXC to serial data valid	—	37	ns
TXCSDH	Serial data hold time from TXC high	8	—	ns
TCDL	TXC to data low	—	30	ns
TCENL	TXC to TXEN low	—	58	ns
TDCDH	TXEN low to start of COL (HD)	—	64	TXC
TCDHW	COL detect width	2	—	TXC

Serial Timing – Transmit (Beginning of Frame)



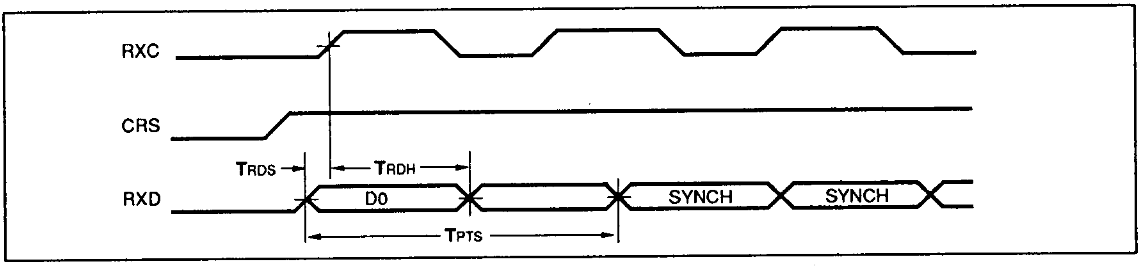
Serial Timing – Transmit (End of Frame, CD Heartbeat)



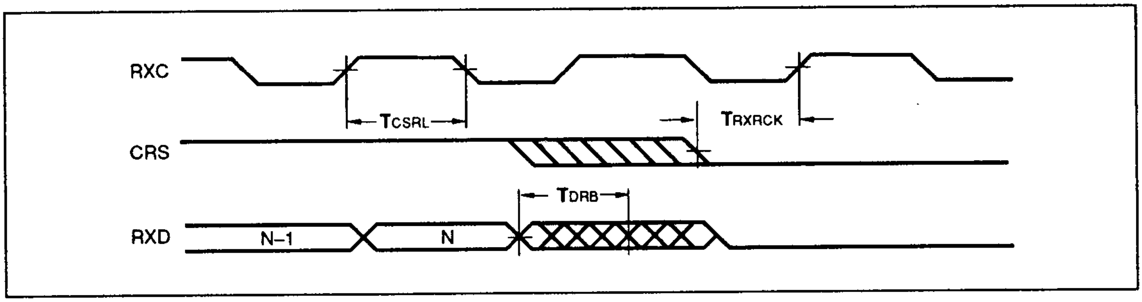
RECEIVE

Symbol	Parameter	Min	Max	Unit
T_{RDS}	RXD setup to RXC high	0	—	ns
T_{RDH}	RXD hold from RXC high	16	—	ns
T_{PTS}	First preamble bit to synch	8	—	RXC
T_{RXRCK}	Min. number of RXC after CRS low	3	—	RXC
T_{DRB}	Maximum of allowed dribble bits	—	6	RXC
T_{CRSL}	RXC to CSN low	0	1	RXC

Serial Timing – Receive (Beginning of Frame)



Serial Timing – Receive (End of Frame, CD Heartbeat)



APPENDIX A

PROGRAMMING EEPROM

Signature of the PI4C4301

Driver programs can recognize the existence of a NIC made of a PI4C4301 by reading the IO ports offset 14H through 1BH. Data in these ports are 6-byte address ID, 1-byte card ID, and 1-byte check sum. If the first three bytes of address ID match the company's address block, and the sum of these eight bytes is equal to FFH, then the card should be made of PI4C4301.

Programming the EEPROM

The port used to program EEPROM is located at IO base offset 1EH. A sample of the code segment is listed below to explain the EEPROM (assume IOBase = 300H).

```
                         out 31eH, 09H
                         out 31eH, 0dH
                         out 31eH, 05H
                         out 31eH, 01H
send_init:
  {
     send CS = 'H' and one CK   ;  CS  __--
                                ;  CK  _--_
                                ;  DI  ____
                                ;  DO  ----
  }

send_0:
  {
     send DI = '0' and one CK when CS is high
                                ;  CS  ----
                                ;  CK  _--_
                                ;  DI  ____
                                ;  DO  ----
  }

send_1:
  {
     send DI = '1' and one CK when CS is high
                                ;  CS  ----
                                ;  CK  _--_
                                ;  DI  ----
                                ;  DO  ----
  }

send_end:
  {
     send CS = 'L' and one CK at the end of data
                                ;  CS  ____
                                ;  CK  _--_
                                ;  DI  ----
                                ;  DO  ----
  }
```

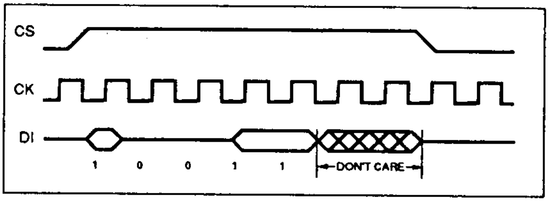
```
main ()
  begin

; send a WRITE ENABLE signal through the PI4C4301 to EEPROM.

; IOBase = 300H

      call send_init;
      call send_1;
      call send_0;
      call send_0;
      call send_1;
      call send_1;
      call send_0;
      call send_0;
      call send_0;
      call send_0;
      call send_end;
  end
```

The waveform must be as indicated.



NOTE: The frequency of CK must not be over 1 MHz.

Instruction Set.

Instruction	Start Bit	OP Code	Address	Input Data
READ	1	10	(A5–A0)	
WEN (Write Enable)	1	00	11XXXX	
WRITE	1	01	(A5–A0)	D15–D0
WRALL (Write All Registers)	1	00	01XXXX	D15–D0
WDS (Write Disable)	1	00	00XXXX	
ERASE	1	11	(A5–A0)	
ERAL (Erase All Registers)	1	00	10XXXX	

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Data in the EEPROM are defined as follows:

Word	Description
0	Physical Address Byte 0 & 1
1	Physical Address Byte 2 & 3
2	Physical Address Byte 4 & 5
3	IO & ROM base address settings
4	IRQ channel selection, ROM size selection, some other characteristics selection
5	Card ID and Checksum
6–63	User Defined

Physical Address is the address block assigned by IEEE Block Assignment Committee plus NIC's address ID .

Bits in Word 3 & 4 are explained as:

WORD 3

D15	D14	D13	D12	D11	D10	D9	D8
Reserved	1	LB	NIS	ISH	SEEQ	ROM	0

D7	D6	D5	D4	D3	D2	D1	D0
NS	SEL	SA6	SA5	SA16	SA15	SA14	SA13

Bit	Symbol	Description
D15		Reserved
D14	1	
D13,D12	LB, NIS	Loopback and Media Selection. Setting of LB will put NIS output into tri-state. Resetting this bit will make the NIS pin reflect the value of the NIS bit. T7213 twisted-pair is selected with NIS set to high.
D11	ISH	Interrupt Sharing. Setting of this bit enables the IRQ channel to be shared with some other interface card. IRQ sharing is used in IBM Family-1 PS/2 model 30 or lower computers.
D10	SEEQ	Set when TXC is postive trigger, clear when negative trigger.
D9	ROM	Set high to enable remote boot ROM. Set low to disable ROM decoding.
D8	0	
D7	NS	Set when RXC is positive trigger, clear when negative trigger.
D6,D5,D4	SEL, SA6, SA5	Base IO Selection. The eight combinations of these bits decide the Base IO address as below: SEL SA6 SA5 0 0 0 ; Base IO Address=0300H 0 0 1 ; Base IO Address=0320H 0 1 0 ; Base IO Address=0340H 0 1 1 ; Base IO Address=0360H 1 0 0 ; Base IO Address=0800H* 1 0 1 ; Base IO Address=1800H 1 1 0 ; Base IO Address=2800H 1 1 1 ; Base IO Address=3800H

Bit	Symbol	Description
D3–D0	SA16–SA13	Base ROM Address. ROM occupies as much space as the user chooses. It may be located on 8K-byte boundary of C and D segment. ROM is active with ROM bit set high. The eleven combinations of SA16 thru SA13 define its base addresses. SA16 SA15 SA14 SA13 0 0 0 0 ; Base ROM Address=C0000H 0 0 0 1 ; Base ROM Address=C2000H 0 0 1 0 ; Base ROM Address=C4000H 0 0 1 1 ; Base ROM Address=C6000H 0 1 0 0 ; Base ROM Address=C8000H 0 1 0 1 ; Base ROM Address=CA000H 0 1 1 0 ; Base ROM Address=CC000H 0 1 1 1 ; Base ROM Address=CE000H 1 0 0 0 ; Base ROM Address=D0000H 1 0 0 1 ; Base ROM Address=D2000H 1 0 1 0 ; Base ROM Address=D4000H 1 0 1 1 ; Base ROM Address=D6000H 1 1 0 0 ; Base ROM Address=D8000H 1 1 0 1 ; Base ROM Address=DA000H 1 1 1 0 ; Base ROM Address=DC000H

WORD 4

D15	D14	D13	D12	D11	D10	D9	D8
X	X	X	QCSN	8K	NE1	LEDS1	LEDS0

D7	D6	D5	D4	D3	D2	D1	D0
1	SA10	ROMS1	ROMS0	1	INTS2	INTS1	INTS0

Bit	Symbol	Description
D15–D13		Reserved
D12	QCRS	Set when CRS is negative available, clear when positive available.
D11	8K	Set to decode the R/W width of the local RAM to 8K, otherwise the R/W width of the local RAM is 16K.
D10	NE1	Set when using NE1000 driver. Clear for NE2000 mode.
D9,D8	LEDS0, LEDS1	LED Flash Speed Select. These two bits can select the flash period of LED when PI4C4301 is receiving or transmitting a package. LEDS1 LEDS0 0 0 ; 26.25 msec 0 1 ; 52.5 msec 1 0 ; 105 msec 1 1 ; 210 msec
D7	0	
D6	SA10	When ROM size is 32K, pin 117 will become MA14 of the ROM address pin. If not, pin 117 will be determined by this bit. Set pin 117 will be 245 Gz, clear pin 117 will be "H".

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Bit	Symbol	Description
D5,D4	ROMS0–ROMS1	ROM Size Select. These two bits can select boot ROM size as: ROMS1 ROMS0 0 0 ; 8K 0 1 ; 16K 1 0 ; 32K 1 1 ; Reserved
D3	1	
D2–D0	INTS2–INTS0	Interrupt Select. The seven combinations of INTS2 through INTS0 define the IRQ channel used. INTS2 INTS1 INTS0 0 0 0 ; IRQ15 @ 0 0 1 ; IRQ 3 * 0 1 0 ; IRQ 4 0 1 1 ; IRQ 5 1 0 0 ; IRQ 9 1 0 1 ; IRQ 10 1 1 0 ; IRQ 11 1 1 1 ; IRQ 14 @: IRQ15 cannot be programmed as shared IRQ4 .

WORD 5: Card ID and Checksum

D15–D8	D7–D0
Checksum	Card ID

The sum of byte 0 to byte 5 (word 0 to word 2) and byte 10, byte 11 (word 5) should be FFH.