## KMCJ532512

512K x 32 / 1M x 16 Fast Page Mode

### GENERAL DESCRIPTION

The KMCJ532512 is the industry standard high capacity DRAM memory card and consists of SAMSUNG's advanced TSOP 4M B/W DRAM devices.

The SAMSUNG memory card family is designed to protect the internal circuitry from electrostatic discharge by using metal plates on the top and bottom side of the card. And the memory card supports the JEIDA standard to provide system upgradability and exchangeability.

The memory card allows the user to switch x32/x16 for the ease of system interface. The memory card is designed to suit for memory capacity expansion and applications which handles large data.

### FEATURES

- Performance range :

| | tRAC | tCAC | tRC |
|---|---|---|---|
| KMCJ532512 - 6 | 60 ns | 15 ns | 110 ns |
| KMCJ532512 - 7 | 70 ns | 20 ns | 130 ns |
| KMCJ532512 - 8 | 80 ns | 20 ns | 150 ns |

- Organization : 512Kx32 / 1Mx16
- Power Supply : 5V±5%
- Fast Page Mode Operation
- TTL compatible inputs and outputs
- All inputs buffered except $\overline{RAS}$ inputs
- Extended refresh : 1024 cycles/128 ms
  - $\overline{RAS}$ only and Hidden refresh
  - $\overline{CAS}$ before $\overline{RAS}$ refresh
- Supported Industry Standard (JEIDA / JEDEC)
  - Connector type : 88 pin two piece (Two Row)
  - Card Dimensions : 85.6 x 54.0 x 3.3 (mm)



### PIN CONFIGURATION

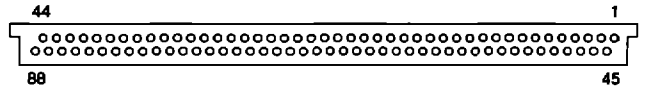
| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Vss | 16 | A4 | 31 | NC | 46 | DQ16 | 61 | A9 | 76 | PD8 |
| 2 | DQ0 | 17 | NC | 32 | NC | 47 | DQ17 | 62 | NC | 77 | NC |
| 3 | DQ1 | 18 | A6 | 33 | NC | 48 | DQ18 | 63 | Vss | 78 | NC |
| 4 | DQ2 | 19 | A8 | 34 | DQ8 | 49 | DQ19 | 64 | NC | 79 | NC |
| 5 | DQ3 | 20 | NC | 35 | NC | 50 | DQ20 | 65 | NC | 80 | DQ24 |
| 6 | DQ4 | 21 | NC | 36 | DQ9 | 51 | DQ21 | 66 | $\overline{CAS2}$ | 81 | DQ25 |
| 7 | DQ5 | 22 | $\overline{RAS0}$ | 37 | Vcc | 52 | DQ22 | 67 | Vss | 82 | DQ26 |
| 8 | DQ6 | 23 | $\overline{CAS0}$ | 38 | DQ10 | 53 | DQ23 | 68 | $\overline{CAS3}$ | 83 | DQ27 |
| 9 | Vcc | 24 | $\overline{CAS1}$ | 39 | DQ11 | 54 | NC | 69 | NC | 84 | DQ28 |
| 10 | DQ7 | 25 | NC | 40 | DQ12 | 55 | NC | 70 | $\overline{WE}$ | 85 | DQ29 |
| 11 | NC | 26 | $\overline{RAS2}$ | 41 | DQ13 | 56 | Vss | 71 | PD1 | 86 | DQ30 |
| 12 | NC | 27 | Vcc | 42 | DQ14 | 57 | A1 | 72 | PD3 | 87 | DQ31 |
| 13 | A0 | 28 | PD2 | 43 | DQ15 | 58 | A3 | 73 | Vss | 88 | Vss |
| 14 | A2 | 29 | PD4 | 44 | Vss | 59 | A5 | 74 | PD5 | | |
| 15 | Vcc | 30 | PD6 | 45 | Vss | 60 | A7 | 75 | PD7 | | |

### PIN DESCRIPTION

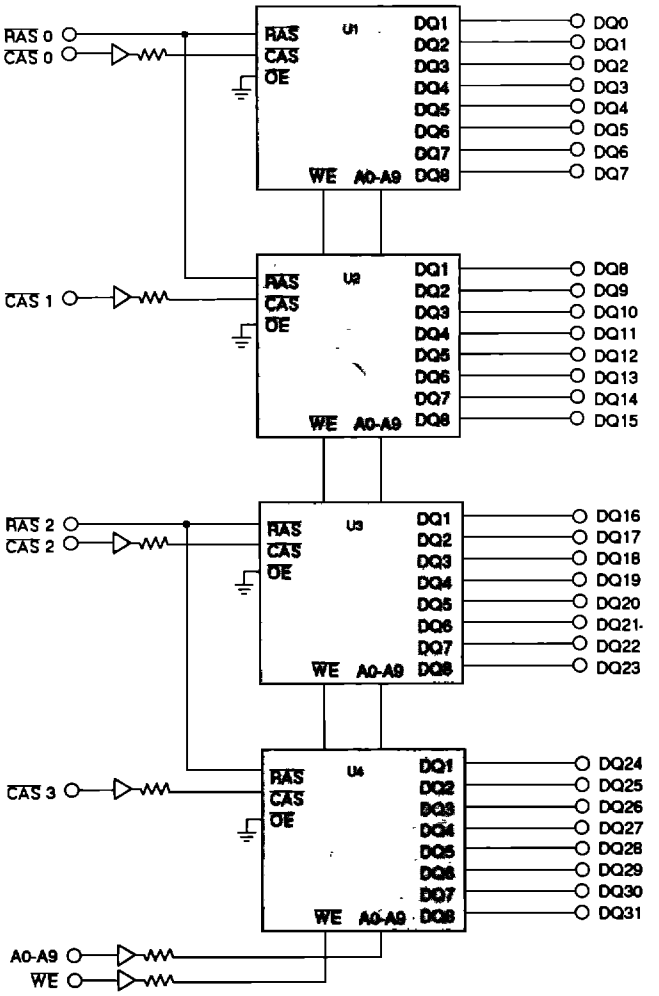
| | |
|---|---|
| A0 - A9 | Address Inputs |
| DQ0 - DQ31 | Data Input / Outputs |
| $\overline{RAS0}$, $\overline{RAS2}$ | Row Address Strobe |
| $\overline{CAS0}$ - $\overline{CAS3}$ | Column Address Strobe |
| $\overline{WE}$ | Read / Write Input |
| Vcc | Power (+5V) |
| Vss | Ground |
| NC | No Connection |

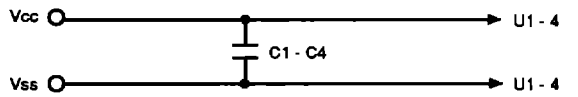
| | 60 ns | 70 ns | 80 ns |
|---|---|---|---|
| PD1 | NC | NC | NC |
| PD2 | GND | GND | GND |
| PD3 | GND | GND | GND |
| PD4 | GND | GND | GND |
| PD5 | NC | NC | NC |
| PD6 | NC | GND | NC |
| PD7 | NC | NC | GND |
| PD8 | NC | NC | NC |

### PIN CONNECTOR



**FUNCTIONAL BLOCK DIAGRAM**



### ABSOLUTE MAXIMUM RATINGS *

| Item | Symbol | Rating | Units |
|---|---|---|---|
| Input Voltage on any pin relative to Vss : $\overline{RAS}$ pin | $V_{IN1}$ | -1.0 to +7.0 | V |
| Input Voltage on any pin relative to Vss : except $\overline{RAS}$ pin | $V_{IN2}$ | -0.5 to Vcc+0.5 | V |
| Output Voltage on any pin relative to Vss | $V_{OUT}$ | -1.0 to +7.0 | V |
| Voltage on Vcc supply relative to Vss | $V_{CC}$ | -0.5 to +7.0 | V |
| Storage Temperature | Tstg | -20 to +70 | °C |
| Power Dissipation | $P_D$ | 2.8 | W |
| Short Circuit Output Current | Ios | 50 | mA |

*Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exxposure to absolute maximum rating conditions for extended periods may affect device reliability.

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### RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T = 0 to 70 °C)

| Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.75 | 5.0 | 5.25 | V |
| Ground | Vss | 0 | 0 | 0 | V |
| Input High Voltage | $V_{IH}$ | 2.4 | - | Vcc+1 | V |
| Input Low Voltage | $V_{IL}$ | -1.0 | - | 0.8 | V |
| Operating Temperature | $T_A$ | 0 | - | 55 | °C |

**DC AND OPERATING CHARACTERISTICS** (Recommended operating conditions unless otherwise noted.)

| Parameter | Part No | Symbol | Min | Max | Units |
|---|---|---|---|---|---|
| OPERATING CURRENT* ($\overline{RAS}$, $\overline{CAS}$, Address cycling @tRC=min.) | KMCJ532512 - 6 | $I_{CC1}$ | - | 360 | mA |
| | KMCJ532512 - 7 | | - | 320 | mA |
| | KMCJ532512 - 8 | | | 280 | mA |
| STANDBY CURRENT($\overline{RAS}$=$\overline{CAS}$=$V_{IH}$) | | $I_{CC2}$ | - | 8 | mA |
| RAS-ONLY REFRESH CURRENT* ($\overline{CAS}$= $V_{IH}$, $\overline{RAS}$ cycling@tRC =min.) | KMCJ532512 - 6 | $I_{CC3}$ | - | 360 | mA |
| | KMCJ532512 - 7 | | - | 320 | mA |
| | KMCJ532512 - 8 | | | 280 | |
| FAST PAGE MODE CURRENT* ($\overline{RAS}$=$V_{IL}$, $\overline{CAS}$ cycling: tPC= min.) | KMCJ532512 - 6 | $I_{CC4}$ | - | 320 | mA |
| | KMCJ532512 - 7 | | - | 280 | mA |
| | KMCJ532512 - 8 | | | 260 | |
| STAND BY CURRENT ($\overline{RAS}$=$\overline{CAS}$=Vcc–0.2V) | | $I_{CC5}$ | - | 0.8 | mA |
| CAS-BEFORE-RAS REFRESH CURRENT* ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.) | KMCJ532512 - 6 | $I_{CC6}$ | - | 360 | mA |
| | KMCJ532512 - 7 | | - | 320 | mA |
| | KMCJ532512 - 8 | | | 280 | mA |
| BATTERY BACK UP CURRENT - only Low Power ver. ($\overline{CAS}$=$\overline{CAS}$ before $\overline{RAS}$ cycling or 0.2V, $\overline{WE}$,/A0-A9=Vcc–0.2V or 0.2V, $D_{IN}$=Vcc–0.2V or open, tRC=125us, tRAS=min. ~ 1us) | | $I_{CC7}$ | - | 1.2 | mA |
| INPUT LEAKAGE CURRENT (Any input 0 ≤ $V_{IN}$ ≤ 6.5V, all other pins not under test = 0 volts.) | $\overline{RAS}$ pin | $I_{IL}$ | -20 | 20 | uA |
| | else $\overline{RAS}$ pin | | -1 | 1 | |
| OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ $V_{OUT}$ ≤ 5.5V) | | $I_{OL}$ | -10 | 10 | uA |
| OUTPUT HIGH VOLTAGE LEVEL($I_{OH}$ = -5mA) | | $V_{OH}$ | 2.4 | - | V |
| OUTPUT LOW VOLTAGE LEVEL($I_{OL}$ = 4.2mA) | | $V_{OL}$ | - | 0.4 | V |

* NOTE : $I_{CC1}$, $I_{CC3}$, $I_{CC4}$ and $I_{CC6}$ are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current.

**CAPACITANCE** (T = 25 °C)

| Item | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input capacitance : A0-A9 | $C_{IN1}$ | - | 15 | pF |
| Input capacitance : $\overline{WE}$ | $C_{IN2}$ | - | 15 | pF |
| Input capacitance . $\overline{RAS0}$, $\overline{RAS2}$ | $C_{IN3}$ | - | 30 | pF |
| Input capacitance : $\overline{CAS0}$-$\overline{CAS3}$ | $C_{IN4}$ | - | 15 | pF |
| Input/Output capacitance : DQ0-DQ31 | $C_{DQ1}$ | - | 10 | pF |

**AC CHARACTERISTICS** (0°C≤Ta≤55°C, Vcc=5.0V±5%. See notes 1,2.)

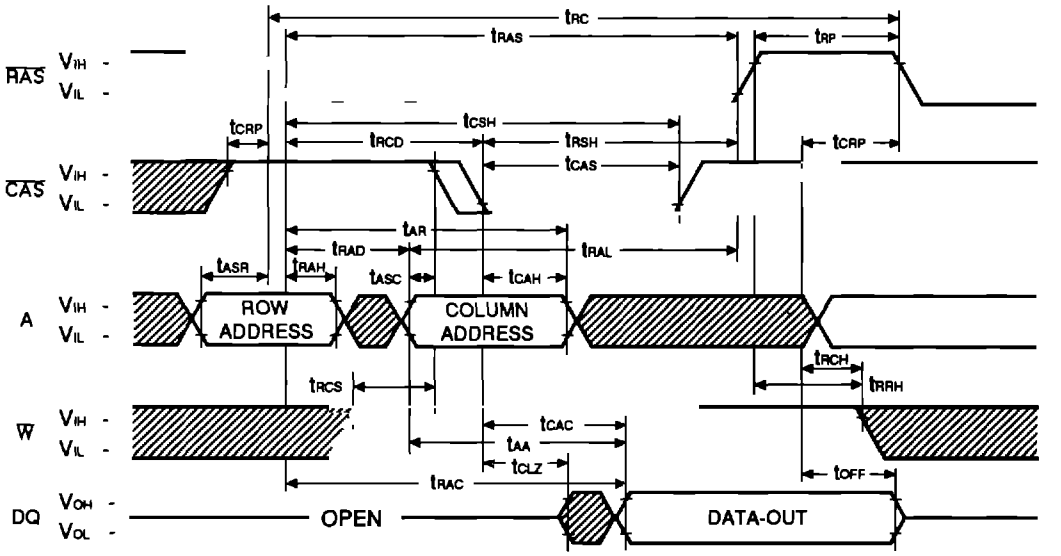
| STANDARD OPERATION | Symbol | KMCJ532512-6 | | KMCJ532512-7 | | KMCJ532512-8 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Random read or write cycle time | tRC | 120 | | 140 | | 160 | | ns | |
| Access time from $\overline{RAS}$ | tRAC | | 60 | | 70 | | 80 | ns | 3,4 |
| Access time from $\overline{CAS}$ | tCAC | | 22 | | 27 | | 27 | ns | 3,4,5 |
| Access time from column address | tAA | | 37 | | 42 | | 47 | ns | 3,11 |
| $\overline{CAS}$ to output in Low-Z | tCLZ | 0 | | 0 | | 0 | | ns | 3 |
| Output buffer turn-off delay | tOFF | 0 | 22 | 0 | 27 | 0 | 27 | ns | 7 |
| Transition time (rise and fall) | tT | 3 | 50 | 3 | 50 | 3 | 50 | ns | 2 |
| $\overline{RAS}$ precharge time | tRP | 40 | | 50 | | 60 | | ns | |
| $\overline{RAS}$ pulse width | tRAS | 60 | 10,000 | 70 | 10,000 | 80 | 10,000 | ns | |
| $\overline{RAS}$ hold time | tRSH | 22 | | 27 | | 27 | | ns | |
| $\overline{CAS}$ hold time | tCSH | 60 | | 70 | | 80 | | ns | |
| $\overline{CAS}$ pulse width | tCAS | 22 | 10,000 | 27 | 10,000 | 27 | 10,000 | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | tRCD | 18 | 38 | 18 | 43 | 20 | 53 | ns | 4 |
| $\overline{RAS}$ to column address delay time | tRAD | 13 | 23 | 13 | 28 | 13 | 33 | ns | 11 |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | tCRP | 17 | | 17 | | 17 | | ns | |
| Row address set-up time | tASR | 7 | | 7 | | 7 | | ns | |
| Row address hold time | tRAH | 8 | | 8 | | 13 | | ns | |
| Column address set-up time | tASC | 2 | | 2 | | 2 | | ns | |
| Column address hold time | tCAH | 22 | | 22 | | 22 | | ns | |
| Column address hold referenced to $\overline{RAS}$ | tAR | 50 | | 55 | | 60 | | ns | 6 |
| Column Address to $\overline{RAS}$ lead time | tRAL | 37 | | 42 | | 47 | | ns | |
| Read command set-up time | tRCS | 2 | | 2 | | 2 | | ns | |
| Read command hold referenced to $\overline{CAS}$ | tRCH | 2 | | 2 | | 2 | | ns | 9 |
| Read command hold referenced to $\overline{RAS}$ | tRRH | 2 | | 2 | | 2 | | ns | 9 |
| Write command hold time | tWCH | 10 | | 15 | | 15 | | ns | |
| Write command hold referenced to $\overline{RAS}$ | tWCR | 45 | | 55 | | 60 | | ns | 6 |
| Write command pulse width | tWP | 10 | | 15 | | 15 | | ns | |
| Write command to $\overline{RAS}$ lead time | tRWL | 22 | | 27 | | 27 | | ns | |
| Write command to $\overline{CAS}$ lead time | tCWL | 15 | | 20 | | 20 | | ns | |
| Data-in set-up time | tDS | 2 | | 2 | | 2 | | ns | 10 |
| Data-in hold time | tDH | 22 | | 22 | | 22 | | ns | 10 |
| Data-in hold referenced to $\overline{RAS}$ | tDHR | 50 | | 55 | | 60 | | ns | 6 |
| Refresh period | tREF | | 128 | | 128 | | 128 | ms | |
| Write command set-up time | tWCS | 2 | | 2 | | 2 | | ns | 8 |
| $\overline{CAS}$ setup time (C-B-R refresh) | tCSR | 17 | | 17 | | 17 | | ns | |
| $\overline{CAS}$ hold time (C-B-R refresh) | tCHR | 17 | | 17 | | 17 | | ns | |
| $\overline{RAS}$ precharge to $\overline{CAS}$ hold time | tRPC | 22 | | 22 | | 22 | | ns | |
| Access time from $\overline{CAS}$ precharge | tCPA | | 42 | | 47 | | 52 | ns | 3 |
| Fast Page mode cycle time | tPC | 47 | | 52 | | 57 | | ns | |
| $\overline{CAS}$ precharge time (Fast page) | tCP | 10 | | 10 | | 10 | | ns | |
| $\overline{RAS}$ pulse width (Fast page ) | tRASP | 60 | 100K | 70 | 100K | 80 | 100K | ns | |
| $\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh) | tWRP | 10 | | 10 | | 10 | | ns | |
| $\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh) | tWRH | 10 | | 10 | | 10 | | ns | |
| $\overline{CAS}$ precharge(C-B-R counter test) | tCPT | 20 | | 25 | | 30 | | ns | |

**NOTES**

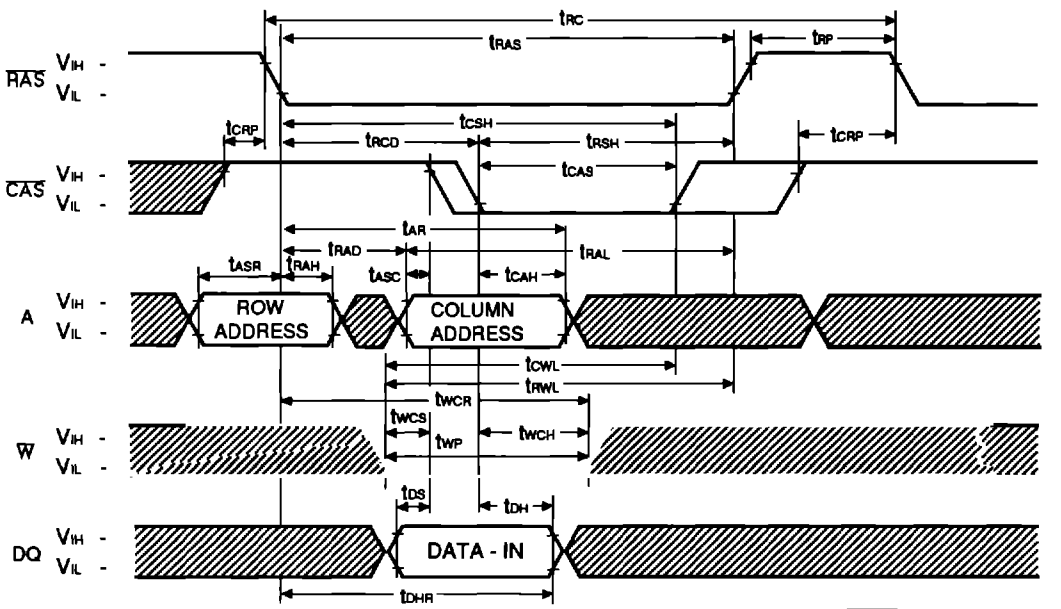
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD ≥ tRCD(max).
6. tAR, tWCR, tDHR are referenced to tRAD(MAX)
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenc -ed to VOH or VOL.
8. tWCS is non restrictive operating parameter. It included in the data sheet as electrical characteristic only. If tWCS≥tWCS(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
11. Operation within the tRAD(max) limit insures that tRAC (max) can be met. tRAD(max) is specified as reference point only. If tRAD is greater than the specified tRAD (max) limit, then access time is controlled by tAA.

## TIMING DIAGRAM

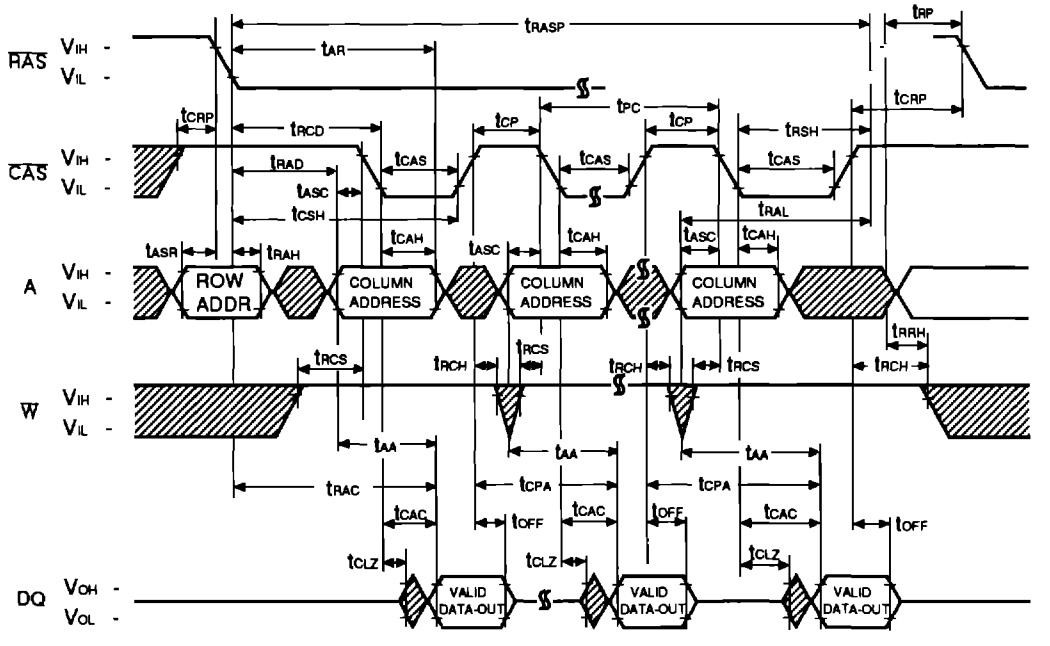
### READ CYCLE



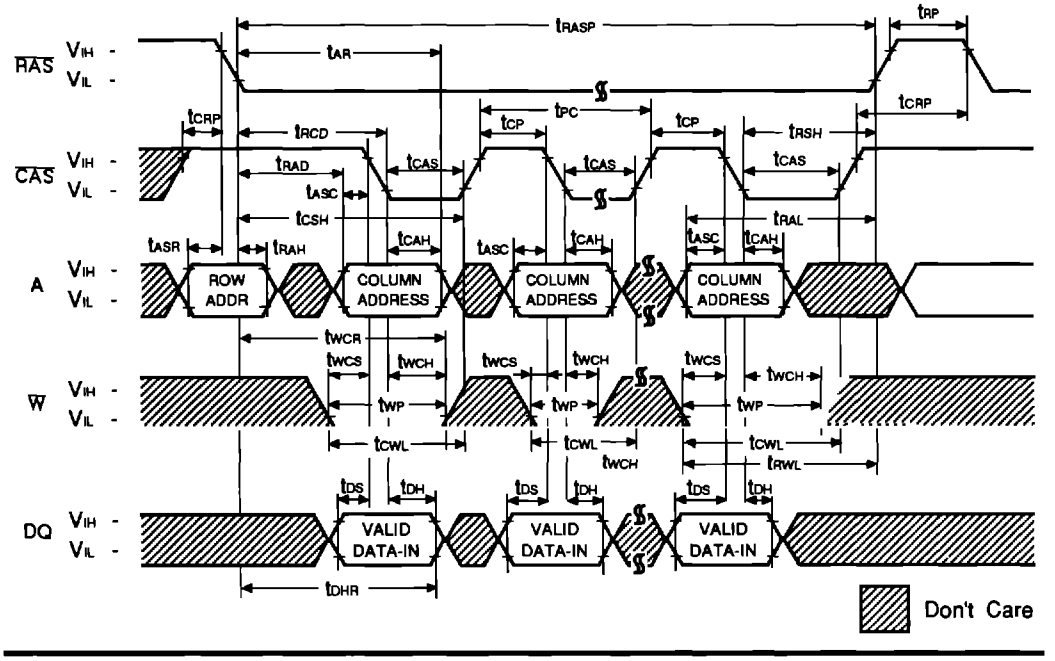

### WRITE CYCLE (EARLY WRITE)



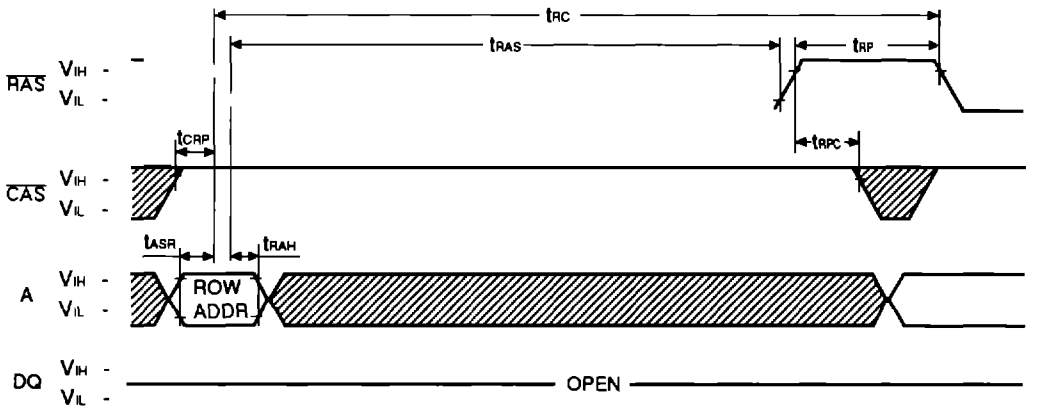
## FAST PAGE MODE READ CYCLE




## FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

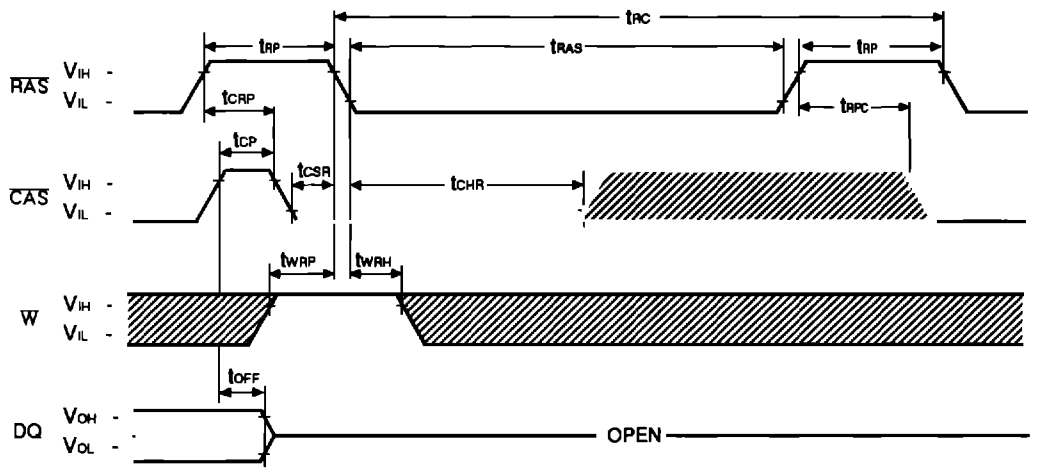


### $\overline{RAS}$-ONLY REFRESH CYCLE




NOTE : $\overline{W}$ = Don't care

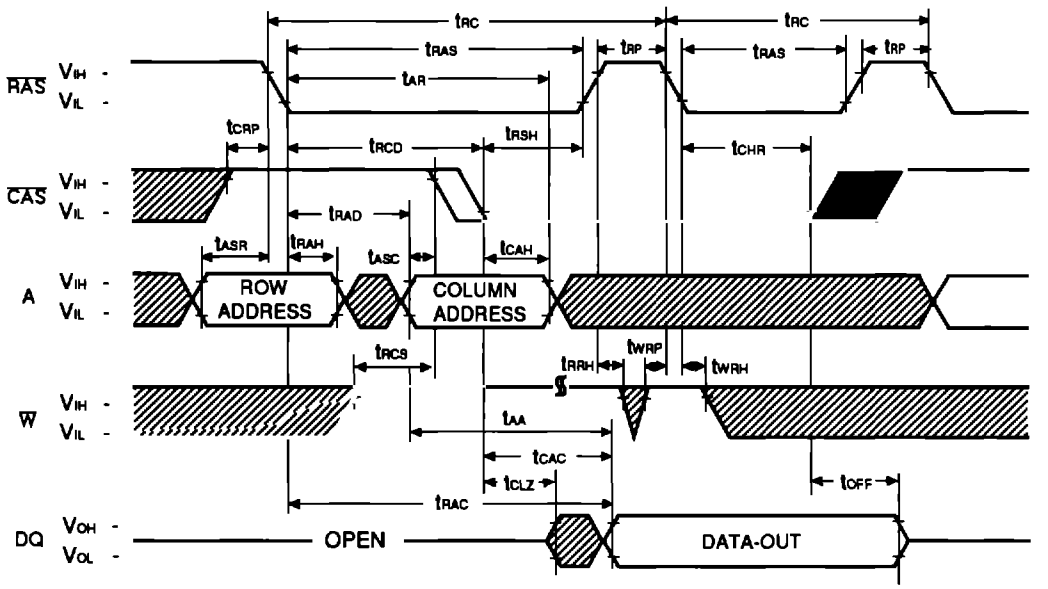
### $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



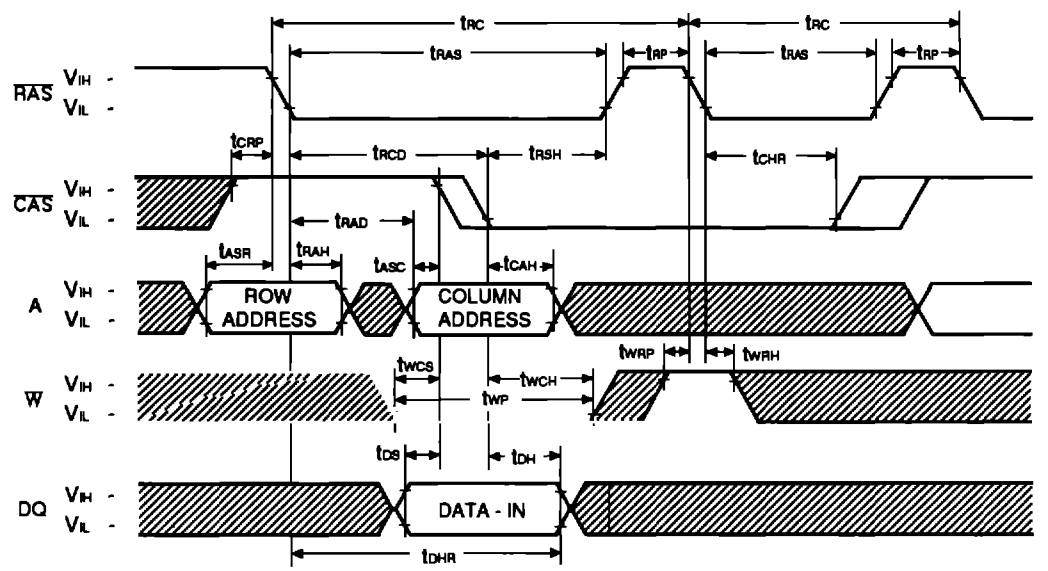

NOTE : A = Don't Care

Don't Care

### HIDDEN REFRESH CYCLE (READ)

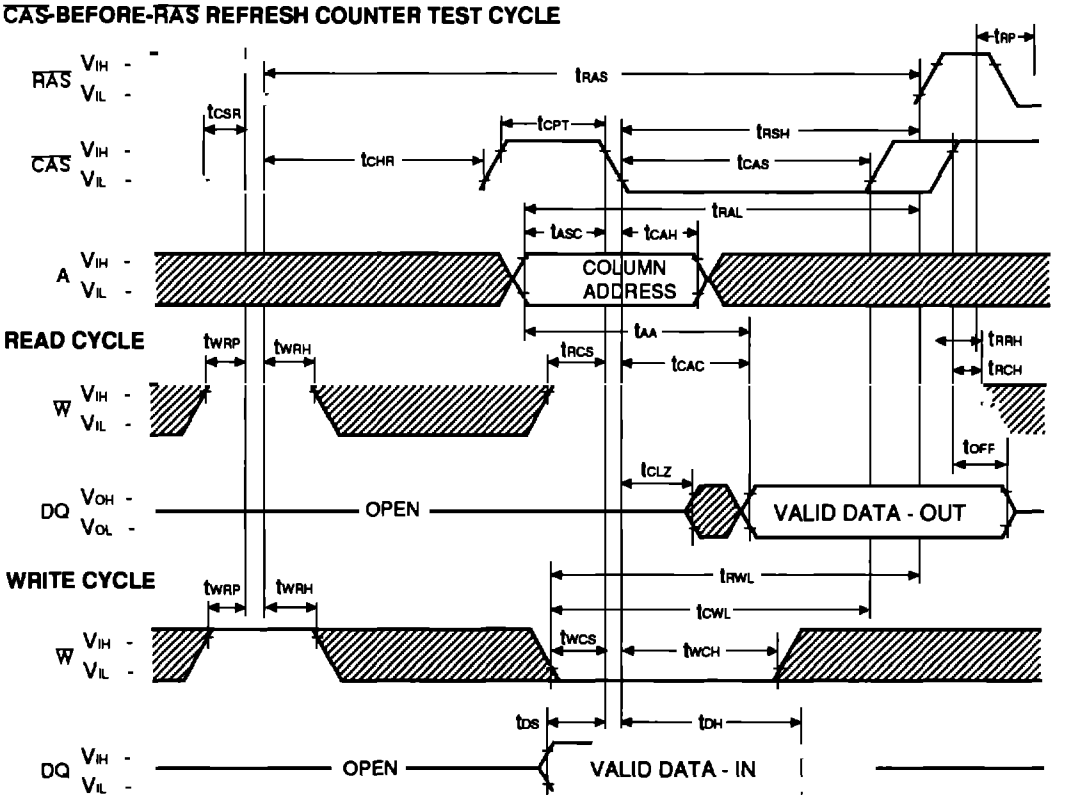



### HIDDEN REFRESH CYCLE (WRITE )




Don't Care

## CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



**PACKAGE DIMENSIONS**