FAST CMOS
8-INPUT UNIVERSAL
SHIFT REGISTER

IDT74FCT299T/AT/CT

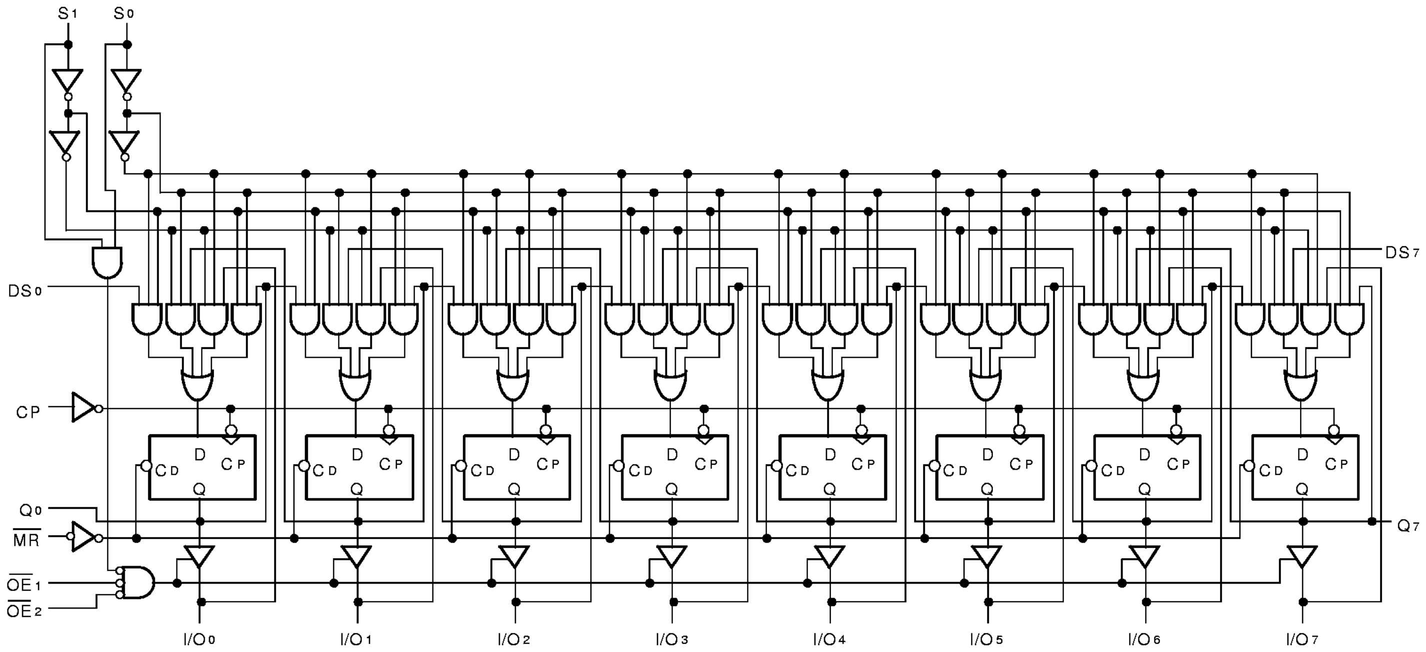
FEATURES:

- Std., A and C speed grades
- Low input and output leakage ≤1µA (max.)
- Extended commercial range of –40°C to +85°C
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- Power off disable outputs permit "live insertion"
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Available in PDIP, SOIC, and QSOP packages

DESCRIPTION:

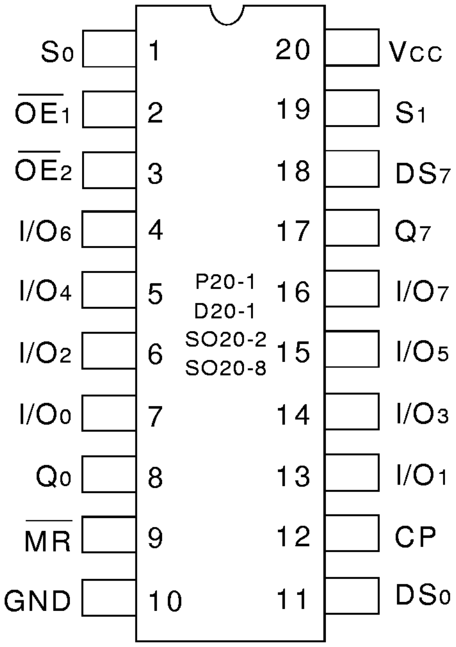
The IDT74FCT299T/AT/CT are built using an advanced dual metal CMOS technology. The IDT74FCT299T/AT/CT are 8-input universal shift/storage registers with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. A separate active low Master Reset is used to reset the register.

FUNCTIONAL BLOCK DIAGRAM



© 1999 Integrated Device Technology, Inc.

PIN CONFIGURATION



PDIP/ SOIC/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Max.	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–65 to +120	mA

8T-link

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

8T-link

NOTE:

1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
CP	Clock Pulse Input (Active Edge Rising)
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)
I/O_0–I/O_7	Parallel Data Inputs or 3-State Parallel Outputs
O_0, O_7	Serial Outputs

FUNCTION TABLE[1]

Inputs				Response
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset Q_0–Q_7 = LOW
H	H	H	↑	Parallel Load; $I/O_n \to Q_n$
H	L	H	↑	Shift Right; $DS_0 \to Q_0$, $Q_0 \to Q_1$, etc.
H	H	L	↑	Shift Left; $DS_7 \to Q_7$, $Q_7 \to Q_6$, etc.
H	L	L	X	Hold

NOTE:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH clock transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current(4)	V_{CC} = Max., V_I = 2.7V		—	—	±1	µA
I_{IL}	Input LOW Current(4)	V_{CC} = Max., V_I = 0.5V		—	—	±1	µA
I_I	Input HIGH Current(4)	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.,(3) V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –8mA	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15mA	2	3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	—	0.3	0.5	V
I_{OFF}	Input/Output Power Off Leakage(5)	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.01	1	mA

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = -55°C.
5. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V(3)		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current (4)	V_{CC} = Max. Outputs Open $\overline{OE}_1$ = $\overline{OE}_2$ = GND $\overline{MR}$ = V_{CC} S_0 = S_1 = V_{CC} DS_0 = DS_1 = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/MHz
I_C	Total Power Supply Current (6)	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}_1$ = $\overline{OE}_2$ = GND $\overline{MR}$ = V_{CC} S_0 = S_1 = V_{CC} DS_0 = DS_7 = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	3.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2	5.5	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}_1$ = $\overline{OE}_2$ = GND $\overline{MR}$ = V_{CC} S_0 = S_1 = V_{CC} DS_0 = DS_7 = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	7.3(5)	
			V_{IN} = 3.4V V_{IN} = GND	—	6	16.3(5)	

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

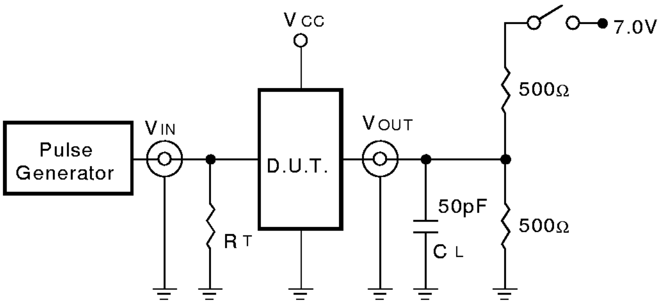
			IDT74FCT299T		IDT74FCT299AT		IDT74FCT299CT		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7	C_L = 50pF R_L = 500Ω	2	10	2	7.2	2	6.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n		2	12	2	7.2	2	6.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7		2	10	2	7.2	2	6.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n		2	15	2	8.7	2	6.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}_n$ to I/O_n		1.5	11	1.5	6.5	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}_n$ to I/O_n		1.5	7	1.5	6	1.5	6	ns
t_{SU}	Set-up Time HIGH or LOW S_0 or S_1 to CP		7.5	—	3.5	—	3.5	—	ns
t_{SU}	Set-up Time HIGH or LOW I/O_n, DS_0 or DS_7 to CP		5.5	—	4	—	4	—	ns
t_H	Hold Time HIGH or LOW S_0 or S_1 to CP		1	—	1	—	1	—	ns
t_H	Hold Time HIGH or LOW I/O_n, DS_0 or DS_7 to CP		1.5	—	1.5	—	1.5	—	ns
t_W	CP Pulse Width HIGH or LOW		7	—	7	—	5	—	ns
t_W	$\overline{MR}$ Pulse Width LOW		7	—	7	—	5	—	ns
t_{REM}	Recovery Time		7	—	7	—	5	—	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum units are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



Octal link

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

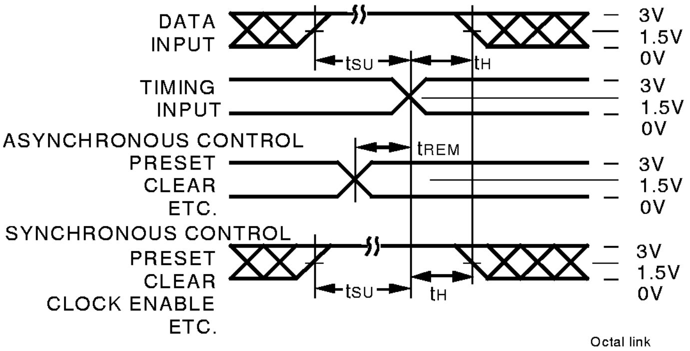
8-link

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

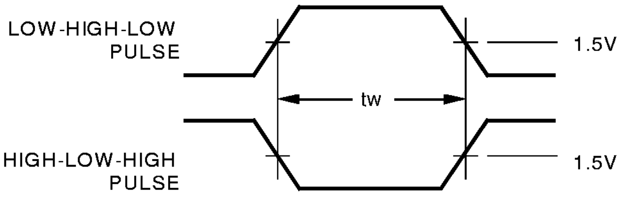
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD, AND RELEASE TIMES



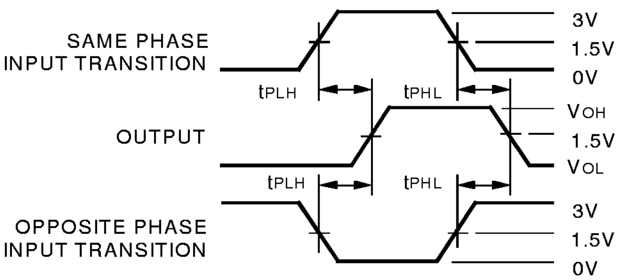
Octal link

PULSE WIDTH



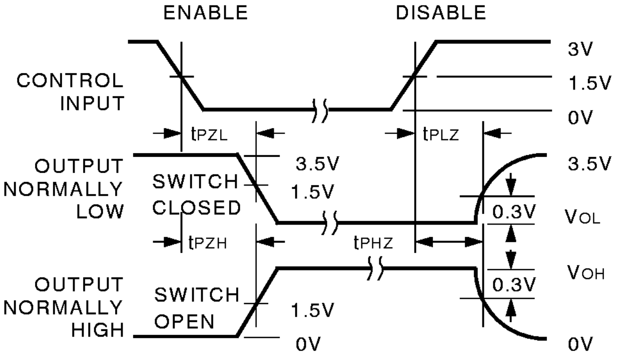
Octal link

PROPAGATION DELAY



Octal link

ENABLE AND DISABLE TIMES



Octal link

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $t_F \leq 2.5ns$; $t_R \leq 2.5ns$

ORDERING INFORMATION

IDT __XX__ FCT __X__ __XXXX__ __X__ __X__

Temperature Range	Family	Device Type	Package	Process
XX	X	XXXX	X	X

Process

Blank	Commercial

Package

P	Plastic DIP (P20-1)
D	CERDIP (D20-1)
SO	Small Outline IC (SO20-2)
Q	Quarter-size Small Outline Package (SO20-8)

Device Type

299T 299AT 299CT	8-Input Universal Shift Register

Family

Blank	High Drive

Temperature Range

74	- 40°C to +85°C

IDT

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com*

**To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.*

The IDT logo is a registered trademark of Integrated Device Technology, Inc.