010654

Am2600/9600/9601

Retriggerable Monostable Multivibrators

Distinctive Characteristics:

- Retriggerable 0 to 100% duty cycle.
- 50ns to ∞ output pulse width range.
- Am2600 guaranteed pulse width change of less than 1% over 0°C to +75°C temperature range.
- 100% reliability assurance testing including high temperature bake, temperature cycling, centrifuge and package hermeticity testing in compliance with MIL-STD-883.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.
- Mixing privileges for obtaining price discounts. Refer to price list.

FUNCTIONAL DESCRIPTION

The Am2600, Am9600 and Am9601 are DC-level sensitive retriggerable monostable multivibrators which provide an output pulse whose duration and accuracy depend on external timing components.

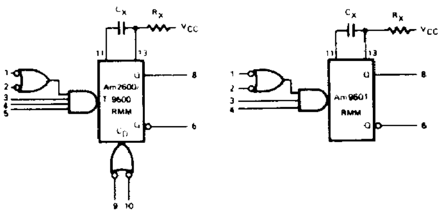
Provision is made for triggering on the rising or falling edge of an input signal. All inputs are DC coupled making triggering independent of input rise and fall times. Each time the output of the logic network at the trigger input goes from a FALSE (LOW) condition to a TRUE (HIGH) condition triggering occurs independent of the state of the monostable.

The AM 2600 and 9600 are the equivalent of the 9601 with an additional active HIGH input and an active LOW reset facility. When a $\overline{C}_D$ input on the Am 2600 or 9600 goes LOW the multivibrator resets independent of its present state or input conditions.

The Am2600 is a selected Am9600 with a guaranteed pulse width change of less than 1% over the temperature range 0°C to +75°C.

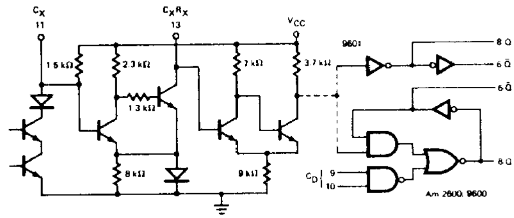
LOGIC DIAGRAMS

Am2600/9600 — Am9601



V_{CC} = Pin 14
Gnd = Pin 7

INTERNAL TIMING CIRCUITRY

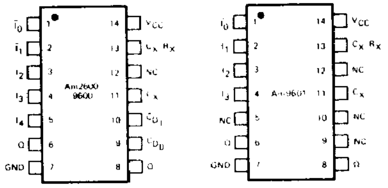


ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am2600	Molded DIP	0°C to +75°C	AM260059B
Am2600	Hermetic DIP	0°C to +75°C	AM260059F
Am2600	Hermetic DIP	−55°C to +125°C	AM260051F
Am2600	Hermetic Flat Pak	−55°C to +125°C	AM260051M
Am2600	Dice	Note	AM2600XXD
Am9600	Molded DIP	0°C to +75°C	U6E960059X
Am9600	Hermetic DIP	0°C to +75°C	U6A960059X
Am9600	Hermetic DIP	−55°C to +125°C	U6A960051X
Am9600	Hermetic Flat Pak	−55°C to +125°C	U3I960051X
Am9600	Dice	Note	UXX9600XXD
Am9601	Molded DIP	0°C to +75°C	U6E960159X
Am9601	Hermetic DIP	0°C to +75°C	U6A960159X
Am9601	Hermetic DIP	−55°C to +125°C	U6A960151X
Am9601	Hermetic Flat Pak	−55°C to +125°C	U3I960151X
Am9601	Dice	Note	UXX9601XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAMS
Top View



NC = No connection

MAXIMUM RA ; (Above which the useful life may be impaired)

Storage Temperat.	−65°C to +150°(
Temperature (Ambient) Under Bias	−55°C to +125°(
Supply Voltage to Ground Potential (Pin 14 to Pin 7) Continuous	−0.5 V to +8 \
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to $+V_{CC}$ ma:
DC Input Voltage	−0.5 V to +5.5
Output Current, Into Outputs LOW	50 m.
DC Input Current	−30 mA to +5 m.

ELECTRICAL CHARACTERISTICS

Am260059/960059X/960159X T_A = 0°C to +75°C (COM grade)
Am260061/960061X/960151X T_A = −55°C to +125°C (MIL grade)

Parameters	Operating Range	Test Conditions	LIMITS T_A = MIN Min	T_A = MIN Max	T_A = +25°C Min	T_A = +25°C Typ	T_A = +25°C Max	T_A = MAX Min	T_A = MAX Max	Units
V_{OH} Output HIGH Voltage	MIL or COM	V_{CC} = MIN., I_{OH} = −0.96 mA	2.40		2.40	3.6		2.40		Volts
V_{OL} Output LOW Voltage	MIL	I_{OL} = 8 x I_{IL} MAX.		0.40		0.2	0.40		0.40	Volts
	COM	I_{OL} = 8 x I_{IL} MAX.		0.45		0.2	0.45		0.45	
V_{IH} Input HIGH Voltage	MIL		2.00		1.70			1.50		Volts
	COM		1.90		1.80			1.60		
V_{IL} Input LOW Voltage	MIL			0.85			0.90		0.85	Volts
	COM			0.85			0.85		0.85	
I_{IL} Input Load Current	MIL	V_{IN} = 0.40 V, V_{CC} = MAX.		−1.60		−1.10	−1.60		−1.60	mA
		V_{IN} = 0.40 V, V_{CC} = MIN.		−1.24		−0.97	−1.24		−1.24	
	COM	V_{IN} = 0.45 V, V_{CC} = MAX.		−1.60		−1.00	−1.60		−1.60	
		V_{IN} = 0.45 V, V_{CC} = MIN.		−1.41		−0.90	−1.41		−1.41	
I_{IH} Reverse Input Current	MIL or COM	V_{CC} = MAX., V_{IN} = 4.5 V		60		2	60		60	μA
I_{SC} Short Circuit Current	MIL	V_{CC} = 5.0 V, V_O = 1.0 V − 9600, 2600			−10		−25			mA
	COM	V_O = 0.0V − 9601			−10		−35			
I_{PD} Power Supply Current	2600 9600 MIL	V_{CC} = 5.0 V R_X = 10 kΩ		24		19	24		24	mA
	2600 9600 COM	V_{CC} = 5.0 V R_X = 10 kΩ		26		19	26		26	
	9601	V_{CC} = MAX. GND Pin 11 R_X = 10 kΩ		25		19	25		25	

Switching Characteristics (T_A = 25°C unless otherwise specified)

Parameters			Test Conditions	Am 2600/9601 Min	Am 2600/9601 Typ	Am 2600/9601 Max	Am9600 Min	Am9600 Typ	Am9600 Max	Units
t_{pd+}	Turn Off Delay Negative Trigger Input to True Output		V_{CC} = 5.0 V, C_L = 15 pF R_X = 5 kΩ, C_X = 0 pF		25	40		27	45	ns
t_{pd-}	Turn On Delay Negative Trigger Input to False Output				25	40		27	40	ns
$t_{pw(min)}$	Minimum Output Pulse Width	True (Q) Output	V_{CC} = 5.0 V, C_L = 15 pF R_X = 5 kΩ, C_X = 0 pF		45	65		50	70	ns
		False ($\bar{Q}$) Output			55	75		60	80	
t_{pw}	Output Pulse Width Variation	Mil	V_{CC} = 5.0 V, C_L = 15 pF R_X = 10 kΩ, C_X = 1000 pF	3.08	3.42	3.76	3.20	3.42	3.76	μs
		Com		3.08	3.42	3.76	3.08	3.42	3.76	
C_{STRAY}	Maximum Allowable Wiring Capacitance to Ground		Pin 13 = GND			50			50	pF
R_X	Timing Resistor over temperature range (Note 5)			5		50	5		50	kΩ
t_{pd-} ($\bar{C}_D$)	Delay from $\bar{C}_D$ to Q output LOW				11	17		11	17	ns

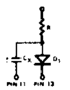
Am 2600		Test Conditions	Min	Typ	Max	Units
$\Delta t_{pw}(T)$	Maximum Output Pulse Width Percentage Change over temperature range 0°C to +75°C	V_{CC} = 5.0 V, C_L = 15 pF R_X = 10 kΩ, C_X = 1000 pF		0.5	1.0	%

Note 1. Maximum current defined by DC Input Voltage.
2. Pulse tested.
3. Unless otherwise noted, tests are conducted with a 10 kΩ resistor from V_{CC} to Pin 13 (R_X).
4. Limit for −55°C to +125°C operation is 25 kΩ.

OPERATION RULES

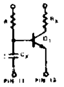
1. An external resistor R_X and an external capacitor C_X are required as shown in the logic diagram. The values of R_X may vary from 5.0 kΩ to 50 kΩ for 0°C to +75°C operation and 5.0 kΩ to 25 kΩ for −55°C to +125°C operation. C_X may vary from 0 to any value necessary and obtainable.
2. If a fixed value of R_X is used, the following values are recommended: R_X = 30 kΩ for 0°C to +75°C operation; R_X = 10 kΩ for −55°C to +125°C operation.
3. The output pulse width T is defined as follows:

   $T = 0.32 R_X C_X [1 + \frac{0.7}{R_X}]$ (For C_X greater than 10^3 pF) Where: R_X is in kΩ, C_X is in pF, T is in ns. For $C_X < 10^3$ pF see Fig. 12.
4. If electrolytic type capacitors are to be used, it is recommended that they have low leakage. For capacitors with a high reverse leakage the following circuits can be used:



$R < 0.6 R_X$ (Max)

D_1: any silicon type diode, such as FD700



This circuit also allows larger value of R to be used for longer output pulse width.

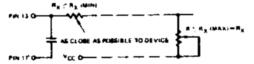
$R \leq R_X (0.7)(h_{FE}Q)$

R_X (min) ≤ R_X ≤ R_X (max)

Q Any NPN silicon device with sufficient h_{FE} at low currents, such as 2N2511

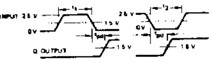
   Both circuits prevent reverse voltage across C_X. The pulse width T for the circuits is defined as follows.

   $T \approx 0.30 RC_X [1 + \frac{0.7}{R}]$ Where: R is in kΩ, C_X is in pF, T is in ns.
5. To obtain variable pulse width, by remote trimming, the following circuit is recommended:

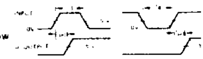


6. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
7. Input Trigger Pulse Rules. $t_1, t_2, t_3, t_4 > 40$ ns

   Input to Pin 1
   Pins 2, (1), 4 & 5 = High



   Input to Pin 3 (4)(5)
   Pin 4 (3) (5) = High Pins 1 or 2 = Low



8. The retriggerable pulse width is calculated as shown below:

   $t_w = t_{pw} + t_{pd+} = 0.32 R_X C_X (1 + \frac{0.7}{R_X}) + t_{pd+}$

   The retrigger pulse width is equal to the pulse width t_{pw} plus a delay time. For pulse widths greater than 500 ns, t_w can be approximated as t_{pw}.

   NOTE: Retriggering will not occur if the retrigger pulse comes within $0.32 R_X C_X (\frac{0.7}{R_X})$ ns after the initial trigger pulse.
9. Reset Operation — The Am 2600/9600 have an active LOW reset facility. By applying a low to either reset input, any timing cycle can be terminated or any new cycle inhibited until the low reset input is removed. Trigger inputs will not produce spikes in the output when a reset is held low.

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS:

$\overline{CD}_0$, $\overline{CD}_1$ The asychronous direct clear inputs of the 9600. A LOW on either of these inputs will reset the monostable independent of other conditions.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

$\overline{I}_0$, $\overline{I}_1$ The active LOW inputs of the Am 2600/9600/9601. With all other inputs HIGH a HIGH to LOW transition on either of these inputs will cause triggering.

I_2, I_3, I_4 The active HIGH inputs of the Am 2600/9600/9601 with either $\overline{I}_0$ or $\overline{I}_1$ inputs LOW a LOW to HIGH transition on any input I_2, I_3, I_4 with the remaining inputs HIGH will cause triggering.

Input Unit Load One T²L gate input load. In the HIGH state it is equal to I_R and in the LOW state it is equal to I_F.

Q The TRUE output of the monostable.

$\overline{Q}$ The FALSE output of the monostable.

Triggering The switching of the monostable from the stable state to the unstable state and start of the timing cycle.

SWITCHING TERMS:

t_{pd+} The propagation delay from a HIGH to LOW transition on $\overline{I}_0$ or $\overline{I}_1$ to the TRUE (Q) output LOW to HIGH transition.

t_{pd-} The propagation delay from a HIGH to LOW transition on $\overline{I}_0$ or $\overline{I}_1$ to the FALSE ($\overline{Q}$) output HIGH to LOW transition.

$t_{pw(min)}$ The minimum TRUE (Q) output pulse width with C_X = 0 pF, R_X = 5 kΩ.

Δt_{pw} The output pulse width variation with C_X=1000 pF, R_X=10 kΩ.

Δt_{pw} (T) The Am 2600 maximum pulse width percentage change over the temperature range 0°C to +75°C of the TRUE (Q) output from the pulse width at 25°C.

OPERATIONAL TERMS:

I_{IL} Forward input load current, for unit input load.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{IH} Reverse input load current with V_R applied to input.

I_{SC} Output current when output set to V_{OH} condition but forced low.

Negative Current Current flowing out of the device.

P_{DISS} The power dissipated within the circuit with input and output terminals open.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage. Refer to figure 14.

V_{IL} Maximum logic LOW input voltage. Refer to figure 14.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

PERFORMANCE CURVES

Input C[illegible]eristics

Input Load Current Versus Input Voltage

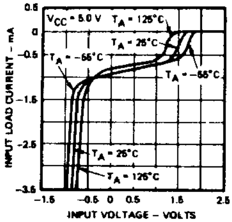


Figure 1

Input Leakage Current Versus Input Voltage

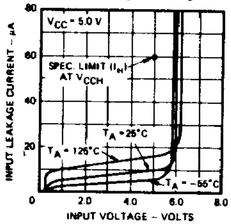


Figure 2

Power Dissipation

Power Dissipation Versus Ambient Temperature

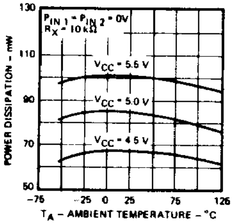


Figure 3

Output Characteristics

Output Current Versus Output Voltage (High State)

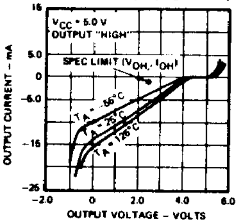


Figure 4

Output Current Versus Output Voltage (Low State)

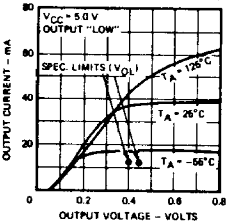


Figure 5

Switching Characteristics

Typical Negative Trigger Delay Time Versus Ambient Temperature

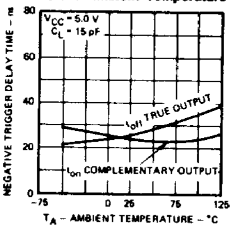


Figure 6

Pulse Width Characteristics

Normalized Output Pulse Width Versus Ambient Temperature

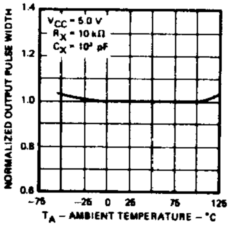


Figure 7

Normalized Output Pulse Width Versus Supply Voltage

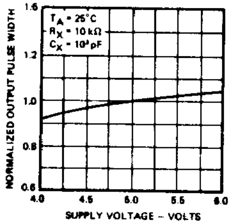


Figure 8

Normalized Output Pulse Width Versus Operating Duty Cycle

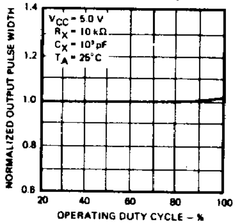


Figure 9

Pulse Width Versus Timing Resistance

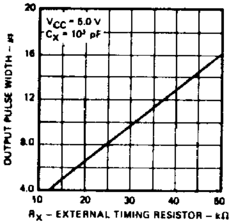


Figure 10

Typical Output Pulse Width Versus Ambient Temperature

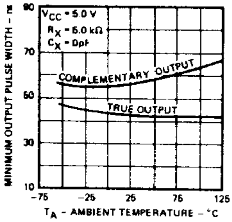


Figure 11

Output Pulse Width Versus Timing Resistance and Capacitance

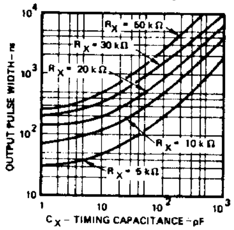


Figure 12

Am 2600 Normalized Output Pulse Width Versus Ambient Temperature

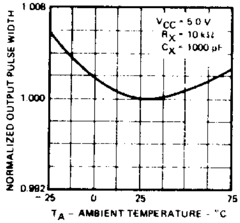


Figure 13

TRUTH TABLES
Am 2600/9600

$\overline{I}_0$	$\overline{I}_1$	I_2	I_3	I_4	$\overline{CD}_0$	$\overline{CD}_1$	OPERATION
H→L	H	H	H	H	H	H	Trigger
H	H→L	H	H	H	H	H	Trigger
L	X	L→H	H	H	H	H	Trigger
X	L	L→H	H	H	H	H	Trigger
L	X	H	L→H	H	H	H	Trigger
X	L	H	L→H	H	H	H	Trigger
L	X	H	H	L→H	H	H	Trigger
X	L	H	H	L→H	H	H	Trigger
X	X	X	X	X	L	X	Reset
X	X	X	X	X	X	L	Reset

Am9601

$\overline{I}_0$	$\overline{I}_1$	I_2	I_3	OPERATION
H→L	H	H	H	Trigger
H	H→L	H	H	Trigger
L	X	L→H	H	Trigger
X	L	L→H	H	Trigger
L	X	H	L→H	Trigger
X	L	H	L→H	Trigger

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
H→L = Transition from HIGH to LOW Voltage Level
L→H = Transition from LOW to HIGH Voltage Level

Table I

Am 2600/9600/9601 LOADING RULES

Input/Output Am 2600/9600	9601	Pin No.'s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
$\overline{I}_0$	$\overline{I}_0$	1	1		
$\overline{I}_1$	$\overline{I}_1$	2	1	—	—
I_2	I_2	3	1	—	—
I_3	I_3	4	1	—	—
I_4	NC	5	1	—	—
$\overline{Q}$	$\overline{Q}$	6	—	16	8
GND	GND	7	—	—	—
Q	Q	8		16	8
$\overline{C}_{D0}$	NC	9	1	—	—
$\overline{C}_{D1}$	NC	10	1	—	—
C_X	C_X	11	—	—	—
NC	NC	12	—	—	—
C_X R_X	C_X R_X	13	—	—	—
V_{CC}	V_{CC}	14	—	—	—

NC = No Connection

Table II

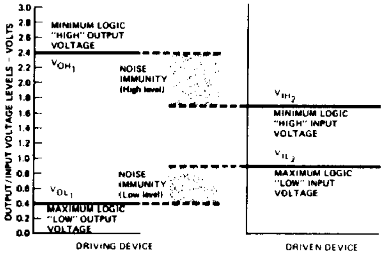
MSI INTERFACING RULES

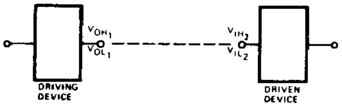
Interfacing Digital Family	Equivalent Input Unit Load HIGH	Equivalent Input Unit Load LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Table III

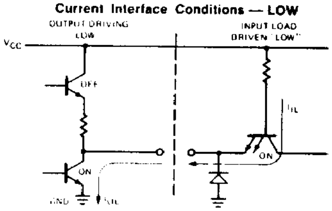
INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH





Current Interface Conditions — LOW



Current Interface Conditions — HIGH

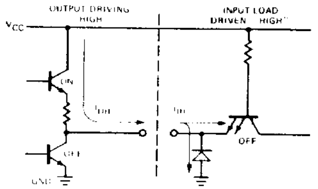
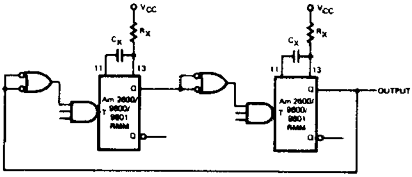


Figure 14

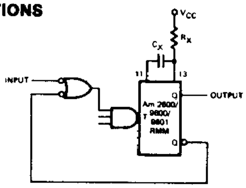
Am 2600/9600/9601 APPLICATIONS



Astable Multivibrator

Frequency of operation is dependent upon value of R_X and C_X.

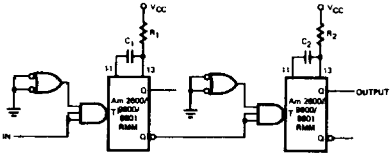
Figure 15



Frequency Division

This configuration makes the Am 2600/9600/9601 non-trigger-able and capable of frequency division.

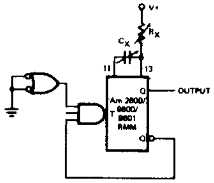
Figure 16



Delayed Pulse Generation

The first Am 2600/9600/9601 determines the time T_1 before the initiation of the output pulse. The second Am 2600/9600/9601 determines T_2, the output pulse width.

Figure 17



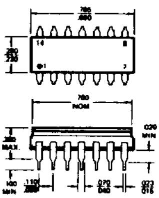
Resistance-to-Frequency Converter

The multivibrator is connected as an astable with the frequency controlled by a variable resistor or capacitor.

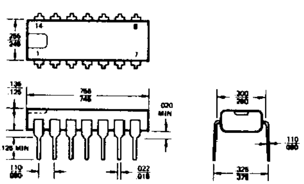
Figure 18

PHYSICAL DIMENSIONS
Dual In-Line

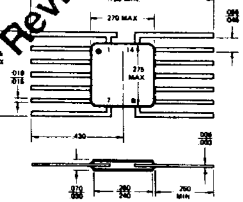
Hermetic



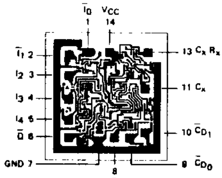
Molded



Flat Package



Metallization and Pad Layout



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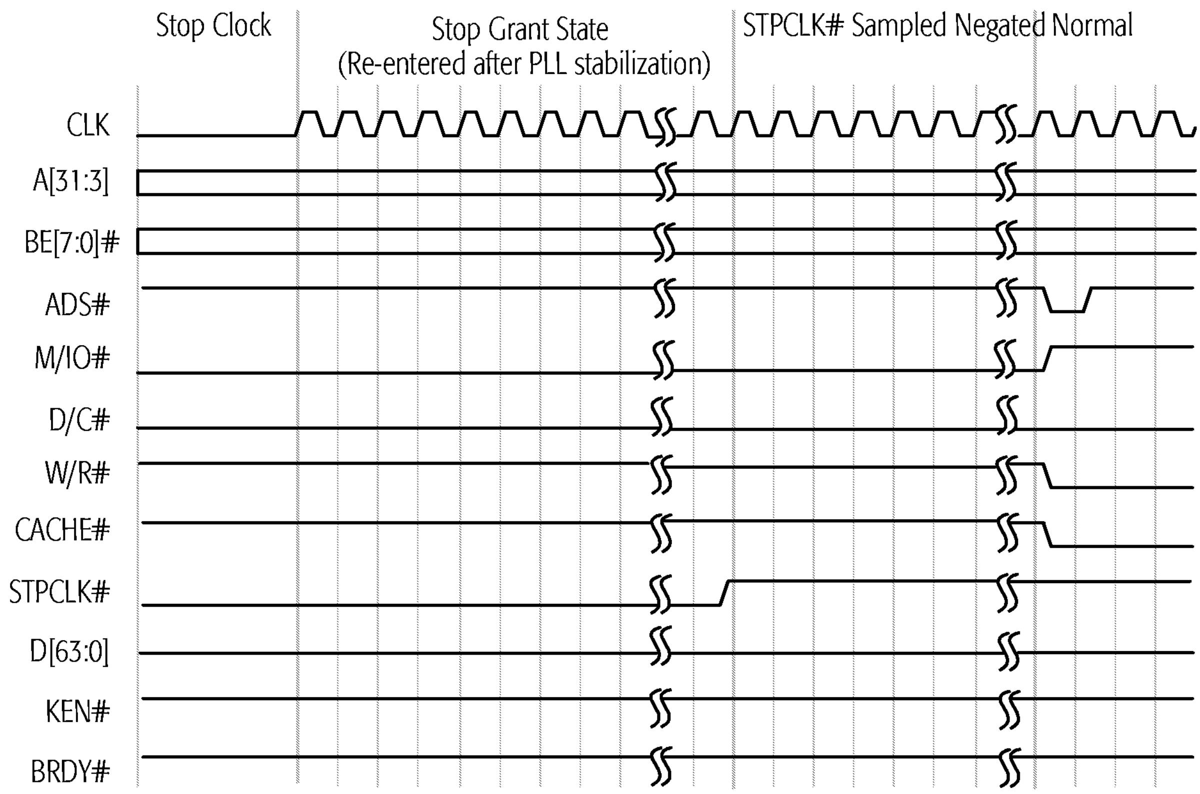

Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

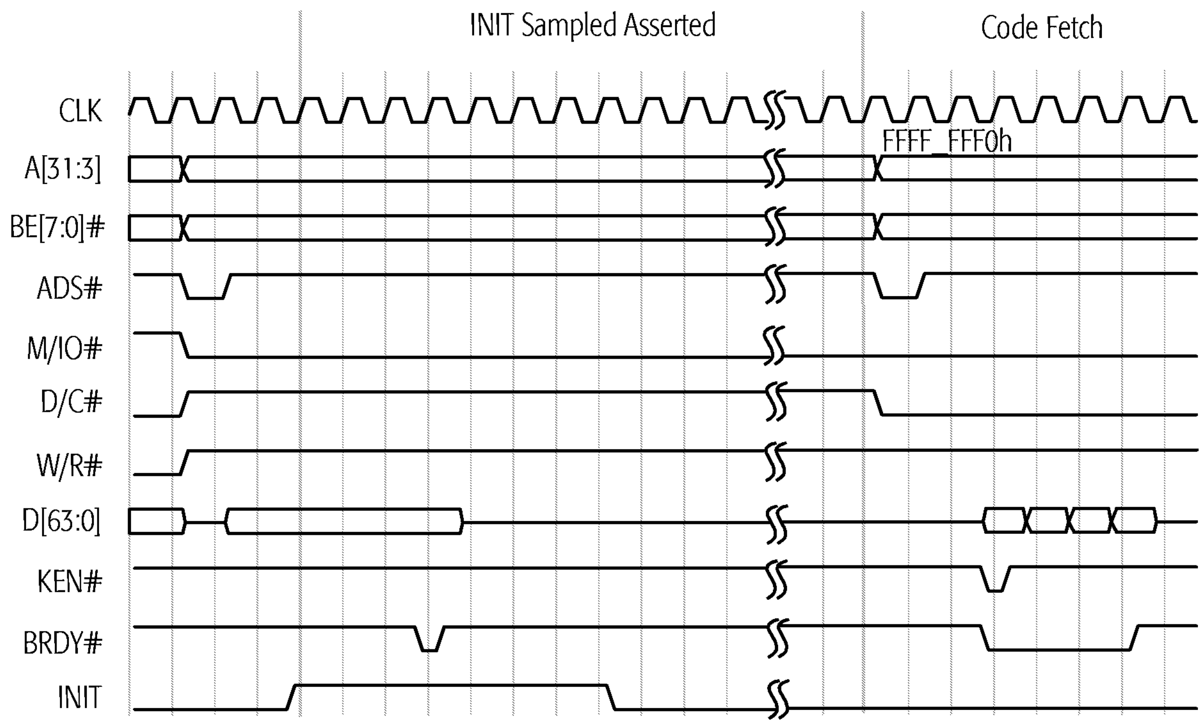

Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See "CLK Switching Characteristics" on page 255 for clock specifications. See "Electrical Data" on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.