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TC35854F

ATM Segmentation and Reassembly Chip

Applications

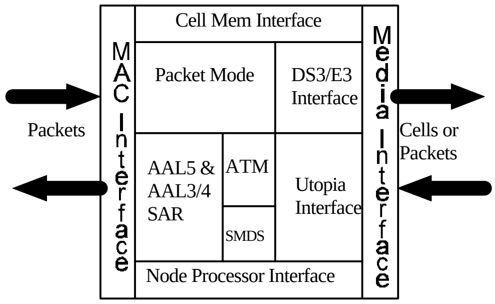
- ATM User Network Interface (UNI) or SMDS Subscriber Network Interface (SNI) on bridges, routers, and adapters

Features

- ANSI, CCITT and ATM Forum compliant ATM User Network Interface
- Explicit rate flow control ATM Forum UNI 4.0 compliant
- SMDS SIP-2 and SIP-1 (single CPE) according to TR-TSV-000772 and TR-TSV-000773
- AAL3/4 and AAL5 support
- Up to 4095 VPI/VCI circuits supported and up to 1K MIDs per VPI/VCI circuit
- Support up to 4 CBR VP tunnels
- Supports PVC and SVC connections
- Supports F4 and F5 OAM flows
- Traffic shaper supporting peak rate, sustained rate, minimum guaranteed rate, maximum burst size, and priority level
- Support MCR>0 services in ER scheme
- Quantum Flow Control support
- GFC control support
- FLOWmaster™ flow-controlled circuits
- Statistical multiplexing which allows 200% overbooking of bandwidth for VBR traffic
- UTOPIA compliant media interface.
- Full OC3 line-rate segmentation and reassembly for UTOPIA link
- 32-bit CRC generation and checking for AAL5 and SMDS packets
- Open MAC-style interface for packet transfer at 100 Mb/s and 200 Mb/s
- Two priority packet queues in MAC-style receive interface
- Motorola M68000 family style node processor interface
- 20-bit addressing, supporting 1 Megaword (64-bit word) SRAM buffer
- Packet relay mode of operation to support HDLC or Frame Relay over DS3/E3/HISSI links (using Brooktree Bt8330)

Technology

- 0.4µm CMOS, 240 pin HQFP package (175 signal pins)



Description

TC35854F has been designed for use in an ATM User Network Interface (UNI), a SMDS Subscriber Network Interface (SNI), or a general packet relay interface.

Transmit packets are sent to TC35854F on a flow-controlled, byte-wide interface that runs at 12.5 MHz or 25 MHz. Each packet contains a circuit identifier header. A packet is segmented according to the AAL type specified for that circuit and is placed on a linked-list cell queue in memory. Up to 4095 circuits are supported. The cell queues are serviced by a traffic shaper. The traffic shaper supports CBR, VBR, ABR and UBR traffic. For CBR and VBR, the traffic shaper meters out the cells on a particular circuit according to peak rate, sustained rate, minimum guaranteed rate, maximum burst size and priority. Statistical multiplexing for VBR traffic is possible, which allows up to 200% overbooking. For ABR traffic, TC35854F implements the explicit rate flow control (ER) ATM Forum UNI 4.0 compliant, the Quantum Flow Control (QFC), and Digital's FLOWmaster™ flow control. TC35854F also supports Generic Flow Control (GFC) ITU-T SG13 compliant. When used on a FLOWmaster™ link or QFC link, all ABR circuits are given equal/fair access to available bandwidth with guaranteed lossless operation. Relative priorities between CBR, VBR circuits, ABR circuits and UBR circuits are supported.

When TC35854F receives cells, synchronization is achieved through UTOPIA signaling. VPI/VCI/(MID) fields are then mapped to a local circuit identifier directly. Cells are checked, reassembled, and placed on one of two packet queues according to the priority set per circuit. AAL CRCs are also checked. The packets are then passed to the receive MAC interface, where a header is attached to identify the associated circuit.

In SMDS mode, single CPE (pt-pt) DQDB access is supported. SMDS SIP-3 32-bit CRC generation and checking can be done by TC35854F.

The packet relay mode is supported when ATM/SMDS SAR function in the chip is disabled. This allows relaying of arbitrary packet types over the attached transmission links (up to 52 Mb/s).

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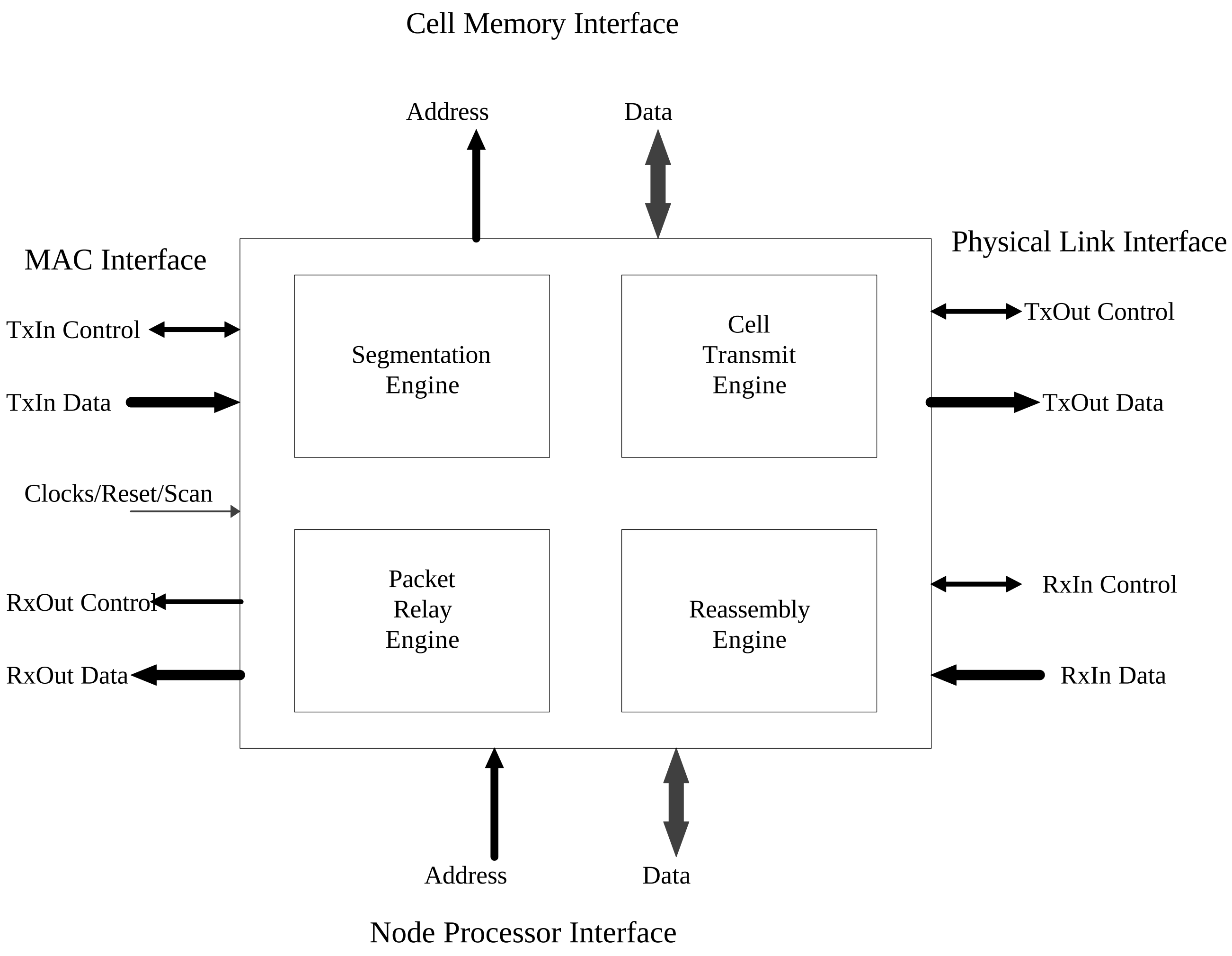
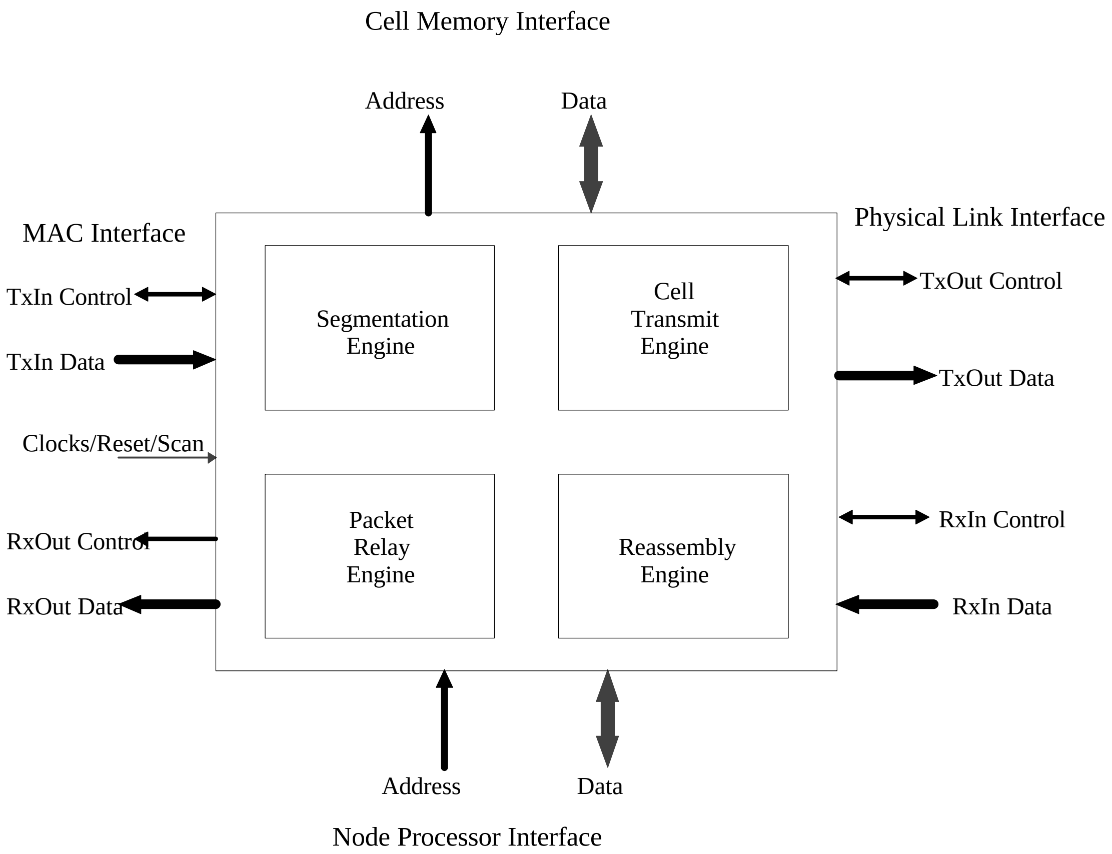


TC35854F provides the functions required to implement a variety of high-performance ATM User Network Interfaces and/or SMDS Subscriber Network Interfaces. This includes packet stream to circuit selection, ATM Adaptation Layer (AAL), segmentation and reassembly (SAR), and cyclic redundancy check (CRC) generation and checking. It contains mechanisms to support traffic shaping, varieties of ATM flow control protocols, and Operations Administration and Maintenance (OAM) flows. There are a large number of programmable options available to control and implement each of these functions. TC35854F interfaces with a variety of Physical layer chips by UTOPIA level 1.

TC35854F Interfaces



The following interfaces are used in TC35854F:

- Media Access Control (MAC) interface
- Physical link interface
- Cell memory interface
- Node processor interface

Media Access Control

Packets are sent to TC35854F for transmission on the ATM/SMDS link using a byte-wide data interface with one parity bit (TxInData) that runs at 12.5 MHz or 25 MHz. The control interface (TxIn Control) includes packet delineation and byte flow control. The flow control signal is used to hold off transmission of data during periods where no buffers are available for the data to be transmitted. The receive portion of the packet interface is also byte wide for data with one parity bit (RxOut Data), and runs at the same speed as the transmit interface. There is a separate control channel (RxOut Control), which indicates receive packet delineation and error status. There is no flow control on the receive side.

Physical Link Interface

The Physical link interface consists of a byte-wide data path for both transmit (TxOut Data) and receive (RxIn Data). In all modes, the link interface is slaved from the link clock inputs. Speed matching FIFOs are used between clock boundaries. Byte transmission/reception to/from the link is controlled by control lines. This interface is UTOPIA level 1 compliant. This interface can also connect with Brooktree Bt8330 Multimegabit HDLC formatter.

Cell Memory Interface

The cell memory interface consists of a 64-bit data bus (Cell Memory Data), with two additional parity bits and a 20-bit address bus (Cell Memory Address). Write enable and output enable signals are provided separately. A TC35854F memory word is 64 bits wide. TC35854F is capable of addressing up to 1 M word (8 MBytes) of memory. The memory read/write cycle time is 40 ns. Back-to-back reads, writes, read followed by write, and write followed by read are possible. The external memory is used for storing ATM cells that are awaiting transmission or are being reassembled, records, traffic schedules and free buffer pools. The amount of memory required depends on the number of circuits being used in a particular application. 1 MB of memory is sufficient to support 1023 circuits or 4095 circuits without rate control with some loss of performance. For 4095 circuits with full functionality, 1MB of memory will NOT work and 4MB is recommended.

Node Processor Interface

The node processor interface uses a 16-bit data and 7-bit address configuration. It uses a synchronous Motorola 68K style interface, running at 12.5 or 25 MHz. All of the chip control and status registers (CSRs) can be accessed directly through this interface. The external memory is also accessed indirectly through this interface.

Reset

TC35854F can be reset to its default initial value by applying a low signal to the reset pin for longer than four periods of the main (25 MHz) clock. TC35854F can also be reset by writing a “1” to the Reset bit of the control CSR

TC35854F Features

Transmit

Segmentation	Cell Transmit

- Supports up to 4095 VC connections
- Segments packets according to AAL3/4 and AAL5
- Generates 32-bit CRC for AAL5 packets
- Processes SMDS SIP-2
- Conducts header lookup for circuit selection based on generic format, FDDI format, and short address format.
- Inserts 32-bit FDDI CRC on a per packet basis (optional)
- Provides programmable header strip on received packets on a per VC basis
- Supports IP over AAL5 on a per circuit basis
- Converts DA and SA between canonical and FDDI bit-order formats on a per packet basis
- Provides flow control on the MAC interface
- Provides odd or even parity checking for each byte on MAC interface (including idle byte between packet) (optional)
- Supports back-to-back packet processing
- Interfaces 100 Mbit/sec and 200 Mbit/sec byte transfer rates
- Supports “cut through” segmentation
- SMDS CRC insertion on per circuit and per packet basis
- Adds 16-bit or 32-bit HDLC CRC in packet relay mode on per packet basis. CRC could be stripped too.
  Strips up to 63 bytes of packet header in packet relay mode.

- Services up to 4095 independent VC connection queues
- Uses a precomputed static schedule to establish an arbitrary peak cell rate (PCR) on a per VC basis for constant bit rate traffic for CBR and VBR traffic
- Provides minimum guaranteed bandwidth (minimum cell rate - MCR) per circuit
- Uses a token-based scheme to establish an average (sustainable) cell rate with an associated burst tolerance for VBR traffic on a per VC basis
- Assigns relative priorities to different classes of circuits
- Introduces zero cell delay variation on output cell stream using the scheduler
- Flexible bandwidth granularity
- Provides access to high-priority, per circuit queues for F4, F5 OAM flows and metasignalling channels through the node processor interface
- Transmits programmable “unassigned” cells during idle periods
- Discard timed-out cells according to bridge protocol
- Supports FLOWmaster™
- Supports Quantum Flow Control
- Supports Explicit Rate scheduling

TC35854F Features (Cont.)

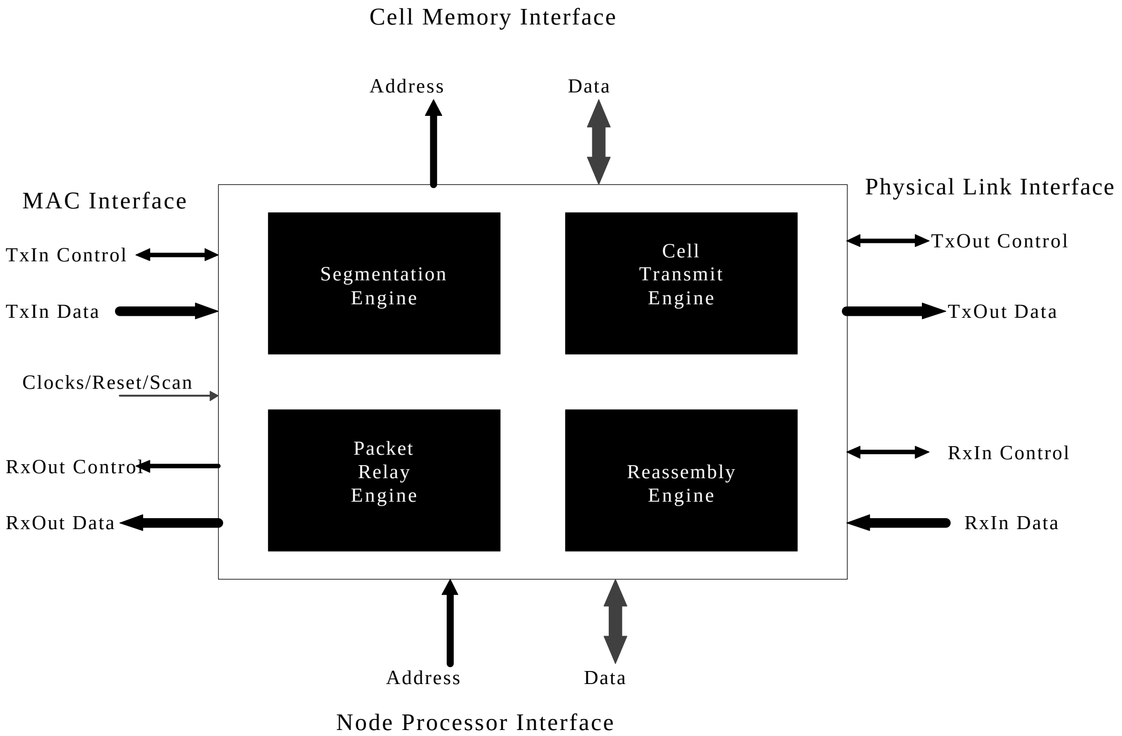
Receive

Reassembly	Packet Relay

- Provides flexible support for reassembly on up to 4095 circuit identifiers
    - Up to 4 VPIs
    - Up to 4095 VCIs per VPI (1-255)
    - Up to 1024 MIDs per VCI
- Unused VPIs, VCIs, MIDs can individually generate interrupts
- Flow 5 OAM cells identified and passed with cell headers
- Reassembles AAL5 packet (with or without stripping of packet trailer)
    - Packet CRC check
    - Packet length check
- Reassembles AAL3 and AAL4 packet with support for multiple MIDs (AAL4)
    - Cell CRC check
    - Cell type check
    - Cell length check
- Checks SMDS packet CRC
- Index into 4095 entry table used by packet dequeuer for packet header
- Packet timestamp for aging of reassembly
- Firmware triggered discard of partial packets for resource recovery on time-out
- Maximum packet length checking
- Minimum free cell threshold , below which new packets are not started, so that existing packets can complete reassembly (can be disabled on per circuit basis)

- De-queue packets from two prioritized queues
- Attaches prefix header (0 to 30 bytes) to each outgoing packet
- Strips the first 3 bytes of data from an RFC 1483 packet in ATM/SMDS mode (optional)
- Appends FDDI CRC (optional)
- Checks FDDI CRC in ATM/SMDS mode (optional)
- Generates odd or even parity for each byte on MAC interface
- Converts DA and SA between canonical and FDDI bit order formats (optional)
- Provides programmable filler insertion (up to 15 bytes) between packets
- Strips 16-bit or 32-bit HDLC CRC in packet relay mode

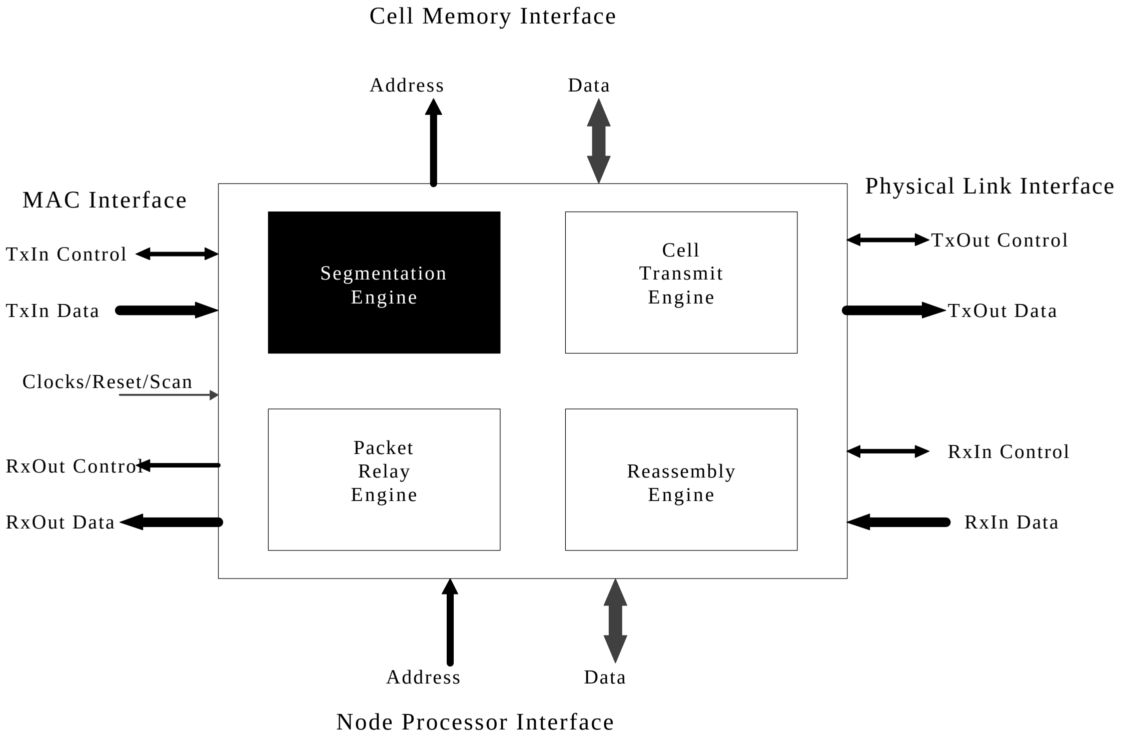
TC35854F Blocks



The internals of TC35854F consists of four main blocks:

- Segmentation engine
- Cell transmit engine
- Reassembly engine
- Packet relay engine

Segmentation Engine



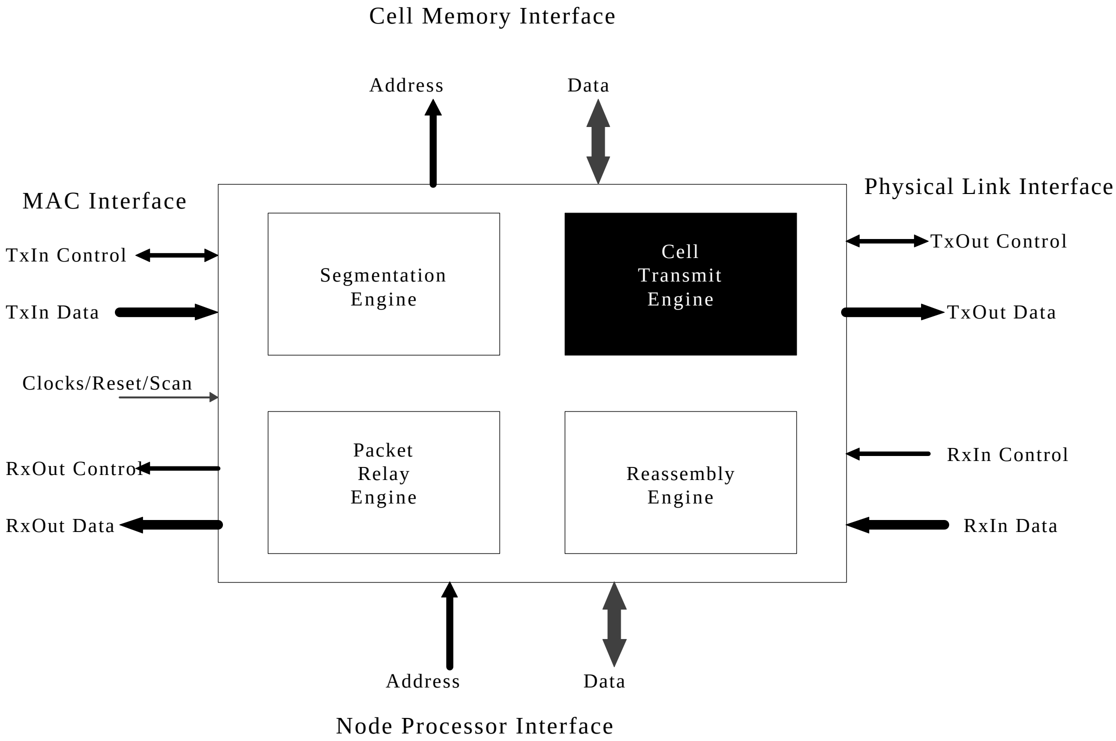
This engine segments packets into either AAL3/4 cells or AAL5 cells according to the virtual circuit state that is set up for the packet. At the start of a packet, the segmentation engine uses a region of the header to identify the particular circuit that the cells should be queued on. Up to 4095 separate circuit queues are supported. The region of the header used is programmable and depends on the packet format.

A per VC programmable number of bytes (up to 127) can be stripped from the head of the packet before segmentation, e.g., a FDDI header can be stripped. The last four bytes of a packet which could represent a MAC CRC can also be stripped. Three bytes of zero padding can be added to the start of every packet to conform with the requirements for "VC multiplex based FDDI bridge packet format" as specified in RFC 1483. This option is available on a per circuit basis. The DA and SA fields in FDDI packets can be converted between canonical and FDDI bit-order formats on a per packet basis.

The cells resulting from segmentation are stored in external SRAM for transmission by the cell transmit engine. Transmission can occur while the rest of the packet is still being segmented and hence transmit "cut through" is supported. Either a 32-bit FDDI CRC or SMDS CRC can be inserted at the appropriate place at the end of the packet during segmentation.

If TC35854F is running in packet relay mode, the data pulled from MAC interface are directly put into the transmit FIFO. 16-bit or 32-bit HDLC CRC can be added on per packet basis. Up to 63 bytes of the packet header could be stripped. 4-byte of data at the end of the packet could also stripped. All of these are controlled by the software.

Cell Transmit Engine



The cell transmit engine services up to 4095 transmit queues for CBR, VBR, ABR and UBR traffic. CBR and VBR traffic is served according to a precomputed traffic schedule that is stored in external SRAM. This schedule table can be used for peak-rate traffic shaping on a per circuit basis. The manner in which this table is filled out can also allow prioritization of traffic and overbooking of bandwidth. The granularity of bandwidth assigned to circuits is programmable.

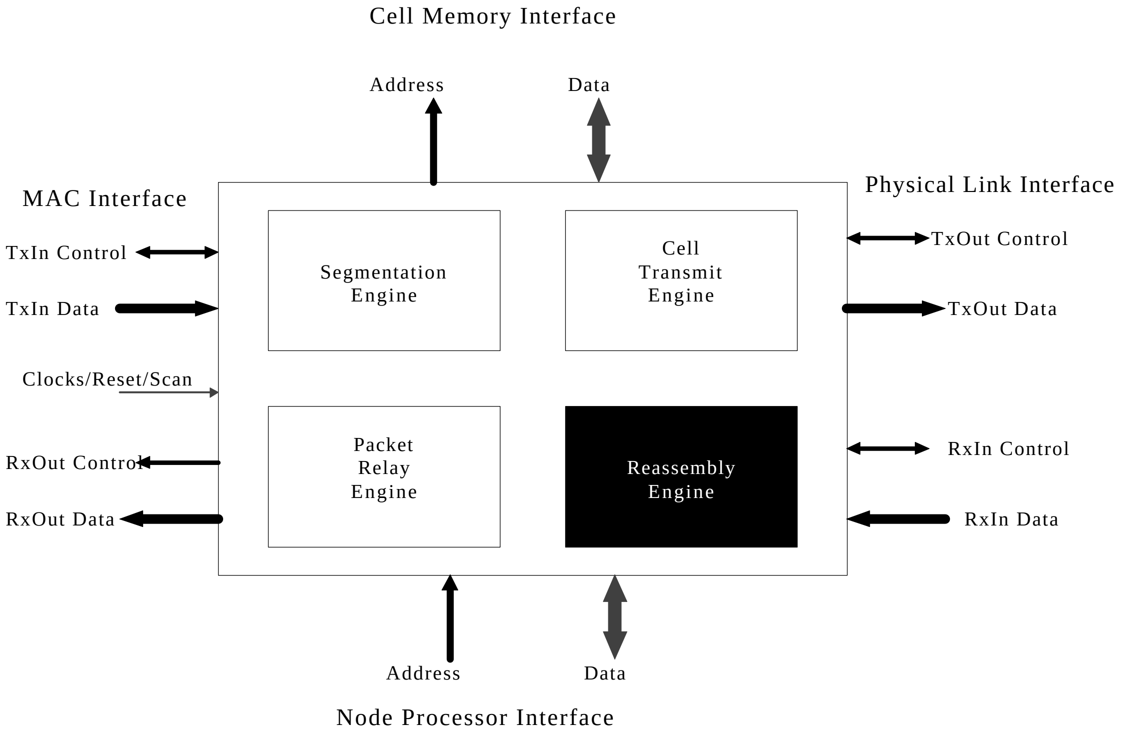
The cell transmit engine controls the average rate of cell transmission and "burst size" per circuit. It uses a "token-bucket" scheme, where a number of tokens are given to a circuit at some periodic refresh rate. When a cell is transmitted on a circuit, the number of tokens is decremented by one. When the number of tokens is reduced to zero, no further cells can be transmitted on that circuit until the tokens are replenished. The number of tokens that are replenished determines the "burst size", i.e., the maximum number of cells that can be sent at the peak rate. Token replenishment is performed by a firmware-triggered indirect operation.

ABR traffic services are ATM Forum UNI 4.0 specification and/or Quantum Flow Control (QFC) specification compliant.

The cell transmit engine supports the transmission of any arbitrary cell per circuit by providing a scratched area in external SRAM for storing up to 64 cells. This mechanism takes transmission priority over normal data cells stored in the 4095 queues. This is typically used for transmitting OAM cells and certain QFC control cells. When there are no data cells ready for transmission, the cell transmit engine sends unassigned cells with all zero ATM head and 0x6a payloads. It also checks bridge packet timed out condition. If any cell stays in the SRAM longer than 2 second, the cell is discarded.

A FIFO exists in the cell transmit engine to act as a data buffer for the Utopia Interface and as a synchronizer.

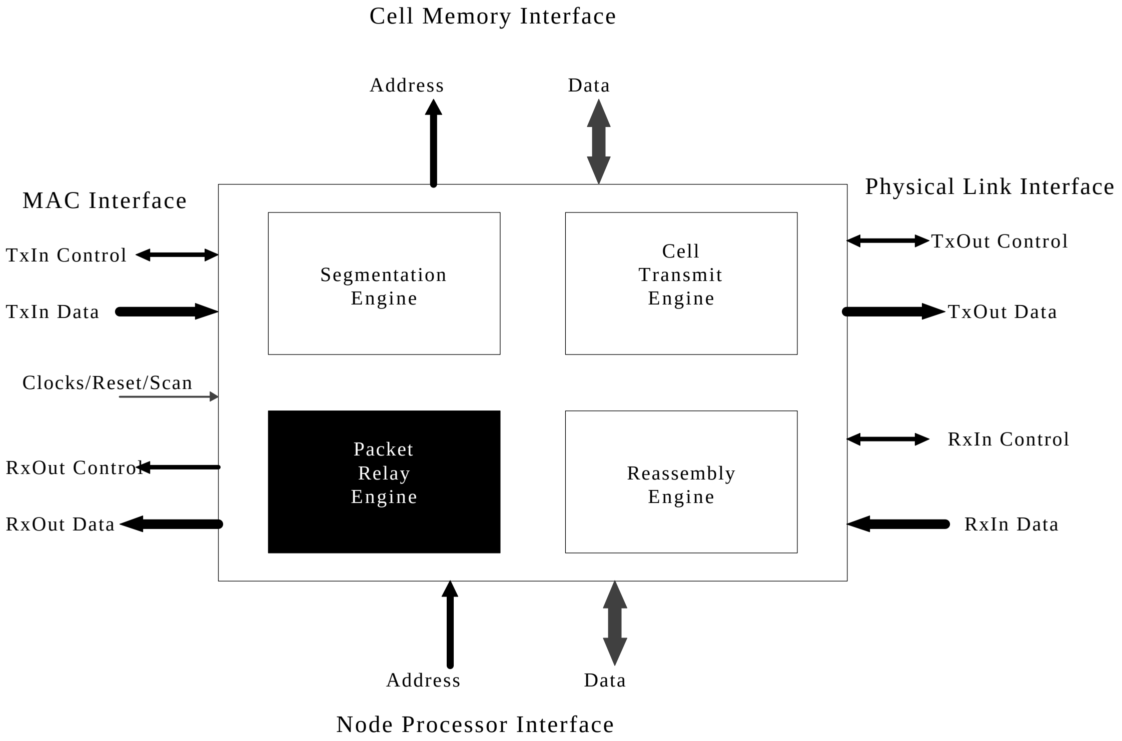
Reassembly Engine



The reassembly engine receives cells in byte-wide format from the link. A FIFO is used to provide data buffering for the reassembly engine and as a synchronizer.

Packet reassembly begins by taking a cell from the FIFO and looking up the receive circuit state that is stored in external SRAM. The index to the receive circuit state table is based on individual lookups of the VPI field, the VCI field, and possibly, the MID field if AAL3/4 is being used. Full address decode of the MID field (0 - 1023) is supported. Partial address decode of the VCI field is supported (0 - 4095) in ATM network. When in SMDS mode, VCI is always 65535. If the circuit lookup indicates that the cell should be accepted, the cell is written to a free cell buffer in external memory. If a packet reassembly is completed by the addition of this cell, the list of cells comprising the packet is moved to one of two packet lists, depending on priority bit setting for this circuit, and the circuit state is cleared. Otherwise, the circuit state is updated and written back to memory. Full AAL5 or AAL3/4 checking is done, including CRC checking, length field checking, segment type checking, and sequence number checking. The reassembly engine handles a large number of exception cases and provides indications via interrupt registers. It supports packet reassembly time-out and implements a receive buffer management scheme that avoids live-lock conditions. This guarantees forward progress when receiving packets.

Packet Relay Engine



The packet relay engine services two prioritized queues each of which contains a list of cell buffers that represents reassembled packets. The reassembly engine places reassembled packets onto this queue and indicates to the packet relay engine when a packet is ready for servicing.

Each packet contains a pointer to the circuit that it was received on. The packet relay engine can add a variable size header (0-30 bytes) of arbitrary information to each packet, on a per circuit basis. The header can also be restricted so that it is added only if a MAC multicast packet is detected. The packet relay engine can reverse the bit order of fields in the packet that correspond to the MAC Destination Address (DA) and Source Address (SA). The first three bytes of the reassembled packet can be stripped, on a per circuit basis. This provides conformance with "VC multiplex based FDDI bridge format packets" as specified in RFC 1483. OAM traffic is treated by always adding a header from a fixed location (index = 0) in the packet header table. The packet header and the complete OAM cell (including the 8-byte cell buffer header) are passed to the MAC interface.

The packet relay engine can check the integrity of a 32-bit MAC CRC at the end of a packet, if it exists. Alternatively, it can add a 32-bit CRC to the end of the packet. The computation of this CRC includes any added header bytes.

The RxOut interface uses the MAC protocol to deliver packets. This protocol delineates the packets with start and end markers and it indicates the status of the packet, e.g., good or bad CRC.

When TC35854F is running in the packet relay mode, The RxOut pulls out data directly from the link receive FIFO. 16-bit or 32-bit HDLC CRC can be checked and could be stripped by the RxOut. All packets can be prefixed a header from a fixed location (index = 0) in the packet header table.

Detailed Description

Figure 1 shows a detailed block diagram of TC35854F chip with its associated interface signals. The operation of these interfaces and blocks, from a user's point of view, is discussed in the following sections.

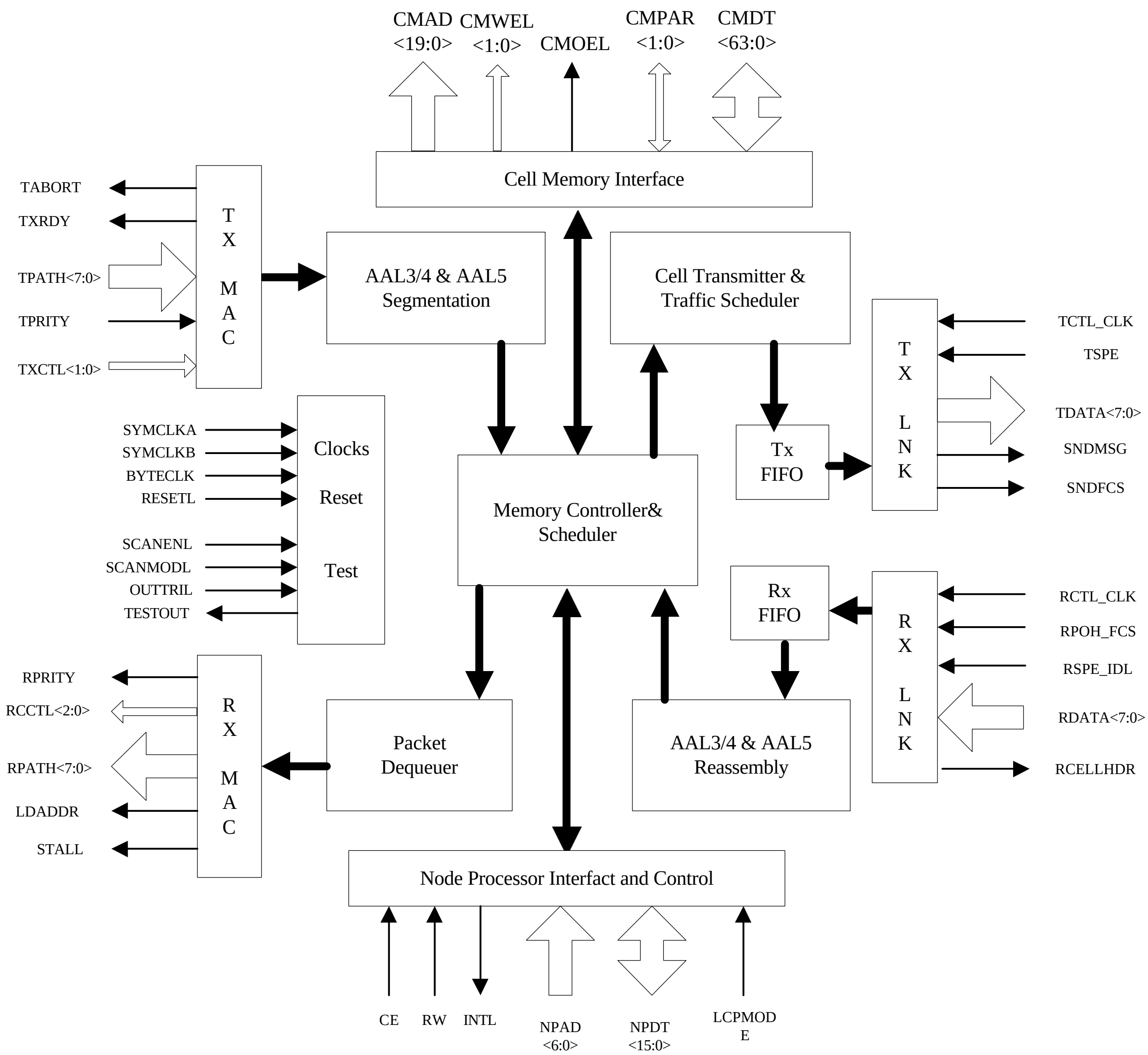


Figure 1 Detailed Block Diagram of TC35854F

Segmentation Engine (TxIn Process)

The segmentation engine consist of:

- Transmit MAC interface
- AAL segmentation block

Transmit Mac Interface Operation

The transmit MAC interface transfers data at a rate of 100 Mb/s or 200 Mb/s on the byte-wide, unidirectional data bus (TPATH<7:0>). The transfer rate is programmable using the *mac40* bit in CSR 0. TC35854F has the ability to hold off data transfers using the TXRDY signal. Aborted transmissions by TC35854F are indicated by the TABORT signal. TC35854F checks the parity of TPATH if the *txPrityCk* bit in CSR 0 equals 1. The *lcpPrtySel1* bit in CSR 0 is exclusive-ored with the parity of TPATH before comparing it to the TPRITY pin and hence the type of parity is programmable. If parity checking is enabled and a parity error is detected, the packet is discarded. Control of the packet transfer is dictated by the control signals TXCTL<1:0>.

- **Transmit Data Path Control**

Table 1 summarizes the interpretation of the TPATH bus as controlled by the TXCTL signals.

Table 1 Interpretation of TXCTL Signals in Transmit MAC Interface

TXCTL<1:0>	TPATH<7:0>	Function
0 0	xxxx xxxx	FILLER (TPATH is unspecified.)
0 1	pppp pppp	TX_START (TPATH contains the first byte of the packet. Only a TX_DATA or FILLER can follow this.)
1 0	Axxx xxxx	TX_END (TPATH contains information describing whether the frame was aborted by the source. A is the abort bit. If A=1, then TC35854F aborts the transmission of this packet. If the abort request happens within one cell's worth of data, TC35854F drops the packet. If the request happens later, it invalidates the AAL frame by corrupting the AAL5 CRC-32 and setting the frame length to zero. For an AAL3/4 frame, it sets the cell length to all ones.)
1 1	dddd dddd	TX_DATA (TPATH contains the second, third, ... and subsequent bytes of the packet. TX_END or TX_DATA or FILLER can follow this signal.)

The following sequence of transfers occurs during normal packet transmission:

1. Zero or more FILLERs
2. One TX_START
3. Many TX_DATAs and one or more FILLERs
4. One TX_END

This sequence is repeated for subsequent packets. TC35854F can handle back-to-back packet transfers without any FILLER inserted between the transfers. FILLER is allowed between TX_START and TX_END. Table 2 shows the type of protocol violations that can occur and the resulting action taken by TC35854F:

Table 2 Protocol Violations on Transmit MAC Interface

#	Protocol Violation	TC35854F Action
1	TX_DATA or TX_END indication given between FILLER and TX_START.	TX_DATA and TX_END indications are ignored and an interrupt (*tiUnexptSopIntr*) is set.
2	TX_START between TX_START and TX_DATA, or TX_END, FILLER.	This is treated as an abort request for the current packet. If the abort request happens within one cell's worth of data, TC35854F drops the packet. If the request happens later, it invalidates the AAL frame by corrupting the AAL5 CRC-32 (by inverting it) and setting the frame length to zero. For an AAL3/4 frame, it sets the cell length to all ones. The *tiUnexptSopIntr* interrupt is set. TABORT is asserted for one byte clock cycle.
3	TX_END occurring before the last byte of the circuit lookup field in the packet being transferred, or before the 10th byte of the packet, which one is longer.	This is treated as an abort request for the current packet. This abort request happens within one cell's worth of data and TC35854F drops the packet. The *tiUnexptSopIntr* interrupt is set.

Transmit Flow Control

TC35854F can be configured to operate in a mode where the link bandwidth is less than the transmit MAC transfer rate. TC35854F must therefore have a mechanism for flow-controlling the source. This is achieved using the TXRDY signal.

When TC35854F cannot accept the next byte transfer it deasserts (low) TXRDY (at t+0 ns). The source detects the TXRDY signal (at t+30 ns for 200 Mb/s mode and at t+60 ns for 100 Mb/s mode) and repeats the current TX_DATA byte until TXRDY is asserted. Once TXRDY is asserted, the next TX_DATA transfer is initiated. TXRDY only applies to TX_DATA transfers. The source can send TX_END or TX_START at any time, regardless of the value of TXRDY.

Figure 2 shows the operation of TXRDY from a timing point of view.

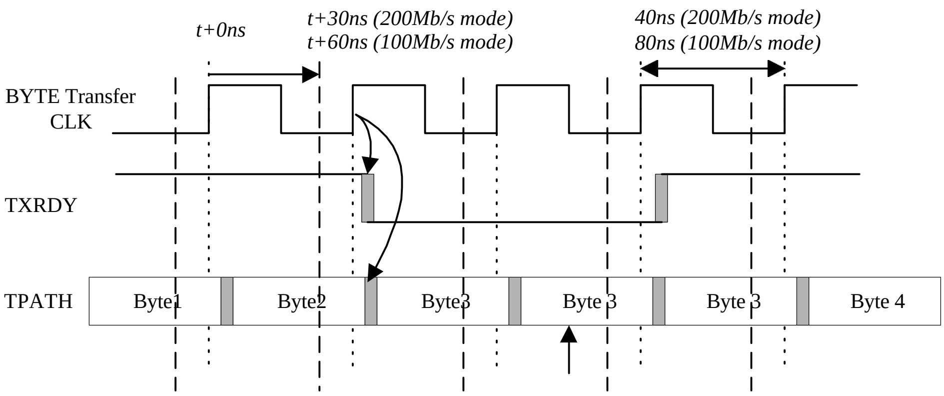


Figure 2 TXRDY Operation on Transmit MAC Interface

AAL Segmentation

The AAL segmentation block performs three main functions:

- Circuit lookup
- Packet formatting
- AAL segmentation processing

- **Circuit Lookup and Packet Formatting**

TC35854F provides a variety of flexible mechanisms for transmitting arbitrary packet formats onto a suitable virtual circuit. There are three principal classes of circuit lookup formats used:

1. Generic format
2. FDDI compatibility format
3. Short addresses format

These formats are shown in Figure 3 and Figure 4. TC35854F has two circuit lookup modes of operation. In the first mode, formats 1 and 2 are used and every packet transmitted from the source to TC35854F transmit MAC interface contains a three-byte packet request header. Table 3 Packet Request Header Fields describes the use of this header. In the second mode, format 3 is used and four-byte packet request headers are used. In both modes, the packet request header is dropped and never transmitted. In the first mode, the "lookup header" can be transmitted, depending on the selected stripping options.

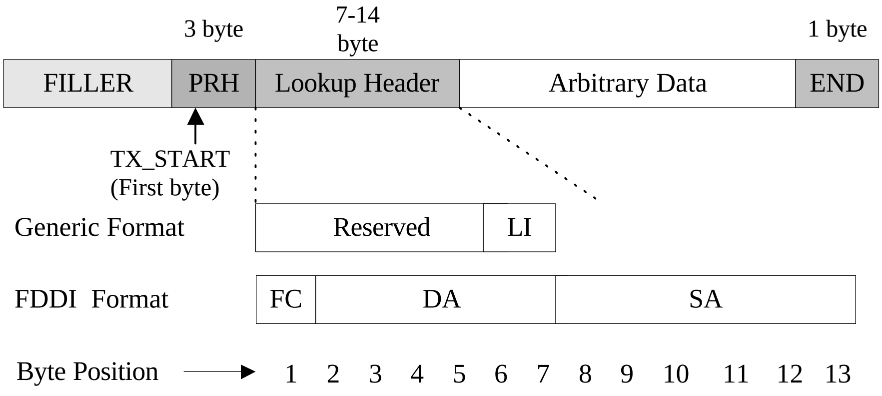


Figure 3 TC35854F Long Transmit Packet Formats for Circuit Lookup

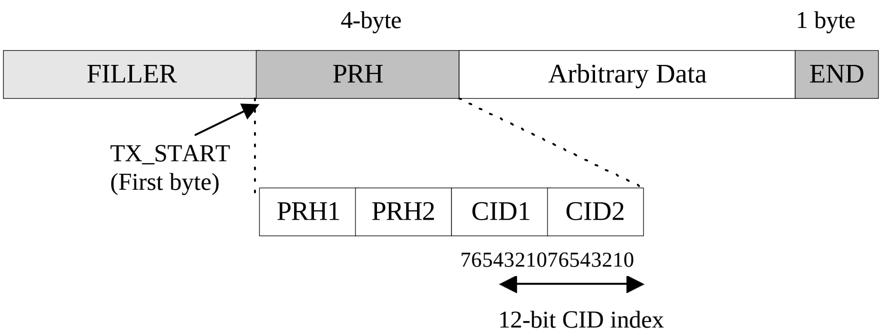


Figure 4 TC35854F Short Transmit Packet Formats for Circuit Lookup

- **Packet Request Header**

The three-byte packet request header is common to the first three packet formats used for circuit lookup. Table 3 contains a description of the packet request header fields.

Table 3 Packet Request Header Fields

Byte	Symbol	Name	Function
1	PRH1<7:0>	Packet Request Header 1	**xxxx xxxx** Field is reserved for future use.
2	PRH2<7:0>	Packet Request Header 2	**RxFx xxxx** R = 1: Reverse the bit order of bytes 2 - 13 of the lookup header. R = 0: Do not reverse the bit order. F = 1: Insert a 32-bit FDDI CRC at the end of the packet. CRC computation begins with the first byte after packet header stripping. Ignored if either R = 1 or the circuit has stdFddiMode enabled (RFC 1483). F = 0: Do not insert a 32-bit FDDI CRC.
3	PRH3<7:0>	Packet Request Header 3	**xxxx xxxx** Field is reserved for future use.

The packet request header is always stripped and discarded by the segmentation engine before placing data in cell buffers.

- **Generic Format Lookup Header**

This is the format of the lookup header that is used for the most general type of applications. Table 4 contains a detailed description of the fields used in the generic lookup header.

Table 4 Generic Format Lookup Header Fields

Byte	Symbol	Name	Function
1 - 5	Reserved <39:0>	Reserved 1	**xxxx xxxx** These bytes are reserved for future use.
6	LI1<7:0>	Lookup Index 1	**xxxx CCCC** The least significant nibble of this byte contains the four most significant bits of the 12-bit index for this packet. This index is the circuit identifier used to lookup the transmit circuit record table if *bridgedFlag* (CSR2) is not set to 1. If *bridgedFlag* (CSR2) is set to 1, *bridgedVc* (CSR2) is used as circuit identifier for this packet to lookup the transmit circuit record table.
7	LI2<7:0>	Lookup Index 2	**CCCC CCCC** This byte contains the eight least significant bits of the 12-bit lookup index for this packet. This index is the circuit identifier used to lookup the transmit circuit record table if *bridgedFlag* (CSR2) is not set to 1. If *bridgedFlag* (CSR2) is set to 1, *bridgedVc* (CSR2) is used as circuit identifier for this packet to lookup the transmit circuit record table.

To use the generic lookup format, the *tiShortAddr* (CSR 1) field and the *fddiComp* (CSR 0) field must be set to zero. The *pktHdrStrip* field in the transmit circuit record should be set to seven. This strips the full lookup header and transmits all following bytes up to the TX_END data byte. The END byte is not transmitted.

- **FDDI Compatible Lookup Format**

This format can be used when the source is transmitting FDDI packets and wants to direct the packets onto circuits based on the destination MAC 48-bit address. Table 5 contains a detailed description of the fields used in the FDDI compatible lookup header.

Table 5 FDDI Compatible Format Lookup Header Fields

Byte	Symbol	Name	Function
1	FC<7:0>	Frame Control	**FFFF FFFF** This byte is not used.
2 - 7	DA<47:0>	Destination Address	**DA<47:47>** Contains the I/G bit of the 48-bit address. **DA<46:10>** Contains 37 bits of the 48-bit address that are used in the following manner, if *bridgedFlag* (CSR2) is not set to 1. If *bridgedFlag* (CSR2) is set to 1, always use *bridgedVc* (CSR2) as circuit identifier for this packet to lookup the transmit circuit record table. • If *fddiComp* = 1 (CSR 0), compare this field with *daConst* in CSR 9, CSR 10, and CSR 11. If the comparison is true, use DA<11:0> as circuit identifier for this packet. If the comparison is false, use the *bridgedVc* (CSR2) as circuit identifier for this packet. • If *fddiComp* = 0, use DA<11:0> as circuit identifier for this packet without comparing with *daConst*. **DA<11:0>** Contains the 12 bits that are used as circuit identifier for this packet to lookup the transmit circuit record table.
8 - 13	SA<47:0>	Source Address	**SA<47:0>** Contains 48 bits that make up the MAC source address. This field is not used as circuit identifier.

To use the FDDI compatible lookup format, the *tiShortAddr* (CSR 1) field must be set to zero. The format of the transmitted packet depends on the values used in the *pktHdrStrip* field, the *crcStrip* bit, and the *stdFddiMode* in the transmit circuit record.

Table 6 shows some of the options possible.

Table 6 Example Settings for Packet Transmit Formats From FDDI Frames.

Transmit Packet Format	pktHdrStrip	crcStrip	stdFddiMode
Standard FDDI	0	0	0
FDDI PDU	1 3	1	0
VC multiplexed FDDI frame as per RFC1483	0	0 or 1	1
Raw IP packet	21	1	0

The generic lookup header is a simplified version of the FDDI lookup header. The difference is that the FDDI lookup mode uses the base compare constant and maps all traffic not matching the base constant to a circuit identified defined in *bridgeVc* (CSR 2). For example, this might be used for bridging traffic onto a specific VC, while routed traffic would match the base constant and be mapped to other VCs.

- **Short Lookup Format**

This format can be used when the source is transmitting generic packets and wants to direct the packets onto circuits based on the VC number. When this short addresses format is used, the packet request header has the different format and length, as shown in Table 7. These 4-byte packet request headers are always stripped.

Table 7 Packet Request Header Fields

Byte	Symbol	Name	Function
1	PRH1<7:0>	Packet Request Header 1	**xxxx xxxx** Field is reserved for future use.
2	PRH2<7:0>	Packet Request Header 2	**xxFx xxxx** F = 1: Insert a 32-bit FDDI CRC at the end of the packet. CRC computation begins with the first byte after packet header stripping. Ignored if the circuit has stdFddiMode enabled (RFC 1483). F = 0: Do not insert a 32-bit FDDI CRC.
3	PRH3<7:0> (CID1)	Lookup Index 1	**xxxx CCCC** The least significant nibble of this byte contains the four most significant bits of the 12-bit circuit identifier for this packet. This circuit identifier is used to look up the transmit circuit record table.
4	PRH4<7:0> (CID2)	Lookup Index 2	**CCCC CCCC** This byte contains the eight least significant bits of the 12-bit circuit identifier for this packet. This circuit identifier is used to look up the transmit circuit record table.

To use this short lookup format, *tiShortAddr* (CSR 1) must be set to 1. The format of the transmitted packet depends on the values used in the *pktHdrStrip* field, the *crcStrip* bit, the *stdFddiMode* in the transmit circuit record. TC35854F supports per VC header stripping up to 127 bytes. If *stdFddiMode* in the circuit record is set to 1, 3 bytes of zero will be added in front of the packet before it is transmitted. If *crcStrip* in the circuit record is set to 1, the last 4 bytes of the packet is stripped.

- **AAL Segmentation Processing**

Once the CID is obtained from a packet lookup header, the transmit circuit record is looked up using the CID as an index. If the *AAL* bit is zero, the packet is segmented according to the rules of AAL3/4. Otherwise, the packet is segmented according to the rules of AAL5. The segmented packet is stored on a linked list of cell buffers stored in external memory. This linked list waits for servicing by the cell transmit engine. Transmit "cut-through" is supported where the beginning of a packet can be transmitted as cells before the rest of the packet is reached. As mentioned previously, the format of the transmitted packet also depends on the values used in the *pktHdrStrip* field, the *crcStrip* bit, the *stdFddiMode* in the transmit circuit record.

- **SMDS Packet (SIP-3) Processing**

SMDS packets (SIP-3) transmitted through MAC interface has two formats: FDDI encapsulated, and raw format. Table 8 shows different stripping for these two formats, where the *stdFddiMode, pktHdrStrip* and *crcStrip* fields are in the circuit record.

Table 8 Per VC Packet Header Stripping for SMDS Packets

Transmit from	stdFddiMode	pktHdrStrip	crcStrip
FDDI packet	0	21	1 or 0
Raw packet	0	0	0

To transmit a SMDS packet, the *AAL* bit is set to zero and the *isSmds* bit is set to 1. After the necessary header stripping, a SMDS packet is segmented according to the rules of AAL3/4. Referring to TR-TSV-000774 for the SMDS SIP-3 format, the number of bytes of the packet that are segmented is decided by the *BAsize* field in the SMDS packet. TC35854F supports SMDS CRC insertion on a per-VC and per-packet basis. If the *smdsCRC* bit in the circuit record is set to 1 and the *CIB* bit in the packet header is also set to 1, CRC-32 is inserted into the SMDS packet. The *bridge* field of the SMDS packet header is skipped when CRC-32 is computed.

Cell Transmit Engine (TxOut)

The cell transmit engine consists of:

- Programmable traffic shaper and cell transmitter
- Transmit FIFO

Programmable Traffic Shaper and Cell Transmitter

TC35854F services up to 4 CBR VPs. Each VP is represented by a VP index. Two control and status registers (CSR 60 and 61) are used to map an 8-bit VP value to a 2-bit VP index. VP 0 is always mapped to VP index 0. The other 3 VPs are mapped to index 1, 2 or 3. Each VP can have up to 4095 cell queues. Each cell queue of a CBR VP is served with either a round-robin of all ABR circuits with cells to send, or according to a precomputed traffic schedule and a "token-bucket" scheme for all non-ABR circuits. The whole link bandwidth is partitioned among served CBR VPs, which is represented by a slot in the traffic schedule. The traffic schedule controls the minimum guaranteed peak rate and the peak rate of a non-ABR virtual circuit. The "token-bucket" scheme controls the sustained rate of a non-ABR virtual circuit.

The transmit schedule table is described in the *External SRAM Memory Map and Data Structures* section of this document. Figure 5 shows a logical representation of the schedule table.

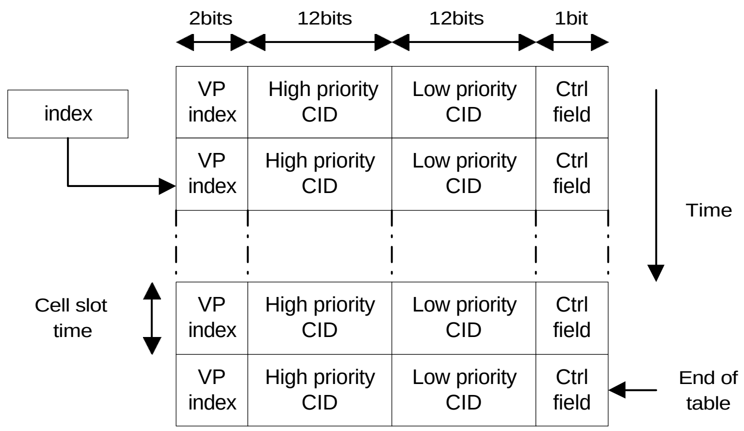


Figure 5 Logical Representation of the Transmit Schedule Table Used for Peak Rate Traffic Shaping

Each row in the schedule table represents a "send-cell opportunity" for a VP, which is indicated by the "VP index" field, called current VP. Hence, the number of rows that a VP has in the schedule table represents the guaranteed peak rate for that VP. Two non-ABR CID entries in each row indicate that up to 2 non-ABR circuits of the current VP can potentially use this opportunity to send a cell with higher priority than ABR circuits of the VP. The CID in the "High priority CID" field is served first. If there is no service required by this CID, the opportunity is passed to the CID in the "Low priority CID" field. Hence, the number of entries that a CID has in the "High priority CID" field represents the minimum guaranteed peak rate for a circuit The passing of the send opportunity continues to the ABR circuits of the VP, then UBR circuits of the VP, until a circuit makes a claim and sends a cell. If no circuit of the current VP has anything to send, and if the current VP is VP 0, an "unassigned cell" is transmitted with

0x6a as payloads. If the current VP is not VP 0 and the current VP has nothing to send, the service opportunity is passed to the ABR and UBR circuits of VP 0, with the ABR circuits have higher priority than the UBR circuits. The schedule index is then incremented and points to the next row of the VP that can legally send a cell for the next cell time. The number of rows in the schedule table determines the bandwidth granularity with the maximum 3392. The characteristics of the traffic shaper are determined by the algorithm used to fill out the traffic schedule table.

In each cell time slot, the following classes or CID are checked in the prioritized order. If running in FLOWmaster mode, replace the QFC with FLOWmaster in the list.

- High priority CID in the current row
- Low priority CID in the current row
- The VC at the head of the ER queue of the VP indicated by the VP index in the current row, whose service time is due.
- The VC at the head of the QFC queue of the VP indicated by the VP index in the current row
- The VC at the head of the ER queue of the VP 0
- The VC at the head of the QFC queue of the VP 0
- The VC at the head of the UBR queue.
- If the slow queue is due (see the *ER operation* section), the VC at the head of the slow queue is chosen at 25% bandwidth.

The average (sustained) rate of cell transmission and "burst size" for each VBR circuit can be controlled by a "token-bucket" scheme. A number of tokens is given to each circuit, using the *credits* field in the transmit CID record at some periodic refresh interval. Each time a cell is sent, the number of tokens is decremented by one. If the circuit has no tokens, it cannot send a cell. The number of tokens that are refreshed determines the "burst size", i.e., the maximum number of cells that can be sent at the peak rate. The number of tokens and the refresh interval determines the average (sustained) cell rate.

Cell Transmitter

A cell is transmitted using the following steps:

I. The traffic scheduler finds a circuit with a cell to transmit or generates an unassigned cell as described above.

II. The transmit circuit state is read from the transmit circuit table to confirm that:
   a) The circuit is valid.
   b) There are some tokens or credits for this circuit if the traffic type is VBR, ABR or flow controlled CBR in the FLOWmaster mode.
   c) There is either a data cell, or an OAM cell, or QFC buffer state check (BSC) control cell, or ER resource management cell (RM) ready. Transmission priority is given to OAM traffic if this is non-ABR circuit; transmission priority is given to BSC cell if it is under QFC control; if it is an ER circuit, OAM cells are treated as data cell and obeying the ER protocol.

III. The cell is moved to the transmit FIFO.

IV. The transmit state is updated and is written to external memory.

TC35854F scheduling logic uses a “rdyvector” to find if a CBR or VBR circuit has data ready to send. The rdyvector is 4095 bits, one bit per VCI. Indirect operations are available to set or clear individual bits in the scoreboard, or to write or read the bits for 16 VCIs at a time (internal to TC35854F, the rdyvector is implemented as RAM, 256 words by 16 bits). For proper operation, the rdyvector needs to be initialized to all zeroes; TC35854F reset does not perform this initialization. After initialization, no further operations are needed for normal operation. For ER circuit, the bit in the rdyvector indicates if ATDF condition is met to reduce current rate.

Transmit FIFO

The transmit FIFO provides an asynchronous interface between the core of the chip which runs at 25 MHz and the transmit link port which runs at a variable clock rate from 0 to 25 MHz. The size of the FIFO is 56 bytes. An error condition occurs if the FIFO underflows, i.e., the FIFO is empty. If this condition occurs, *txFIFOEmptyIntr* is set. It indicates a hardware fault and the chip must be reset.

Reassembly Engine (RxIn)

The reassembly engine consists of the following:

- Receive FIFO
- AAL Reassembler

An external ATM framing chip is used in TC35854F. Framing and synchronizing is done in the external chip. TC35854F will use its framing indication. This is supported by TC35854F for UTOPIA PHY interfaces.

Receive FIFO

The receive FIFO provides synchronization between the link and system clock domains. It buffers received data to smooth the burstiness of the packet reassembly process. The reassembly completes processing of a cell slightly faster than the cell time on a STS-3c link, but bursts and pauses occur during the cell processing. An error condition occurs if the FIFO overflows, i.e., the FIFO is full. If this condition occurs, *rxFIFOFull* interrupt is set. It indicates a hardware fault and the chip must be reset.

AAL Reassembler

The reassembly processor looks up the circuit state as described in the *External SRAM Memory Map and Data Structures* section of this document. The receive circuit record contains the state necessary to reassemble the packets. The receive AAL reassembler can reassemble cells into packets according to the rules of either AAL3/4 or AAL5.

If the circuit lookup indicates that the cell should be accepted, the cell payload is written to a free cell buffer in external memory. If a packet is completed by receipt of the cell, the list of cells that make up the packet is moved to one of two packet lists (setable per VC) and the circuit state is cleared. Otherwise, the circuit state is updated and written back to memory.

If a packet consistency check (a function of AAL) fails, cells making up the partly assembled packet are returned to the free cell list.

Packet Relay Engine (RxOut)

The packet relay engine consists of the following:

- Packet dequeuer
- Receive packet formatter
- Receive MAC interface

Packet Dequeuer

The packet dequeuer services two prioritized linked list of cell buffers that the AAL reassembler has already delineated into packet boundaries. One bit field, *pktList1*, in the receive circuit record indicates to which queue this circuit should be placed. If *pktList1* is set to one, all packets of this circuit are put into the higher priority queue. Otherwise, all packets of this circuit are put into the lower priority queue. OAM cells are always put on the higher priority queue. The packet dequeuer always serves the higher priority queue first. Only when the higher priority queue is empty can the other queue is served. The packet dequeuer forwards the packet from one of two queues to the receive packet formatter.

Receive Packet Formatter

The receive packet formatter uses the packet header table described in the *External SRAM Memory Map and Data Structures* section of this document to format the packet before the packet is sent out the receive MAC interface. The following formatting options are available:

- Add up to 30 bytes of arbitrary packet header data.
- Strip three bytes of the received packet header (used to strip the pad bytes of VC multiplexed FDDI traffic).
- Optionally add the header if the received packet is determined to be a multicast packet (this only applies to FDDI packets).
- Add or check 32-bit FDDI CRC in the trailer of a received packet.
- Reverse the bit order of the DA and SA bytes of a FDDI packet.

After passing through the packet formatter, the bytes are sent out the receive MAC interface.

Receive MAC Interface

The receive MAC interface transfers data at a rate of 100 Mb/s or 200 Mb/s on the byte-wide, unidirectional data bus (RPATH<7:0>). The transfer rate is controlled by the value of *mac40* in CSR 0. There is no mechanism available to flow-control this interface. The byte transfer operations are controlled by the RCCTL signals.

Table 9 summarizes the interpretation of the RPATH bus as controlled by the RCCTL signals.

Table 9 Interpretation of RPATH Bus as Controlled by RCCTL

RCCTL<2:0>	RPATH<7:0>	Function
0 0 0	k000 0000	**FILLER** k = 0 for FILLER between frames k = 1 for FILLER within a frame TC35854F never sends FILLER between END_DATA and FRAME_STATUS. Only START_DATA or DATA can follow FILLER (irrespective of the value of k).
1 0 1	dddd dddd	**START_DATA** TPATH contains the first byte of the packet. Only DATA , FILLER, or END_DATA can follow START_DATA.
0 0 1	dddd dddd	**DATA** RPATH contains a byte of the packet. Only DATA, FILLER, or END_DATA can follow DATA.
0 1 1	c000 0100	**END_DATA (ED)** RPATH contains information on the integrity of a packet. TC35854F has the ability to do a FDDI CRC-32 check on a packet. This is programmable on a per circuit basis. c = 1: A CRC-32 error was detected. c = 0: No CRC-32 error was detected. Only FRAME_STATUS follows END_DATA.
0 1 0	0110 1100	**FRAME_STATUS (FS)** RPATH contains a fixed encoding for compliance with the MAC protocol that indicates: • Three frame status symbols are present. • Error detected indicator is false. • Address recognized indicator is true. • Frame copied indicator is true. Only FILLER or START_DATA can follow FRAME_STATUS.

The following sequence of transfers occurs during normal packet transmission:

1. Zero or more FILLERs
2. One START_DATA
3. Many DATAs (with FILLERs possible)
4. One END_DATA
5. One FRAME_STATUS

This sequence is repeated for subsequent packets. TC35854F will not send back-to-back packet transfers without any FILLER inserted between the frames. However, if an application requires a minimum number of FILLERs between packet transfers, this can be set using *roNumFillBytes* in CSR 5. No FILLER is sent between END_DATA and FRAME_STATUS. TC35854F receive packet format is shown in Figure 6.

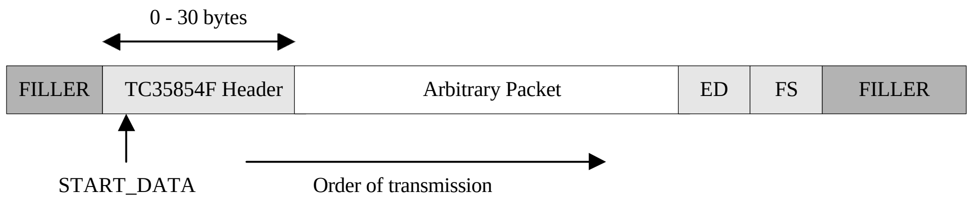


Figure 6 TC35854F Receive Packet Format

The STALL and LDADDR signals on the receive MAC interface can be used for CAM lookup operations on fields in the receive packet header. The STALL signal is driven low whenever a FILLER byte is sent on the RPATH bus. Otherwise, STALL is high.

The LDADDR signal is driven high for a single byte time, two byte times before START_DATA. This can be used to set up the timing of CAM compares. The timing is shown in Figure 7.

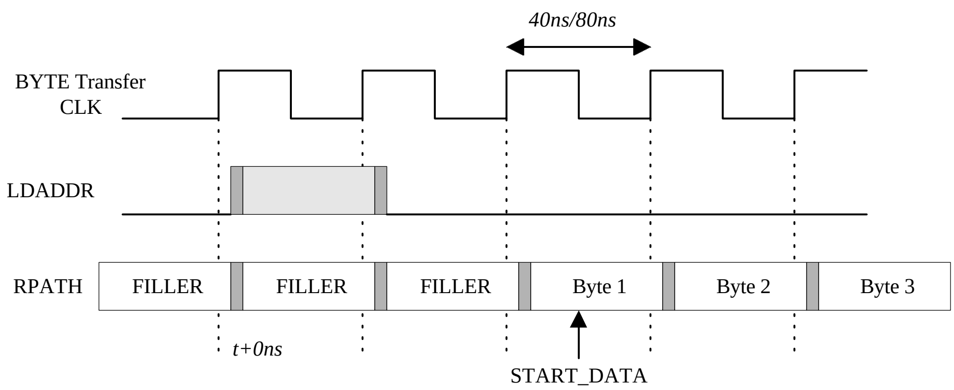
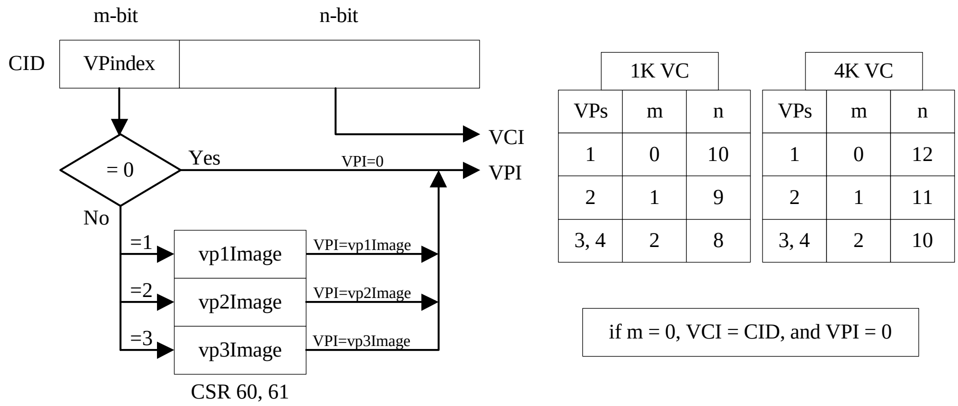


Figure 7 LDADDR Timing

Mapping between VPI/VCI and TC35854F CID

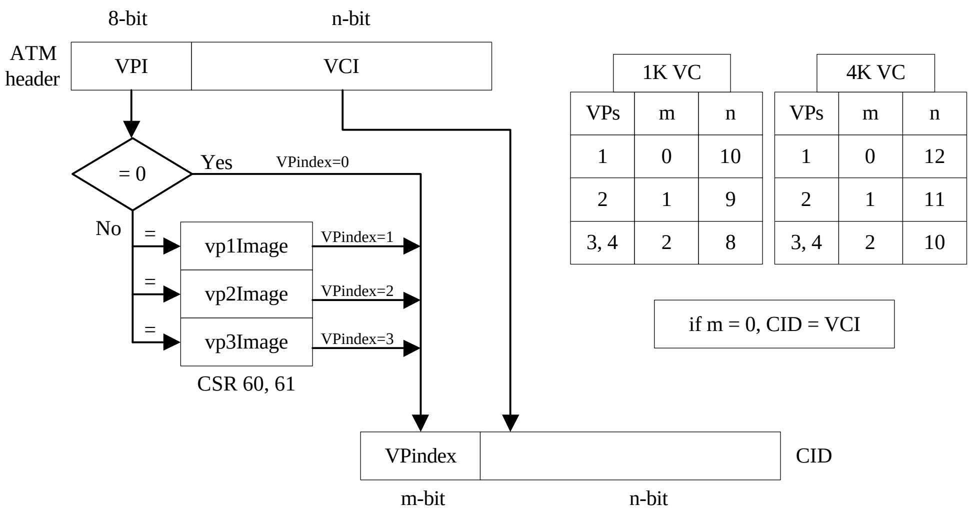
TC35854F uses an internal circuit identifier (CID) to represent each circuit. The mapping between ATM VPI/VCI and CID obeys the rules shown in Figure 8. The number of VP (VPs) served is indicated in the numberVP field in CSR 1 bits < 10:9>. Each of vp1Image, vp2Image and vp3Image in CSR 60 and 61 contains the real VPI which is mapped to VP index 1, 2, and 3. These values are used as VPI in the transmitted cells and VPI in the received cells are compared with these value to be mapped to VP index.



1K VC			4K VC		
VPs	m	n	VPs	m	n
1	0	10	1	0	12
2	1	9	2	1	11
3, 4	2	8	3, 4	2	10

if m = 0, VCI = CID, and VPI = 0

a. Tx Mapping CID to VPI/VCI



1K VC			4K VC		
VPs	m	n	VPs	m	n
1	0	10	1	0	12
2	1	9	2	1	11
3, 4	2	8	3, 4	2	10

if m = 0, CID = VCI

b. Rx Mapping VPI/VCI to CID

Figure 8 Mapping between ATM VPI/VCI and CID

Explicit Rate Operation

Explicit Rate functionality in TC35854F is ATM Forum documentation af-tm-0056.000 compliant. It is described in the following parts:

- Rate range in TC35854F
- ER parameters
- Transmit policy based on round-robin and explicit rate
- RM cell processes

For more details, see standard documentation "*ATM Forum af-tm-0056.000*".

Rate Range in TC35854F

TC35854F supports rate ranges from 64 kb/s (~150cell/s) to 155Mbit/s (~330k cell/s), with rate granularity about 0.78% link bandwidth. In addition to this rate range, TC35854F also supports 32 kbit/s (~75cell/s) and 10 cell/s rates.

ER Parameters

TC35854F supports all ER parameters defined in the ATM Forum documentation af-tm-0056.000 but some parameters are only supported in certain ranges. Table 10 lists the parameters and their ranges.

Table 10 ER Parameters in TC35854F

Label	Range
PCR, MCR, ICR, ACR	10 cell/s, 32kbit/s, 64kbit/s - 155Mbit/s with granularity of 0.78% link BW
RIF, RDF	power of two, ranging from 1/32768 to 1.
Nrm	32 or 256, selected by CSR 0 bit <6>
Mrm	fixed constant 2
CRM	integer, ranging from 0 to 255
ADTF	fixed at 500ms
Trm	fixed at 100ms
CDF	zero or power of two ranging from 1/16 to 1
TCR	fixed at 10 cells per second

Transmit Policy

Transmission of cells on circuits under ER control is done using round-robin to fairly select circuits that are enabled, service time due, and have traffic to be sent. All ER circuits whose service times are due form a queue. The VC at the head of the queue is served and removed from the queue. After this VC is served, and it meets all transmission criteria, it is rescheduled to a future time according to its rate. Otherwise, this VC is dequeued. When rescheduling a VC to a future time, it is current time plus Δt, which is obtained by looking up the Rate ABR Schedule Offset Table with its ACR as index. The description of the Rate ABR Schedule Offset Table can be found in the *External SRAM Memory Map and Data Structures* section. When this VC is served, the priorities for cells to transmitted are: QFC BSC cell if in QFC mode, OAM cell and data cell or RM cell according to the ATM Forum documentation af-tm-0056.000.

In order to support 32kbit/s, the VC is scheduled as if for 64kbit/s but is served only every other service opportunity.

All VCs with rate 10 cell/s form a special queue called the slow queue. When the service time is due for the slow queue (about 100ms), the slow queue is served using 25% of the link bandwidth. When the queue is served, the VC at the head of the queue is served, removed from the head and rescheduled to the end of the queue. The service is continued until all VCs in the queue have been served. The software keeps a timer for the slow queue. Every 100ms, the software sets slowErDue bit in CSR register (CSR 2, bit<13>) to 1. After receiving this signal, TC35854F clears the bit and starts to serve the slow queue. The cells sent for any slow queue VC are among: in -rate OAM cell, out-of-rate forward RM cell, out-of-rate backward RM cell, and in-rate QFC control cell if in the QFC mode. The priorities of these cells are: in-rate QFC control cell if in QFC mode, in-rate OAM cell and out-of-rate RM cell.

If TC35854F is also in either QFC or FLOWmaster mode, the ER VC must also obey credit control rules as well as its rate limitation. An ABR VC can send a cell only if it has credits except for QFC BSC cells. If TC35854F is also running GFC control, an ABR VC can send a cell only if GFC GO-COUNT is not zero and TRANSMIT is set to 1.

RM Cell Processing

In-rate RM cells are served according to the rules defined in the ATM Forum documentation af-tm-0056.000. Out-of-rate forward RM cells can be generated at a rate no more than 10 cell/s. It is triggered by the software through indirect operation, described in the *Control/Status Register Descriptions* section.

When a forward RM cell is received, it is written into the RM cell pool, which is described in the *External SRAM Memory Map and Data Structures* section, and waits for transmission by the transmit engine. If the previous forward RM cell for this VC has not been transmitted when the new forward RM cell is received, the previous one is overwritten by the newly received forward RM cell. At the same time, the VC is remembered in a FIFO called out-of-rate turn-around RM FIFO. Up to 4 VCs can be stored in the FIFO. When there is a chance to send an out-of-rate backward RM cell, the VC at the head of FIFO is served and its backward RM cell is sent out-of-rate. This VC is removed from the FIFO. Note, this VC is still waiting for in-rate transmission of the backward RM cell even if it is removed from the out-of-rate backward RM FIFO.

If local congestion happens which is indicated by the number of receive buffers being under the threshold required to receive any new packet, CI and NI bits in all backward RM cells are set to 1 until the local congestion is resolved. Per VC state also records the EFCI bit of the latest received data cell which is also used to mark CI and NI bit in the backward RM cell for this VC.

The rate of a VC is adjusted, either when a backward RM cell is received, or other criteria are met as defined in the ATM Forum documentation af-tm-0056.000. The rate adjustment would be 10 cell/s to either 32kbit/s or 64kbit/s or above and vice versa. In order to avoid some VC to be stuck in the slow queue, RIF should be chosen such that the rate adjustment would allow rate to jump from 10cell/s to or above 64kbit/s.

When a RM cell is received, besides checking for valid VPI and VCI, its protocol ID is checked and the cell is discarded if a wrong protocol ID is detected. An interrupt is asserted at the same time. If zero ER received in a backward RM cell is detected, an interrupt is also asserted. Both interrupts are maskable.

Receive Buffer Management

When in QFC mode or FLOWmaster mode, TC35854F uses credit flow control to prevent cell loss due to receive buffer congestion. The RxIn logic maintains three pools of cells when either QFC or FLOWmaster is enabled - a static credit control pool, a dynamic credit control pool, and a pool for circuits not under credit flow control.

The static pool corresponds to the number of credits that the upstream transmitter can use immediately, even if no acks are returned to it. This is equal to the sum of the initial credit count on every credit controlled circuit. In FLOWmaster, the initial credit count for each VC is defined in the bslVcLimitDef0 field, CSR 62 bits <13:7>. In QFC mode, the bslVcLimitDef0, bslVcLimitDef1, bslVcLimitDef2, and bslVcLimitDef3 fields in CSR 62 and 63, contain the initial credit count for each VC of all VPs.

The dynamic pool is used for circuits for whose credits are being returned to allow a packet to reassemble. At the time that a packet starts reassembly, a decision is made about whether or not there are enough free cells in the dynamic cell pool to allow the packet to complete reassembly (assuming a MTU size packet). If so, then the *flowOn* bit is set in the Rx circuit record and a credit is allowed to be returned to the upstream node for every cell received in the packet.

The pool for circuits without credit control is used for any circuit not using credit flow control and OAM traffic. It is kept separate to guarantee resources for credit controlled circuits. The *minRxFrCell* field in CSR 19 applies only to these circuits without credit control.

A packet can start reassembly at a time when there are not enough resources in the dynamic pool to allow complete reassembly. Resources in the static pool are used to store the cells of the packet, and two counts of credits not yet returned are kept. One count is for cells which do not consume the cell pool for credit control circuits, including RM cells and OAM cell. RM cells do not use any buffer while OAM cells consume buffers from the non-credit-control pool. The other count keeps track of cells consuming the buffers from the credit control pool. The RxIn logic tracks which circuits are “stuck” (using static resources) and the circuits are automatically “activated” when resources are available in the dynamic pool - credits which equal to the sum of the two counts, are then returned to match all cells received while stuck and the circuit is allowed to complete the packet in the dynamic pool.

If a packet completes reassembly in the static pool, the cells of the packet are (effectively) moved to the dynamic pool, and the packet is forwarded to the MAC interface, though credits are not returned to the upstream node until the circuit can be activated.

The size of the static pool should be initialized as appropriate to the number of setup circuits in CSR 42. The sum of the static and dynamic pool sizes is set as the Rx Free Cell list size in CSR 30/CSR 31. The pool size for circuits without credit control is set in CSR 41. All cells are initially in a single linked list of free cells, but the three counters track the separate allocations.

A suggested allocation of cell pools might be 33% for Tx, 67% for Rx. The credit control Rx pool must be larger than the sum of credits on all circuits, and allow room to reassemble several packets simultaneously (the MTU (CSR4) setting is significant to this calculation). The non-credit-control cell pool should be large enough for OAM and non-credit-control traffic, such as ILMI and signaling VCs.

CSR 43 contains the current number of cells that the RxIn logic has committed to receive (but has not yet received) by deciding to allow circuits to complete reassembly of the current packet.

The RxIn logic will not allow a circuit to use more than the maximum per-circuit allocation of the static pool specified by either bslVcLimitDef0, or bslVcLimitDef1, or bslVcLimitDef2, and or bslVcLimitDef3 fields in CSR 62 and 63, depending on VP index for the circuit.

The RxIn logic uses a “scoreboard” to track circuits with unreturned credits. The scoreboard is 4095 bits, one bit per VCI. Indirect operations are available to set or clear individual bits in the scoreboard, or to write or read the bits for 16 VCIs at a time (internal to TC35854F, the scoreboard is implemented as RAM, 256 words by 16 bits). For proper operation, the scoreboard needs to be initialized to all zeroes; TC35854F reset does not perform this initialization. After initialization, no further operations are needed for normal operation.

The scoreboard is arranged such that all circuits of different VPs have the equal chance to be promoted. The following tables show each CID position in the scoreboard in different conditions, where all CIDs are expressed by hexadecimal.

Table 11 CID Locations in the Scoreboard for Different Conditions

	CID locations for 4K circuits with 1, 3 or 4 VPs supported															
Bit =>	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
word 0	0	400	800	c00	100	500	900	d00	200	600	a00	e00	300	700	b00	f00
word 1	1	401	801	c01	101	501	901	d01	201	602	a01	e01	301	701	b01	f01
word 2	2	402	802	c02	102	502	902	d02	202	601	a02	e02	302	702	b02	f02
									. . . .							
word ff	ff	4ff	8ff	cff	1ff	5ff	9ff	dff	2ff	6ff	aff	eff	3ff	7ff	bff	fff

	CID locations for 4K circuits with 2 VPs supported															
Bit =>	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
word 0	0	800	400	c00	100	900	500	d00	200	a00	600	e00	300	b00	700	f00
word 1	1	801	401	c01	101	901	501	d01	201	a02	601	e01	301	b01	701	f01
word 2	2	802	402	c02	102	902	502	d02	202	a01	602	e02	302	b02	702	f02
								. . . .								
word ff	ff	8ff	4ff	cff	1ff	9ff	5ff	dff	2ff	aff	6ff	eff	3ff	bff	7ff	fff

	CID locations for 1K circuits with 1, 3 or 4 VPs supported															
Bit =>	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
word 0	0	100	200	300												
word 1	1	101	201	301												
word 2	2	102	202	302						Not used						
			. . . .													
word ff	ff	1ff	2ff	3ff												

	CID locations for 1K circuits with 2 VPs supported															
Bit =>	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
word 0	0	200	100	300												
word 1	1	201	101	301												
word 2	2	202	102	302						Not used						
			. . . .													
word ff	ff	2ff	1ff	3ff												

FLOWmaster™ Operation

FLOWmaster functionality can be partitioned into the following parts:

- FLOWmaster cell format
- Transmit policy (based on best-effort round-robin and credit counts)
- Ack reception (and increment of transmit credit count)
- Ack transmission policy
- Credit resync protocol support

In FLOWmaster mode TC35854F uses receive buffer management describe in the *Receive Buffer Management* section.

FLOWmaster Cell Format

FLOWmaster operation uses an ATM cell header format that differs from traditional ATM cell headers. The VPI (8 bits) and VCI (16 bits) fields of a traditional ATM cell are changed. Instead, the header carries an ACK (12 bits) field and a VCI (12 bits) field. When the ACK field is non-zero, then its value represents a single credit being returned for the VCI identified by the value. (VPI values are not used with FLOWmaster links.)

FLOWmaster Transmit Policy

Transmission of cells on circuits using FLOWmaster is done using round-robin to fairly select circuits that are enabled, have credits available to allow transmission, and have traffic to be sent. The round-robin is described in greater detail in the *Cell Transmit Engine (TxOut)* section of this document.

When a cell is transmitted, the credit count decrements. If the credit count drops to zero or the number of cells to be sent drops to zero, then the circuit is taken out of the round-robin until both counts are non-zero.

FLOWmaster Ack Reception

Received cells can carry credit acks from the upstream ATM entity. When an ack is received, the transmit circuit record for the VCI specified by the ack value is incremented by one.

This operation requires an exact mapping of VCI value to the transmit circuit identifier (CID). FLOWmaster circuits require an exact mapping (VCI value = CID value = Packet Header Index value).

FLOWmaster Ack Transmission

The RxIn logic determines when to send an ack to the upstream node depending on whether the current circuit is being allowed to complete packet assembly. If so, then acks are returned immediately. A “single credit FIFO” is used for this operation.

The RxIn logic can, at times, activate a circuit that had used cells from the static pool, resulting in several accumulated acks that need to be returned. A separate, “multiple credit FIFO” is used for this operation.

Any acks are transmitted from the single credit FIFO. Because acks can only be added to this FIFO one per link cell time and the transmit opportunities will match this rate (within 20 ppm), an overflow of the single credit FIFO is very unlikely. At worst, in 50,000 cells, there may be one additional ack that could contribute to an overflow condition. TC35854F handles this condition by moving this single ack to an interrupt register, so that firmware can implement a backup FIFO structure. This event causes the lcpCreditTaken interrupt, and occurs if the single credit FIFO exceeds the *rxSCredFifoThresh* threshold set in CSR 19. The single credit FIFO size is eight entries.

Acks can be inserted into the multiple credit FIFO by firmware or due to circuit activation. Neither will occur if the multiple credit FIFO is full, so overflow of this FIFO is not possible. The size of this FIFO is four entries; each entry is a VCI and a 6-bit count.

TxOut pulls out acks from the credit FIFO and puts it into the ATM cell header. The action can be done before cells are put into the transmit FIFO, or after cells are put into the transmit FIFO. If inserting acks to the cell header occurs after cells are put into the transmit FIFO, the link clock (TCTL_CLK) must be running synchronously with the SYMCLKA and meets the conditions shown in Figure 9.

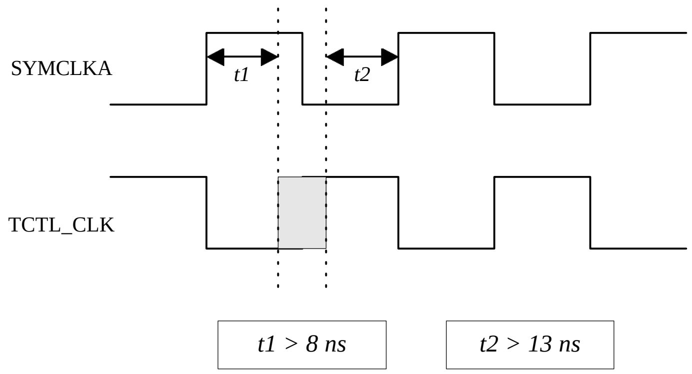


Figure 9 Timing Requirement for Adding Credits After Tx FIFO

Support for FLOWmaster Credit Resync

The FLOWmaster credit resync protocol is used to perform an audit of the flow control credits, so that any credits lost due to bit error corruption of cell headers on the link can be recovered. The protocol is essentially that an upstream stops sending traffic on the circuit to be resynced, sends a Resync Request (on a reserved, well-known VCI), and the downstream node returns a Resync Ack (on the well-known VCI) when its buffers for the VCI have been emptied and acks returned. When the upstream node receives the Resync Ack, the credit count for the VCI should be equal to the initial count; if not, lost credits can be replenished at this time. At completion, traffic can resume.

TC35854F provides an indirect operation to stop traffic on a circuit (see the *portMode* field of CSR 11). The Resync Request can be sent through the MAC interface or by the OAM mechanism. When the Resync Ack is received, the update credits indirect operation can be used to reset the correct credit count and restart traffic.

For the downstream side of the resync protocol, firmware should check the circuit status to determine whether the VCI has not returned acks by reading the Rx Circuit state - if so, an indirect operation (force_next_flow) can be used to put the circuit at the head of the list of circuits to be activated and the firmware should wait until that happens. In either case, the next check is whether all acks for the VCI have been returned - an indirect operation to check the credit FIFOs for a specified VCI is provided for that purpose. And finally, the Resync Ack can be sent through the MAC interface or by the OAM mechanism.

Quantum Flow Control Operation

Quantum Flow Control (QFC) is a cell-relay protocol characterized by quantized buffer state feedback. TC35854F implements the following functions defined in QFC specification FCC-SPEC-95-1, Version 2.0:

- ABR services on Virtual Channel Connections (VCCs) for short link, and
- ABR VCCs carried within a CBR VPC for short link 8-bit counters.

For more details, see standard documentation "*Quantum Flow Control, FCC-SPEC-95-1, Version 2.0*".

QFC Counters in TC35854F

Table 12 shows all counters in TC35854F to support QFC. $Limit_{vcdef}$ and $Limit_{link}$ registers are stored in the firmware.

Table 12 QFC Counters

Name	Width	Basis	TC35854F	Comments
txCount	8 bits	per VC	RW	Transmit Counter
bsuFwdCount	8 bits	per VC	RW	Used by Transmit
bslVcLimitDef	7 bits	per VP - CSR	RO	Used by Transmit
bslLinkLimit	27 bits	per VP - CSR	RO	Used by Transmit
linkBsuFwdCount	28 bits	per VP - local	RW	Used by Transmit
linkTxCount	28 bits	per VP - local	RW	Used by Transmit
N4	3 bits	per VP - CSR	RO	System-wide
unSentCount	8 bits	per VC	RW	Implementation Specific, receive
unsentOtherCredits	8 bits	per VC	RW	Implementation Specific, receive
FwdCount	8 bits	per VC	RW	Used by Receive
N2Count	8 bits	per VC	RW	Used by Receive
linkN2Count	16 bits	per VP - local	RW	Used by Receive
linkRxCount	28 bits	per VP - local	RW	Used by Receive
linkFwdCount	28 bits	per VP - local	RW	Used by Receive
linkN2	16 bits	per VP - CSR	RO	System-wide
vcN2	8 bits	per VP - CSR	RO	System-wide

QFC Protocol Units

Table 13 shows all QFC protocol control units and how TC35854F processes them. For cells carried on VP RCC_VC, the priorities to serve are: BSL/BSR/ACP, BSC(link), BSU. TC35854F does not support vendor defined Message_Type, does not support BSU_Type other than for VCC, Physical link and Tunnel in a BSU cell, does not support Check_Type other than for VCC, Physical link and Tunnel in a BSC cell. Any exception will cause an interrupt. When a control unit is received, its Protocol_ID and Revision_ID are also checked and corresponding interrupt is asserted if an exception occurs.

Table 13 QFC Protocol Units

Name	Carried on	TC35854F Operations
BSU	VP RCC_VC	generated and processed by TC35854F.
BSC	VP RCC_VC and VCC	triggered by the software through indirect operation; generated and processed by TC35854F.
BSLind BSLconf	VP RCC_VC	generated and processed by the software; transmitted through OAM pool.
BSRind BSRconf	VP RCC_VC	generated and processed by the software; transmitted through OAM pool; TC35854F marks Tx_starttime, Rx_receivetime, Rx_forwardtime and Tx_stoptime using values from the local timer with the granularity of 240ns (CSR 78 and CSR 79).
ACPind ACPconf	VP RCC_VC	generated and processed by the software; transmitted through OAM pool.

Transmit and Receive Operations

- Initialize all counters to zero.
- Sending cell operations for a QFC VC:

When sending a cell except BSC cell, the equation [1] in QFC spec is checked and txCount as well as linkTxCont increment. When sending a BSC cell, the above equation is not checked and the counters are not incremented. If this connection is also rate ABR, Nrm counter is not incremented, either. Note, all other QFC protocol control units are not carried on QFC connections. Hence no counters are updated.

- RxIn receiving cell operations for a QFC connection:

When a cell other than a BSC cell is received, the linkRxCounter for the VP increments. If the circuit is not stuck (see the *Receive Buffer Management* section), VC N2count, VC fwdCount, link N2count and link fwdCount increment. If the circuit is stuck, either VC unsentCount or rmUnsentCount increments. If a BSC cell is received, no counters are updated. RxIn then update corresponding counters according to equation [3] in QFC specification. At the same time, a BSU record is composed for the connection. Note, all other QFC protocol control units are not carried on QFC connections. Hence no counters are updated for them.

- M-cell space between two BSU cells of a VP can be guaranteed by scheduling the VP with at least 17 cell time slots apart in the schedule table.

BSU Cell Processing

- Packing and Sending BSU cell operations:

When either vcN2 cells for a VC or linkN2 cells for a VP have been forwarded, RxIn composes a BSU record by sending either VC fwdCount or VP fwdCount into a 5-stage FIFO along with CID and vpIndex; and resets corresponding N2 counter.

A BSU cell is composed when N4 BSU records have been put into the cell. All BSU cells are from Tx free cell pool. Eight free cells are reserved for BSU cells.

The software can request to compose a BSU record for a connection no matter what N2 value is. To do

so, the software will put such a request through indirection operation.
BSU records are automatically generated for each VP every N2(l) cell times. This helps ensure credits are returned in a timely manner.

- Unpacking received BSU cell operations:

When a BSU cell is received, the corresponding Forward_Count is updated. The VPI field in the ATM head is mapped to VP index by checking CSR 60 and CSR 61. The obtained VP index and the VCI field in the ATM head are mapped to TC35854F internal CID as described in the *Mapping between ATM VPI/VCI and TC35854F CID* section.

BSC Cell Process

Sending BSC cells is triggered by the software through indirection operation and TC35854F generates requested BSC cells on the fly and puts the corresponding latest Tx_Count into the cell. BSC cells are not under credit control. If this connection is also a rate ABR, Nrm counter is not incremented when the BSC cell is sent. If this ABR also has other cells to send, this ABR is rescheduled in the next slot.

When a BSC cell is received, corresponding counters are updated according to equation [3] in the QFC specification. A BSU record is immediately composed for the connection.

Other Control Cells

All other controls are generated by the Lcp and put into OAM cell pool of RC_VCC (30) of that VP. RCC_VC is CBR and scheduled statically. The ACP and BSL cells are then served in the same way as for CBR OAM cells. For BSR cell, 2 bits in the cell header indicate if need to insert Tx_starttime, Rx_receivetime or Rx_forwardtime. When these control cells are received, they are treated by the RxIn as OAM cells except BSR indication cell (message type 6). For this cell, RxIn will insert Rx_receivetime field the value from BSR_timer. All limit counters are updated by the LCP from BSL cells.

Call Setup

Call setup in general should follow the procedures shown in Table 6 and Table 7 in the QFC specification.
One caution should be made. That is before connection [i] is opened, validEntry fields in both Tx CID record and Rx CID record for the connection [i] must be set to zero, besides setting all counters to zeros. These two fields are set to 1 only after all setup procedures have been finished. Setting these two fields to 1 is the last step in the Call Setup procedure. The reason is TC35854F does not have limit for each VC. All VCs of one VP have the same limit (CSR 62/63).

Call Clearing

Call clearing procedure in TC35854F has the following steps.

- Prior to sending a RELEASE message
    1. Invalidate the connection in both transmit and receive, and flush all buffered cells for the connection through following indirect operations in sequence:
        - INVALID_TX: write 14 to the portMode field (CSR 11) and CID to CSR 17.
        - DROP_TX_PKT: write 15 to the portMode field (CSR 11) and CID to CSR 17.

       This operation can be presented to TC35854F about 2 cell times after the previous request done.

- DROP_RX_PKT_INV: write 11 to the portMode field (CSR 11) and CID to CSR 17.

2. Increment BSU_Fwd_Count [link] and Fwd_Count [link] by the number of buffers freed through the following indirect operations:
   - SINGLE_CYCLE_RD_CM: write 1 to portMode field (CSR 11) and address of Tx CID record word1 to get listSize in transmit side.
   - SINGLE_CYCLE_RD_CM: write 1 to portMode field (CSR 11) and address of Rx CID record word1 to get listSize in receive side.
   - LINK_COUNT_OP: write 18 to portMode field (CSR 11) and set the wordAddr field accordingly to update BSU_Fwd_Count[link].
   - LINK_COUNT_OP: write 18 to portMode field (CSR 11) and set the wordAddr field accordingly to update Fwd_Count[link].
3. Reset all counters in Tx CID record and Rx CID record for connection[i] through indirect read/write memory operations.

- Upon receiving a RELEASE message and prior to sending the RELEASE COMPLETE message, the above steps should be performed, if not already done.

Generic Flow Control (GFC)

This section briefly describes the GFC implementation in TC35854F. For more details, see standard documentation "*ITU-T SG13, Revised version of I.150 TD41(Plen), November 1994 Geneva*" and "*ITU-T SG13, Revised version of I.361 TD42(Plen), November 1994 Geneva*".

GFC is the one way flow control scheme where the TC35854F is controlled equipment and the switch that TC35854F is connected is the controlling equipment.

In the GFC protocol, the assigned ATM connections are divided into two categories: controlled and uncontrolled. In TC35854F, all connections for CBR and VBR traffic are uncontrolled and the rest of the connections, i.e. ABR, UBR are controlled. Only default mode (one queue mode) in the GFC specification is supported by TC35854F.

The GFC field in ATM cell header contains 4 bits. The definition of each bit is decided by the characteristics of the equipment. The bits recognized by TC35854F are shown in Table 14 and Table 15. In the direction towards TC35854F, the combinations of values of the GFC field recognizable by TC35854F are show in Table 16. All other combinations are ignored by TC35854F. In the direction from TC35854F to the switch, the possible GFC field settings by TC35854F are shown in Table 17.

Table 14 GFC Field Definition from Controlling Equipment to TC35854F

Bit	Name	Value	Functions
0 (MSB)	HALT	0 - no halt 1 - halt	Halt stops TC35854F's transmission towards network of assigned ATM layers cells of any ATM connections.
1	SET_A	0 - not set 1 - set	This filed applies to controlled ATM connections for default mode. When SET is received, GFC_GO_CNT increments (CSR 9, bits <4:3>), but not larger than 2.
2	unused	0	Always 0 in the default mode
3 (LSB)	unused	0	Always 0.

Table 15 GFC Field Definition from TC35854F to Controlling Equipment

Bit	Name	Value	Functions
0 (MSB)	unused	0	Always 0.
1	CTRL_CONN	0 - uncontrolled 1 - controlled	This field indicates if the cell belongs to a controlled connection (1) or an uncontrolled connection (0). If it is a controlled connection, GFC_GO_CNT decrements (CSR 9, bits <4:3>). If this field is zero, no more controlled cells can be sent until it is set to bigger than zero.
2	unused	0	Always 0 in the default mode.
3 (LSB)	CTRL_EQUP	0 - uncontrolled 1 - controlled	This field indicates if the equipment is GFC controlled (1) or not GFC controlled (0). It is the copy of the GFC_ENABLE field in CSR 9 bit <1>.

Table 16 Combinations of bits in the GFC Field toward TC35854F

Combinations (bits 0 1 2 3)	Functions
0 0 0 0	no halt, not set
1 0 0 0	halt, not set
0 1 0 0	no halt, set
1 1 0 0	halt, set

Table 17 Possible GFC Field Settings by TC35854F

Combinations (bits 0 1 2 3)	Functions
0 0 0 0	TC35854F is uncontrolled.
0 0 0 1	TC35854F is controlled. Cell is unassigned or on an uncontrolled ATM connection.
0 1 0 1	TC35854F is controlled. Cell is on a controlled ATM connection.

The GFC_ENABLE field in CSR 9 bit<1> is set by the software. If it is 1, TC35854F will perform GFC functions. If it is 0, TC35854F will not perform GFC functions.

When a cell is received, if its HALT or SET_A bit is set, or if the GFC_VALUE field in CSR 9 bit<2> is 1, GFC_VALUE is set to 1. The HALT field is copied to the transmit field in CSR 9 bit <0>. If this bit is zero and GFC_ENABLE is set to 1, no more assigned cells can be sent. If the SET_A is 1, the GFC_GO_CNT field in CSR 9 bit <4:3> increments. The maximum value of the GFC_GO_CNT is 2. When a controlled cell is sent and GFC_ENABLE is set to 1, GFC_GO_CNT decrements. if GFC_GO_CNT is zero, no more controlled cells can be sent until it goes back to larger than zero.

If TC35854F is in QFC mode, link BSC cells are uncontrolled, since they are carried on CBR connections RCC_VC. VC BSC cells are controlled and carried on ABR connections.

Initialization

TC35854F requires many different steps to configure and initialize before operation. These steps can be summarized as:

- Initialize off-chip memory (tables and cell lists) using the cell memory write indirect operation
- Initialize on-chip memory (ready/credit vector, scoreboard) using indirect operations
- Configure CSRs for selected operation, enable operation

Many features of TC35854F can be configured in different ways - there is not a standard configuration. Variations of the memory tables might include space for AAL4 MIDs in the Rx tables, schedule tables of different sizes for different schedule granularity's, space for a second schedule table, and different splits of the cell pool between Tx and Rx. For FLOWmaster and QFC, the Rx cell pool is further partitioned.

Initialization of the off-chip memory consists mainly of writing initial values to all entries in the tables (or, as a minimum, any entry that could be used in the expected operation, as a read of an uninitialized entry could result in a cell memory parity error; for example, all entries in the Rx VCI table should be initialized, as a cell could be received on any VCI due to misconfiguration). Also, the cell data structures should be linked into two free cell lists by writing the cell headers with the address of the next cell in the list (essentially, write to address N with data N+7). If any ER circuits are to be supported, all tables for ER should be set correctly.

The Tx ready and scoreborad on-chip memories are not initialized by the chip reset, and should be cleared. For the Tx ready vectors, this requires that the bits for each CID/circuit be individually cleared with the txRdy indirect operation. The Rx FLOWmaster or QFC stuck circuits scoreboard can be initialized 16 bits at a time, so only 256 executions of the scoreboard indirect operations are required.

Initialize ER on-chip RAM: Not required. Work list entries always written internally before being read.

The only order significant to the setting of CSR values is that the configuration should be all set up before any of the process enables in CSR 0 are turned on (txInEnable, txOutEnable, rxInEnable, rxOutEnable, and linkEnable; alternately, for pkt mode, txPktEnable and rxOutEnable). The free cell list CSRs are set based on the allocation of the cell pool between Tx and Rx; the packet list CSRs can be left as their reset values.

Operation: Circuit Setup/Teardown and Monitoring

Once TC35854F is enabled for operation, the processor interface and CSRs will be used for ongoing tasks such as monitoring operation, setting up or tearing down circuits, updating credits, and handling interrupts.

Circuit setup consists of the following steps:

- Write the Tx CID table entry for the circuit.
- If the circuit is placed in the schedule table, then write a new schedule table and modify the schedTblSel field in CSR 0 bit<8> to point to it.
- Write the RxOut Packet Header table entry for the circuit.
- Write the Rx CID table entry for the circuit.

- If it is QFC circuit, setup should also follow the descriptions in the *Quantum Flow Control Operation* section.

Circuit teardown consists of the following steps:

- Invalidated the circuit through indirect operation INVALID_TX.
- Wait for about 2 cell times then move remaining Tx cells in the circuit to the free list through the indirect operation DROP_TX_PKT.
- If the circuit was scheduled, remove from the schedule table (by writing a new schedule table and flipping the schedTblSel field in CSR 0 bit<8>, or rewriting the old table in place).
- Mark the Rx CID table entry invalid by triggering the DROP_RX_PKT_INV indirect operation.
- Once the packet list is empty, or enough time has elapsed that any packets on the circuit have been forwarded, mark the RxOut Packet Header table entry invalid.

Monitoring could include:

- Scanning Rx CID entries for timed out packets - at each scan, read the Timer Msp CSR and scan for packets with timestamp that predate the current time by some fixed value determined by the interval between scans and the time-out threshold desired. When an old packet is found, discard by triggering the dropPkt indirect operation.
- Scanning Tx CID entries for timed out packets - at each scan, read Tx CID entry to get the address of the first cell in the list, read the cell head of the cell to get time stamp and read the Timer Msp CSR to check if the cell is timed out. If so, invalidate the circuit by issuing indirect operation INVALID_TX and drop the whole list through indirect operation DROP_TX_PKT.
- Scanning Tx CID entries for ADTF checking if there are any ER circuits running - at each scan, read the Timer Msp CSR and compare it with the value in the lastRm field in Tx CID record word 2. If it is over ADTF (500ms), the bit for this CID in the ready vector is set through Tx ready vector indirect operation.
- Collecting Tx and Rx cell counter values.

Credit updates are performed for VBR circuits, with a frequency and credit increment calculated for the particular circuit's traffic contract.

Interrupt handling would start with reading the interrupt registers to determine the cause. Many interrupts are just events to be counted. Some (primarily those in the TxIntr CSR 45) should be considered fatal events, indicating a malfunction of the chip, either due to a hardware fault or misconfiguration. See the CSR descriptions for details.

External Components

TC35854F requires external memory to operate, except in the case of packet mode (which only requires that the CMDT/CMPAR pins be hardwired to values for Packet Header Table entry 0). Many different fast SRAM components with access time equal to or faster than 15 ns will work with TC35854F.

Signal Descriptions

Table 18 TxIn Interface

Signal	Pin No.	I/O	Type	Name/Function
TABORT	170	O	TTL	**Transmit Abort:** This output signal is asserted high to indicate that TC35854F has aborted the current packet transmission. This may be due to a TPATH parity error, a TXCTL protocol error, or an abort indication in the end of packet. It is asserted for only one MAC interface cycle (which can be either 40ns or 80ns).
TXRDY	179	O	TTL	**Transmit Ready:** This output signal is asserted high to indicate that TC35854F is ready to accept additional data transfers. It is deasserted low when TC35854F is not ready, in which case the packet source should repeat the data on TPATH until this signal is asserted again.
TPATH<7:0>	171,172, 173,174, 175,176, 177,178	I	TTL	**Transmit Data Path:** This is an 8-bit input bus used to transfer data from a packet source to TC35854F. TC35854F will transfer the data to the link in a format selected by the many chip configuration controls.
TPRITY	169	I	TTL	**Transmit Parity:** Parity signal for TPATH. TC35854F can check for correct parity value.
TXCTL<1:0>	167,168	I	TTL	**Transmit Control:** This 2-bit input bus indicates the type of information present on TPATH<7:0> as follows: 00 FILLER (IDLE) 01 START 10 END 11 DATA

Table 19 TxOut Interface				
Signal	**Pin No.**	**I/O**	**Type**	**Name/Function**
TCTL_CLK	15	I	TTL	**Tx Link Clock:** Function depends upon operation mode: Pkt TXBCK:0 - 6.5 MHz byte clock driven by Bt8330. Every clock requires valid data. ATM TxClk - 25 MHz UTOPIA clock using rising edge SMDS
TSPE	18	I	TTL	**Tx Link Control Input :** for ATM or SMDS mode only: Use as TxClAv - when asserted (high), PHY can accept a byte (UTOPIA1) or a full cell(UTOPIA2, UTOPIA3, UTOPIA4).
TDATA<7:0>	21, 22, 23, 24, 25, 26, 27, 28	O	LVTTL	**Tx Link Data:** Byte-wide data to link.
SNDMSG	17	O	LVTTL	**Tx Link Control Output 0:** Function depends upon operation mode: Pkt Asserted high for valid data to link. ATM Use as TxSoc - asserted high in first byte of cell SMDS
SNDFCS	16	O	LVTTL	**Tx Link Control Output 1:** Function depends upon operation mode: Pkt Asserted high only to send abort indication. ATM Use as TxEnab*. Asserted low during sending of SMDS cell from TC35854F to PHY.

Please see UTOPIA specification for TxClk, TxClAv, TxSoc and TxEnab*.

Table 20 RxIn Interface				
Signal	**Pin No.**	**I/O**	**Type**	**Name/Function**
RCTL_CLK	14	I	TTL	**Rx Link Clock:** Function depends upon operation mode: Pkt RXBCK - 6.5 MHz byte clock driven by Bt8330. Every clock accompanies valid data. Selected as internal RCLK. ATM RxClk - 25 MHz UTOPIA clock SMDS
RPOH_FCS	13	I	TTL	**Rx Link Control Input 0:** Function depends upon operation mode: Pkt Use as VALFCS - indicates HDLC abort and CRC status. ATM Use as RxSOC - when asserted (high), indicates SMDS first byte of a cell on RDATA.
RSPE_IDL	4	I	TTL	**Rx Link Control Input 1:** Function depends upon operation mode: Pkt Use as IDLE - indicates HDLC packet framing. ATM Use as RxClav - when asserted (high), PHY has a byte (UTOPIA1) or a full cell (UTOPIA2, UTOPIA3, UTOPIA4) for TC35854F.
RDATA<7:0>	5 - 12	I	TTL	**Rx Link Data:** Byte-wide data from link.
RCELLHDR	3	O	LVTTL	**Rx Link Control Output 0:** for ATM or SMDS mode only: Use as RxEnab*. Always asserted low so that cells are sent from PHY with minimal latency. TC35854F can accept cells at line rate (but can have a FIFO error if cells accumulate, then are released faster than line rate).

Please see UTOPIA specification for RxClk, RxSoc,RxClav and RxEnab*.

Table 21 RxOut Interface

Signal	Pin No.	I/O	Type	Name/Function
RPRITY	193	O	TTL	**Receive Parity Signal:** This output indicates the parity of RPATH<7:0>. The polarity of this parity is programmable (CSR 0, bit 10, lcpPrtySel1).
RPATH<7:0>	183 - 186, 188, 189, 191, 192	O	TTL	**Receive Data Path:** This is an 8-bit output bus used to transfer packet data from TC35854F.
RCCTL<2:0>	194, 196, 197	O	TTL	**Receive Control:** This 3-bit bus indicates the type of data present on the RPATH<7:0> bus: EndDataDisc 111 FrameStatusDisc 110 StartData 101 EndDataKeep 011 FrameStatusKeep 010 Data 001 Filler 000
LDADDR	199	O	TTL	**Load Address:** This signal is asserted high in the first byte of a received packet and can be used to time CAM address lookups.
STALL	200	O	TTL	**Stall:** This signal is asserted low during filler cycles on the bus.

Table 22 Cell Memory Interface

Signal	Pin No.	I/O	Type	Name/Function
CMAD<19:0>	131,132,133,134 137,138,139,140, 141,144,147,148, 152,153,154,155, 156,159,160,161	O	LVTTL	**Cell Memory Address Bus:** Address lines to the cell memory SRAM.
CMWE0L CMWE1L	145,146	O	LVTTL	**Cell Memory Write Enable Strobes:** Asserted low to strobe write data from TC35854F into the cell memory SRAM. Two copies of an identical signal, to minimize delay due to fanout.
CMOEL	130	O	LVTTL	**Cell Memory Output Enable:** Asserted low in read cycles to enable cell memory SRAM to drive data onto CMDT signals.
CMDT<63:0>	35,36,37,38,40,41, 43,44,45,47,48,49, 50,52,55,56,57,58, 59,63,64,65,66,67, 69,70,72,73,74,77, 78,79,81,82,84,85, 86,87,88,93,94,95, 96,97,99,101,102, 103,104,106,107, 108,110,111,114, 115,116,117,118, 122,123,124,125, 126	I/O	TTL	**Cell Memory Data Bus:** Bi-directional data bus between TC35854F and the cell memory SRAM.
CMPAR<1:0>	34,128	I/O	TTL	**Cell Memory Parity:** Two bi-directional bits used to read/write parity in cell memory SRAM. CMPAR<1> represents even parity of the odd-numbered CMDT bits and CMPAR<0> represents even parity of the even-numbered CMDT bits.

Table 23 Clocks and Reset Interface

Signal	Pin No.	I/O	Type	Name/Function
RESETL	206	I	TTL	**Reset Low:** This an active-low reset signal which resets TC35854F to a default inactive state (refer to the CSR description for reset values). To reset TC35854F, this pin should be held low for at least two 40ns clock cycles. (Alternately, the RESET CSR bit can be used).
BYTECLK	205	I	TTL	**Byte Clock:** This is a 12.5 MHz input clock. It is used for byte transfers across the MAC interface when TC35854F is running in 100 Mb/s MAC mode, and for the processor interface timing when LCPMODE is 0. The maximum skew between BYTECLK and SYMCLKA is 10 ns. If LCPMODE=1 and MAC is run at 200Mb/s, BYTECLK is not needed - set BYTCLK = 1
SYMCLKA	163	I	TTL	**Clock A Signal:** This is a 25 MHz input clock. It is used by most of the internal state machines of TC35854F that run at 25 MHz. The maximum skew between SYMCLKA and SYMCLKB is 1 ns.
SYMCLKB	164	I	TTL	**Clock B Signal:** This is a 25 MHz input clock that lags SYMCLKA by 90 degrees (i.e., 10 ns). It is used by the cell memory, internal RAM and the MAC interfaces. The maximum skew between SYMCLKA and SYMCLKB is 1 ns.

Table 24 Node Processor Interface

Signal	Pin No.	I/O	Type	Name/Function
CE	217	I	TTL	**Chip Enable:** This signal selects the chip to participate as slave in a read or write bus transaction with the node processor. This signal is active low.
RW	218	I	TTL	**Read Write:** This signal determines whether the transaction is a read or write. A value of one indicates read and zero indicates write.
INTL	2	O	LVTTL	**Interrupt:** This signal indicates that TC35854F has an interrupt to be serviced by the node processor. This signal is active low.
NPDT <15:0>	219,220, 222,225, 226,227, 228,229, 230,232, 233,234, 235,237, 238,239	I/O	TTL	**Node Processor Data:** These pins form a bi-directional data bus connecting TC35854F to the node processor. The processor addressable CSR space of TC35854F is accessed by means of this bus (in conjunction with CE, RW, and NPAD*).
NPAD <6:0>	207,208, 212,213, 214,215, 216	I	TTL	**Node Processor Address:** These pins are the address lines which select a 16-bit word in the CSR space of TC35854F.
LCPMODE	182	I	CMOS	**LCP Operation Mode:** This selects the processor interface timing for 80ns or 40ns cycles. Set to 0 for 80ns (phase based on BYTECLK) or 1 for 40ns.

Table 25 Scan/Test Interface

Signal	Pin No.	I/O	Type	Name/Function
SCANMODL	204	I	TTL with pull-up	This is used for production test only. If 1, normal operation.
SCANENL	203	I	TTL with pull-up	This is used for production test only. If 1, normal operation.
OUTTRIL	202	I	TTL with pull-up	This is used for production test only. If 1, normal operation.
TESTOUT	201	O	LVTTL	This is used for production test only.

Preliminary

Timing Specifications

Clock Timing

Figure 10 and Table 26 describe the TC35854F clock timing.

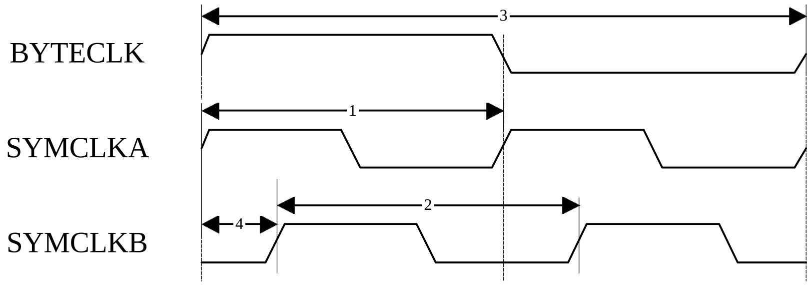


Figure 10 TC35854F Clocks

Table 26 TC35854F Clock Parameters

Number	Name	Value	Duty Cycle
3	BYTECLK period	80 ns	50 ± 10 %
1	SYMCLKA period	40 ns	50 ± 10 %
2	SYMCLKB period	40 ns	50 ± 10 %
4	SYMCLKB offset	10 ± 1.5 ns	-

NOTE: All timing requirements are preliminary and subject to change upon production release.

MAC Interface Timing

Preliminary

Transmit MAC Interface Timing (100 Mb/s)

Figure 11 and Table 27 describe the 100 Mb/s transmit MAC interface timing.

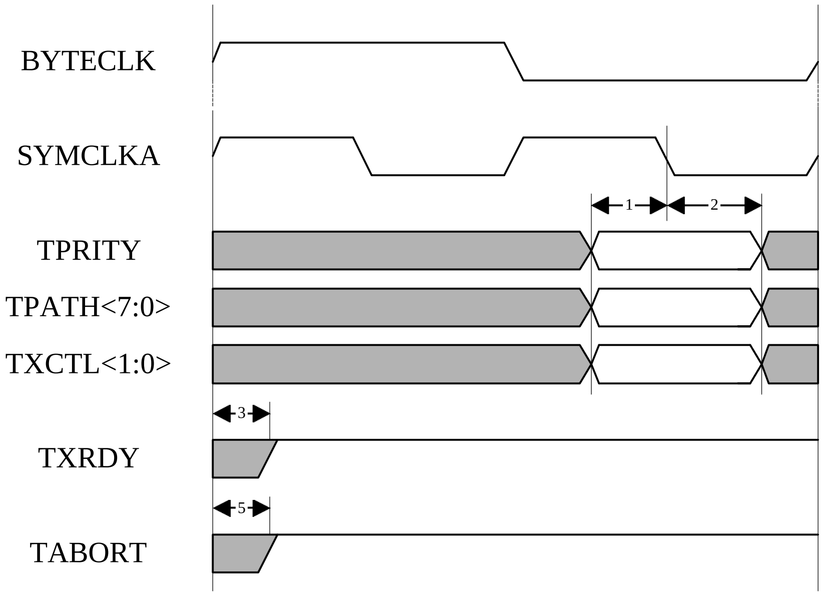


Figure 11 100 Mb/s Transmit MAC Interface Timing

Table 27 100 Mb/s Transmit MAC Interface Timing

Number	Name	Min	Max
1	Input signal setup time	5 ns	-
2	Input signal hold time	10 ns	-
3	Time to TXRDY asserted	-	15 ns
4	Time to TXRDY deasserted	-	15 ns
5	Time to TABORT asserted	-	15 ns
6	Time to TABORT deasserted	-	15 ns

NOTE: All time specifications with reference to SYMCLKA.
NOTE: All timing requirements are preliminary and subject to change upon production release.

Transmit MAC Interface Timing (200 Mb/s)

Preliminary

Figure 12 and Table 28 describe the 200 Mb/s transmit MAC interface timing.

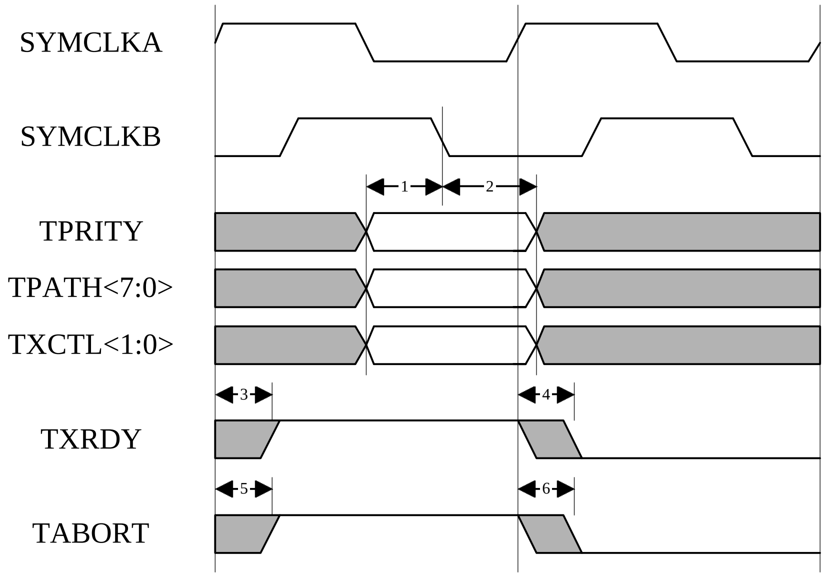


Figure 12 200Mb/s Transmit MAC Interface Timing

Table 28 200 Mb/s Transmit MAC Interface Timing			
Number	**Name**	**Min**	**Max**
1	Input signal setup time	5 ns	-
2	Input signal hold time	10 ns	-
3	Time to TXRDY asserted	-	15 ns
4	Time to TXRDY deasserted	-	15 ns
5	Time to TABORT asserted	-	15 ns
6	Time to TABORT deasserted	-	15 ns

NOTE: All timing requirements are preliminary and subject to change upon production release.

Preliminary

Receive 100 Mb/s MAC Interface Timing

Figure 13 and Table 29 describe the 100 Mb/s receive MAC interface timing.

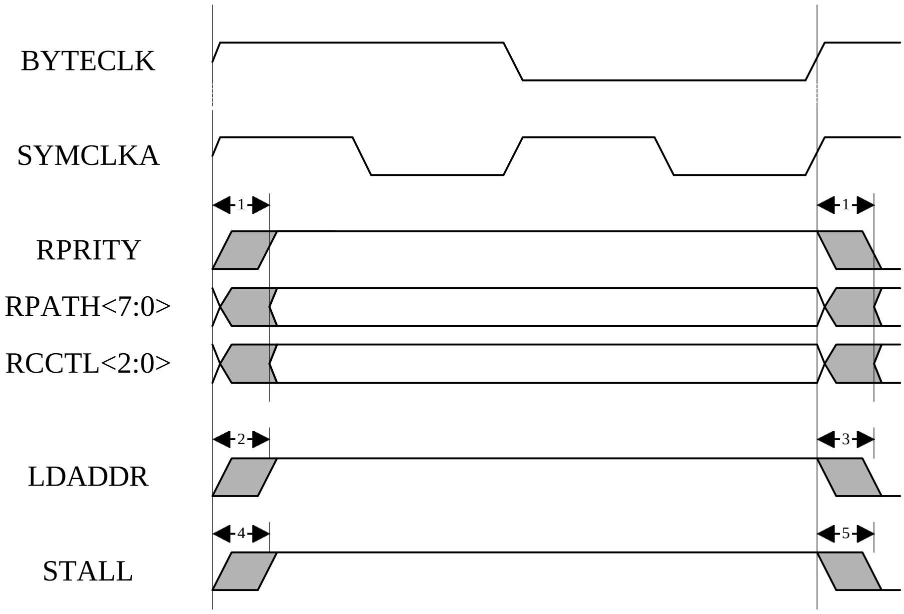


Figure 13 100Mb/s Receive MAC Interface Timing

Table 29 100 Mb/s Receive MAC Interface Timing			
Number	**Name**	**Min**	**Max**
1	Time to ouput signal stable	-	15 ns
2	Time to LDADDR asserted	-	15 ns
3	Time to LDADDR deasserted	-	15 ns
4	Time to STALL asserted	-	15 ns
5	Time to STALL deasserted	-	15 ns

NOTE: All time specifications with reference to SYMCLKA.
NOTE: All timing requirements are preliminary and subject to change upon production release.

Receive MAC 200 Mb/s Interface Timing

Preliminary

Figure 14 and Table 30 describe the 200 Mb/s receive MAC interface timing.

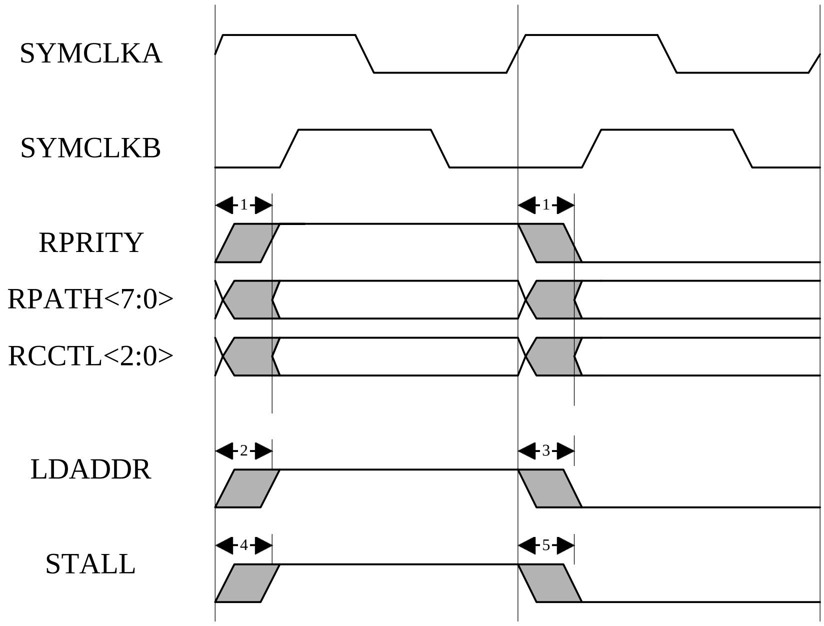


Figure 14 200Mb/s Receive MAC Interface Timing

Table 30 200Mb/s Receive MAC Interface Timing

Number	Name	Min	Max
1	Time to output signal stable	-	15 ns
2	Time to LDADDR asserted	-	15 ns
3	Time to LDADDR deasserted	-	15 ns
4	Time to STALL asserted	-	15 ns
5	Time to STALL deasserted	-	15 ns

NOTE: All timing requirements are preliminary and subject to change upon production release.

Link Interface Timing

Preliminary

Transmit Link Interface Timing

Figure 15 and Table 31 describe the transmit link interface timing.

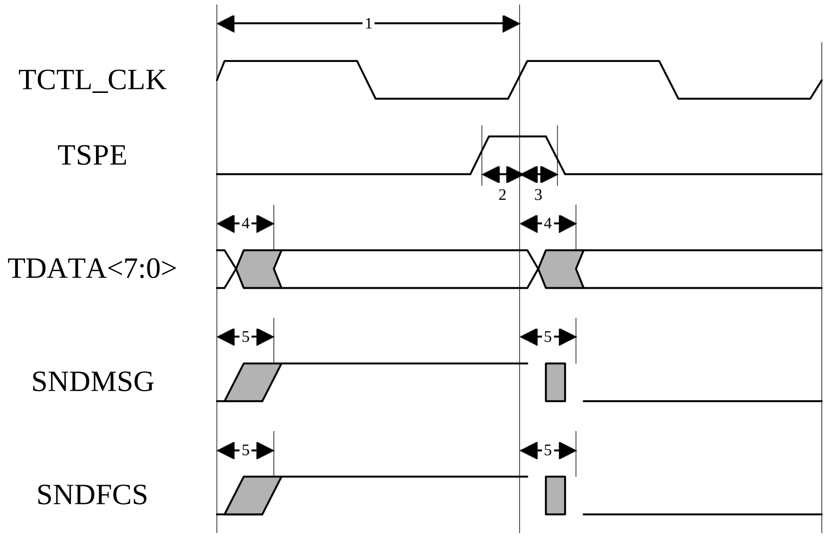


Figure 15 Transmit Link Interface Timing

Table 31 Transmit Link Interface Timing			
Number	**Name**	**Min**	**Max**
1	TCTL_CLK period	0 MHz	25 MHz
2	TSPE setup time	4 ns	-
3	TSPE hold time	1 ns	-
4	Time to TDATA driven	-	20 ns
5	Time to output signal driven	-	20 ns

NOTE: All timing requirements are preliminary and subject to change upon production release.

Receive Link Interface Timing

Preliminary

Figure 16 and Table 32 describe the receive link interface timing.

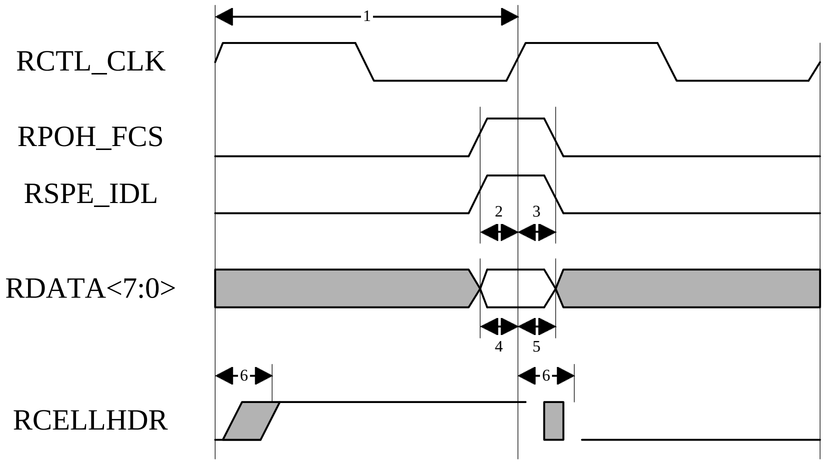


Figure 16 Receive Link Interface Timing

Table 32 Receive Link Interface Timing

Number	Name	Min	Max
1	RCTL_CLK period	0 MHz	25 MHz
2	Input signal setup time	5 ns	-
3	Input signal hold time	1 ns	-
4	RDATA setup time	5 ns	-
5	RDATA hold time	1 ns	-
6	Time to output signal driven	-	20 ns

NOTE: All timing requirements are preliminary and subject to change upon production release.

Node Processor Interface Timing

Preliminary

Figure 17 and Table 33 describe the node processor interface timing.

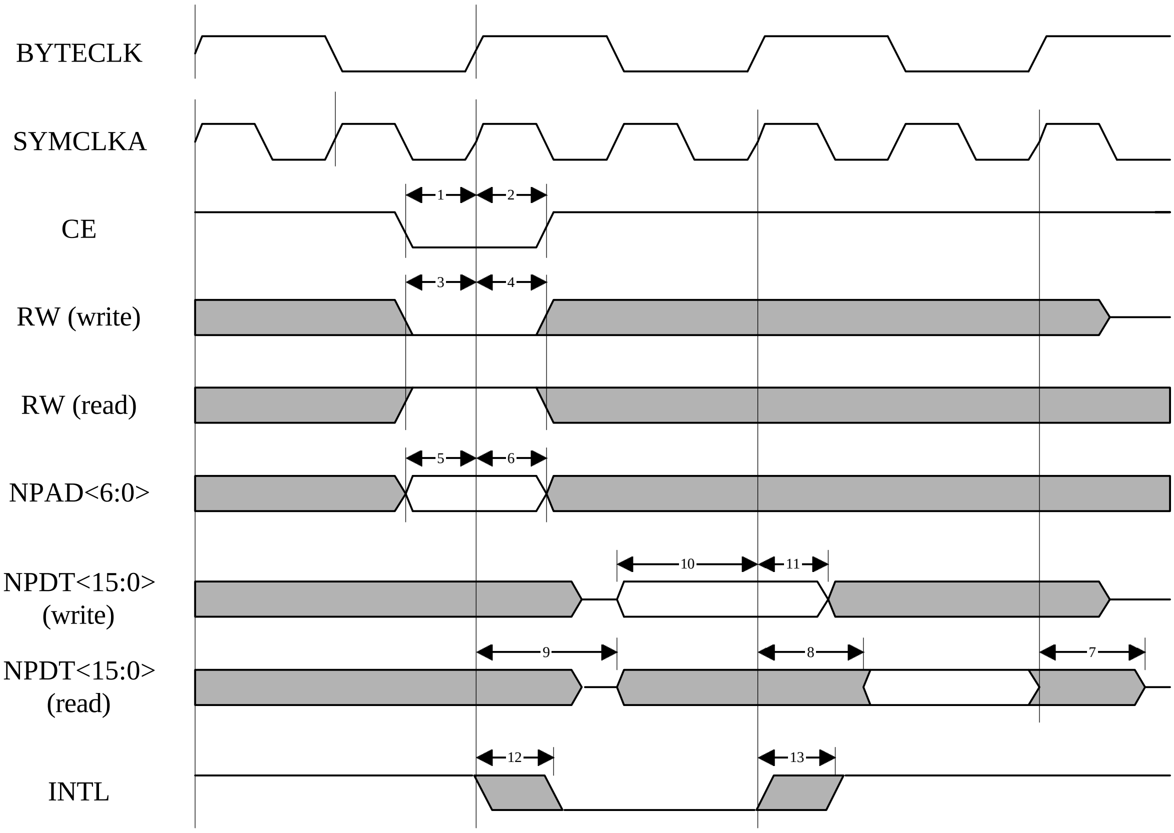


Figure 17 Node Processor Interface Timing - LCPMODE = 0

Node Processor Interface Timing

Preliminary

Figure 18 and Table 33 describe the node processor interface timing.

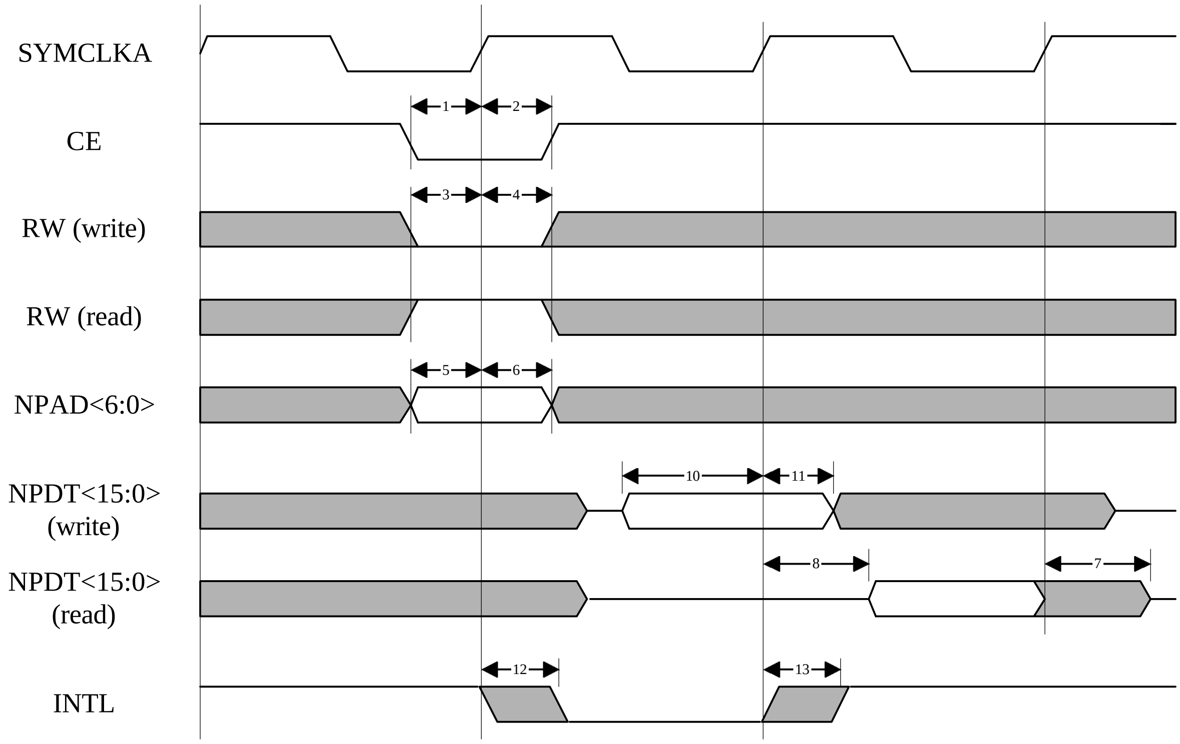


Figure 18 Node Processor Interface Timing - LCPMODE = 1

Node Processor Interface Timing (Cont.)

Preliminary

Table 33 Node Processor Interface Timing			
Number	**Name**	**Min**	**Max**
1	CE setup time	5 ns	-
2	CE hold time	5 ns	-
3	RW setup time	5 ns	-
4	RW hold time	5 ns	-
5	NPAD setup time	5 ns	-
6	NPAD hold time	5 ns	-
7	Time to NPDT high impedance	-	27 ns
8	Time to NPDT valid (read)	-	27 ns
9	Time to NPDT driven (read)	-	27 ns
10	NPDT setup time (write)	5 ns	-
11	NPDT hold time (write)	5 ns	-
12	Time to INTL asserted	-	20 ns
13	Time to INTL deasserted	-	20 ns

NOTE: All time specifications with reference to SYMCLKA, regardless of LCPMODE.
NOTE: All timing requirements are preliminary and subject to change upon production release.

Cell Memory Interface Timing

Preliminary

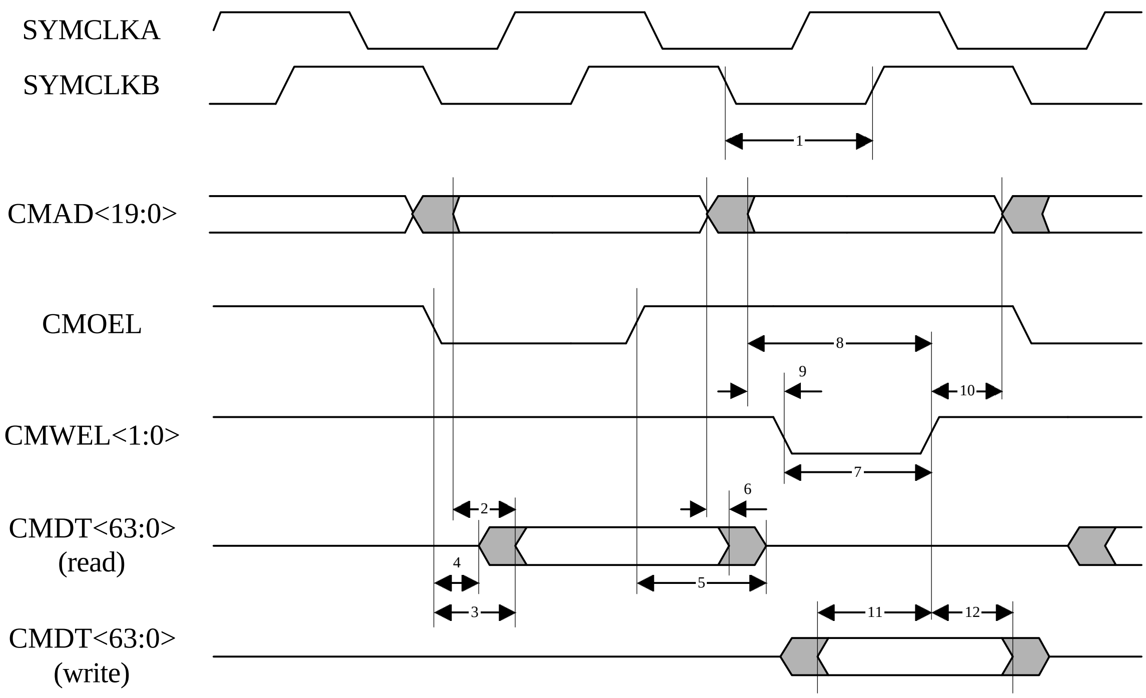


Figure 19 Cell Memory Interface Timing (Read/Write/Read Cycle)

Preliminary

Table 34 Cell Memory Interface Timing			
Number	Name	Min	Max
1	SYMCLKB low pulse width (tcp)		
2	Address Access Time	-	15 ns
3	Output Enable Access Time	-	15 ns
4	Output Enable Time from Output Enable	1 ns	-
5	Output Disble Time from Output Enable	-	8 ns
6	Output Data Hold Time from Address Change	5 ns	-
7	Write Pulse Width	tcp - 5 ns	-
8	Address Valid to End of Write	12 ns	-
9	Address Setup Time	0 ns	-
10	Write Recovery Time	0 ns	-
11	Data Setup Time	8 ns	-
12	Data Hold Time	0 ns	-

NOTE: All timing requirements are preliminary and subject to change upon production release.
NOTE: These timing are when 9 SRAM (including parity) are used.

External SRAM Memory Map and Data Structures

Name	Address Range		Size		Description
	4K VC	1K VC	4K VC	1K VC	
Packet Header Table	0x00000 - 0x03fff	0x00000 - 0x00fff	16,384 words	4096 words	Each VC has one entry in the table. Each entry consumes 4 words.
Transmit Circuit Identifier (CID) Table	0x04000 - 0x07fff	0x01000 - 0x01fff	16,384 words	4096 words	Each VC has one transmit CID record entry in the table. Each entry consumes 4 words.
OAM Cell Table	0x08000 - 0x081ff	0x02000 - 0x021ff	512 words		Contains up to 64 OAM cells that have been queued for transmission.
Receive Circuit Identifier (CID) Table	0x08200 - (txFListHeadInit - 1)	0x02200 - (txFListHeadInit - 1)	Variable (at least 3072 words for 1K VC and 12288 words for 4K VC)		Contains receive VCI/MID tables and CID record entries for all VCs. Each VCI/MID entry consumes 3 words.
Transmit Cell Buffer Pool	txFListHeadInit - (rxFListHeadInit - 1)		Variable		Contains transmit cell buffers. Each cell buffer consumes 7 words.
Receive Cell Buffer Pool	rxFListHeadInit - (taCellBase - 1) or 0x1f2bf		Variable		Contains receive cell buffers. Each cell buffer consumes 7 words.
Turned Around RM Cell Table (for ER support only)	0x1bf00 - 0x1deff (taTblBase - 0x1deff)	0x1d700 - 0x1deff (taTblBase - 0x1deff)	8192 words	2048 words	Each VC has one turn around RM cell entry. Each entry consumes 2 words.
Rate ABR Schedule Offset Table (for ER support only)	0x1df00 - 0x1dfff		256 words		Contains 64 entries for 6-bit mantissa from floating point rate expression. Each entry consumes 4 words.
Reserved Table (for ER support only)	x01e000 - 1f2bf		4800 words		*Must be initialized and reset to zero*
Transmit Static Schedule Table 1	0x1f2c0 - 0x1f95f		1696 words		Contains the traffic schedule tables.
Transmit Static Schedule Table2	0x1f960 - 0x1ffff		1696 words		Each word contains two schedule entries.

TxFListHeadInit initialized value of the transmit free list head given in CSR 22 and CSR 23.

RxFListHeadInit initialized value of the receive free list head given in CSR 28 and CSR 29.

taTblBase real base is given by memoryLimit (CSR 1) concatenated by taTblBase. For example, for 2MB memory, **taTblBase** = 0x3bf00 or 0x3d700 (4K and 1K circuits respectively).

Rate ABR Schedule Offset Table Base - real value for the base is given by concatenating 0x1df00 to the 3-bit memoryLimit (CSR 1) to form 20-bit full address. For example, for 4MB memory, Rate ABR Schedule Offset Table Base = 0x7df00

Static Schedule Table bases - real bases are given by memoryLimit (CSR1) concatenated by values shown here. For example, for 8MB memory, Static Schedule Table bases = 0xff2c0 and 0xff960.

The Turned Around RM Cell Table, Rate ABR Schedule Offset Table and Reserved Table are used for supporting ER only. If there is no ER circuit is running, these tables can be used for cell pools. The Reserved Table must be initialized and reset to zero when running ER circuits.

In operation, only one transmit static schedule table is used. The other is used for updating the scheduler.

Packet Header Table

The packet header table contains 4096 records, allowing a single record per receive circuit. Each record consumes 4 words as shown in Table 35 and all records are stored contiguously from the table base.

Table 35 Packet Header Record

Word 0	See table below
Word 1	Header Bytes 7-14
Word 2	Header Bytes 15-22
Word 3	Header Bytes 23-30

63	validEntry	31	Header Byte 3
62	addHdr	30	
61	padStrip	29	
60	hdrLen	28	
59		27	
58		26	
57		25	
56		24	
55	addHdrIfMc	23	Header Byte 4
54	reserved	22	
53	addCrc	21	
52	reverseMode	20	
51	checkFDDICrc	19	
50	stripHDLCCrc	18	
49	unused	17	
48		16	
47	Header Byte 1	15	Header Byte 5
46		14	
45		13	
44		12	
43		11	
42		10	
41		9	
40		8	
39	Header Byte 2	7	Header Byte 6
38		6	
37		5	
36		4	
35		3	
34		2	
33		1	
32		0	

<63> validEntry - When set, indicates whether a record contains valid data - if 0, then the data is not valid and (probably) should not have been referenced.

<62> addHdr - When set, indicates that the record contains a header that should always be added to the start of the packet.

<61> padStrip - When set, the first three bytes of the packet are stripped (for RFC 1483 support).

<60:56> hdrLen - Length (in bytes) of the header to be added - should not be zero if either addHdr or addHdrIfMc is set.

<55> addHdrIfMc - When set (and addHdr is 0), a header is added to packet if the individual/group (I/G) bit is set (one) in the DA (denoting a multicast address). DA field is considered to be bytes 2 through 7 after any RFC 1483 stripping, and the I/G bit is the MSB of the first byte of DA if the fddiReverse bit in the CSR control and test register (bit 5) is not set or the I/G bit is the LSB of the first byte of DA, if the fddiReverse bit is set to 1.

<54> reserved - This bit should be set to 0.

<53> addCrc - When set, a 32-bit CRC is calculated over the packet and appended to the end. Note that if a header is added by TC35854F, CRC calculation begins from the first byte of added header.

<52> reverseMode - When set, the FDDI CRC calculation covers the bit-reversed bytes of the DA and SA fields (bytes 2 through 13 of the packet). Otherwise, non-bit-reversed DA and SA fields are covered by the CRC computation.

<51> checkFDDICrc - When set, a 32-bit CRC calculated over the packet is compared to the last four bytes of the packet. The compare status is included as part of the frame status signaled after the packet.

<50> stripHDLCCrc - When set and the chip is in packet mode, the HDLC CRC at the end of the packet is stripped (4-byte stripping if the rxCrc32 field (bit 0 in the CSR configuration register) is set to 1; otherwise, 2-byte stripping).

The remaining fields (up to 30 bytes) can be added to the start of any packet.

Transmit Circuit Identifier Table

The transmit circuit identifier table contains 4096 records. There is a single record per transmit circuit. Each record consumes 4 words as shown in Table 36. All records are stored contiguously from the base of the table.

Table 36 Transmit Circuit Identifier Record

Word 0

63	pktHdrStrip	31	MID	AAL5Ctrl
62		30		
61		29		
60		28		
59		27		
58		26		
57		25		
56	crcStrip	24		
55	stdFddiMode	23		
54	smdsCrcMode	22		
53	reserved	21	reserved	
52	tAAL	20		
51	TailAddr	19		
50		18		
49		17		
48		16		
47		15	reserved	
46		14		
45		13		
44		12	isSmds	
43		11	ListSizeLimit	
42		10		
41		9		
40		8		
39		7		
38		6		
37		5		
36		4		
35		3		
34		2		
33		1		
32		0		

<63:57> pktHdrStrip - This field indicates that the number of bytes stripped off a packet when AAL segmentation is performed. Zero means no stripping.

<56> crcStrip - If this bit is set to 1, the 32-bit FDDI CRC is stripped from the packet when segmenting the packet. For short address packet format, if the circuit is SMDS, this bit must be set to 0. For other packet format, if the circuit is SMDS, this bit must be set to 1.

<55> stdFddiMode - When set, three bytes of zero padding are prefixed to the front of the packet (for RFC 1483 support) when the packet is segmented into AAL3/4 or AAL5 cells. Note that if this bit is set, any request at the MAC interface to append a FDDI CRC to a packet is ignored.

<54> smdsCrcMode - When set, the 32-bit SMDS CRC should be inserted into the SIP-3 packet if the CRC indication bit (CIB) in the packet is set. Ignored if isSMDS (bit 12) is not also set.

<52> tAAL - When set, AAL5 segmentation is performed; otherwise, AAL3/4 segmentation is performed.

<51:32> tailAddress - This field contains the 20-bit tail pointer to the linked list of cells for this circuit.

<31:22> / <31:16> AAL4mid / AAL5ctrl - This part of the word is shared. If AAL3/4 is chosen, this field represents the transmit MID value (10 bits). If AAL5 is chosen, it represents the AAL5 control field value (16 bits).

<12> isSmds - When set, it indicates that only SMDS traffic is transmitted on this circuit and the third and fourth bytes (after any stripping) are used as the packet length (to determine the end of data to be sent).

<11:0> listSizeLimit - indicates the maximum size of the linked list (in number of cell buffers) for this circuit. If the listSize is larger than the listSizeLimit when a new packet is started, the packet is dropped. This requires that listSizeLimit must be no larger than (0xfff - maxPktSize - 1)

Word 1

63	idleState
62	cidStopTraffic
61	AALcp
60	sendOamCell
59	oamIndex
58	
57	
56	
55	
54	
53	dataEfciBit
52	sendVpBSCcell
51	HeadAddr
50	
49	
48	
47	
46	
45	
44	
43	
42	
41	
40	
39	
38	
37	
36	
35	
34	
33	
32	

31	credits	expectNullCell	Not used
30		fmCredits	sendVcBSCcell
29			QFCcredAvail
28			bsuFwdCount
27			
26			
25			
24			
23			
22			
21			
20			reserved
19			
18			
17			
16	rRmAvail		
15	traffType		
14			
13	creditCtrl		
12	validEntry		
11	ListSize		
10			
9			
8			
7			
6			
5			
4			
3			
2			
1			
0			

<63> idleState - When set, this circuit is in idle state. Otherwise, it is in active state. This bit should be set to 1 for ALL transmit CID records as part of initialization.

<62> cidStopTraffic - When set, cells from this circuit are not transmitted. (This bit should be set through an indirect operation using CSR 18.)

<61> AALcp - This field is a copy of the AAL field in word 0. It is placed in word 1 for memory access optimization. *This field must set to 0 for the circuit of QFC RCC_VC (CSR 10) for each VP*.

<60> sendOamCell - When set, it indicates that an OAM cell has been loaded into the OAM table at a location given by oamIndex and that the cell is ready for transmission. (This bit and the oamIndex field (bits 59:54) should be set through an indirect operation using CSR 18).

<59:54> oamIndex - This field is an index to the location of a cell in the OAM table that is ready to be transmitted on this circuit.

<53> dataEfciBit - This field contains the EFCI in last received data cell. It is ignored if it is not an ER circuit.

<52> sendVpBscCell - For CBR circuit, this bit indicates if a BSC cell for this VP to which this circuit belongs, need to be transmitted. When this bit is set, the transmit engine then generates a BSC cell on fly with the latest txCount of the VP and clears this bit. This bit should be only set for RCC_VCI (CSR 80) of a VP.

<51:32> headAddress - It contains the 20-bit head pointer of the linked list for this circuit.

<31:17> This field is shared among token transmit control, FLOWmaster mode and QFC mode.

When used as token transmit control:

<31:17> credits - This field contains the number of transmit credits (tokens) for this circuit if this circuit is not a CBR. This field is decremented by one each time a cell is sent on this circuit. If there are zero credits in this field, the cell transmit engine will not send any cells on this circuit. This field can be updated at some periodic interval to reflect the desired sustained rate of traffic on this circuit. It can also be used for transmit cell accounting by keeping a running total of the number of credits used. For CBR circuit, this field is ignored.

When used for FLOWmaster:

<31> expectNullCell - This field indicates if this VC is scheduled and there is no credits for this VC, it is not an error if this bit is set to 1. This is used in ER operation above FLOWmaster flow control. After sending the previous cell consumed the last credit, the VC is still rescheduled, hoping before the next chance, the fmCredits would be updated. If it is not, then a NULL cell is sent and no interrupt is inserted.

<30:17> fmCredits - This field contains the credits field for FLOWmaster circuit. Every time a cell is sent, it decrements. It increments when an ACK is received.

When used for QFC:

<30> sendVcBSCcell - This field indicates if a BSC cell for this VC need to be transmitted. When this bit is set, the transmit engine then generates a BSC cell on fly with latest txCount information in the next word and clear this bit. This bit should never be set for RCC_VCI (CSR 10) of a VP. Set by indirect operation

<29> QFCcredAvail - This field is set by the transmit engine to indicate if there are more QFC VC credits for this circuit. The QFC VC credits is determined by txCount in word 2, bsuFwdCount and VC limit default (CSR 64, 65).

<28:21> bsuFwdCount. The bsuFwdCount works together with the txCount in next word and bslLimitVcDef[vp] (CSR 62-63) control transmission of this circuit. Only if txCount is equal to less than bslLimitVcDef[vp] + bsuFwdCount, a cell is transmitted and at the same time, txCount increments. The bsuFwdCount is updated at some periodic interval to reflect the desired sustained rate of traffic on this circuit.

<16> rRmAvail - For an ABR circuit, this field indicates if there is a turned-around RM cell available for this VC in the turned around RM cell table. After the turned around RM cell is sent in rate, this bit is cleared to zero. The bit is set to 1 when the reassembly engine receives a RM cell with its direction bit set to 1. Note, this bit is not cleared to zero when this RM cell is sent out-of-rate.

<15:14> traffType

<13:13> creditCtrl
These two fields work together to indicate the traffic type supported and traffic status shown as follows.

traffType	creditCtrl	Definitions
0 0	0	CBR traffic
0 0	1	FLOWmaster CBR traffic
0 1	x	ER traffic
1 0	x	QFC or FLOWmaster traffic
1 1	0	UBR traffic
1 1	1	VBR traffic

<12> validEntry - When set, it indicates whether a record contains valid data. If 0, then the data is not valid and should not have been referenced; the tiInvalidEntry interrupt is set and the packet is discarded.

<11:0> listSize - It contains the size (number of cell buffers) of the linked list for this circuit.

Word 2

63	Crm	31	txCount
62		30	
61		29	
60		28	
59		27	
58		26	
57		25	
56		24	
55	CrmCount	23	ICRexp
54		22	
53		21	
52		20	
51		19	ICRman
50		18	
49		17	
48		16	
47	firstTurn	15	
46	deltaTError	14	
45		13	
44		12	
43		11	
42		10	ignoreTimeStamp
41		9	skipService
40		8	lastRM
39	NrmCount	7	
38		6	
37		5	
36		4	
35		3	
34		2	
33		1	
32		0	

<63:56> Crm - This field contains the limit for a number of forward RM cells can be sent without rate reduction before receiving first returned RM cell.
<55:48> CrmCount - This field is the counter counting the number of forward RM cells sent before receiving first returned RM cell. When this matches the value of the Crm field, necessary rate reduction is required. When first returned RM cell is received, this field is cleared to zero.
<47> firstTurn - This one bit field indicates that returned RM cell has higher priority than data cells.
<46:40> deltaTError - This field records the offset between calculated scheduled time which is not an integer and actual scheduled time which is an integer for this VC. This offset is considered when next time this VC is rescheduled.
<39:32> NrmCount - This field contains the counter to count the number of cells sent between two forward RM cells when this circuit has ABR traffic and is under UNI 4.0 protocol control.
<31:24> txCount - This field contains QFC transmit counter, which works together with bsuFwdCount and limitCount in word 1 to control the cell rate of this circuit.
<23:18> ICRexp - This field contains the exponent field - 4 of initial cell rate in ER flow control. For

example, if ICR has exponent 8, this field is set to 4.
<17:11> ICRman - This field contains mantissa field of initial cell rate in ER flow.
<10> ignoreTimeStamp - This one bit field indicates that if time stamp should be checked for packets of this circuit. If this bit is set to 0, time stamp is checked and time-out packets are discarded. Otherwise, time stamp is not checked.
<9> skipService - This one bit indicate if this circuit is served every other service opportunities. This is mainly used to support 32kb/s rate circuit in TC35854F.
<8:0> lastRM - This field contains the time stamp when last forward RM cell is sent. Every time a forward RM cell is transmitted in rate, the transmit engine copies the value of CSR 78 bits <11:3> of the timer to this field and it is then used to determine if the current rate of the circuit should be reduced (ACR).

Word 3

63	nzACR	31	nzMCR
62	ACRexp	30	MCRexp
61		29	
60		28	
59		27	
58		26	
57	ACRman	25	MCRman
56		24	
55		23	
54		22	
53		21	
52		20	
51		19	
50		18	
49		17	
48	PCRexp	16	Unused
47		15	
46		14	
45		13	
44		12	
43	PCRman	11	CDF
42		10	
41		9	
40		8	RDFset
39		7	
38		6	
37		5	
36		4	RIFset
35		3	
34	Unused	2	
33		1	
32	validER	0	clearCrmCount

<63:49> - These three fields contains actual cell rate information in ER flow control:

<63> nzACR - This 1 bit field indicates if ACR is zero. 1 - non-zero and 0 zero.

<62:58> ACRexp - This field contains exponent field of actual cell rate.

<57:49> ACRman - This field contains mantissa field of actual cell rate.

<48:35> - These two fields contains peak cell rate information in ER flow control:

<48:44> PCRexp - This field contains exponent field of peak cell rate.

<43:35> PCRman - This field contains mantissa field of peak cell rate.

<32> validER - This one bit field is set to 1 only when validEntry in word 1 set to 1 and traffType in word 1 is set to 01 (ER traffic). For all other cases, it is set to zero.

<31:17> - These three fields contains minimum cell rate information in ER flow control:

<31> nzMCR - This 1 bit field indicates if MCR is zero. 1 - non-zero and 0 zero.

<30:26> MCRexp - This field contains exponent field of minimum cell rate.

<25:17> MCRman - This field contains mantissa field of minimum cell rate.

<11:9> CDFset - This field contains the cutoff decrease factor defined in the ATM Forum TM

specification. The settings to this field correspond to the following CDF values:

CDFset	0	1	2	3	4	7
CDF	1	1/2	1/4	1/8	1/16	0

<8:5> RDFset - This field contains the rate reduce factor defined in ATM TM specification. The value of RDF for this circuit is 1/ (2^n), where n is the value of RDFset.
<4:1> RIFset - This field contains the rate increase factor defined in ATM TM specification. The value of RIF for this circuit is 1/(2^n), where n is the value of RIFset.
<0> clearCrmCount - This field indicates that the CrmCount in word 2 should be cleared to zero.

Rate ABR Schedule Offset Table

This table is used to store the reciprocals of traffic rate. The rate is in the floating point format as shown below. Among 2 bytes of the rate representation, there are 5-bit exponent, 9-bit mantissa and 1-bit *nz* field.

resvd	1-bit *nz*	5-bit exponent *e*	9-bit mantissa *m*

According to the rate range supported by TC35854F, the exponent *e* has the range from 7 to 18 inclusive. TC35854F uses 6 most significant bits out of 9 bits of the mantissa to calculate the reciprocal. The rest 3 least significant bits of the mantissa are treated as zero. The reciprocals of the rate in TC35854F is in the fixed point format with 12 bits of integer and 9 bits of fraction. These reciprocals are used to calculate the offsets stored in this table. Each offset record in this table is referred to a reciprocal of one mantissa, which consumes 4 words for 12 different exponents. Each offset record as well as one word of a record are shown in Table 37 When rescheduling a rate ABR traffic, its next service time would be current time plus offset of its current rate from this table.

Table 37 Offset Record for One Mantissa (0 - 63)

Word 0	exponent *e* = 7	exponent *e* = 11	exponent *e* = 15
Word 1	exponent *e* = 8	exponent *e* = 12	exponent *e* = 16
Word 2	exponent *e* = 9	exponent *e* = 13	exponent *e* = 17
Word 3	exponent *e* = 10	exponent *e* = 14	exponent *e* = 18

63	integer1	31	fraction2
62		30	
61		29	
60		28	
59		27	
58		26	
57		25	
56		24	unused
55		23	integer3
54		22	
53		21	
52		20	
51	fraction1	19	
50		18	
49		17	
48		16	
47		15	
46		14	
45		13	
44	unused	12	
43	integer2	11	fraction3
42		10	
41		9	
40		8	
39		7	
38		6	
37		5	
36		4	unused
35		3	
34		2	
33		1	
32		0	

<63:52> integer1 - Contains the integer part of the offset for exponent 7 (8, 9, 10) and one mantissa.

<51:45> fraction1 - Contains the fraction part of offset for exponent 7 (8, 9, 10) and one mantissa.

<43:32> integer2 - Contains the integer part of the offset for exponent 11 (12, 13, 14) and one mantissa.

<31:25> fraction2 - Contains the fraction part of offset for exponent 11 (12, 13, 14) and one mantissa.

<23:12> integer3 - Contains the integer part of the offset for exponent 15 (16, 17, 18) and one mantissa.

<11:5> fraction3 - Contains the fraction part of offset for exponent 15 (16, 17, 18) and one mantissa.

OAM Cell Table

This table is used to store OAM or any other arbitrary cells that should be transmitted. An external firmware process loads an OAM cell record into this table at a specified index. This index is loaded into a record in the transmit CID table. The OAM cell record consumes 8 words as shown in Table 38.

The same data structure is used to store received OAM cells in the receive packet queue, except that only 7 words are used (same as data cells) and the data structure is overlaid on cells from the Receive cell pool, rather than entries in the OAM cell table.

Table 38 OAM Cell Record

Word 0	Cell Header - see table below
Word 1	Data Word
Word 2	Data Word
Word 3	Data Word
Word 4	Data Word
Word 5	Data Word
Word 6	Data Word
Word 7	Not used

63	ATM Cell Header (4 bytes)
62	
61	
60	
59	
58	
57	
56	
55	
54	
53	
52	
51	
50	
49	
48	
47	
46	
45	
44	
43	
42	
41	
40	
39	
38	
37	
36	
35	
34	
33	
32	

31	BSRind	
30	BSRconf	
29	cellType	
28	OAM marker	QFCctrl
27	unused	
26		
25		
24		
23		
22		
21		
20		
19	nextCellAddr	
18		
17		
16		
15		
14		
13		
12		
11		
10		
9		
8		
7		
6		
5		
4		
3		
2		
1		
0		

Word 0, <63:32> ATM OAM header - Contains the four most significant bytes of the OAM cell header. Bits <63:60> are the GFC field of the header, etc.

Word 0, <31> BSRind - If this bit is set, this OAM cell is QFC BSR indication cell. When the transmit engine sends this cell, the copy of the local 28-bit timer will be inserted into Tx_starttime field.

Word 0, <30> BSRconf - If this bit is set, this OAM cell is QFC BSR confirmation cell. When the transmit engine sends this cell, the copy of the local 28-bit timer will be inserted into Rx_forwardtime field.

Word 0, <29> cellType - Set to 1 to indicate that this is an OAM cell buffer. Otherwise, it is user data buffer. Used primarily with received cells to differentiate between normal packets and OAM cells in the Receive packet queue.

Word 0, <28> OAM marker - Set to 1 to indicate that this OAM cell buffer is in use, that is this OAM cell has not been transmitted by the transmit engine. It is cleared after the cell has been transmitted.

Note, word 0 <28> is read as ‘QFCctrl’ in the receive side. If this bit is set to 1, the cell is under QFC flow control.

Word 1-6, <63:0> - Data - Contains bytes 0-47 of the OAM cell payload. Byte 0 is located in word 1, bit positions <63:56>.

Turned Around RM Cell Table

The turned around RM cell table contains 4096 records. Each record is for one CID and contains 2 words as shown in Table 39. This table is written by the reassembly engine and read by the cell transmit engine. The reassembly engine writes only first 16-byte payload of a turned around RM cell into the table. When the cell transmit engine sends the cell, it generates the rest part of the ATM cell on fly with necessary changes made to the following fields: DIR, BN, CI, NI, ER.

Table 39 Turned Around RM Cell Record Table

Word 0	First 8 bytes of a RM cell payload
Word 1	Second 8 bytes of a RM cell payload

Receive Circuit Identifier Tables

Multilevel demultiplexing of received ATM cell head (VPI, VCI, and MID demultiplexing (if AAL3/4 is being used on this circuit) is necessary to get to the final receive circuit identifier.

TC35854F supports 4 VPIs chosen from full range of VPI field, i.e., 0 - 255. The VPI demultiplexing is done by matching received VPI field with 4 VPI indices. A three entries of the VPI mapping table (CSR 60, 61) maps real VPIs to VPI indices which are 0, 1, 2 and 3 with VPI 0 is always mapped to VPI index 0. If no matching can be found, the cell is discarded and an interrupt is asserted. The method mapping ATM VPI/VCI to TC35854F CID is described in the *Mapping between VPI/VCI and TC35854F CID* section.

The receive CID table consists of rxCidRec table and rxMidRec table necessary the proper circuit identifier (CID). The overall table and the lookup procedure is shown in Figure 20.

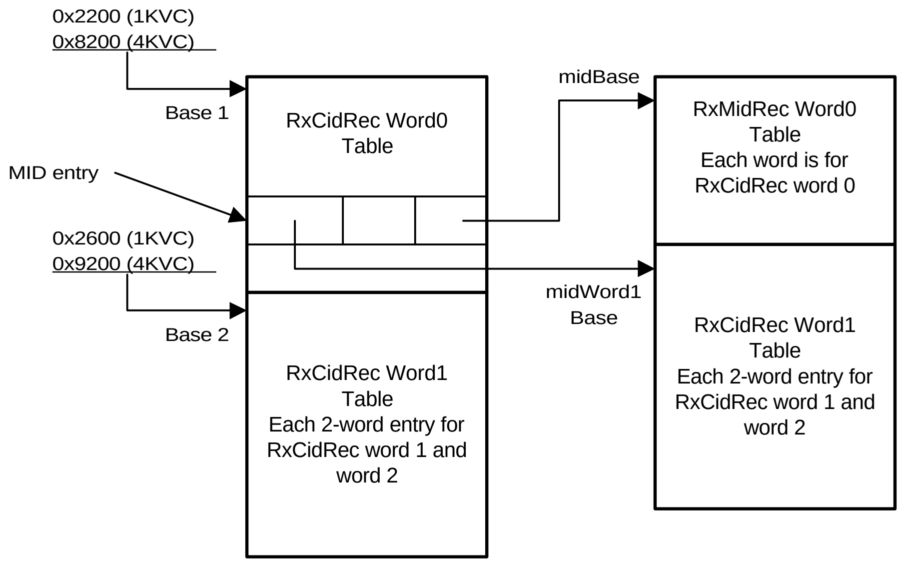


Figure 20 Receive CID Record Tables

The receive CID record tables have the following tables:

- A table called *rxCidRecWord0 Table* for the first entry of rxCidRec (word 0) for each circuit at base address 0x8200 for 4K VC or 0x2200 for 1K VC.
- A table called *rxCidRecWord1 Table* for the 2nd and third entries of rxCidRec (word 1 and word 2) for each circuit at base address 0x9200 for 4K VC or 0x2600 for 1K VC.
- Multiple receive MID tables, each table has two sub-tables: a table for *rxMidRecWord0 Table* for

the first entry of rxMidRec for each MID at base address midBase which is in the entry of rxCidRecWord 0 Table for its VC; and a table called *rxCidRecWord1 Table* for the second and third entries (word 1 and word 2) of rxMidRec for each MID at base address midWord1Base, which is also in the entry of rxCidRecWord0 Table for its VC.

In the case of FLOWmaster operation, there is only rxCidRec table. In the case of SMDS mode, there is only one entry in the rxCidRec table to give MID table bases: midBase and midWord1Base.

Each AAL5 circuit has its 3-word entry in the rxCidRec table, one word in rxCidRecWord0 Table and the rest in rxCidRecWord1 Table. For an AAL3/4 circuit, it has one word entry in the rxCidRecWord0 Table and each of its MID has 3-word entry in the MID record table, one word in rxMidRecWord0 Table and the rest in rxMidRecWord1 Table. When an ATM cell is received, the VCI boundary checking is done first by comparing VCI against the maximum VCI supported for different number of VPs supported (hard coded). The reassembly engine then gets the CID for this circuit by concatenating VP index with VCI. The resulted CID is used to obtain the pointers to the Rx CID table and/or MID table entry. Up to 1024 MIDs per VCI are possible. The MID record contains MID table base pointers and a limit indication. The MID field in the AAL3/4 subhead is added to the MID table bases to get an index to the CID record for this circuit. The address pointer for a CID to the rxCidRecWord0 Table is 0x8200 for 4K VC or 0x2200 for 1K VC plus CID value. The address pointer for a CID to the rxCidRecWord1 Table is 0x9200 for 4K VC (0x8200 + 0x1000) or 0x2600 (0x2200 + 0x400) for 1K VC plus 2 * CID value. The MID record formats in the rxMidRecWord0 Table and rxMidRecWord1 Table are exactly are the same as those in the rxCidRecWord0 Table and rxCidRecWord1 Table. The receive CID record is shown Table 40 in and Table 41.

Table 40 Receive MID Record

63	midWord1Base	31	unused
62		30	
61		29	midLimit
60		28	
59		27	
58		26	
57		25	
56		24	
55		23	
54		22	
53		21	
52		20	
51		19	midBase
50		18	
49		17	
48		16	
47		15	
46		14	
45		13	
44		12	
43	unused	11	
42		10	
41		9	
40		8	
39		7	
38		6	
37		5	
36		4	
35		3	
34	midActive	2	
33	Active	1	
32	validEntry	0	

<63:44> midWord1Base - Contains a 20-bit address pointer to the base of the second MID table associated with this circuit - rxMidRecWd1 Table, which is for word 1 and word 2 of the MID record. The MID records in the rxMidRecWd1 Table are stored in increasing order, i.e., address pointer of MID 0x0 in the rxMidRecWd1 Table is midWord1Base and address pointer of any MID in the rxMidRecWd1 Table is (midWord1Base + 2 * MID field).

<34:34> midActive - When set, indicates that at least one MID is active on this circuit. If this bit is asserted, the reassembly engine must lookup the MID table to find the appropriate CID record. This is always set for MID records.

<33:33> Active - When set, indicates that traffic received on this MID will not generate an "invalidMid" interrupt if the validEntry bit is not set.

<32:32> validEntry - When set, indicates that this entry is valid. When clear (0), the entry is not valid, cells on this VP are discarded, and an “invalidVpi” interrupt is set, unless the Active bit is set.

<29:20> midLimit - Contains a 10-bit value that indicates the limit of the MID table address space for this circuit. This number must be an *even* number for design optimization. The valid MID values are from 0 to midLimit - 1.

<19:0> midBase - Contains a 20-bit address pointer to the base of the first MID table associated with this circuit - rxMidRecWd0 Table, which is for word 0 of the MID record The MID records are stored in increasing order, i.e., address pointer of MID 0x0 is midBase and address pointer of any MID is (midBase + MID field) in the rxMidRecWd0 Table .

Table 41 Receive CID Record

Word 0

Bit	Field
63	unSentCount
62	
61	
60	
59	
58	
57	
56	
55	fwdCount
54	
53	
52	
51	
50	
49	
48	
47	seqNum
46	
45	
44	
43	timeStamp
42	
41	
40	
39	
38	AAL
37	
36	expectERRmCell
35	expectQFCRmCell
34	midActive
33	pktActive
32	validEntry

Bit	Field
31	flowOn
30	listSize
29	
28	
27	
26	
25	
24	
23	
22	
21	
20	
19	headAddr
18	
17	
16	
15	
14	
13	
12	
11	
10	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

<63:56> unSentCount - For any QFC or FLOWmaster circuit for which flowOn is not set, this field specifies the number of credits from data cells that are being held and that must be returned. (= Rx_Count - Fwd_Count)

<55:48> fwdCount - For any QFC circuit for which flowOn is set, this field specifies the number of cells forwarded through MAC interface.

<47:44> seqNum - This 4-bit field contains the sequence number of the current cell for AAL3/4 processing.

<43:39> timeStamp - This 5-bit field contains a timestamp that is used for packet reassembly time-out purposes, copied from CSR 78, Timer MSP, bits 10:6, when the packet starts reassembly. The external microprocessor is responsible for checking this field.

<38:37> AAL - This 2-bit field indicates the type of AAL processing that should be done on packets received on this circuit.

0 0	AAL3/4 processing
0 1	AAL5 processing
1 0	SMDS and AAL3/4 processing
1 1	OAM cell processing

<36> expectERRmCell - When set, it indicates that this circuit is under the explicit rate (ER) flow control and ER RM cells are expected to come in.

<35> expectQFCRmCell - When set, it indicates that this circuit is under the QFC flow control and QFC RM cells are expected to come in.

<34> midActive - Set to 0 for RxCid records reached directly from VCI lookup after VPI; set to 1 for RxCid records reached through MID lookup.

<33> pktActive - For circuits with validEntry set, this field indicates that a packet is currently being reassembled on this circuit (when set). When validEntry is not set, then this bit indicates whether cells seen on this VCI should cause an “invalidVci” interrupt.

<32> validEntry - When set, indicates that this entry is valid. When clear (0), the entry is not valid, cells on this VCI are discarded, and the “invalidVci” interrupt is set, unless the Active bit is set.

<31> flowOn - Set by RxIn to mark a “flowing circuit”, on which a packet reassembly is guaranteed to complete in the FLOWmaster cell pool and credits are returned for any received cell.

<30:20> listSize - This field specifies the number of cells received in the current packet and in the linked list.

<19:0> HeadAddr - This-20 bit field contains the pointer to the head of the linked list used in reassembling packets on this circuit.

Word 1

Bit	Field
63	crc32State
62	
61	
60	
59	
58	
57	
56	
55	
54	
53	
52	
51	
50	
49	
48	
47	
46	
45	
44	
43	
42	
41	
40	
39	
38	
37	
36	
35	
34	
33	
32	

Bit	Field
31	violThresh
30	flowCircuit
29	SMDScrcActive
28	waitBsc
27	N2Count
26	
25	
24	
23	
22	
21	
20	
19	tailAddr
18	
17	
16	
15	
14	
13	
12	
11	
10	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

<63:32> CrcState - This 32-bit field contains the CRC state for AAL5 CRC or SMDS CRC processing.

<31> violThresh - When set, this indicates that this circuit can start reassembly of new packets regardless of whether the Rx free list cell count is under the threshold set by minRxFrCell (CSR 19, <7:0>).

<30> flowCircuit - If FLOWmaster field (CSR 3, bit 6) is set, this bit indicates if the circuit obeys FLOWmaster rules and uses the FLOWmaster cell pool (set to 1) or not (set to 0). If QFC field (CSR 3, bit 5) is set, this bit indicates if the circuit obeys QFC rules and uses the QFC cell pool (set to 1) or not (set to 0). When not set, the circuit uses the cell pool without FLOWmaster. This field must be 0 for links without FLOWmaster or QFC.

<29> SMDScrcActive (also AAL5passALL) - This 1-bit field has a dual function. If the AAL field is set to SMDS, then this field is set to the value of the CIB bit in the current packet (if set, then the 32-bit SMDS CRC is checked). If the AAL field indicates AAL5 processing, then it indicates that the

complete AAL5 frame (including padding, control, length, and CRC) should be passed to the packet relay engine when this bit is set.

<28> waitBsc - This 1-bit field indicates if all cells should be discarded for this circuit in QFC mode (CSR 3, bit 5). If this bit is set to 1, all cells of this circuit are discarded and no interrupts are generated until a BSC cell for this circuit is received. Upon receiving the first BSC cell for this circuit, this bit is cleared to zero and all cells are processed normally. This can be used for initialization when automatically setting up QFC PVC circuit.

<27:20> N2Count - For any QFC circuit for which flowOn is set, this field specifies the number of cells forwarded through MAC interface since last time a BSU cell element is composed. When this value matches N4 (CSR 59) a BSU cell element is composed and this field is cleared.

<19:0> tailAddr -This 20-bit field contains the pointer to the tail of the linked list used in reassembling packets on this circuit.

Word 2

63	HdrIndex	31	
62		30	
61		29	
60		28	
59		27	
58		26	
57		25	
56		24	
55		23	
54		22	
53		21	
52		20	
51	unsentOtherCredits	19	
50		18	
49		17	
48		16	
47		15	
46		14	
45		13	
44		12	
43	putInPktList1	11	
42	reserved	10	
41		9	
40		8	
39		7	
38		6	
37		5	
36		4	
35		3	
34		2	
33		1	
32		0	

<63:52> HdrIndex - This 12-bit field contains the index to the packet header table to be used for all packets reassembled on this circuit.

<51:44> unsentOtherCredits - This 8-bit field contains unsent credits for non-data cells, including OAM cells, ER RM cells.

<43> putInPktList1 - This bit indicates if packets of this circuit should put to the higher priority queue.

Transmit Schedule Tables

The transmit schedule tables contains five tables. One is for CBR scheduling and the rest is for ABR services scheduling. In the CBR schedule table, Each 64-bit word contains two records as shown in Table 42. Every cell time, a transmit schedule record is read. A circuit identifier in the record is chosen according to the traffic priority as described in the Cell Transmit Engine (TxOut) section if there is data ready to send. If no CID is ready, an unassigned cell is sent. Wraparound on the table is indicated in the control field.

The scheduling tables for ABR services are in fixed bases and sizes. The transmit engine manages these tables to give ABR circuits services compliant to the ATM Forum and QFC specifications.

The memory map for the scheduling tables have room for two CBR schedule tables. Both of them have fixed bases. One is for current usage and the other one is used to modify the schedule table. One CSR bit schedTblSel indicates which table is in use currently. When the CBR table is wrapped around, the transmit engine looks schedTblSel bit to choose which table is used for next time.

Table 42 Transmit Schedule Record

Bit	Field	Bit	Field
63	VPI1	31	VPI2
62		30	
61	CBRcid1	29	CBRcid2
60		28	
59		27	
58		26	
57		25	
56		24	
55		23	
54		22	
53		21	
52		20	
51		19	
50		18	
49	VBRcid1	17	VBRcid2
48		16	
47		15	
46		14	
45		13	
44		12	
43		11	
42		10	
41		9	
40		8	
39		7	
38		6	
37	ABRckt1	5	ABRckt2
36	reserved	4	reserved
35		3	
34		2	
33		1	
32	ctrl1	0	ctrl2

<63:62> VPI1 - This field contains the CBR VPI which is assigned the record 1 in the word.

<61:50> CBRcid1 - This field contains a VC which has the highest priority to be served in this time slot. The VC scheduled in this field can be a CBR VC, an ABR VC for its MCR portion, or a VBR VC for its sustained rate portion.

<49:38> VBRcid1 - This field contains a VC which has the second highest priority to be served in this time slot, which could be any CBR or VBR VC for its peak rate portion.

<37> ABRckt1 - When set, this field indicates that the VC scheduled in the CBRcid1 field is an ABR circuit.

<32> ctrl1 - This field indicates wrap-around. If it is 1, the transmit engine will look at the first entry of the CBR table in the next time slot. Otherwise, the next entry will be looked at.

<31:30> VPI2 - This field contains the CBR VPI which is assigned the record 2 in the word.

<29:18> CBRcid2 - This field contains a VC which has the highest priority to be served in this time slot. The VC scheduled in this field can be a CBR VC, an ABR VC for its MCR portion, or a VBR VC for its

sustained rate portion.
<17:6> VBRcid2 - This field contains a VC which has the second highest priority to be served in this time slot, which could be any CBR or VBR VC for its peak rate portion.
<5> ABRckt2 - When set, this field indicates that the VC scheduled in the CBRcid2 field is an ABR circuit.
<0> ctrl2 - This field indicates wrap-around. If it is 1, the transmit engine will look the first entry of the CBR table in the next time slot. Otherwise, the next entry will be looked.

Transmit/Receive Cell Buffer Pools

The transmit and receive cell buffer pools contain lists of cell buffers that are chained together. Multiple linked lists can exist within each pool at any given time. Each active transmit and receive circuit contains its own linked list. A linked list is characterized by the following parameters:

- Head pointer
- Tail pointer
- List size

These parameters are stored in the transmit and receive CID records for each circuit. Processes add cell buffers to the tail and consume cell buffers from the head of the linked list. In addition to linked lists per transmit/receive circuits, there are three other important lists used:

- Transmit free list
- Receive free list
- Receive packet list

When a cell buffer is to be added to the tail of an active circuit/packet linked-list, it is taken from the head of the appropriate free list. Similarly, if a cell buffer is to be consumed from the head of the active circuit/packet linked-list, it is returned to the tail of the appropriate free list. When the reassembly engine completes reassembly of a packet, it moves all of the cell buffers associated with that packet to the tail of the receive packet list. This packet list is serviced by the packet relay engine, which returns the cell buffers to the receive free list when the cell buffer payloads are sent out the RxOut interface. The cell buffers are returned to the free list one at a time.

When TC35854F is initialized, all of the linked lists parameters should be set to the appropriate values, i.e., the circuit lists and packet list should set the head and tail pointers to a value of zero and the list sizes should also be set to zero. The transmit and receive free cell lists must be initialized such that all of the cell buffers in the pool are chained together and the resulting head pointers, tail pointers, and list sizes are placed in the appropriate CSRs.

The structure of a transmit/receive cell buffer is shown in Table 43. The size of a cell buffer is 56 bytes. Two flavors exist:

- Data cell buffer
- OAM cell buffer (these cells use the structure show under the OAM table)

Table 43 Transmit/Receive Cell Buffers

Word 0	Cell Header - see table below
Word 1	Data Word
Word 2	Data Word
Word 3	Data Word
Word 4	Data Word
Word 5	Data Word
Word 6	Data Word

Data Cell Buffer Header

63	hdrIndex
62	
61	
60	
59	
58	
57	
56	
55	
54	
53	
52	
51	reserved
50	
49	
48	txTimeStamp (tx only, reserved on rx)
47	
46	
45	
44	
43	
42	
41	
40	
39	reserved
38	
37	
36	
35	
34	
33	
32	

31	bme
30	
29	cell type
28	flowCid
27	reserved
26	cellDiscard
25	cellLength
24	
23	
22	
21	
20	
19	nextCellAddr
18	
17	
16	
15	
14	
13	
12	
11	
10	
9	
8	
7	
6	
5	
4	
3	
2	
1	
0	

<63:52> hdrIndex - This 12-bit field contains the index to the packet header table.

<48:40> txTimeStamp - This field records the time when this cell is put into the cell memory by the segment engine which copies the value of bits <11:3> of the Timer Msp register in (CSR 78) to this field. When the cell transmit engine transmits the cell, it checks the timeStamp against the current value of the bits <11:3> of the Timer Msp register (CSR 78). If it is older than 2 seconds, the cell is discarded.

<31:30> bme -This 2-bit field indicates the begin, middle, or end of the packet. It is also used to indicate a single segment packet.

0 0	middle of packet
0 1	end of packet
1 0	begin of packet
1 1	single segment packet

<29:29> cellType - This field indicates the cell type and the record format. If 0, it indicates a normal cell (described as this cell format); if 1, it indicates an OAM cell (with the format shown above).

<28:28> flowCid - This bit is a FLOWmaster/QFC indicator, which is used to trigger incrementing QFC N2count and fwdCount, or returning credit in FLOWmaster mode.

<26:26> cellDiscard - This field indicates if this cell should be discarded by the packet relay engine.

<25:20> cellLength - This 6- bit field contains the length of the data field (in bytes) in the cell buffer.

<19:0> nextCellAddr - This 20-bit field contains the pointer to the next cell buffer in the linked list.

Control/Status Register Descriptions

The contents of the control status registers are shown in Table 44 through Table 125. The LCP and TC35854F columns of the tables indicate whether fields are read/write (RW), read-only (RO), or write-only (WO) by the microprocessor and TC35854F, respectively. The following table lists the control status register and its address offset.

CSR Number and Name	Address offset	Table number
CSR 0 Control	0x000	Table 44
CSR 1 Test	0x002	Table 45
CSR 2 Bridging Circuit Indicator	0x004	Table 46
CSR 3 Configuration	0x006	Table 47
CSR 4 Maximum Packet Length	0x008	Table 48
CSR 5 Packet Processing	0x00A	Table 49
CSR 6 DA III	0x00C	Table 50
CSR 7 DA II	0x00E	Table 51
CSR 8 DA I	0x010	Table 52
CSR 9 GFC Control Register	0x012	Table 53
CSR 10 Block Address	0x014	Table 54
CSR 11 Indirect Operations	0x016	Table 55
CSR 12 Data Word 0	0x018	Table 56
CSR 13 Data Word 1	0x01A	Table 57
CSR 14 Data Word 2	0x01C	Table 58
CSR 15 Data Word 3	0x01E	Table 59
CSR 16 Status	0x020	Table 60
CSR 17 CID Register	0x022	Table 61
CSR 18 Credits Register	0x024	Table 62
CSR 19 Min Rx Free Cells	0x026	Table 63
CSR 20 TxFreeList Head Lsp	0x028	Table 64
CSR 21 TxFreeList Head Msp	0x02A	Table 65
CSR 22 TxFreeList Tail Lsp	0x02C	Table 66
CSR 23 TxFreeList Tail Msp	0x02E	Table 67
CSR 24 TxFreeList Size Lsp	0x030	Table 68
CSR 25 TxFreeList Size Msp	0x032	Table 69
CSR 26 RxFreeList Head Lsp	0x034	Table 70
CSR 27 RxFreeList Head Msp	0x036	Table 71
CSR 28 RxFreeList Tail Lsp	0x038	Table 72
CSR 29 RxFreeList Tail Msp	0x03A	Table 73
CSR 30 RxFreeList Size Lsp	0x03C	Table 74
CSR 31 RxFreeList Size Msp	0x03E	Table 75
CSR 32 RxPacketList1 Head Lsp	0x040	Table 76
CSR 33 RxPacketList1 Head Msp	0x042	Table 77
CSR 34 RxPacketList1 Tail Lsp	0x044	Table 78
CSR 35 RxPacketList1 Tail Msp	0x046	Table 79
CSR 36 RxPacketList2 Head Lsp	0x048	Table 80
CSR 37 RxPacketList2 Head Msp	0x04A	Table 81

CSR 38	RxPacketList2 Tail Lsp	0x04C	Table 82
CSR 39	RxPacketList2 Tail Msp	0x04E	Table 83
CSR 40	Rx Active FLOWmaster pkts	0x050	Table 84
CSR 41	Non FLOWmaster Free Cells	0x052	Table 85
CSR 42	Static Credits Committed	0x054	Table 86
CSR 43	Dynamic Cells Committed	0x056	Table 87
CSR 44	AAL5 Error CID Register	0x058	Table 88
CSR 45	Tx Interrupts	0x05A	Table 89
CSR 46	Rx Interrupts	0x05C	Table 90
CSR 47	Link Interrupts	0x05E	Table 91
CSR 48	RxIn Credit Interrupts	0x060	Table 92
CSR 49	Tx Interrupt Mask	0x062	Table 93
CSR 50	Rx Interrupt Mask	0x064	Table 94
CSR 51	Link Interrupt Mask	0x066	Table 95
CSR 52	RxIn Credits Interrupts Mask	0x068	Table 96
CSR 53	Tx Cell Counter	0x06A	Table 97
CSR 54	Rx Cell Counter	0x06C	Table 98
CSR 55	VP 3 Bandwidth	0x06E	Table 99
CSR 56	VP 2 Bandwidth	0x070	Table 100
CSR 57	VP 1 Bandwidth	0x072	Table 101
CSR 58	VP 0 Bandwidth	0x074	Table 102
CSR 59	QFC N4 Register	0x076	Table 103
CSR 60	VPI Images Register 1	0x078	Table 104
CSR 61	VPI Images Register 2	0x07A	Table 105
CSR 62	BSL VC Limit Default 0	0x07C	Table 106
CSR 63	BSL VC Limit Default 1	0x07E	Table 107
CSR 64	BSL Link Limit VP 0 Lsp	0x080	Table 108
CSR 65	BSL Link Limit VP 0 Msp	0x082	Table 109
CSR 66	BSL Link Limit VP 1 Lsp	0x084	Table 110
CSR 67	BSL Link Limit VP 1 Msp	0x086	Table 111
CSR 68	BSL Link Limit VP 2 Lsp	0x088	Table 112
CSR 69	BSL Link Limit VP 2 Msp	0x08A	Table 113
CSR 70	BSL Link Limit VP 3 Lsp	0x08C	Table 114
CSR 71	BSL Link Limit VP 3 Msp	0x08E	Table 115
CSR 72	N2 Value For VC Register 1	0x090	Table 116
CSR 73	N2 Value For VC Register 2	0x092	Table 117
CSR 74	N2 Value For Link Register 1	0x094	Table 118
CSR 75	N2 Value For Link Register 2	0x096	Table 119
CSR 76	N2 Value For Link Register 3	0x098	Table 120
CSR 77	N2 Value For Link Register 4	0x09A	Table 121
CSR 78	Timer Msp	0x09C	Table 122
CSR 79	Timer Lsp	0x09E	Table 123
CSR 80	QFC RCC_VC Register	0x0A0	Table 124
CSR 81	Bottom Rate Registerr	0x0A2	Table 125

Table 44 CSR 0 Control

Address Offset: 0x000

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RO	0	**fddiComp**	7	RW	RO	0	**intrClrMode**
14	RW	RO	1	**mac40**	6	RW	RO	0	**NrmCountSel**
13	RW	RO	0	**linkEnable**	5	RW	RO	0	**txInEnable**
12	RW	RO	0	**resetEnable**	4	RW	RO	0	**txOutEnable**
11	RW	RO	0	**txPrityCk**	3	RW	RO	0	**rxInEnable**
10	RW	RO	1	**lcpPrtySel1**	2	RW	RO	0	**rxOutEnable**
9	RW	RO	1	**isLifoFlag**	1	RW	RO	0	**txPktEnable**
8	RW	RO	0	**schedTblSel**	0	RW	RO	0	**loopbackEnable**

<15> fddiComp - FDDI DA Comparison Procedure Control - This bit selects the FDDI destination address (DA) mapping to CID procedure in the TxIn process. If this bit is set, and if 35 bits <46:12> for supportVc bit in CSR 1 is set 1, or 37 bits <46:10> for supportVc in CSR 1 is set to 0, of the DA match with daConst in CSR 6, CSR 7 and CSR 8, or then bits <11:0> for supportVc set to 1, or bits <9:0> for supportVc set to 0, of the DA are used to select the transmit virtual circuit. All other DAs select the default VC defined in bridgeVc field in CSR 2. When this bit is 0, the bridgeVc field in CSR 2 defines the transmit virtual circuit.

0 The 10 /12 least significant bits of the DA always selects the transmit circuit.
1 If the comparison fails, bridgeVc is used. Only if the comparison matches are the 10/12 least significant bits used as the transmit circuit.

<14> mac40 - MAC Interface Cycle Time Control - This bit controls the cycle time of the byte transfers across the MAC interface on both transmit and receive.

0 80 ns cycle time (12.5 MHz). This results in a transfer rate of 100 Mb/s.
1 40 ns cycle time (25.0 MHz). This results in a transfer rate of 200 Mb/s.

<13> linkEnable - Link Enable Control - This bit turns on and off the transmission of data from the TxOut process. This control bit only has significance if the TxOut process is enabled (CSR 0, txOutEnable, <4:4>).

0 Sends unassigned (null) cells only
1 Sends data cells

<12> resetEnable - TC35854F Reset Control - Software reset of TC35854F. The bit should be set to reset the chip, then cleared to terminate the reset event.

0 No action, or terminate reset event after 1 -> 0 transition
1 Resets TC35854F.

<11> txPrityCk - MAC Transmit Parity Check Control - Enable or disable parity checking on the transmit TPATH pins of the MAC interface. Set to 1 to enable parity checking.

<10> lcpPrtySel1 - Select Parity Type Control - Select odd or even parity on the MAC interface.

0 Specifies even parity.
1 Specifies odd parity.

<9> isLifoFlag - ABR VC List Insertion Style - Select the style to insert rescheduled ABR VC to the list at the next service time slot.

0 Insert new VC at the end of the list.
1 Insert new VC at the head of the list.

<8> schedTblSel - CBR Schedule Table Indicator - Select one of two CBR schedule tables to use.
0 Use Transmit Static Schedule Table1.
1 Use Transmit Static Schedule Table2.

<7> intrClrMode - Clear Interrupt Control
This bit controls the policy for clearing interrupts in TC35854F. The bit value is decoded as follows :
0 Interrupts are cleared by writing a 1. Clear counters by writing any non-zero value to them.
1 Interrupts are cleared on a read operation. A write to the interrupt register is flagged as an illegal access.

<6> NrmCountSel - ER Parameter Nrm Selection
This bit selects the value used for Nrm defined in ATM Forum ABR services. The bit value is decoded as follows :
0 Use 32 as Nrm control value.
1 Use 256 as Nrm control value.

<5> txInEnable - TxIn Enable Control - Set to 1 to enable the TxIn process. The TxIn process segments packets into cells from the transmit MAC interface. The cells are placed in appropriate circuit queues in cell memory. In packet mode, this bit is ignored.

<4> txOutEnable - TxOut Enable Control - Set to 1 to enable the TxOut process. The TxOut process services the transmit circuit queues in cell memory according to a traffic shaper scheduler. TxOut decouples the cell rate by adding null cells (unassigned cells) to the output when no data cells can be transmitted. Data cells are transmitted only if linkEnable (CSR 0, <13:13>) is asserted. Otherwise, null cells are transmitted. This feature is used for link initialization. When the Physical layer is declared "up", controlling firmware can assert linkEnable to turn on data transfer. In packet mode, this bit is ignored.

<3> rxInEnable - RxIn Enable Control - Set to 1 to enable the RxIn process. The RxIn process reassembles cells received on the link into packets. When RxIn is disabled, cell synchronization is maintained, but the cells are ignored and no packets are reassembled. In packet mode, this bit is ignored.

<2> rxOutEnable - RxOut Enable Control - Set to 1 to enable the RxOut process to send packets to the MAC interface (from either reassembled ATM packets or, in packet mode, HDLC packets).

<1> txPktEnable - Transmit Packet Enable Control - Set to 1 to enable packet mode transmission. In packet mode, packets are accepted at the MAC interface and passed to the link interface, after going through a speed matching FIFO. This bit is ignored in SMDS or ATM mode.

<0> loopbackEnable - LoopbackEnable Control - Set to 1 to enable link side loopback in TC35854F. When TC35854F is placed in loopback mode, the transmit cell stream is fed back into the RxIn process in UTOPIA interface packet format. Both Tx and Rx link processes use a 12.5 MHz (internally generated) clock. The rising edge of the loopback clock is in phase with the rising edge of SYMCLKA. Loopback only operates properly for atm=1 in CSR 3.

Table 45 CSR 1 Test

Address Offset: 0x002

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RO	0	**outRteBrmEnable**	7	RW	RO	01	**linkInterface**
14	RW	RO	0	**configureER**	6				
13	RW	RO	0	**memoryLimit**	5	RW	RO	0	**addCredit**
12					4	RW	RO	0	**tiShortAddr**
11					3	RW	RO	0	**rxFddiReverse**
10	RW	RO	0	**numberVp**	2	RW	RO	0	**softState**
9					1	RW	RO	0	**forceAllIntr**
8	RW	RO	0	**supportVc**	0	RW	RO	0	**lcpTestModeEl**

<15> outRteBrmEnable - ER out-of-rate BRM enable - This 1 bit field indicates if out-of-rate backward RM cell operation is enabled. If this operation is enabled, this bit is set to 1. Otherwise, set this bit to 0.

<14> configureER - ER Connection Indicator - This 1 bit field indicates if the current TC35854F configureation supports ER connections. If TC35854F is configured to support ER, this bit is set to 1. Otherwise, set this bit to 0.

<13:11> memoryLimit - Size of External Memory - This field indicates the size of the external memory. Up to 8 megabytes of external memory can be supported by TC35854F. This field should be set as follows.

<13 12 11> = 0 0 0 1 Mega bytes external memory
<13 12 11> = 0 0 1 2 Mega bytes external memory
<13 12 11> = 0 1 1 4 Mega bytes external memory
<13 12 11> = 1 1 1 8 Mega bytes external memory

<**10:9> numberVp - Number of VP supported -** This field contains the value indicating the number of VP supported by TC35854F.

0 1 VP (VPI = 0) supported.
1 2 VP (VPI = 0 included) supported
2 3 VP (VPI = 0 included) supported
3 4 VP (VPI = 0 included) supported

<8> supportVc - Maximum Number of VCs Support Control - This bit indicates the maximum number of VC supported by TC35854F. Up to 4K VC can be supported.

0 The maximum number of VC supported is 1K.
1 The maximum number of VC supported is 4K.

<7:6> linkInterface - Link Interface Type - This field specifies the type of the link interface. Several modes are supported, as follows:

0 UTOPIA, octet level
1 UTOPIA, cell level
2 UTOPIA, cell level, 200ns delay which is only used for FLOWmaster
3 UTOPIA, cell level, 400ns delay which is only used for FLOWmaster

See the pin descriptions for details of how each mode affects their behavior. This field is valid for ATM or SMDS mode.

<5> addCredit - Add Credit At Final Stage - This bit determines whether FLOWmaster credit acks are inserted into the transmit cell stream before or after the transmit cell FIFO. It should only be set to 1 when the link clock is operating synchronously with the rest of chip.

0 Add credit before FIFO
1 Add credit after FIFO

<4> tiShortAddr - MAC Address Format Selection - This bit selects either the FDDI type CID table lookup for transmit packets or the short address mode.

0 FDDI type lookup packets.
1 Short address lookup packets.

<3> rxfddiReverse - DA and SA Address Receive Bit Order Control - This bit controls the bit order of the RPATH output pins for bytes within the 48-bit DA and SA fields of FDDI packets, i.e., the 12 bytes following the first byte of the packet.

0 The bit order of the pins is the same as all other fields in the packet.
1 The bit order within each byte is reversed, e.g., 10010111 -> 11101001, for the above 12 bytes.

This bit has no effect on any other bytes of the packet. The bit reversal is the same for all receive virtual circuits, i.e., it will provide consistent bit ordering for all DAs and SAs if and only if the initial bit order received is consistent.

NOTE: The DA and SA bit order on TRANSMIT is controlled on a per packet basis by a bit in the packet header request as described in section.

<2> softState - Software State - This bit is reserved for the software usage.

<1> forceAllIntr - Force All Interrupts Control - If set to 1, all interrupts will be forced set. For normal operation, set to 0.

<0> lcpTestModeEl - Ram Test Mode Enable - Setting this bit to 1 allows direct access to the internal RAMs. This is used for chip testing only. Set to 0 for normal operation.

Table 46 CSR 2 Bridging Circuit Indicator

Address Offset: 0x004

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15				**Unused**	7				
14					6				
13	RW	RW	0	**slowErDue**	5				
12	RW	RO	0	**bridgeFlag**	4				
11	RW	RO	0	**bridgeVc**	3				
10					2				
9					1				
8					0				

<13> slowErDue - Low Rate ABR Queue Timer - This register contains the flag for low rate ABR VC queue. It is set to 1 every 100ms by the software. After it is set to 1, TC35854F sets it to 0 next cycle (40ns). When it is set to 1, the low rate ABR whose rates are lower than 32 kb/s are served in FIFO fashion until all VCs in the queue has been served.

<12> bridgeFlg - Bridging Circuit Indicator - This field indicates if all circuits should be transmitted on one bridging circuit, which is indicated by the next field called bridgeVC. By setting this bit to 1, all circuits will be transmitted to ATM network on the same VCI which is indicated by the value in the bridgeVc field.

<11:0> bridgeVc - Bridging Circuit Identifier - The value of this 12-bit field is used indicate the VCI for all circuits bridged on when the bridgeFlag field in this word is set to 1. When bridgeFlag is set 0, this field is ignored.

Table 47 CSR 3 Configuration

Address Offset: 0x006

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RO	1	**atm**	7				
14	RW	RO	0	**pkt**	6	RW	RO	0	**flowMaster**
13	RW	RO	0	**smds**	5	RW	RO	0	**QFC**
12				**Unused**	4	RW	RO	0	**flowCtrlRm**
11					3	RW	RO	0	**txCrc**
10					2	RW	RO	0	**rxCrc**
9					1	RW	RO	0	**txCrc32**
8					0	RW	RO	0	**rxCrc32**

<15> atm - ATM Mode Control - Set to 1 to select ATM operation mode. In ATM mode, transmit outbound packets are segmented into cells by the TxIn process and sent to the link interface by TxOut. RxIn receives inbound cells and reassembles them into packets. These packets are transmitted across the receive MAC interface by RxOut. Only one of the ATM, PKT, or SMDS mode bits can be asserted.

<14> pkt - Pkt Mode Control - Set to 1 to select packet operation mode. In packet mode, transmit outbound packets are taken in on the transmit MAC interface and passed to the outbound link transmit interface after passing through a speed matching FIFO. Similarly, inbound receive packets are taken from the link and passed through a receive speed matching FIFO and passed to the receive MAC interface. Only one of the ATM, PKT, or SMDS mode bits can be asserted.

<13> smds - SMDS Mode Control - Set to 1 to select SMDS operation mode. SMDS mode differs from ATM mode only in the use of cell headers (see modes of operation for details). Only one of the ATM, PKT, or SMDS mode bits can be asserted.

<6> flowMaster - Select FLOWmaster Link - If set to 1, this bit selects FLOWmaster cell header format. Otherwise, regular ATM cell header format is used.

<5> QFC - Select QFC Link - If set to 1, TC35854F is running QFC flow control on ABR traffic. Otherwise, other congestion control is used, for example, UNI 4.0 flow control, for all ABR traffic.

<4> flowCtrlRm - Select FLOWmaster Control Mode for ER RM Cells - If set to 1, all ER RM cells are under credit control if the link is running FLOWmaster mode. Otherwise, all ER RM cells are not under credit control. This bit is ignored if the flowMaster field (bit <6>) is set to zero.

<3> txCrc - Add Transmit CRC Control - Set to 1 to enable the calculation and addition of CRCs to transmitted packets when TC35854F is in packet mode.

<2> rxCrc - Receive CRC Checking Control - Set to 1 to enable the checking of CRCs on received packets when TC35854F is in packet mode. If the bit is asserted and a CRC error is detected, this is indicated in the status information at the end of the packet send on the receive MAC interface.

<1> txCrc32 - Transmit CRC Selection Control - This bit selects one of two possible CRCs to be added to packets when TC35854F is in packet mode and txCrc is asserted. A 16-bit CRC or a 32-bit (Autodin) CRC can be selected.
0 16-bit CRC
1 32-bit CRC

<0> rxCrc32 - Receive CRC Selection Control - This bit selects one of two possible CRCs to be checked for received packets when TC35854F is in packet mode and rxCrc is asserted. A 16-bit CRC or a 32-bit (Autodin) CRC can be selected.
0 16-bit CRC
1 32-bit CRC

Table 48 CSR 4 Maximum Packet Length

Address Offset: 0x008

bit	Host	Chip	Reset	Name		bit	Host	Chip	Reset	Name
15				Unused		7				
14						6				
13						5				
12						4				
11						3				
10	RW	RO	0	**maxPktLength**		2				
9						1				
8						0				

<10:0> maxPktLength - Maximum Packet Length - Any packet being reassembled by RxIn that exceeds this number of cells is discarded (cell count, not byte count).

Table 49 CSR 5 Packet Processing

Address Offset: 0x00a

bit	Host	Chip	Reset	Name		bit	Host	Chip	Reset	Name
15	RW	RO	0	**pktHdrStrip**		7				
14						6				
13						5				
12						4				**Unused**
11						3				
10						2				
9	RW	RO	0	**pktCrcStrip**		1				
8	RW	RO	0	**roNumFillBytes**		0				

<15:10> pktHdrStrip - Packet Header Strip Count - When TC35854F is in packet mode (CSR 4, pkt, <14:14>), this value is used to count the number of bytes to be stripped from the start of the packet.

<9> pktCrcStrip - Packet CRC Strip Indication - This bit controls the stripping of a 32-bit CRC at the end of a packet when TC35854F is in packet mode. No stripping occurs if the CRC is not present as indicated in byte 2 (<5:5> appendCrc) of the packet request header.

0 Do not strip CRC. Add CRC if requested in byte 2 of the packet request header.

1 Strip CRC unless byte 2 of the packet request header indicates CRC is not present.

<8:5> roNumFillBytes - Number of Receive Out FILLERs - This field indicates the minimum number of filler codes to be sent by RxOut between packets on the receive MAC interface. This relaxes requirements on the attached chip to TC35854F for packet processing (e.g., address lookups).

Table 50 CSR 6 DA III

Address Offset: 0x00c

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RO	0	**daConst3**	7				
14					6				
13					5				
12					4				
11					3				
10	RW	RO	0	**Protocol_ID**	2				**Unused**
9					1				
8					0				

<15:11> daConst3 - Destination Address Compare Constant Part III - This field contains the third part of the destination address compare constant. It represents bits <4:0> of the 37-bit DA comparison constant if the CSR bit supportVc (CSR1, <8>) is set to 0. If the CSR bit supportVc (CSR1, <8>) is set to 1, bits <15:14> are set to zero and bits <13:11> represent bits <2:0> of the 35-bit DA comparison constant. Refer to CSR 9 for a complete description.

<10:3> Protocol_ID - QFC Protocol_ID field in a protocol control unit - This field contains the value used for the Protocol_ID field in a QFC protocol control units.

Table 51 CSR 7 DA II

Address Offset: 0x00e

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RO	0	**daConst2**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

<15:0> daConst2 - Destination Address Compare Constant Part II - This field contains the second part of the destination address compare constant. It represents bits <20:5> of the 37-bit DA compare constant if the CSR bit supportVc (CSR1, <8>) is set to 0, or bits <18:3> of the 35-bit DA compare constant if the CSR bit supportVc (CSR1, <8>) is set to 1. Refer to CSR 9 for a complete description.

Table 52 CSR 8 DA I

Address Offset: 0x010

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RO	0	**daConst1**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

<15:0> daConst1 - Destination Address Compare Constant Part I - This field contains the first part of the destination address compare constant. It represents bits <36:21> of the 37-bit DA compare constant if the CSR bit supportVc (CSR1, <8>) is set to 0, or represents bits <34:19> of the 35-bit DA compare constant if the CSR bit supportVc (CSR1, <8>) is set to 1. If the CSR bit fddiComp (CSR0, <15:15>) is set to 1, the 37-bit DA compare constant is used to compare against bits <46:10> of the incoming FDDI DA field of the packet if the CSR bit supportVc (CSR1, <8>) is set to 0, or the comparison is against bits <46:12> of incoming FDDI DA field of the packet if the CSR bit supportVc (CSR1, <8>) is set to 1. If both fields are the same, bits <9:0> (supportVc = 0) or <11:0> (supportVc = 1) of the FDDI DA field represent a pointer to the appropriate entry in the Tx CID record table. If two fields are unequal, then CSR field bridgeVc (CSR 3, bits <11:0>) is the pointer to the Tx CID record table entry.

Table 53 CSR 9 GFC Control Register

Address Offset: 0x012

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15				**Unused**	7				
14					6				
13					5	RW	RO	1	**GFC_EQUIP**
12					4	RW	RW	1	**GFC_GO_CNT**
11					3				
10					2	RW	RW	0	**GFC_VALUE**
9					1	RW	RO	0	**GFC_ENABLE**
8					0	RW	RW	1	**transmit**

<5> GFC_EQUIP - GFC Controlled Equipment Indicator - This field indicates to the far end if TC35854F is capable to support GFC control. This bit is copied to the least significant bit of the GFC field of each transmitted cell. The local processor can set this bit to 1 or 0.

<4:3> GFC_GO_CNT - GFC Control on Controlled ATM Connections - This field contains the permission for a controlled ATM connection to send a cell. In TC35854F, CBR and VBR are GFC uncontrolled connections and the rest are GFC controlled connections. Every time a controlled connection sends a cell, this field is decremented. When a SET_A in the last received ATM cell header is set to 1, and this field is less than 2, it increments. For more details, see the *Generic Flow Control* section. It is ignored if CSR GFC_ENABLE bit is set to zero.

<2> GFC_VALUE - GFC Field Value Indicator - This field contains the OR result of CSR GFC_VALUE, SET_A bit and HALT bit in the last received ATM cell head GFC field. The local processor reads this bit and at the same time, clears the bit. This can be used for the local processor to make decision if the far-end switch is capable to support GFC control.

<1> GFC_ENABLE - GFC Control Mode Indicator - This field indicates if TC35854F should turn on GFC control. If this bit is set to 1, TC35854F is running GFC control mode and becomes GFC controlled equipment. The GFC field in transmitted cells are set accordingly. If this bit is zero, all GFC fields are set to 0 except the least significant bit, which is the copy of CSR GFC_EQUIP bit.

<0> transmit - GFC Transmit Bit Register - This field contains the value of GFC TRANSMIT bit from last received ATM cell header. If this bit is zero and CSR bit GFC_ENABLE is set to 1, all ATM connection transmissions are stop, and a NULL cell is transmitted. This bit must be set to 1 in order to make any ATM connection transmissions. This bit is ignored if CSR bit GFC_ENABLE is set to zero.

Table 54 CSR 10 Block Address

Address Offset: 0x014

bit	Host	Chip	Reset	Name		bit	Host	Chip	Reset	Name
15				**Unused**		7				
14						6				
13						5				
12						4				
11	RW	RO	0	**blkPtr**		3				
10						2				
9						1				
8						0				

<11:0> blkPtr - Indirect Memory Operation Block Address - This field contains the 12 MSBs (i.e., <19:8>) of the 20-bit memory address used to access cell memory. This field is concatenated with the 8 bits of wordAddr (i.e., <7:0> of the 20-bit address) to form the complete 20-bit address for a LcpPrc indirect cell-memory operation.

Table 55 CSR 11 Indirect Operations

Address Offset: 0x016

bit	Host	Chip	Reset	Name		bit	Host	Chip	Reset	Name
15				**Unused**		7	RW	RW	0	**wordAddr**
14						6				
13						5				
12	RW	RO	0	**portMode**		4				
11						3				
10						2				
9						1				
8						0				

<12:8> portMode - Indirect Operation Selection and Trigger - This 5-bit field and the following wordAddr field consist of the only 16-bit trigger registers in TC35854F CSRs. When this register is written, an operation specified by portMode, as shown below, is triggered in TC35854F. Before the local processor writes this register, it waits until the CSR portDone bit (CSR16, bit <15>) is set (i.e., = 1). As soon as this register is written by the local register, TC35854F clears the portDone (i.e., = 0) to block any further write operations until the current operation is finished. TC35854F resets the portDone bit to 1, when the situation allows the local processor to have next indirect operation. The field is decoded as follows.

0 **EXT_IDLE -** Idle operation.

1 **SINGLE_CYCLE_RD_CM -** Performs a single read cycle and loads the contents of the cell memory into the indirect access data and status registers. The cell memory address is written into blkPtr (12 MSBs) and wordAddr (8 LSBs). The read data is presented in the drWord CSRs 12-15.

2 **SINGLE_CYCLE_WR_CM -** Performs a single write cycle and loads the contents of the indirect access data registers into the cell memory. The cell memory

address is written into blkPtr (12 MSBs) and wordAddr (8 LSBs). The data is written into the drWord CSRs 12-15 and then transferred to cell memory by LcpPrc.

3 **WR_OAM_CELL -** This operation updates txOut's state to indicate that a new OAM cell is ready for transmission on a particular circuit. Preceding this operation, an OAM cell is written into cell memory using indirect writes. The local processor then loads the specified CID into the CID register (CSR 17, cid) and the OAM cell index into the 6 least significant bits of the wordAddr. The trigger action is writing the value 3 into portMode. The Tx CID entry corresponding to the CSR cid field is modified by loading the OAM cell index from wordAddr. Finally, certain scheduling operation is required so that the transmit engine has chance to send this OAM cell.

4 **UPDATE_TX_CREDITS -** This operation updates the transmit credits for each circuit using the credit field in Tx CID table. These credits control the average rate of cell transmission on a circuit. When a cell is transmitted, the credit field in the transmit CID record is decremented by one. This operation is used to replenish the credits at appropriate intervals and appropriate credit increments to maintain a contracted average rate and maximum burst size. The local processor writes the number of credits and the CID into csrCredits (CSR 18), and CID (CSR 17) registers respectively. The trigger operation occurs by writing the value 4 to portMode. TC35854F reads the old credits from the transmit CID record. It writes the new number of credits into the transmit CID record. The old credits value is written back to csrCredits (CSR 18, <15:0>). This is used by the local processor for transmit cell accounting.

5 **STOP_TRAFFIC -** This operation stops the transmit traffic of a circuit. The local processor writes the specified CID into the CID register (CSR 17, cid). The trigger action is writing the value 5 into portMode. LcpPrc reads the Tx CID record using the value in the CID register. The CID record entry is modified by setting the cidStopTraffic to 1. At the same time, the corresponding bit in the Tx CID ready vector is cleared. When TxOut finds the cidStopTraffic bit in CID record is set, cidReady bit is also cleared. This is used to stop FLOWmaster circuit traffic in order to resynchronize the circuit's credits.

6 **FORCE_NEXT_FLOW_CID -** This action forces a CID to be the next flowing circuit presented by the scoreboard on the receive side when in FLOWmaster mode (CSR 3, <6>). The CID operated on is determined by the value in the CID register (CSR 17,<11:0>). The value 6 is written into portMode to trigger the operation. The local processor can use this operation as part of the credit resynchronization operation.

7 **SCOREBOARDOP -** This bit specifies an operation to scoreboard RAM, specified by the bits <1:0> of the wordAddr field (CSR 11). It allows the local processor to set, clear, or read one bit in the RAM or write the whole word to the RAM. The CID operated on is determined by the value in the CID register (CSR 17). The desired operation in wordAddr <1:0> is encoded as follows.

Value	Function
00	LCP_CLEAR
01	LCP_SET
10	LCP_READ
11	LCP_WRITE

When the LCP_READ operation is performed, the returned data is in the drWord0 (CSR 12) register; when the LCP_WRITE operation is performed, the data to be written into the scoreboard is from the drWord0 (CSR 12) register. The write is to 16 CIDs at once, using the eight least significant bits of the CID register. The LCP_WRITE operation is performed only when the rxInEnable bit (CSR 0) is set to zero. The other operations are performed when the rxInEnable bit (CSR 0) is set to one.

8 **SEND_CREDITS** - This triggers a write to the multiple credit FIFO, with the CID specified by the cid field of CSR 17 and a credit count using the lowest six bits of wordAddr. portDone will be set immediately and other indirect operations can be executed, but the credits may not immediately enter the FIFO. When they do, the sendCreditsDone bit is set.

9 **CHECK_CREDFIFO** - This triggers a check of the single and multiple credit FIFOs for the CID value specified by the cid field of CSR 17. If the CID is found to be present in either FIFO, then the LSB of wordAddr is set to 1, otherwise it is cleared to 0.

10 **DROP_RX_PKT** - This operation informs RxIn to drop a packet that is currently being reassembled on a particular circuit. This procedure is used if the local processor firmware determines that a packet reassembly time-out has occurred and the packet needs to be trashed. The processor writes the receive CID to the CSR cid (CSR 17). A 10 is written to portMode to trigger the operation. If the request circuit is AAL4 or SMDS type, MID value is indicated in the blkPtr field in CSR 10. RxIn reads the CSR cid register, accesses the record, and returns the current list of cells being reassembled to the receive free cell pool. At the same time, the listSize, headAddr and tailAddr fields in the receive circuit record are cleared to zero.

11 **DROP_RX_PKT_INV** - Same as DROP_RX_PKT, plus marks the Rx CID as invalid so that no new traffic is accepted. But the listSize, headAddr and tailAddr fields in the receive circuit record are not cleared.

12 **TX_CID_RDY_OP** - This operation sets, clears, or reads a bit in the Tx CID ready vector. Up to 4095 CID ready entries are stored in the internal chip RAM. The processor writes the CID value to the CID register (CSR 17, <11:0>) and the desired operation to wordAddr using the following encoding:

00	LCP_CLEAR
01	LCP_SET
10	LCP_READ
11	LCP_WRITE

The operation is triggered by writing 12 to portMode. The scheduling engine services the requested operation. If a read is requested, the returned data is sent to wordAddr. To allow faster initialization, the Write Rdy Vector operation writes the contents of Data Word 0 (CSR 12) to 16 CIDs starting at TxCid (CSR 17). (The specified CID is assumed to be a multiple of 16.)

13 **SEND_BSC_CELL -** This triggers a request to send a QFC BSC cell for a circuit indicated by the cid field of CSR 17 <11:0>. The circuit identifier record is read. If the circuit is the RCC circuit, sendVpBscCell bit is set to 1. Otherwise, sendVcBscCell bit is set to 1. The modified record is then written back. After the transmit engine sends the request BSC cell, the corresponding bit is cleared to zero. Before Lcp puts this request, it reads the record through indirect read to check if sendVpBscCell or sendVcBscCell bit is cleared.

14 **INVALID_TX -** This triggers a request to change validEntry bit in the circuit identifier record to 0. The request circuit is indicated in the cid filed of CSR 17 <11:0>. LcpPrc reads the Tx CID record using the value in the CID register. The CID record entry is modified by setting the validEntry to 0. At the same time, cidReady bit is cleared. When TxOut finds the validEntry bit in CID record is 0, cidReady bit is also cleared.

15 **DROP_TX_PKT -** This triggers a request to drop a list of cells for a circuit, which is pointed by HeadAddr, TailAddr and listSize in the circuit identifier record for this circuit. The request CID is indicated by the *cid* field of CSR 17 <11:0>. The *txReqDone* bit (CSR 18) will be cleared to zero immediately to prevent lcp from overwritting another same request before this one is done by TC35854F. *portDone* will be set immediately to 1 so that other indirect operations can be executed, but the requested discarding packet operation may not be done immediately. When it is done, the *txReqDone* bit is set to 1 (CSR 18) and the lcp can put another such a request. Note, the validEntry bit in the circuit identifier record for this circuit must already be cleared to zero, and the local processor must wait for about 2 cell transmission time before presenting this request. When the transmit engine performs the operation, cid ready vector is also cleared to zero, but the HeadAddr, TailAddr and listSize fields in the circuit identifier record are not changed.

16 **COMP_BSU_RECORD -** This triggers a request to compose a BSU record for a VC and its VP. The served CID is indicated by the *cid* field of CSR 17 <11:0>. The *compBsuDone* bit (CSR 18) will be cleared to zero immediately to prevent lcp from overwritting another same request before this one is done by TC35854F. *portDone* will be set immediately so that other indirect operations can be executed, but the requested BSU record may not be composed immediately. When it is done, the *compBsuDone* bit is set (CSR 18) and the lcp can put another such a request.

17 **SEND_RM_CELL -** This triggers a request to send an out-of-rate forward RM cell for the CID specified by the cid field of CSR 17 (<11:0>). The *txReqDone* bit (CSR 18) will be cleared to zero immediately to prevent lcp from overwritting another same request before this one is done by TC35854F. *portDone* will be set immediately so that other indirect operations can be executed, but the requested out-of-rate forward RM cell may not be generated and sent immediately. When it is done, the *txReqDone* bit is set (CSR 18) and the lcp can put another such a request.

18 **LINK_COUNT_OP -** This triggers a request to access QFC link counters of one VP. Requested counters include Tx_Count and Bsu_Fwd_Count in the transmit side, N2_Counter, Fwd_Count and Rx_Count in the receive side. This operation can be used by the software for QFC resource managements, for

example, releasing connection and reclaiming the link buffers. For details, refer to the section Quantum Flow Control, Call Clearing. The operation is triggered when 18 is written into the portMode field and at the same time, the wordAddr field is decoded as follows.

bits <1:0> vpi - requested VP index;
bit <2> Rx/tx select -
0: selects transmit side.
1: selects receive side.
bit <3> clear linkN2Count control -
0: do not clear link N2 counter
1: clear link N2 counter of the VP defined in bits <1:0>.
bit <4> count select -
0: linkRxCount if bit <2> is 1, or linkTxCount if bit <2> is 0.
1: linkFwdCount if bit <2> is 1, or linkBsuFwdCount if bit <2> is 0.
bit <5> read/set select -
0: read link counters. The contents of selected counter is put into drWord1<11:0> (CSR 13) and drWrod0<15:0> (CSR 12).
1: set selected link counter to the value specified in drWord1<11:0> (CSR 13) and drWrod0<15:0> (CSR 12).

<7:0> wordAddr - Word Address - This field is used for the above described indirect operations for the local processor. The details are shown in the following table.

portMode value	Operations	Host write wordAddr	TC35854F write wordAddr
1	SINGLE_CYCLE_RD_CM	8 LSB SRAM address	none
2	SINGLE_CYCLE_WR_CM	8 LSB SRAM address	none
3	WR_OAM_CELL	<5:0> OAM index	none
4	UPDATE_TX_CREDITS	none	none
5	STOP_TRAFFIC	none	none
6	FORCE_NEXT_FLOW_CID	none	none
7	SCOREBOARDOP	<1:0> operation mode	none
8	SEND_CREDITS	<5:0> credit count	none
9	CHECK_CREDFIFO	none	<0> cid in FIFO status
10	DROP_RX_PKT	none	none
11	DROP_RX_PKT_INV	none	none
12	TX_CID_RDY_OP	<1:0> operation mode	<0> cid rdy status
13	SEND_BSC_CELL	<0> send VP BSC	none
14	INVALID_TX	none	none
15	DROP_TX_PKT	none	none
16	COMP_BSU_RECORD	none	none
17	SEND_RM_CELL	none	none
18	LINK_COUNT_OP	<1:0> VP index <2> Rx/tx select <3> clear N2 control <4> counter select <5> read/write select	none

Table 56 CSR 12 Data Word 0

Address Offset: 0x018

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RW	0	**drWord0**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

Table 57 CSR 13 Data Word 1

Address Offset: 0x01a

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RW	0	**drWord1**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

Table 58 CSR 14 Data Word 2

Address Offset: 0x01c

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RW	0	**drWord2**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

Table 59 CSR 15 Data Word 3

Address Offset: 0x01e

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RW	0	**drWord3**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

These 4 registers (CSR 12, CSR 13, CSR 14 and CSR 15) are used for some indirect operations as shown below.

portMode	Operations	drWord3	drWord2	drWord1	drWord0	Written by
1	SINGLE_CYCLE_RD_CM	data <63:48>	<47:32>	<31:16>	<15:0>	TC35854F
2	SINGLE_CYCLE_WR_CM	data <63:48>	<47:32>	<31:16>	<15:0>	Host
7	SCOREBOARDOP					
	read operation	-	-	-	data	TC35854F
	write operation	-	-	-	data	Host
12	TX_CID_RDY_OP					
	write operation	-	-	-	data	Host
19	LINK_COUNT_OP	-	-	<11:0>	data	
	read operation			data		TC35854F
	write operation					Host

Table 60 CSR 16 Status

Address Offset: 0x020

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RO	RW	1	**portDone**	7	RO	WO	0100	**Revision**
14	RO	RW	1	**sendCredDone**	6				
13	RO	RW	1	**txReqDone**	5				
12	RO	RW	1	**compBsuDone**	4				
11	RO	RW	0	**localCongestInd**	3	RO	RW	0	**lcpState**
10				**Unused**	2				
9					1				
8					0				

<15> portDone - Port Done - If set, this field indicates that the indirect operation state machine is idle, any previous operation has completed, and the port is available for a further operation; if clear, then an indirect operation is still in progress (and no new operation can be initiated until it completes).

<14> sendCredDone - LCP Send Credits Done - If set, this field indicates that the machine for sending FLOWmaster credits to an upstream node is idle, any previous credits have been put into the multiple credit FIFO, and the SEND_CREDITS indirect operation can be triggered again; if clear, then credits are still waiting for a slot in the multiple credit FIFO (and would be lost if another SEND_CREDITS operation was triggered).

<13> txReqDone - LCP Request Done - If set, this field indicates that previous request from the LCP has been done. The requests include sending out-of-rate forward RM for a cid in the ER application and dropping a list of cells of one circuit in the transmit side. The LCP can put another request.

<12> compBsuDone - Send QFC BSU Cell Done - If set, this field indicates a BSU record has been generated per Lcp previous request. Lcp then can give another such a request.

<11> localCongestInd - Local congestion indication - If set, this field indicates the receive memory is under threshold indicated by CSR 19 bits <7:0>. No new packets will be accepted. This bit is used to set CI and NI bit in ER RM cell if TC35854F is not in QFC or flowMaster mode. (CSR 3 bit<5> and bit<6>). If TC35854F is in either QFC or flowMaster mode, this bit is ignored. The bit is cleared to 0 when the receive memory is above the threshold.

<7:4> Revision - TC35854F Revision Number - This field indicates the revision number of TC35854F. The current revision number is 4.

<3:0> lcpState - Local Processor Operation State - This field indicates the type of local processor indirect operation that is in progress. The field is decoded as follows:

0000	Idle
0001	Indirect read or write
0010	Update transmit circuit record
0011	Drop transmit cells
0100	Drop receive packets
0101	Set/Clear/Read Tx cid ready vector
0110	Force to promote one FlowMaster or QFC circuit
0111	Set/Clear/Read QFC or FlowMaster score board operations
1000	Send FlowMaster credits
1001	Check FlowMaster credit FIFO
1010	Send QFC BSU cell or ER forward RM cell
1011	Update QFC link counters operations

Table 61 CSR 17 CID Register

Address Offset: 0x022

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15 14 13 12				**Unused**	7 6 5 4				
11 10 9 8	RW	RO	0	**cid**	3 2 1 0				

<11:0> cid - CID Register - This field is used to specify the circuit identifier associated with an indirect operation. Updating credits and writing OAM cells into cell memory are two such operations.

Table 62 CSR 18 Credits Register

Address Offset: 0x024

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15				**Unused**	7 6 5 4				
14 13 12 11 10 9 8	RW	RW	0	**csrCredits**	3 2 1 0				

<14:0> csrCredits - Credits Register - This field is used during the UPDATE_TX_CREDITS indirect operation. When the credits of a particular CID are to be updated, this field holds the new value of credits that will be written into the transmit CID record. When the update is complete, this field holds the old value of credits that was read from the transmit CID record before the update.

Table 63 CSR 19 Min Rx Free Cells

Minimum Number of Rx Free Cells for new pkts
Address Offset: 0x026

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15				**Unused**	7	RW	RO	0	**minRxFrCell**
14	RW	RO	0	**lcpAcceptSCredits**	6				
13	RW	RO	0	**reportCredOnly**	5				
12	RW	RO	0	**rxEnableLowActivate**	4				
11	RW	RO	0	**rxEnableQuickActivate**	3				
10	RW	RO	0	**rxSCredFifoThresh**	2				
9					1				
8					0				

<14> lcpAcceptSCredits - Accept Single Credits - This bit is set and cleared by the firmware to indicate if it can accept a single credit from the chip. RxIn can pass a single credit to the firmware if RxIn needs to return a credit to the far end and the number of entries in the credits FIFO is either greater than or equal to the contents of rxSCredFifoThresh register (CSR 19, <10:8>). If this occurs, the rxScredTaken interrupt (CSR 48, <14>) is set, and the CID is placed in the errorCid CSR (CSR 48, <11:0>). If this bit is zero or the rxScredtaken interrupt is already set (and has not been serviced yet) and the credit FIFO is not full, the credit is written into the FIFO. If the FIFO is full and this bit is set to zero (or the interrupt is already set), the rxSCredFifoOvfl interrupt (CSR 48, <13>) is set. The credits taken by the local processor can be sent to the far end later using SEND_CREDITS indirect operation.

<13> reportCredOnly - Report CID for Credit Events Only - When this bit is set and a cell with a PTI field value of either 2 or 3 in the ATM header is received, the rxCongestionSeen interrupt (CSR 48, <15>) is set, but the errorCid register (CSR 48, <11:0>) is not updated.

<12> rxEnableLowActivate - Enable FLOWmaster Low Threshold Activates - This bit applies to FLOWmaster or QFC mode. When set, it allows a circuit to be activated based on a lower cell count threshold if there is no active packet on the circuit (i.e., a packet completed on the circuit even though it was not "flowing"). The lower threshold is the bslVcLimitDef0 in FLOWmaster mode and one of bslVcLimitDefx for VPs, rather than a MTU plus the value from bslVcLimitDefx.

<11> rxEnableQuickActivate - Enable Quick FLOWmaster Activates - This bit applies to QFC or FLOWmaster mode. When set, it allows a circuit to be activated when a packet completes reassembly if there are adequate resources (the cell count threshold). The threshold used for this "QuickActivate" is controlled by the rxEnableLowActivate CSR bit.

<10:8> rxSCredFifoThresh - Single Credit FIFO Threshold - This field contains the threshold for the single credit FIFO, the point at which single credit write will be transferred to the local processor instead of the FIFO itself, if the local processor is able to accept it. If this field has a value of 7, the transferring credit to the local processor is disabled. This field is used in the flowMaster mode (CSR 3, <6>).

<7:0> minRxFrCell - No New Packets Threshold - This field is the eight MSBs of a 12-bit limit that is the minimum number of cells that must be available on the receive free list before RxIn can start to reassemble a new packet. If the number of free cells is less than this threshold, incoming cells that are not part of the packet being reassembled are ignored.

Table 64 CSR 20 TxFreeList Head Lsp

Address Offset: 0x028

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RW	0	**txfListHeadLsp**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

Table 65 CSR 21 TxFreeList Head Msp

Address Offset: 0x02a

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15				**Unused**	7				
14					6				
13					5				
12					4				
11					3	RW	RW	0	**txfListHeadMsp**
10					2				
9					1				
8					0				

This two registers contain the transmit free list head address, each of which contains a segment of the whole address. Free buffer space for transmit cells are stored as a linked list of cells with a head pointer, a tail pointer and a size within TC35854F cell memory.

CSR 20 <15:0> txfListHeadLsp - Transmit Free List Head Address 1 - This field contains the 16 LSBs of the transmit free list head address.

CSR 21 <3:0> txfListHeadMsp - Transmit Free List Head Address 2 - This field contains the four MSBs of the transmit free list head address.

Table 66 CSR 22 TxFreeList Tail Lsp

Address Offset: 0x02c

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15 14 13 12 11 10 9 8	RW	RW	0	**txfListTailLsp**	7 6 5 4 3 2 1 0				

Table 67 CSR 23 TxFreeList Tail Msp

Address Offset: 0x02e

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15 14 13 12 11 10 9 8				**Unused**	7 6 5 4				
					3 2 1 0	RW	RW	0	**txfListTailMsp**

This two registers contain the transmit free list tail address, each of which contains a segment of the whole address. Free buffer space for transmit cells are stored as a linked list of cells with a head pointer, a tail pointer and a size within TC35854F cell memory.

CSR 22 <15:0> txfListTailLsp - Transmit Free List Tail Address 1 - This field contains the 16 LSBs of the transmit free list tail address.

CSR 23 <3:0> txfListTailMsp - Transmit Free List Tail Address 2 - This field contains the four MSBs of the transmit free list tail address.

Table 68 CSR 24 TxFreeList Size Lsp

Address Offset: 0x030

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RW	0	**txfListSizeLsp**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

Table 69 CSR 25 TxFreeList Size Msp

Address Offset: 0x032

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15				**Unused**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1	RW	RW	0	**txfListSizeMsp**
8					0				

CSR 24 <15:0> txfListSize Lsp - Transmit Free List Size Lsp - This field contains 16 least significant bits of the transmit free list size.

CSR 25 <1:0> txfListSize Msp - Transmit Free List Size Lsp - This field contains 2 most significant bits of the transmit free list size. Free buffer space for transmit cells are stored as a linked list of cells with a head pointer, a tail pointer and a size within TC35854F cell memory.

Table 70 CSR 26 RxFreeList Head Lsp

Address Offset: 0x034

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RW	0	**rxfListHeadLsp**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

Table 71 CSR 27 RxFreeList Head Msp

Address Offset: 0x036

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15				**Unused**	7				
14					6				
13					5				
12					4				
11					3	RW	RW	0	**rxfListHeadMsp**
10					2				
9					1				
8					0				

This two registers contain the receive free list head address, each of which contains a segment of the whole address. Free buffer space for received cells are stored as a linked list of cells with a head pointer, a tail pointer and a size within TC35854F cell memory.

CSR 26 <15:0> rxfListHeadLsp - Receive Free List Head Address 1 - This field contains the 16 LSBs of the receive free list head address.

CSR 27 <3:0> rxfListHeadMsp - Receive Free List Head Address 2 - This field contains the four MSBs of the receive free list head address.

Table 72 CSR 28 RxFreeList Tail Lsp

Address Offset: 0x038

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15 14 13 12	RW	RW	0	**rxfListTailLsp**	7 6 5 4				
11 10 9 8					3 2 1 0				

Table 73 CSR 29 RxFreeList Tail Msp

Address Offset: 0x03a

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15 14 13 12				**Unused**	7 6 5 4				
11 10 9 8					3 2 1 0	RW	RW	0	**rxfListTailMsp**

This two registers contain the receive free list tail address, each of which contains a segment of the whole address. Free buffer space for received cells are stored as a linked list of cells with a head pointer, a tail pointer and a size within TC35854F cell memory.

CSR 28 <15:0> rxfListTailLsp - Receive Free List Tail Address 1 - This field contains the 16 LSBs of the receive free list tail address.

CSR 29 <3:0> rxfListTailMsp - Receive Free List Tail Address 2 - This field contains the four MSBs of the receive free list tail address.

Table 74 CSR 30 RxFreeList Size Lsp

Address Offset: 0x03c

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RW	0	**rxfListSizeLsp**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

Table 75 CSR 31 RxFreeList Size Msp

Address Offset: 0x03e

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15				**Unused**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1	RW	RW	0	**rxfListSizeMsp**
8					0				

CSR 30 <15:0> rxfListSizeLsp - Receive Free List Size Lsp - This field contains the 16 least significant bits of the receive free list size.

CSR 31 <1:0> rxfListSizeMsp - Receive Free List Size Msp - This field contains the 2 most significant bits of the receive free list size. Free buffer space for received cells are stored as a linked list of cells with a head pointer, a tail pointer and a size within TC35854F cell memory.

Table 76 CSR 32 RxPacketList1 Head Lsp

Address Offset: 0x040

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RW	0	**rxPktList1HeadLsp**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

Table 77 CSR 33 RxPacketList1 Head Msp

Address Offset: 0x042

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15				**Unused**	7				
14					6				
13					5				
12					4				
11					3	RW	RW	0	**rxPktList1HeadMsp**
10					2				
9					1				
8					0				

These two registers contain the high priority receive packet list head address, each of which contain a segmentation of the whole address. When cells are reassembled into complete packets, RxIn places the packet on the high priority linked list packet queue with a head pointer, a tail pointer within TC35854F cell memory if putInPktList1 flag in Rx circuit identifier record is set to 1.

CSR 32 <15:0> rxPktList1HeadLsp - High Priority Receive Packet List Head Address 1 - This field contains the 16 LSBs of the high

CSR 33 <3:0> rxPktList1HeadMsp - High Priority Receive Packet List Head Address 2 - This field contains the four MSBs of the high priority receive packet list head address.

Table 78 CSR 34 RxPacketList1 Tail Lsp

Address Offset: 0x044

bit	Host	Chip	Reset	Name	bit	Hos	Chip	Reset	Name
15 14 13 12	RW	RW	0	**rxPktList1HeadLsp**	7 6 5 4				
11 10 9 8					3 2 1 0				

Table 79 CSR 35 RxPacketList1 Tail Msp

Address Offset: 0x046

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15 14 13 12				**Unused**	7 6 5 4				
11 10 9 8					3 2 1 0	RW	RW	0	**rxPktList1TailMsp**

These two registers contain the high priority receive packet list tail address, each of which contain a segmentation of the whole address. When cells are reassembled into complete packets, RxIn places the packet on the high priority linked list packet queue with a head pointer, a tail pointer within TC35854F cell memory if putInPktList1 flag in Rx circuit identifier record is set to 1.

CSR 34 <3:0> rxPktList1TailMsp - High Priority Receive Packet List Tail Address 2 - This field contains the four MSBs of the high priority receive packet list tail address.

CSR 35 <15:0> rxPktList1TailLsp - High Priority Receive Packet List Tail Address 1 - This field contains the 16 LSBs of the high priority receive packet list tail address.

Table 80 CSR 36 RxPacketList2 Head Lsp

Address Offset: 0x048

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RW	0	**rxPktList2HeadLsp**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

Table 81 CSR 37 RxPacketList2 Head Msp

Address Offset: 0x04a

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15				**Unused**	7				
14					6				
13					5				
12					4				
11					3	RW	RW	0	**rxPktList2HeadMsp**
10					2				
9					1				
8					0				

These two registers contain the lower priority receive packet list head address, each of which contain a segmentation of the whole address. When cells are reassembled into complete packets, RxIn places the packet on the lower priority linked list packet queue with a head pointer, a tail pointer within TC35854F cell memory if putInPktList1 flag in Rx circuit identifier record is set to 0.

CSR 36 <15:0> rxPktList2HeadLsp - Low priority Receive Packet List Head Address 1 - This field contains the 16 LSBs of the low priority receive packet list head address.

CSR 37 <3:0> rxPktList2HeadMsp - Low priority Receive Packet List Head Address 2 - This field contains the four MSBs of the low priority receive packet list head address.

Table 82 CSR 38 RxPacketList2 Tail Lsp

Address Offset: 0x04c

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RW	0	**rxPktList2TailLsp**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

Table 83 CSR 39 RxPacketList2 Tail Msp

Address Offset: 0x04e

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15				**Unused**	7				
14					6				
13					5				
12					4				
11					3	RW	RW	0	**rxPktList2TailMsp**
10					2				
9					1				
8					0				

These two registers contain the lower priority receive packet list tail address, each of which contain a segmentation of the whole address. When cells are reassembled into complete packets, RxIn places the packet on the lower priority linked list packet queue with a head pointer, a tail pointer within TC35854F cell memory if putInPktList1 flag in Rx circuit identifier record is set to 0.

CSR 38 <15:0> rxPktList2TailLsp - Low priority Receive Packet List Tail Address 1 - This field is the 16 LSBs of the low priority receive packet list tail address.

CSR 39 <3:0> rxPktList2TailMsp - Low priority Receive Packet List Tail Address 2 - This field is the four MSBs of the low priority receive packet list tail address.

Table 84 CSR 40 Rx Active FLOWmaster pkts

Address Offset: 0x050

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RW	0	**maxFlowingPackets**	7	RW	RW	0	**curFlowingPackets**
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

<15:8> maxFlowingPackets - Maximum Number of Flowing Packets - This is the limit on how many FLOWmaster or QFC circuits can be 'flowing' at one time. If the value is 0xff, then the limit is not enforced. Normally set to 0xff, limit not enforced

<7:0> curFlowingPackets - Current Number of Flowing Packets - This is how many QFC or FLOWmaster circuits have 'flowing' packets in progress. Cannot be written if RxIn is enabled.

Table 85 CSR 41 Non FLOWmaster Free Cells

Address Offset: 0x052

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RW	0	**nonFlowCells**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

<15:0> - nonFlowCells - Non-FLOWmaster traffic cell pool free size - When QFC or FLOWmaster is enabled for the link, this field contains the number of Rx free cells reserved for traffic without credit control.

Table 86 CSR 42 Static Credits Committed

Address Offset: 0x054

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15 14 13 12 11 10 9 8	RW	RW	0	**rxStaticCommit**	7 6 5 4 3 2 1 0				

<15:0> rxStaticCommit - Receive Static Commitment - This field contains the number of free cells remaining in the credit controlled static cell pool.

Table 87 CSR 43 Dynamic Cells Committed

Address Offset: 0x056

bit	Host	Chip	Reset	Name	bit	Hos	Chip	Reset	Name
15 14 13 12 11 10 9 8	RW	RW	0	**rxDynamicCommit**	7 6 5 4 3 2 1 0				

<15:0> rxDynamicCommit - Receive Dynamic Commitment - This field contains the number of free cells in the credit controlled dynamic cell pool that are reserved for packets in progress.

Table 88 CSR 44 AAL5 Error CID Register

Address Offset: 0x058

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15				**Unused**	7				
14					6				
13					5				
12	RO	WO	0	**aal5ErrorIndex**	4				
11	RO	WO	0	**aal5ErrorCid**	3				
10					2				
9					1				
8					0				

<12> aal5ErrorIndex - AAL5 Error CID Indicator - This field indicates for which interrupt aal5ErrorCid (CSR 44, <11:0>) is set. If this bit is 1, it means that the aal5ErrorCid (CSR 44, <11:0>) is set for the overlimitPkt interrupt (CSR 46 <12>). Otherwise, the aal5ErrorCid (CSR 44, <11:0>) is set for the invalidCrc32 (CSR 46 <10>) interrupt.

<11:0> aal5ErrorCid - AAL5 Error CID Register - This field contains the CID which is associated with either the last overlimitPkt interrupt (CSR 46 <12>) or invalidCrc32 (CSR 46 <10>).

Table 89 CSR 45 Tx Interrupts

Address Offset: 0x05a

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RO	WO	0	**cmPrtyError**	7	RO	WO	0	**rxFifoOutOfSync**
14	RO	WO	0	**lcpAccesErrInt**	6	RO	WO	0	**rxFifoFull**
13	RO	WO	0	**txFifoEmptyIntr**	5	RO	WO	0	**txFreeListErrIntr**
12	RO	WO	0	**badRoPktBme**	4	RO	WO	0	**tiUnexptSopIntr**
11	RO	WO	0	**invalidPktHdrIntr**	3	RO	WO	0	**txParityError**
10	RO	WO	0	**toNoCellSendIntr**	2	RO	WO	0	**rRmFofoFullIntr**
9	RO	WO	0	**toNoCreditsIntr**	1	RO	WO	0	**toInvalidEntryIntr**
8	RO	WO	0	**txFifoOutOfSync**	0	RO	WO	0	**tiInvalidEntryIntr**

<15> cmPrtyError - Cell Memory Parity Error Interrupt - This interrupt is set by the memory process. It indicates that a memory word with wrong parity has been detected. This is a hardware error. Upon receiving this interrupt, the local processor should disable the TC35854F and run diagnostics.

<14> lcpAccesErrInt - Processor Access Error Interrupt - This interrupt is set by LcpPrc. It indicates that the local processor performed an illegal operation, e.g., tried to access a non-existing CSR, tried to write a read-only register, or issued an illegal command to the indirect memory access interface.

<13> txFifoEmptyIntr - Transmit FIFO Empty/Overflow Interrupt - This interrupt is set if an error occurs in the transmit FIFO between the link logic and the core logic. In ATM or SMDS mode, the interrupt is set if the FIFO underflows (i.e., a read is requested when the FIFO is empty) because invalid data will be sent on the link. In PKT mode, the interrupt is set if the FIFO overflows (i.e., a write is attempted when the FIFO is full). In this case, data is lost.

<12> badRoPktBme - Bad RxOut Packet BME Field Interrupt - This interrupt is set by RxOut. It indicates that a cell with a wrong BME field was detected in SMDS or ATM mode. The local processor control firmware should service this interrupt by disabling RxOut, clearing the bad packet, and restarting RxOut. Only the BME field in the first cell and last cell of a packet are checked by RxOut. The BME field of cells in the middle of a packet is ignored.

<11> invalidPktHdrIntr - Invalid Packet Header Interrupt - This interrupt is set by RxOut. It indicates that a reassembled packet attempted to access an entry in RxOut's packet header table where the valid bit was not set. In ATM or SMDS mode, the local processor firmware should service this interrupt by disabling RxOut, clearing the bad packet, and restarting RxOut. In PKT mode, RxOut should be disabled. Data from the receive FIFO continues to be thrashed until a new packet starts. Then, RxOut is enabled again.

<10> toNoCellSendIntr - TxOut No Cell To Send Interrupt - This interrupt is set by TxOut. It indicates that the txCidsReady vector bit for this circuit was set, but when TxOut accessed the CID record, it found that there was no cell ready to be sent. If this event occurs, TxOut sets the interrupt bit, clears the txCidReady vector bit, and sends a null(unassigned) cell for this time slot.

<9> toNoCreditsIntr - TxOut No Credits Interrupt - This interrupt is set by TxOut. It indicates that the txCidsReady vector bit for this circuit was set, but when TxOut accessed the CID record, it found that there were no credits for cell transmission. If this event occurs, TxOut sets the interrupt bit, clears the txCidReady vector bit, and sends a null cell for this time slot.

<8> txFifoOutOfSync - Transmit FIFO Out OF Synchronization Interrupt This interrupt is set by TxLnk in ATM or SMDS mode only. It indicates that TxLnk is not in synchronization with the transmit FIFO data, e.g., if a cell header was expected, but the data was marked as being from the payload or vice versa. This can occur if the transmit FIFO goes empty, as indicated by txFifoEmptyIntr. TxLnk resynchronizes within two cell times after the FIFO empty condition is cleared.

<7> rxFifoOutOfSync - Receive FIFO Out OF Synchronization Interrupt - This interrupt is set by RxIn in ATM or SMDS mode only. It indicates that RxIn is not in synchronization with the receive FIFO data, e.g., if a cell header was expected, but the data was marked as being from the payload or vice versa. This can occur if the receive FIFO is full, as indicated by rxFifoFull. RxIn resynchronizes within two cell times after the FIFO full condition is cleared.

<6> rxFifoFull - Receive FIFO Full Interrupt - This interrupt is set by RxIn. It indicates that the receive FIFO has overflowed, i.e., a write to the FIFO is requested when the FIFO is full.

<5> txFreeListErrIntr - Corrupted Tx free list Interrupt - This interrupt is set by TxIn. It indicates that the Tx free list has been corrupted.

<4> tiUnexptSopIntr TxIn Unexpected Start Of Packet Interrupt - This interrupt is set by TxIn. It indicates that an illegal sequence of byte transfers on the transmit MAC interface has occurred, e.g., if an end of packet indication occurs during fill codes. The following sequence of control signals is considered legal by TxIn, where [..] means optional:

..|FILLER|...|FILLER|START DATA|DATA [FILLER]|...|DATA END|FILLER|...

If an incorrect control signal happens during the first cell of a packet, the packet is dropped. If it happens later, TxIn stops accepting more data. It finishes the current packet and invalidates the AAL frame. For AAL3/4, it sets the cell length to all-ones. For AAL5, it sets the frame length to zero and adds a wrong CRC. Thus, the far-end receiver discards this packet.

<3> txParityError - Transmit Parity Error Interrupt - This interrupt is set by TxIn in ATM or SMDS mode and is set by TxPkt in PKT mode. It indicates that a parity error on the byte-wide, transmit MAC data bus has been detected. In ATM or SMDS mode, if a parity error occurs during the first cell of a packet, the packet is dropped. If it happens later, TxIn stops accepting more data. It finishes the current packet and invalidates the AAL frame. For AAL3/4, it sets the cell length to all-ones. For AAL5, it sets the frame length to zero and adds a wrong CRC. Thus, the far-end receiver discards this packet. In PKT mode, TxPkt discards the current byte and the following data bytes until the end of the packet is reached.

<2> rRmFifoFullIntr - Returned RM FIFO Full Interrupt - This interrupt is set by RxIn. It indicates that the returned RM FIFO has overflowed, i.e., a write to the FIFO is requested when the FIFO is full.

<1> toInvalidEntryIntr - TxOut Invalid Entry Interrupt - This interrupt is set by TxOut in ATM or SMDS mode. It indicates that the valid bit in the TxCidRec table for this circuit is not set (i.e., = 1). If this event occurs, TxOut sets the interrupt and sends a null cell for this time slot.

<0> tiInvalidEntryIntr - TxIn Invalid Entry Interrupt - This interrupt is set by TxIn in ATM or SMDS mode. It indicates that either the valid bit in the TxCidRec for this circuit is not set or the CID obtained from the mapping table is not valid (i.e., zero value). TxIn discards the current packet.

Table 90 CSR 46 Rx Interrupts

Receive Packet Interrupts

Address Offset: 0x05c

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RO	WO	0	**roBadCrcIntr**	7	RO	WO	0	**overlimitVCI**
14	RO	WO	0	**invalidSmdsPkt**	6	RO	WO	0	**overlimitMID**
13	RO	WO	0	**overlimitSmdsPkt**	5	RO	WO	0	**invalidVPI**
12	RO	WO	0	**overlimitPkt**	4	RO	WO	0	**invalidVCI**
11	RO	WO	0	**invalidLen**	3	RO	WO	0	**invalidMID**
10	RO	WO	0	**invalidCrc32**	2	RO	WO	0	**invalidCrc10**
9	RO	WO	0	**underthrshold**	1	RO	WO	0	**invalidPTI**
8	RO	WO	0	**noFreeCell**	0	RO	WO	0	**errQfcRevId**

<15> roBadCrcIntr - Receive Bad CRC Detected Interrupt - This interrupt is set by RxOut if one of the following happens.

1. In ATM or SMDS mode, if checkFddiCrc in pktHdrRec for this circuit is set, it indicates that a corrupted FDDI CRC is detected. This bit is set and the EndData byte in the packet is also marked.
2. In PKT mode, it indicates that a bad HDLC CRC16 or CRC32 is detected. This bit is set and the EndData byte in the packet is also marked.

<14> invalidSmdsPkt - Invalid SMDS Packet Interrupt - This interrupt is set by RxIn if the calculated 32-bit CRC for a SMDS packet does not match the packet CRC and the CRC active bit is set in the SMDS packet.

<13> overlimitSmdsPkt - SMDS Packet Limit Exceeded Interrupt - This interrupt is set by RxIn if a SMDS packet exceeds the packet size limit set by maxPktLength (CSR 4, <8:0>).

<12> overlimitPkt - Packet Limit Exceeded Interrupt - This interrupt is set by RxIn if an ATM AAL5 packet exceeds the packet size limit set by maxPktLength (CSR 4, <8:0>). When this bit is set, its corresponding CID is stored in aal5ErrorCid (CSR 44, <11:0>) and aal5ErrorIndex (CSR 44, <12>) is set to 1.

<11> invalidLen - Invalid AAL5 Length Interrupt - This interrupt is set by RxIn if a received ATM AAL5 packet does not match the packet length field in the AAL5 tail. When this bit is set, its corresponding CID is stored in aal5ErrorCid (CSR 44, <11:0>) and aal5ErrorIndex (CSR 44, <12>) is set to 0.

<10> invalidCrc32 - Invalid AAL5 CRC32 Interrupt - This interrupt is set by RxIn if a received ATM AAL5 packet 32-bit CRC is detected to be in error. When this bit is set, its corresponding CID is stored in aal5ErrorCid (CSR 44, <11:0>) and aal5ErrorIndex (CSR 44, <12>) is set to 0.

<9> underthrshold - Under Free Cell Threshold Interrupt - This interrupt is set by RxIn if a SMDS or ATM cell is received which starts a new packet on a circuit, and the Rx free list cell count is under the threshold set by minRxFrCell (CSR 19, <5:0>). This cell and subsequent cells associated with this packet are discarded. Cells with a packet that is in the middle of being reassembled are allowed to pass through provided the number of receive free cells is not zero.

<8> noFreeCell - No Free Cells Available Interrupt - This interrupt is set by RxIn if a SMDS or ATM cell is received and the number of receive free cells is one or zero. No buffer space is available to do further reassembly. This cell is discarded and its associated packet is marked for discard.

<7> overlimitVCI - RxIn Overlimit VCI Interrupt - This interrupt is set by RxIn in ATM or SMDS mode. It indicates that a cell has been received that is outside the VCI limits that was set for a particular VPI.

<6> overlimitMID - RxIn Overlimit MID Interrupt - This interrupt is set by RxIn in ATM AAL3/4 or SMDS mode. It indicates that a cell has been received that is outside the MID limits that was set for a particular VCI

<5> invalidVPI - RxIn Invalid VPI Interrupt - This interrupt is set by RxIn in ATM or SMDS mode. It indicates that a cell was received for which the VPI record valid bit is false, and either the VPI "Active" bit is also false or the ATM header CLP bit is set.

<4> invalidVCI - RxIn Invalid VCI Interrupt - This interrupt is set by RxIn in ATM or SMDS mode if a SMDS or ATM AAL3, AAL5, or F4 OAM cell is received for which the CID record valid bit is false, and either the CID "pktActive" bit is also false or the ATM header CLP bit is set.

<3> invalidMID - RxIn Invalid MID Interrupt - This interrupt is set by RxIn in ATM or SMDS mode if either of two conditions occur:

1. An SMDS or ATM AAL4 cell is received for which the CID record valid bit is false, and either the CID "pktActive" bit is also false or the ATM header CLP bit is set.
2. An SMDS or ATM AAL4 cell is received for which the MID is outside the limits set for the VCI, and either the CID "pktActive" bit is also false or the ATM header CLP bit is set.

<2> invalidCrc10 - RxIn Invalid CRC10 Interrupt - This interrupt is set by RxIn in ATM or SMDS mode. It indicates that a cell was received on an AAL3 or AAL4 circuit with an incorrect CRC10. The current packet is discarded by RxIn.

<1> invalidPTI - RxIn Invalid PTI Interrupt - This interrupt is set by RxIn in ATM or SMDS mode. It indicates that a cell was received with PTI = 7.

<0> errQfcRevId - Error QFC Revision ID - This interrupt is set by RxIn in ATM or SMDS mode when running in QFC (CSR 3, bit <5> is set to 1). It indicates that a QFC protocol control cell was received with wrong QFC Revision ID other than 1.

Table 91 CSR 47 Link Interrupts

Address Offset: 0x05e

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RO	WO	0	**rxStaticAdjusted**	7	RO	WO	0	**tiAbortPktIntr**
14	RO	WO	0	**rxCidStaticOvfl**	6	RO	WO	0	**txQLimitIntr**
13	RO	WO	0	**rxNoFreeFMcells**	5	RO	WO	0	**tiBigPktIntr**
12	RO	WO	0	**rxErrorRPID**	4	RO	WO	0	**errMsgType**
11	RO	WO	0	**txFrListEmptyIntr**	3	RO	WO	0	**rxErrQfcPID**
10	RO	WO	0	**roZeroPktLenIntr**	2	RO	WO	0	**zeroERinRm**
9	RO	WO	0	**badCellLen**	1	RO	WO	0	**txPktTimedOut**
8	RO	WO	0	**badSeqOrSegType**	0	RO	WO	0	**txZeroPayload**

<15> rxStaticAdjusted - This interrupt is set when the rxStaticCommit field has been modified by either a incrStaticCommit or decrStaticCommit operation, in order to notify the firmware that the operation has been completed.

<14> rxCidStaticOvfl - Static Allocation For CID Overflow Interrupt - This bit is set when a cell for a stuck credit controlled circuit is received and no free cell in static pool is available for this circuit. This also means that not returned credits for this CID is over the maximum allowed value, which equals the addition of the content of one bslVcLimitDefx register (CSR 62, CSR 63) and one in QFC mode. In FLOWmaster mode, it equals to the addition of the content of one bslVcLimitDef0 register (CSR 62) and one.

<13> rxNoFreeFMcells - RxIn No Free FLOWmaster Cells - This interrupt is set by RxIn when there are not enough cells in the Rx credit controlled cell pool to accept a cell that arrived. This interrupt should not occur in normal operation and indicates either a chip bug or a configuration error.

<12> rxErrorRPID - Rx Receive Error Protocol ID Interrupt - This interrupt is set by RxIn when received RM cell has wrong protocol ID, which is neither QFC nor ER. Cell discarded.

<11> txFrListEmptyIntr - Transmit Free List Empty Interrupt - Indicates that the transmit free cell list is empty, i.e., there is no more buffer space available to store segmented packets. TxIn deasserts TXRDY on the transmit MAC interface and waits for cells to be returned to the free cell list TxOut. When TxIn detects that the free cell list is no longer empty, it asserts TXRDY and continues processing the packet.

<10> roZeroPktLenIntr - RxOut Zero Packet Length Interrupt - This interrupt is set by RxOut. It indicates one of the following two cases and RxOut processes accordingly.

1. In ATM or SMDS mode, if required to strip 3-byte zero and packet length is less than 4 bytes, or not required to strip 3-byte zero and packet length is zero, RxOut discards the packet.
2. In PKT mode, if stripping HDLC CRC is required and packet length is less than 2 bytes in HDLC CRC16 case or less than 4 bytes in HDLC CRC 32 case, RxOut either discards the packet when the additional packet header is not added by RxOut or marks the bad CRC in EndData byte when the header is added by RxOut.

<9> badCellLen - Bad Cell Length Interrupt - This interrupt is set by RxIn if a SMDS or ATM cell is received on an AAL3 or AAL4 circuit that is not the last cell of a packet and the cell's length is not 44.

<8> badSeqOrSegType - Bad Sequence Or Segment Type Interrupt - This interrupt is set by RxIn if a SMDS or ATM cell is received on an AAL3 or AAL4 circuit, and either the segment type or the sequence number is not consistent with the last cell received on the circuit. This implies that some cells on the circuit have been lost.

<7> tiAbortPktIntr - Transmit Abort Packet Interrupt - This interrupt is set by TxIn in SMDS or ATM mode and by TxPkt in pkt mode. It indicates that a packet was discarded.

<6> txQLimitIntr - Transmit Queue Limit Interrupt - This interrupt is set by TxIn in ATM or SMDS mode. It indicates that a circuit has exceeded the maximum number of cells it is allowed to consume from the free cell buffer pool. When this condition occurs, TxIn sets this bit, discards the current packet, and moves to the next packet for transmission.

<5> tiBigPktIntr - Transmit AAL5 Packet Over Limit Interrupt - This interrupt is set by TxIn in ATM or SMDS mode. It indicates that an AAL5 packet has exceeded the maximum number of bytes, 65535. TxIn then marks the bad AAL5 packet in AAL5 trailer, indicated by zero packet length and wrong AAL5 CRC. The receiver will discard this packet.

<4> errMsgType - Receive Error QFC Control Cell Interrupt - This interrupt is set by RxIn in ATM or SMDS mode and in QFC mode. It indicates that a QFC RM cell is received with incorrect message type. The receiver will discard the cell.

<3> rxErrQfcPID - Rx Receive Error QFC Protocol ID Interrupt - This interrupt is set by RxIn when received QFC RM cell has wrong protocol ID carried on the connections of RCC_VC of each VP.

<2> zeroERinRm - Zero ER field in received backward RM cell Interrupt - This interrupt is set by TxOut when received zero ER field in ER backward RM cell.

<1> txPktTimedOut - Transmit packet timed out Interrupt - This interrupt is set by TxOut when it finds out that the cell to be transmitted has the difference between the content in the timeStamp field in the cell header and the current time (CSR 78 bits <11:3>) larger than 2 seconds.

<0> txZeroPayload - Transmit packet zero length payload Interrupt - This interrupt is set by TxIn when it finds out that segmented packet has zero length payload field. No cells will be generated for this packet.

Table 92 CSR 48 RxIn Credit Interrupts

Address Offset: 0x060

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RO	WO	0	**rxCongestionSeen**	7				
14	RO	WO	0	**rxScredTaken**	6				
13	RO	WO	0	**rxSCredFifoOvfl**	5				
12				**Unused**	4				
11	RO	WO	0	**errorCid**	3				
10					2				
9					1				
8					0				

<15> rxCongestionSeen - Received Cell Experienced Congestion Interrupt - When this bit is set, a cell with its PTI field valued either 2 or 3 in the ATM header is received. The circuit ID this cell belonged to is indicated in the errorCid register (CSR 48, <11:0>).

<14> rxScredTaken - Single Credit FIFO Over Threshold Interrupt - When this bit is set, the single credit FIFO is over the threshold indicated by the rxSCredFifoThresh register (CSR 19, <10:8>). In this case, the local processor should take actions to deal with this "pseudo-overflow".

<13> rxSCredFifoOvfl - Single Credit FIFO Overflow Interrupt - When this bit is set, a write to single credit FIFO results in the FIFO overflow. The corresponding CID is in the errorCid register (CSR 48, <11:0>).

<11:0> errorCid - Receive CID Associated With Credit Actions - This field identifies CIDs for one of the following interrupts:

- rxScredTaken (CSR 48, <14>)
- rxSCredFifoOvfl (CSR 48, <13>)
- rxCongestionSeen (CSR 48, <15>)

Table 93 CSR 49 Tx Interrupt Mask

Transmit Interrupt Mask

Address Offset: 0x062

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RO	0	**cmPrtyErrorMask**	7	RW	RO	0	**rxFifoOutOfSyncMask**
14	RW	RO	0	**lcpAccesErrMask**	6	RW	RO	0	**rxFifoFullMask**
13	RW	RO	0	**txFifoEmptyMask**	5	RW	RO	0	**txFreeListErrMask**
12	RW	RO	0	**badRoPktBmeMask**	4	RW	RO	0	**tiUnexptSopMask**
11	RW	RO	0	**invalidPktHdrMask**	3	RW	RO	0	**txParityErrorMask**
10	RW	RO	0	**toNoCellSendMask**	2	RW	RO	0	**rRmFifoFullMask**
9	RW	RO	0	**toNoCreditsMask**	1	RW	RO	0	**toInvalidEntryMask**
8	RW	RO	0	**txFifoOutOfSyncMask**	0	RW	RO	0	**tiInvalidEntryMask**

<15> cmPrtyErrorMask - Cell Memory Parity Error Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<14> lcpAccesErrMask - Local Processor Access Error Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<13> txFifoEmptyMask - Transmit FIFO Empty Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<12> badRoPktBmeMask - Bad RxOut BME Field Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<11> invalidPktHdrMask - Invalid Packet Header Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<10> toNoCellSendMask - TxOut No Cell To Send Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<9> toNoCreditsMask - TxOut No Credits Available Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<8> txFifoOutOfSyncMask - Transmit FIFO Out Of Synchronization Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<7> rxFifoOutOfSyncMask - Receive FIFO Out Of Synchronization Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<6> rxFifoFullMask - Receive FIFO Full Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<5> txFreeListErrMask - Transmit Free List Error Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<4> tiUnexptSopMask - TxIn Unexpected Start Of Packet Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<3> txParityErrorMask - Transmit Parity Error Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<2> rRmFifoFullIntrMask - Returned RM FIFO Full Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<1> toInvalidEntryMask - TxOut Invalid Entry Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<0> tiInvalidEntryMask - TxIn Invalid Entry Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

Table 94 CSR 50 Rx Interrupt Mask

Receive Cell Interrupt Mask

Address Offset: 0x064

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RO	0	**roBadCrcMask**	7	RW	RO	0	**overlimitVCIMask**
14	RW	RO	0	**invalidSmdsPktMask**	6	RW	RO	0	**overlimitMIDMask**
13	RW	RO	0	**overlimitSmdsPktMask**	5	RW	RO	0	**invalidVPIMask**
12	RW	RO	0	**overlimitPktMask**	4	RW	RO	0	**invalidVCIMask**
11	RW	RO	0	**invalidLenMask**	3	RW	RO	0	**invalidMIDMask**
10	RW	RO	0	**invalidCrc32Mask**	2	RW	RO	0	**invalidCrc10Mask**
9	RW	RO	0	**underthrsholdMask**	1	RW	RO	0	**invalidPTIMask**
8	RW	RO	0	**noFreeCellMask**	0	RW	RO	0	**errQfcRevIdMask**

<15> roBadCrcMask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<14> invalidSmdsPktMask - Invalid SMDS Packet Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<13> overlimitSmdsPktMask - Overlimit SMDS Packet Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<12> overlimitPktMask - Overlimit Packet Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<11> invalidLenMask - Invalid Length Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<10> invalidCrc32Mask - Invalid CRC32 Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<9> underthrsholdMask - Under-Threshold Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<8> noFreeCellMask - No Free Cell Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<7> overlimitVCIMask - Overlimit VCI Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<6> overlimitMIDMask - Overlimit MID Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<5> invalidVPIMask - Invalid VPI Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<4> invalidVCIMask - Invalid VCI Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<3> invalidMIDMask - Invalid MID Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<2> invalidCrc10Mask - Invalid CRC10 Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<1> invalidPTIMask - Invalid PTI Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<0> errQfcRevIdMask - Error QFC Revision ID Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

Table 95 CSR 51 Link Interrupt Mask

Address Offset: 0x066

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RO	0	**rxStaticAdjustedMask**	7	RW	RO	0	**tiAbortPktMask**
14	RW	RO	0	**rxCidStaticOvflMask**	6	RW	RO	0	**txQLimitMask**
13	RW	RO	0	**rxNoFreeFMcellsMask**	5	RW	RO	0	**tiBigPktMask**
12	RW	RO	0	**rxErrorRPIDMask**	4	RW	RO	0	**errMsgTypeMask**
11	RW	RO	0	**txFrListEmptyMask**	3	RW	RO	0	**rxErrQfcPIDMask**
10	RW	RO	0	**roZeroPktLenMask**	2	RW	RO	0	**zeroERinRmMask**
9	RW	RO	0	**badCellLenMask**	1	RW	RO	0	**txPktTimedOutMask**
8	RW	RO	0	**badSeqOrSegTypeMask**	0	RW	RO	0	**txZeroPayloadMask**

<15> rxStaticAdjustedMask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<14> rxCidStaticOvflMask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<13> rxNoFreeFMcellsMask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<12> rxErrorRPIDMask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<11> txFrListEmptyMask - Transmit Free Cell List Empty Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<10> roZeroPktLenMask - RxOut Zero Packet Length Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<9> badCellLenMask - Bad Cell Length Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<8> badSeqOrSegTypeMask - Bad Sequence Or Segment Type Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<7> tiAbortPktMask - Transmit Abort Packet Interrupt Mask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<6> txQLimitMask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<5> tiBigPktMask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<4> errMsgTypeMask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<3> rxErrQfcPIDMask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<2> zeroERinRmMask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<1> txPktTimedOutMask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<0> txZeroPayloadMask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

Table 96 CSR 52 RxIn Credits Interrupts Mask

Address Offset: 0x068

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RO	0	**rxCongestionSeenMask**	7				
14	RW	RO	0	**rxScredTakenMask**	6				
13	RW	RO	0	**rxSCredFifoOvflMask**	5				
12				**Unused**	4				
11					3				
10					2				
9					1				
8					0				

<15> rxCongestionSeenMask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<14> rxScredTakenMask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<13> rxSCredFifoOvflMask - When this value is 1, enable the interrupt. When this value is 0, mask (disable) the interrupt.

<12:0> unused

Table 97 CSR 53 Tx Cell Counter

Address Offset: 0x06a

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RW		**txCellCounter**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

<15:0> txCellCount - Transmit cell counter - This is the counter counting the number of cells transmitted by the transmit engine, not including NULL cells.

Table 98 CSR 54 Rx Cell Counter

Address Offset: 0x06c

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RW		**rxCellCounter**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

<15:0> rxCellCounter - Receive cell counter - This is the counter counting the number cells received, not including NULL cells and cells discarded due to different reasons.

Table 99 CSR 55 VP 3 Bandwidth

Virtual Path #3 Bandwidth

Address Offset: 0x06e

bit	Host	Chip	Reset	Name		bit	Host	Chip	Reset	Name
15 14 13 12				**Unused**		7 6 5 4				
11 10						3 2				
9 8	RW	RO	0	**vp3Bw**		1 0				

<9:0> vp3Bw - VP 3 Bandwidth - This field contains the bandwidth assigned to VP with index 3.

Table 100 CSR 56 VP 2 Bandwidth

Virtual Path #2 Bandwidth

Address Offset: 0x070

bit	Host	Chip	Reset	Name		bit	Host	Chip	Reset	Name
15 14 13 12				**Unused**		7 6 5 4				
11 10						3 2				
9 8	RW	RO	0	**vp2Bw**		1 0				

<9:0> vp2Bw - VP 2 Bandwidth - This field contains the bandwidth assigned to VP with index 2.

Table 101 CSR 57 VP 1 Bandwidth

Virtual Path #1 Bandwidth

Address Offset: 0x072

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15 14 13 12 11 10				**Unused**	7 6 5 4 3 2 1 0				
9 8	RW	RO	0	**vp1Bw**					

<9:0> vp1Bw - VP 1 Bandwidth - This field contains the bandwidth assigned to VP with index 1.

Table 102 CSR 58 VP 0 Bandwidth

Virtual Path #0 Bandwidth

Address Offset: 0x074

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15 14 13 12 11 10				**Unused**	7 6 5 4 3 2 1 0				
9 8	RW	RO	0	**vp0Bw**					

<9:0> vp0Bw - VP 0 Bandwidth - This field contains the bandwidth assigned to VP with index 0. The above bandwidths are used to calculate ABR rates for ER circuits. Bandwidth is expressed as a sub-multiple of 0x0200. For example, if VP0 were allocated 25% of total bandwidth, vp0Bw = 0x200*25% = 0x080. Where fractions of 0x200 do not equal whole numbers, bandwidth value should be rounded up. For example, 20% bandwidth would be expressed as 0x67, not 0x66.

Table 103 CSR 59 QFC N4 Register

Address Offset: 0x076

bit	Host	Chip	Reset	Name		bit	Host	Chip	Reset	Name
15				**Unused**		7				
14						6				
13						5	RW	RO	0	**N4ForVp2**
12						4				
11	RW	RO	0	**N4ForVp0**		3				
10						2	RW	RO	0	**N4ForVp3**
9						1				
8	RW	RO	0	**N4ForVp1**		0				

This register contains the maximum number (called N4 in QFC standard) of BSU records packed into one BSU cell for four VPs supported by TC35854F.

<11:9> N4ForVp0 - QFC N4 Value for VP 0 - This field defines the N4 value for VP 0.

<8:6> N4ForVp1 - QFC N4 Value for VP 1 - This field defines the N4 for VP with index 1.

<5:3> N4ForVp2 - QFC N4 Value for VP 2 - This field defines the N4 value for VP with index 2.

<2:0> N4ForVp2 - QFC N4 Value for VP 3 - This field defines the N4 value for VP with index 3.

Table 104 CSR 60 VPI Images Register 1

Address Offset: 0x078

bit	Host	Chip	Reset	Name		bit	Host	Chip	Reset	Name
15	RW	RO	0	**vp2Image**		7	RW	RO	0	**vp1Image**
14						6				
13						5				
12						4				
11						3				
10						2				
9						1				
8						0				

<15:8> vp2Image - VPI Mapped from VP 2 - This field contains the real VPI which is mapped to VP index 2 internally in TC35854F. If the number of VP is smaller than 3, this field must set to zero.

<7:0> vp1Image - VPI Mapped from VP 1 - This field contains the real VPI which is mapped to VP index 1 internally in TC35854F. If there is only one VP running, this field must be set to zero.

Table 105 CSR 61 VPI Images Register 2

Address Offset: 0x07a

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15				**Unused**	7	RW	RO	0	**vp3Image**
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

<7:0> vp3Image - VPI Mapped from VP 3 - This field contains the real VPI which is mapped to VP index 3 internally in TC35854F. If the number of VP is smaller than 4, this field must be set to zero.

Table 106 CSR 62 BSL VC Limit Default 0

Buffer State Limit, Virtual Circuit Limit Defaults 0

Address Offset: 0x07c

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RW	0	**incrStaticCommit**	7				
14	RW	RW	0	**decrStaticCommit**	6	RW	RO	0	**bslVcLimitDef1**
13	RW	RO	0	**bslVcLimitDef0**	5				
12					4				
11					3				
10					2				
9					1				
8					0				

<15> incrStaticCommit - Request Increment Rx Static Commit - This field is set by the firmware to request that TC35854F increase the Rx Static Commitment pool size by the maximum number of credits on a circuit (the static credits allocation of a VP + 1, the index of the VP is given in CSR 63, maxAIndex field). TC35854F performs the increment when there are adequate uncommitted free cells to do so and clears this field.

<14> decrStaticCommit - Request Decrement Rx Static Commit - This field is set by the firmware to request that TC35854F decrease the Rx Static Commitment pool size by the maximum number of credits on a circuit (the static credits allocation of a VP + 1, the index of the VP is given in CSR 63, maxAIndex field). TC35854F performs the decrement immediately and clears this field.

<13:7> bslVcLimitDef0 - QFC BSL VC Limit Default for VP 0 - In QFC mode, this field contains 7 bits of the VC limit default from BSL for Vp 0. When a QFC connection of VP 0 transmits a cell, the equation [1] in the QFC specification must be met. This field indicates the number of credit controlled cells can be sent before receiving returned credits. In FLOWmaster mode, it also indicates the number that is one less than the maximum number of static credits initialized on any circuit in the FLOWmaster mode. (In general, all circuits of one VP should receive the same number of credits.)

<6:0> bslVcLimitDef1 - QFC BSL VC Limit Default for VP 1 - This field contains 7 bits of the VC limit default from BSL for Vp 1. It is used in the exactly same way as the bslVcLimitDef0 field is used. This field is used in the QFC mode only.

Table 107 CSR 63 BSL VC Limit Default 1

Buffer State Limit, Virtual Circuit Limit Defaults 1

Address Offset: 0x07e

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15 14	RW	RO		**maxAIndex**	7				
13 12 11 10 9 8	RW	RO	0	**bslVcLimitDef2**	6 5 4 3 2 1 0	RW	RO	0	**bslVcLimitDef3**

<15:14> maxAIndex - VP Index of VPI with Largest Static Allocation for VC - This field indicates the VP index which has the largest static credits allocation for VC when the chip is running in the QFC mode. In the FLOWmaster mode, this field must be set to zero.

<13:7> bslVcLimitDef2 - QFC BSL VC Limit Default for VP 2 - This field contains 7 bits of the VC limit default from BSL for Vp 2. It is used in the exactly same way as the bslVcLimitDef0 field is used. This field is used in the QFC mode only.

<6:0> bslVcLimitDef3 - QFC BSL VC Limit Default for VP 3 - This field contains 7 bits of the VC limit default from BSL for Vp 3. It is used in the exactly same way as the bslVcLimitDef0 field is used. This field is used in the QFC mode only.

Table 108 CSR 64 BSL Link Limit VP 0 Lsp

Buffer State Limit for Link, Virtual Path 0, least significant part

Address Offset: 0x080

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15				**Unused**	7				
14					6				
13					5				
12					4				
11					3				
10	RW	RO	0	**bslLinkLimit0Lsp**	2				
9					1				
8					0				

Table 109 CSR 65 BSL Link Limit VP 0 Msp

Buffer State Limit for Link, Virtual Path 0, most significant part

Address Offset: 0x082

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RO	0	**bslLinkLimit0Msp**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

This two registers contain the limit for all QFC connections of VP 0 to send cell. The total number of cells on flight of all QFC connections of VP 0 must be smaller than this limit.

CSR 64 <10:0> bslLinkLimit0Lsp - QFC BSL Link Limit for VP 0 Lsp - This field contains 11 least significant bits of the link limit from BSL for Vp 0.

CSR 65 <15:0> bslLinkLimit0Msp - QFC BSL Link Limit for VP 0 Msp - This field contains 16 most significant bits of the link limit from BSL for Vp 0.

Table 110 CSR 66 BSL Link Limit VP 1 Lsp

Buffer State Limit for Link, Virtual Path 1, least significant part

Address Offset: 0x084

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15				**Unused**	7				
14					6				
13					5				
12					4				
11					3				
10	RW	RO	0	**bslLinkLimit1Lsp**	2				
9					1				
8					0				

Table 111 CSR 67 BSL Link Limit VP 1 Msp

Buffer State Limit for Link, Virtual Path 1, most significant part

Address Offset: 0x086

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RO	0	**bslLinkLimit1Msp**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

This two registers contain the limit for all QFC connections of VP 1 to send cell. The total number of cells on flight of all QFC connections of VP 1 must be smaller than this limit.

CSR 66 <10:0> bslLinkLimit1Lsp - QFC BSL Link Limit for VP 1 Lsp - This field contains 11 least significant bits of the link limit from BSL for Vp 1.

CSR 67 <15:0> bslLinkLimit1Msp - QFC BSL Link Limit for VP 1 Msp - This field contains 16 most significant bits of the link limit from BSL for Vp 1.

Table 112 CSR 68 BSL Link Limit VP 2 Lsp

Buffer State Limit for Link, Virtual Path 2, least significant part

Address Offset: 0x088

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15 14 13 12				**Unused**	7 6 5 4				
11					3				
10 9 8	RW	RO	0	**bslLinkLimit2Lsp**	2 1 0				

Table 113 CSR 69 BSL Link Limit VP 2 Msp

Buffer State Limit for Link, Virtual Path 2, least significant part

Address Offset: 0x08a

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15 14 13 12	RW	RO	0	**bslLinkLimit2Msp**	7 6 5 4				
11 10 9 8					3 2 1 0				

This two registers contain the limit for all QFC connections of VP 2 to send cell. The total number of cells on flight of all QFC connections of VP 2 must be smaller than this limit.

CSR 68 <10:0> bslLinkLimit2Lsp - QFC BSL Link Limit for VP 2 Lsp - This field contains 11 least significant bits of the link limit from BSL for Vp 2.

CSR 69 <15:0> bslLinkLimit2Msp - QFC BSL Link Limit for VP 2 Msp - This field contains 16 most significant bits of the link limit from BSL for Vp 2.

Table 114 CSR 70 BSL Link Limit VP 3 Lsp

Buffer State Limit for Link, Virtual Path 2, least significant part

Address Offset: 0x08c

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15				**Unused**	7				
14					6				
13					5				
12					4				
11					3				
10	RW	RO	0	**bslLinkLimit3Lsp**	2				
9					1				
8					0				

Table 115 CSR 71 BSL Link Limit VP 3 Msp

Buffer State Limit for Link, Virtual Path 3, most significant part

Address Offset: 0x08e

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RO	0	**bslLinkLimit3Msp**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

This two registers contain the limit for all QFC connections of VP 3 to send cell. The total number of cells on flight of all QFC connections of VP 3 must be smaller than this limit.

CSR 70 <15:0> bslLinkLimit3Msp - QFC BSL Link Limit for VP 3 Msp - This field contains 16 most significant bits of the link limit from BSL for Vp 3.

CSR 71 <10:0> bslLinkLimit3Lsp - QFC BSL Link Limit for VP 3 Lsp - This field contains 11 least significant bits of the link limit from BSL for Vp 3.

Table 116 CSR 72 N2 Value For VC Register 1

Address Offset: 0x090

bit	Host	Chip	Reset	Name		bit	Host	Chip	Reset	Name
15 14 13 12 11 10 9 8	RW	RO	0	**vcN2forVp0**		7 6 5 4 3 2 1 0	RW	RO	0	**vcN2forVp1**

Table 117 CSR 73 N2 Value For VC Register 2

Address Offset: 0x092

bit	Host	Chip	Reset	Name		bit	Host	Chip	Reset	Name
15 14 13 12 11 10 9 8	RW	RO	0	**vcN2forVp2**		7 6 5 4 3 2 1 0	RW	RO	0	**vcN2forVp3**

These two registers contain the number of cells forwarded before one BSU record can be composed for one QFC connection of a VP (called N2 in QFC standard). Every time one cell of a QFC connection is forwarded, N2count in the receive circuit identifier record for this connection increments. When N2count reaches value for the VP defined in this CSR, a BSU record is composed and N2count is reset to 0.

CSR 72 <15:8> vcN2forVp0 - N2 value for QFC VCs of VP 0 - This field defines the N2 value for a QFC connection of Vp 0.

CSR 72 <7:0> vcN2forVp1 - N2 value for QFC VCs of VP 1 - This field defines the N2 value for a QFC connection of Vp 1.

CSR 73 <15:8> vcN2forVp2 - N2 value for QFC VCs of VP 2 - This field defines the N2 value for a QFC connection of Vp 2.

CSR 73 <7:0> vcN2forVp3 - N2 value for QFC VCs of VP 3 - This field defines the N2 value for a QFC connection of Vp 3.

Table 118 CSR 74 N2 Value For Link Register 1

Address Offset: 0x094

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RO	0	**linkN2forVp0**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

This register and the following three registers contain the number of cells forwarded before one BSU record can be composed for the link or a tunnel (called N2 in QFC standard). Every time one cell of the link or a tunnel is forwarded, a counter is incremented. When the counter reaches value for the link or a tunnel defined in these CSR registers, a BSU record is composed and the counter is reset to 0.

<15:0> linkN2forVp0 - QFC N2 value for the link - This field defines the N2 value for the link.

Table 119 CSR 75 N2 Value For Link Register 2

Address Offset: 0x096

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RO	0	**linkN2forVp1**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

<15:0> linkN2forVp1 - This field defines the N2 value for the tunnel VP 1.

Table 120 CSR 76 N2 Value For Link Register 3

Address Offset: 0x098

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RO	0	**linkN2forVp2**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

<15:0> linkN2forVp2 - This field defines the N2 value for the tunnel VP 2.

Table 121 CSR 77 N2 Value For Link Register 4

Address Offset: 0x09a

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15	RW	RO	0	**linkN2forVp3**	7				
14					6				
13					5				
12					4				
11					3				
10					2				
9					1				
8					0				

<15:0> linkN2forVp3 - N2 value for tunnel 3 - This field defines the N2 value for the tunnel VP 3.

Table 122 CSR 78 Timer Msp

Address Offset: 0x09c

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15 14 13 12 11 10 9 8	RW	RW	0	**TimerMsp**	7 6 5 4 3 2 1 0				

Table 123 CSR 79 Timer Lsp

Address Offset: 0x09e

bit	Host	Chip	Reset	Name	bit	Host	Chip	Reset	Name
15 14 13 12					7 6 5 4 3 2 1 0				
11 10 9 8	RW	RW	0	**TimerLsp**					

CSR 78 <15:0> TimerMsp
CSR 79 <11:0> TimerLsp

These two registers forms a 28-bit timer in TC35854F used for different purposes. The timer is updated every 240 ns. For QFC application, this is the timer used to measure the round-trip time. For Explicit Rate application, bits <11:3> in CSR 78, Timer Msp register is the measurement for the ADTF time-out used by the transmit engine and the software. The reassembly engine reads the value of bits <10:6> in CSR 78, Timer Msp register at the beginning of the first cell of a new packet and the firmware subsequently uses it for packet reassembly time-out checking. The segmentation engine copies the value of bits <11:3> in CSR 78, Timer Msp to the cell header when it puts a cell into the cell memory and the transmit engine and the firmware use it for bridge packet time-out checking. These two registers should be read only by the LCP in the normal operation. Only under certain circumstances, the LCP may want to reset the timer.

Table 124 CSR 80 QFC RCC_VC Register

Address Offset: 0x0a0

bit	Host	Chip	Reset	Name		bit	Host	Chip	Reset	Name
15 14 13 12				**Unused**		7 6 5 4				
11 10 9 8	RW	RO	1e	**RCC_VC**		3 2 1 0				

<11:0> RCC_VC - QFC RCC_VC Register - This field contains the VCI which is used to carry QFC protocol units.

Table 125 CSR 81 Bottom Rate Registerr

Address Offset: 0x0a2

bit	Host	Chip	Reset	Name		bit	Host	Chip	Reset	Name
15 14 13				**Unused**		7 6 5				
12	RW	RO	0	**bottomRate**		4				
11 10 9 8						3 2 1 0				

<11:0> bottomRate - Lowest rate Register - This field contains the lowest rate for which a VC is scheduled in the schedule table for any rate connections. For any VC with rate larger than this rate, the VC will be scheduled in the schedule table and served every opportunity. For any VC with rate larger than the half of this rate and smaller than this rate, the VC is still scheduled in the schedule table but served every other opportunities. For any VC with rate smaller than the half of this rate, the VC will be put into the slow queue, which is served at the rate equal to or smaller than 10 cells per second. Bits <12:9> of this field represents the 4-bit exponent of the rate and the rest bits are for 9-bit mantissa.

ELECTRICAL CHARACTERISTIC

Preliminary

ABSOLUTE MAXIMUM RATINGS

Vdd(5V)	Supply Voltage(5V)	-0.5V to 7.0V
Vdd(3V)	Supply Voltage(3V)	-0.5V to 5.0V
Vin(5V)	Input Voltage(5V)	-0.5V to Vdd(5V)+0.5V
Pd	Power Dissipation	1.8W
Tsolder	Soldering Temperature (10sec)	240°C
Tstg	Storage Temperature	-65°C to 150°C
Topr	Operating Temperature	0°C to 70°C

DC CHARACTERISTICS

		Min.	Typ.	Max.	Unit
Vdd(5V)	Supply Voltage(5V)	4.75	5.00	5.25	V
Vdd(3V)	Supply Voltage(3.3V)	3.0	3.3	3.6	V
Iddd(5V)	Operating Current(5V)	T.B.D.			
Iddd(3V)	Operating Current(3.3V)	T.B.D.			
Iih	Input High Current (excluding pull-up buffer)			10	µA
Iil	Input Low Current (excluding pull-up buffer)			-10	µA

5V Input/Output and bi-directional (TTL, CMOS)

		Min.	Typ.	Max.	Unit
Vih	Input High Voltage (TTL)	2.0	-	-	V
Vil	Input Low Voltage (TTL)	-		0.8	V
Vih	Input High Voltage (CMOS)	3.0	-	-	V
Vil	Input Low Voltage (CMOS)	-		2.0	V
Voh	Output High Voltage (CMDT) (IOH=0mA)	-	-	Vdd(5V)	V
	Output High Voltage (CMDT) (IOH=-1.5mA)	2.4	-	-	V
Vol	Output Low Voltage (CMDT) (IOL=1.5mA)	-	-	0.4	V
Voh	Output High Voltage (others) (IOH=0mA)	-	-	Vdd(5V)	V
	Output High Voltage (others) (IOH=-2.5mA)	2.4	-	-	V
Vol	Output Low Voltage (others) (IOL=2.5mA)	-	-	0.4	V

Preliminary

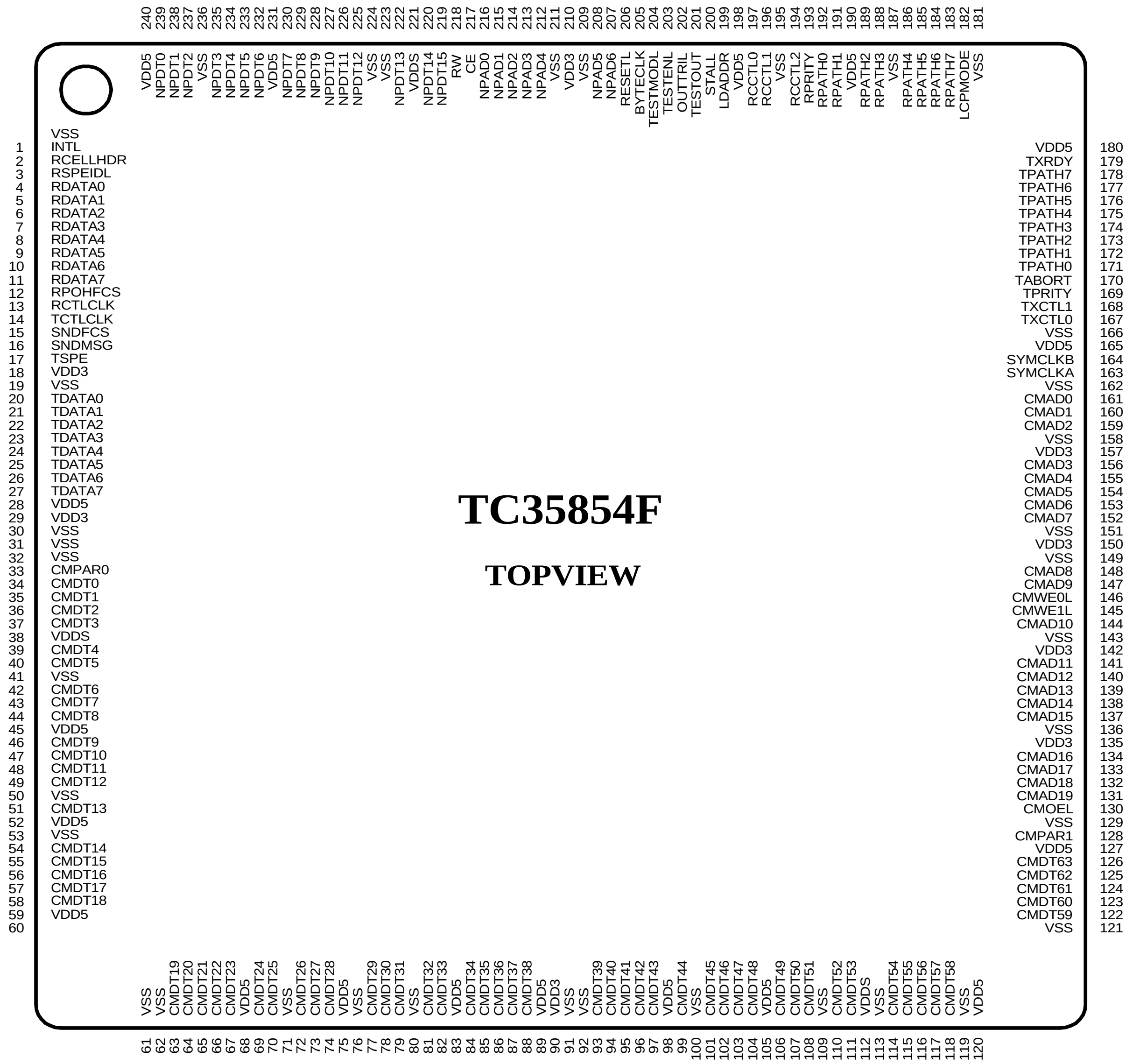
3V Output (LVTTL)

		Min.	Typ.	Max.	Unit
Voh	Output High Voltage (IOH=-0mA)	-	-	Vdd(3V)	V
	Output High Voltage (IOH=-2.5mA)	2.4	-	-	V
Vol	Output Low Voltage (IOL=2.5mA)	-	-	0.4	V

UTOPIA I/F Input/Output

		Min.	Typ.	Max.	Unit
Vih	Input High Voltage	2.0	-	-	V
Vil	Input Low Voltage	-		0.8	V
Voh	Output High Voltage (IOH=0mA)	-	-	Vdd(3V)	V
	Output High Voltage (IOH=-4.0mA)	2.4	-	-	V
Vol	Output Low Voltage (IOL=4.0mA)	-	-	0.4	V

Pin Diagram


TC35854F
TOPVIEW
1 VSS
2 INTL
3 RCELLHDR
4 RSPEIDL
5 RDATA0
6 RDATA1
7 RDATA2
8 RDATA3
9 RDATA4
10 RDATA5
11 RDATA6
12 RDATA7
13 RPOHFCS
14 RCTLCLK
15 TCTLCLK
16 SNDFCS
17 SNDMSG
18 TSPE
19 VDD3
20 VSS
21 TDATA0
22 TDATA1
23 TDATA2
24 TDATA3
25 TDATA4
26 TDATA5
27 TDATA6
28 TDATA7
29 VDD5
30 VDD3
31 VSS
32 VSS
33 VSS
34 CMPAR0
35 CMDT0
36 CMDT1
37 CMDT2
38 CMDT3
39 VDDS
40 CMDT4
41 CMDT5
42 VSS
43 CMDT6
44 CMDT7
45 CMDT8
46 VDD5
47 CMDT9
48 CMDT10
49 CMDT11
50 CMDT12
51 VSS
52 CMDT13
53 VDD5
54 VSS
55 CMDT14
56 CMDT15
57 CMDT16
58 CMDT17
59 CMDT18
60 VDD5
61 VSS
62 VSS
63 CMDT19
64 CMDT20
65 CMDT21
66 CMDT22
67 CMDT23
68 VDD5
69 CMDT24
70 CMDT25
71 VSS
72 CMDT26
73 CMDT27
74 CMDT28
75 VDD5
76 VSS
77 CMDT29
78 CMDT30
79 CMDT31
80 VSS
81 CMDT32
82 CMDT33
83 VDD5
84 CMDT34
85 CMDT35
86 CMDT36
87 CMDT37
88 CMDT38
89 VDD5
90 VDD3
91 VSS
92 VSS
93 CMDT39
94 CMDT40
95 CMDT41
96 CMDT42
97 CMDT43
98 VDD5
99 CMDT44
100 VSS
101 CMDT45
102 CMDT46
103 CMDT47
104 CMDT48
105 VDD5
106 CMDT49
107 CMDT50
108 CMDT51
109 VSS
110 CMDT52
111 CMDT53
112 VDDS
113 VSS
114 CMDT54
115 CMDT55
116 CMDT56
117 CMDT57
118 CMDT58
119 VSS
120 VDD5
121 VSS
122 CMDT59
123 CMDT60
124 CMDT61
125 CMDT62
126 CMDT63
127 VDD5
128 CMPAR1
129 VSS
130 CMOEL
131 CMAD19
132 CMAD18
133 CMAD17
134 CMAD16
135 VDD3
136 VSS
137 CMAD15
138 CMAD14
139 CMAD13
140 CMAD12
141 CMAD11
142 VDD3
143 VSS
144 CMAD10
145 CMWE1L
146 CMWE0L
147 CMAD9
148 CMAD8
149 VSS
150 VDD3
151 VSS
152 CMAD7
153 CMAD6
154 CMAD5
155 CMAD4
156 CMAD3
157 VDD3
158 VSS
159 CMAD2
160 CMAD1
161 CMAD0
162 VSS
163 SYMCLKA
164 SYMCLKB
165 VDD5
166 VSS
167 TXCTL0
168 TXCTL1
169 TPRITY
170 TABORT
171 TPATH0
172 TPATH1
173 TPATH2
174 TPATH3
175 TPATH4
176 TPATH5
177 TPATH6
178 TPATH7
179 TXRDY
180 VDD5
181 VSS
182 LCPMODE
183 RPATH7
184 RPATH6
185 RPATH5
186 RPATH4
187 VSS
188 RPATH3
189 RPATH2
190 VDD5
191 RPATH1
192 RPATH0
193 RPRITY
194 RCCTL2
195 VSS
196 RCCTL1
197 RCCTL0
198 VDD5
199 LDADDR
200 STALL
201 TESTOUT
202 OUTTRIL
203 TESTENL
204 TESTMODL
205 BYTECLK
206 RESETL
207 NPAD6
208 NPAD5
209 VSS
210 VDD3
211 VSS
212 NPAD4
213 NPAD3
214 NPAD2
215 NPAD1
216 NPAD0
217 CE
218 RW
219 NPDT15
220 NPDT14
221 VDDS
222 NPDT13
223 VSS
224 VSS
225 NPDT12
226 NPDT11
227 NPDT10
228 NPDT9
229 NPDT8
230 NPDT7
231 VDD5
232 NPDT6
233 NPDT5
234 NPDT4
235 NPDT3
236 VSS
237 NPDT2
238 NPDT1
239 NPDT0
240 VDD5

Pin Listing By Pin Number

1	VSS	61	VSS	121	VSS	181	VSS
2	INTL	62	VSS	122	CMDT59	182	LCPMODE
3	RCELLHDR	63	CMDT19	123	CMDT60	183	RPATH7
4	RSPEIDL	64	CMDT20	124	CMDT61	184	RPATH6
5	RDATA0	65	CMDT21	125	CMDT62	185	RPATH5
6	RDATA1	66	CMDT22	126	CMDT63	186	RPATH4
7	RDATA2	67	CMDT23	127	VDD5	187	VSS
8	RDATA3	68	VDD5	128	CMPAR1	188	RPATH3
9	RDATA4	69	CMDT24	129	VSS	189	RPATH2
10	RDATA5	70	CMDT25	130	CMOEL	190	VDD5
11	RDATA6	71	VSS	131	CMAD19	191	RPATH1
12	RDATA7	72	CMDT26	132	CMAD18	192	RPATH0
13	RPOHFCS	73	CMDT27	133	CMAD17	193	RPRITY
14	RCTLCLK	74	CMDT28	134	CMAD16	194	RCCTL2
15	TCTLCLK	75	VDD5	135	VDD3	195	VSS
16	SNDFCS	76	VSS	136	VSS	196	RCCTL1
17	SNDMSG	77	CMDT29	137	CMAD15	197	RCCTL0
18	TSPE	78	CMDT30	138	CMAD14	198	VDD5
19	VDD3	79	CMDT31	139	CMAD13	199	LDADDR
20	VSS	80	VSS	140	CMAD12	200	STALL
21	TDATA0	81	CMDT32	141	CMAD11	201	TESTOUT
22	TDATA1	82	CMDT33	142	VDD3	202	OUTTRIL
23	TDATA2	83	VDD5	143	VSS	203	SCANENL
24	TDATA3	84	CMDT34	144	CMAD10	204	SCANMODL
25	TDATA4	85	CMDT35	145	CMWE1L	205	BYTECLK
26	TDATA5	86	CMDT36	146	CMWE0L	206	RESETL
27	TDATA6	87	CMDT37	147	CMAD9	207	NPAD6
28	TDATA7	88	CMDT38	148	CMAD8	208	NPAD5
29	VDD5	89	VDD5	149	VSS	209	VSS
30	VDD3	90	VDD3	150	VDD3	210	VDD3
31	VSS	91	VSS	151	VSS	211	VSS
32	VSS	92	VSS	152	CMAD7	212	NPAD4
33	VSS	93	CMDT39	153	CMAD6	213	NPAD3
34	CMPAR0	94	CMDT40	154	CMAD5	214	NPAD2
35	CMDT0	95	CMDT41	155	CMAD4	215	NPAD1
36	CMDT1	96	CMDT42	156	CMAD3	216	NPAD0
37	CMDT2	97	CMDT43	157	VDD3	217	CE
38	CMDT3	98	VDD5	158	VSS	218	RW
39	VDD5	99	CMDT44	159	CMAD2	219	NPDT15
40	CMDT4	100	VSS	160	CMAD1	220	NPDT14
41	CMDT5	101	CMDT45	161	CMAD0	221	VDD5
42	VSS	102	CMDT46	162	VSS	222	NPDT13
43	CMDT6	103	CMDT47	163	SYMCLKA	223	VSS
44	CMDT7	104	CMDT48	164	SYMCLKB	224	VSS
45	CMDT8	105	VDD5	165	VDD5	225	NPDT12
46	VDD5	106	CMDT49	166	VSS	226	NPDT11

47	CMDT9	107	CMDT50	167	TXCTL0	227	NPDT10
48	CMDT10	108	CMDT51	168	TXCTL1	228	NPDT9
49	CMDT11	109	VSS	169	TPRITY	229	NPDT8
50	CMDT12	110	CMDT52	170	TABORT	230	NPDT7
51	VSS	111	CMDT53	171	TPATH0	231	VDD5
52	CMDT13	112	VDD5	172	TPATH1	232	NPDT6
53	VDD5	113	VSS	173	TPATH2	233	NPDT5
54	VSS	114	CMDT54	174	TPATH3	234	NPDT4
55	CMDT14	115	CMDT55	175	TPATH4	235	NPDT3
56	CMDT15	116	CMDT56	176	TPATH5	236	VSS
57	CMDT16	117	CMDT57	177	TPATH6	237	NPDT2
58	CMDT17	118	CMDT58	178	TPATH7	238	NPDT1
59	CMDT18	119	VSS	179	TXRDY	239	NPDT0
60	VDD5	120	VDD5	180	VDD5	240	VDD5

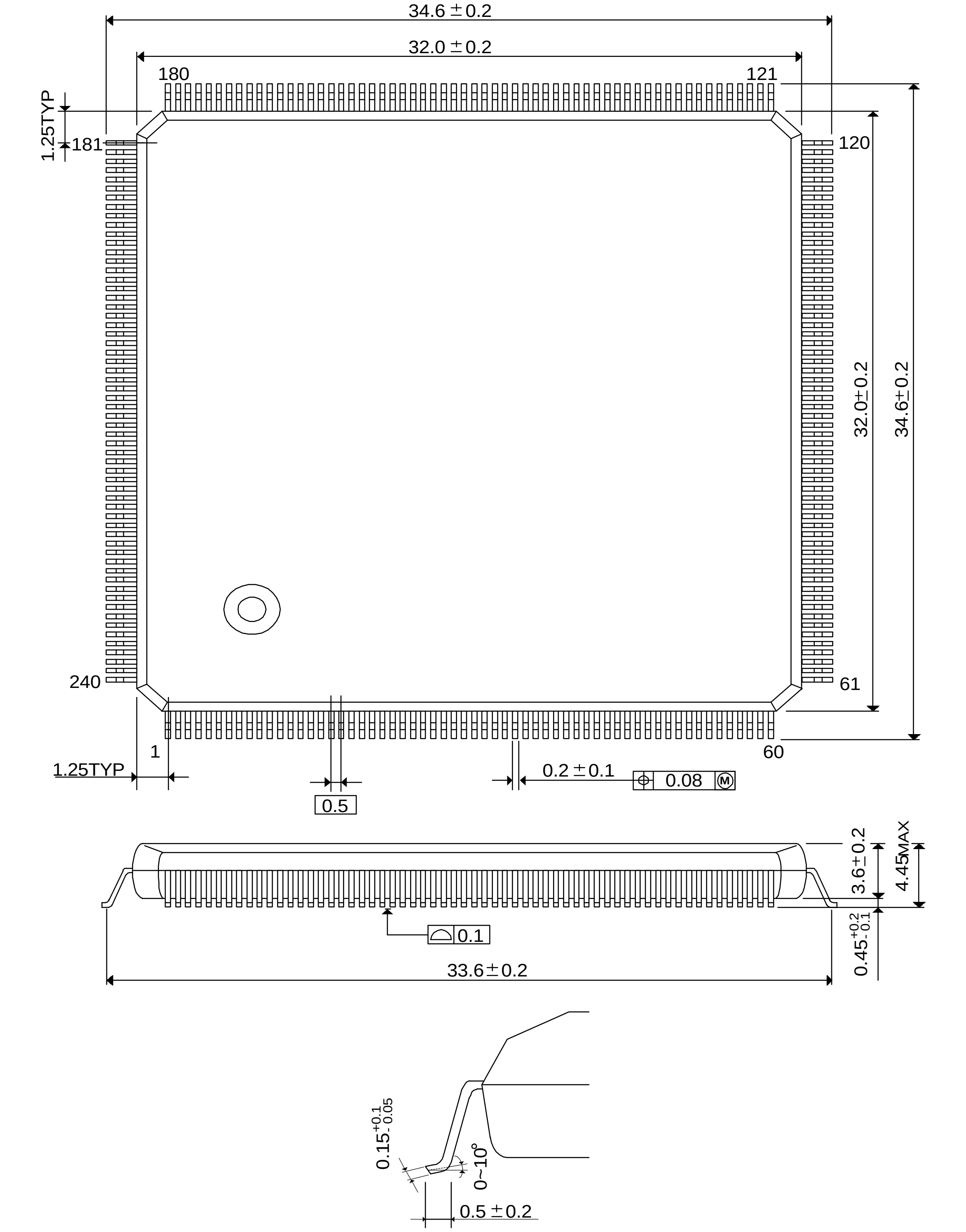
Pin Listing Alphabetically

205	BYTECLK	97	CMDT43	194	RCCTL2	150	VDD3
217	CE	99	CMDT44	3	RCELLHDR	157	VDD3
161	CMAD0	101	CMDT45	14	RCTLCLK	210	VDD3
160	CMAD1	102	CMDT46	5	RDATA0	29	VDD5
144	CMAD10	103	CMDT47	6	RDATA1	39	VDD5
141	CMAD11	104	CMDT48	7	RDATA2	46	VDD5
140	CMAD12	106	CMDT49	8	RDATA3	53	VDD5
139	CMAD13	41	CMDT5	9	RDATA4	60	VDD5
138	CMAD14	107	CMDT50	10	RDATA5	68	VDD5
137	CMAD15	108	CMDT51	11	RDATA6	75	VDD5
134	CMAD16	110	CMDT52	12	RDATA7	83	VDD5
133	CMAD17	111	CMDT53	206	RESETL	89	VDD5
132	CMAD18	114	CMDT54	192	RPATH0	98	VDD5
131	CMAD19	115	CMDT55	191	RPATH1	105	VDD5
159	CMAD2	116	CMDT56	189	RPATH2	112	VDD5
156	CMAD3	117	CMDT57	188	RPATH3	120	VDD5
155	CMAD4	118	CMDT58	186	RPATH4	127	VDD5
154	CMAD5	122	CMDT59	185	RPATH5	165	VDD5
153	CMAD6	43	CMDT6	184	RPATH6	180	VDD5
152	CMAD7	123	CMDT60	183	RPATH7	190	VDD5
148	CMAD8	124	CMDT61	13	RPOHFCS	198	VDD5
147	CMAD9	125	CMDT62	193	RPRITY	221	VDD5
35	CMDT0	126	CMDT63	4	RSPEIDL	231	VDD5
36	CMDT1	44	CMDT7	218	RW	240	VDD5
48	CMDT10	45	CMDT8	203	SCANENL	1	VSS
49	CMDT11	47	CMDT9	204	SCANMODL	20	VSS
50	CMDT12	130	CMOEL	16	SNDFCS	31	VSS
52	CMDT13	34	CMPAR0	17	SNDMSG	32	VSS
55	CMDT14	128	CMPAR1	200	STALL	33	VSS
56	CMDT15	146	CMWE0L	163	SYMCLKA	42	VSS
57	CMDT16	145	CMWE1L	164	SYMCLKB	51	VSS
58	CMDT17	2	INTL	170	TABORT	54	VSS
59	CMDT18	182	LCPMODE	15	TCTLCLK	61	VSS
63	CMDT19	199	LDADDR	21	TDATA0	62	VSS
37	CMDT2	216	NPAD0	22	TDATA1	71	VSS
64	CMDT20	215	NPAD1	23	TDATA2	76	VSS
65	CMDT21	214	NPAD2	24	TDATA3	80	VSS
66	CMDT22	213	NPAD3	25	TDATA4	91	VSS
67	CMDT23	212	NPAD4	26	TDATA5	92	VSS
69	CMDT24	208	NPAD5	27	TDATA6	100	VSS
70	CMDT25	207	NPAD6	28	TDATA7	109	VSS
72	CMDT26	239	NPDT0	201	TESTOUT	113	VSS
73	CMDT27	238	NPDT1	171	TPATH0	119	VSS
74	CMDT28	227	NPDT10	172	TPATH1	121	VSS
77	CMDT29	226	NPDT11	173	TPATH2	129	VSS
38	CMDT3	225	NPDT12	174	TPATH3	136	VSS

78	CMDT30	222	NPDT13	175	TPATH4	143	VSS
79	CMDT31	220	NPDT14	176	TPATH5	149	VSS
81	CMDT32	219	NPDT15	177	TPATH6	151	VSS
82	CMDT33	237	NPDT2	178	TPATH7	158	VSS
84	CMDT34	235	NPDT3	169	TPRITY	162	VSS
85	CMDT35	234	NPDT4	18	TSPE	166	VSS
86	CMDT36	233	NPDT5	167	TXCTL0	181	VSS
87	CMDT37	232	NPDT6	168	TXCTL1	187	VSS
88	CMDT38	230	NPDT7	179	TXRDY	195	VSS
93	CMDT39	229	NPDT8	19	VDD3	209	VSS
40	CMDT4	228	NPDT9	30	VDD3	211	VSS
94	CMDT40	202	OUTTRIL	90	VDD3	223	VSS
95	CMDT41	197	RCCTL0	135	VDD3	224	VSS
96	CMDT42	196	RCCTL1	142	VDD3	236	VSS

Package Outline Drawing

Unit : mm



REFLOW

For epoxy resin molded packages, the material has a storing tendency to absorb moisture. If Surface Mount Device suffers thermal stress of solder reflow under the wet device condition, the reliability of device will be deteriorate remarkably. So dry packing is performed to TC35854F.
TC35854F has some restraint for solder reflow.

Method of Solder Reflow

This device is permitted only Far Infrared Reflow. In the case of Medium / Near Infrared Reflow and V.P.S, the reliability of device will be deteriorate remarkably.

Condition of Solder Reflow

Method of Heat

We recommended Far Infrared Reflow with top/bottom heating.
The soldering should be performed within 30 seconds at more than 210^{o}C and 240^{o}C maximum.

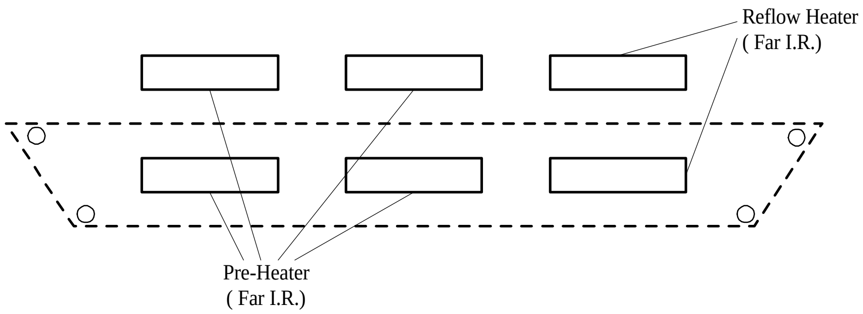


Figure 21 Method of Heat

Recommended Temperature Profile

The soldering should be performed with Recommended temperature profile. Recommended temperature profile is shown in Figure 22.

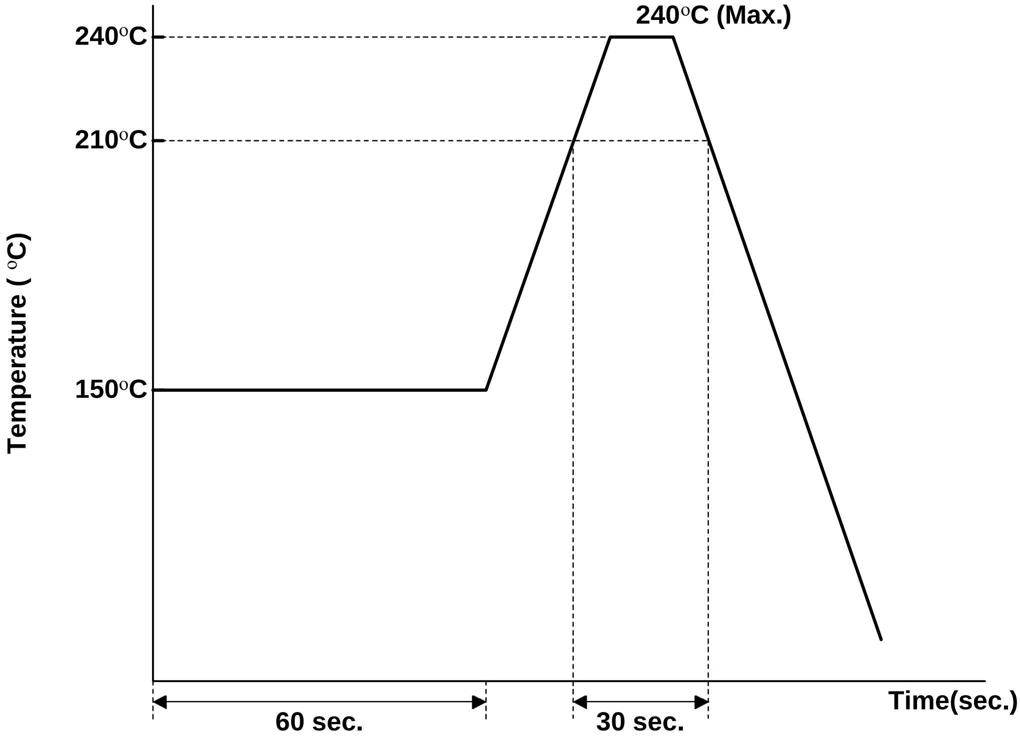


Figure 22 Recommended Temperature Profile for I.R. Soldering

Dry Package

Dry packing is applied to TC35854F. After the customer opens the bag, the parts must be mounted or soldered within 24 hours under normal storage RH = 60%, Ta = 30°C.
If all the parts can not be soldered within the recommended period after opening the bag, pre-baking must be performed. The recommended pre-baking conditions are as follows:

Head proof tray type : 125°C/20hours baking with the original heat proof pack trays