DESCRIPTION

The 8260 Arithmetic Logic Element is a monolithic gate array incorporating four full-adders structured in a look-ahead mode. The device may be used as four mutually independent exclusive NOR or AND gates by proper addressing of the inhibit lines.

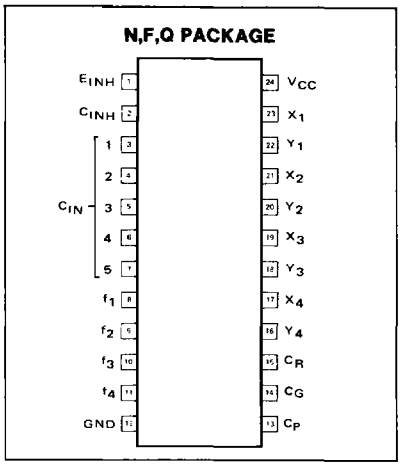
As a four-bit adder the 8260 permits high speed parallel addition of four sets of data and features both simultaneous addition on a character to character and on a bit to bit basis within the package.

When true input variables are used, the true sum is formed at the f output. Inverted input variables produce the complement of the sum of the true variables.

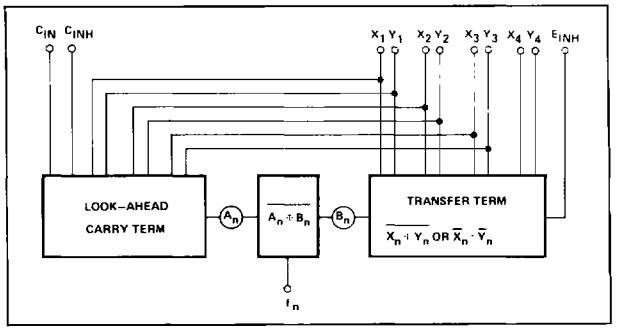
The carry-outs available are: Internally Generated (C_G); Propagated (C_p); and Ripple (C_R). This gives the 8260 complete flexibility when used in Ripple Carry or Anticipated Carry Adder Systems.

PIN CONFIGURATION

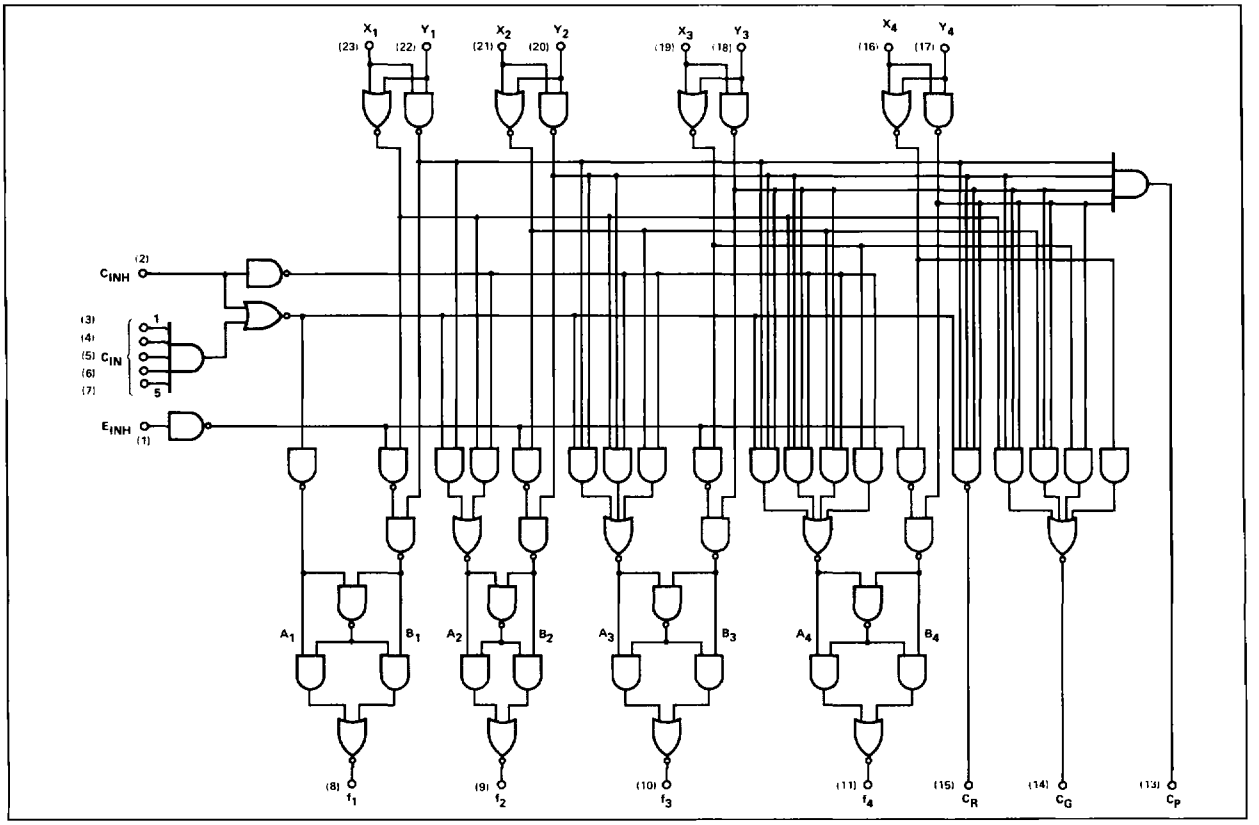
8260-N,F,Q



BLOCK DIAGRAM



LOGIC DIAGRAM



LOGIC

8260-N,F,Q

TRUTH TABLE

$C_{INH} = 1 \longrightarrow A_n = 1$
$C_{INH} = 0 \longrightarrow A_n = \downarrow$

C_{IN}	A_1	A_1	X_1	Y_1	A_2	A_2	X_2	Y_2	A_3	A_3	X_3	Y_3	A_4
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	1	0	0	0	1	0
		0	1	0	0	0	1	0	0	0	1	0	0
		0	1	1	1	0	1	1	1	0	1	1	1
		1	0	0	0	1	0	0	0	1	0	0	0
		1	0	1	1	1	0	1	1	1	0	1	1
		1	1	0	1	1	1	0	1	1	1	0	1
		1	1	1	1	1	1	1	1	1	1	1	1

A_n	B_n	f_n
0	0	1
0	1	0
1	0	0
1	1	1

E_{INH}	X_n	Y_n	B_n
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

SWITCHING CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 54$

PARAMETER	LIMITS TYP	LIMITS MAX	UNIT
Propagation Delay			
X_n, Y_n, C_{in} to C_R	14	20	ns
X_n, Y_n to C_p, C_G	14	20	
X_n, Y_n to f_n	24	33	
C_{in} to f_n	14	22	

MODE OF OPERATION

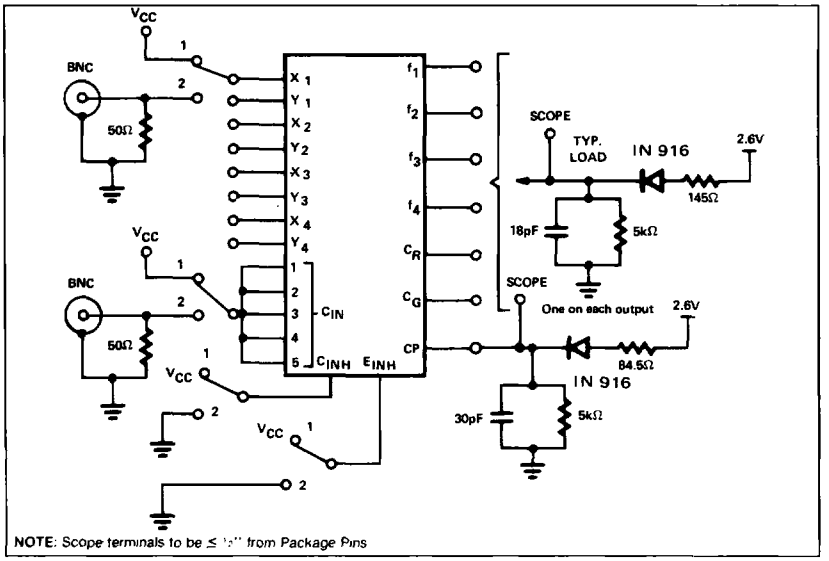
INPUTS	Least Significant C_{IN} Inputs to be*	CONTROLS C_{INH}	CONTROLS E_{INH}	f	
X_n, Y_n	0	0	0	Σ_n	Add
	0	0	1	--	Not used
	0	1	0	$X_nY_n + \overline{X}_n\overline{Y}_n$	Coincidence
	0	1	1	X_nY_n	AND
$\overline{X}_n$, $\overline{Y}_n$	1	0	0	$\overline{\Sigma}_n$	Add
	1	0	1	---	Not Used
	1	1	0	$\overline{X}_n\overline{Y}_n + X_nY_n$	Coincidence
	1	1	1	$\overline{X}_n\overline{Y}_n$	AND

*Least significant of a "Multiple Package" adder system

AC TEST TABLE

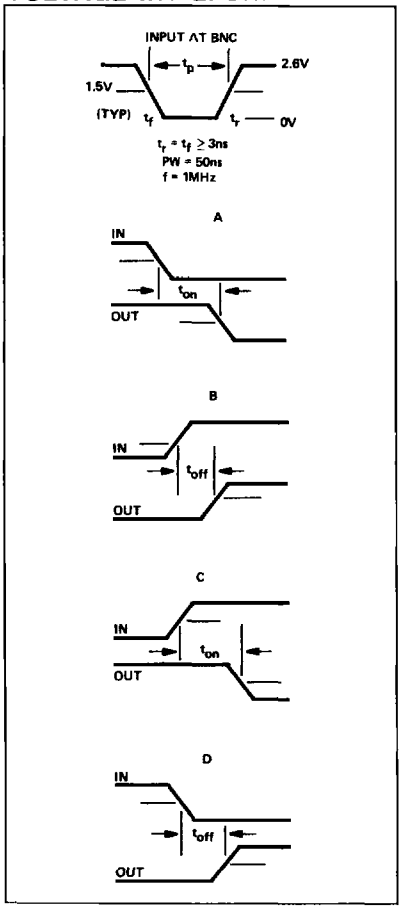
STEP NO.	DELAY FROM-TO	DRIVEN INPUTS	SWITCH POSITION: OTHER INPUTS X_1	Y_1	X_2	Y_2	X_3	Y_3	X_4	Y_4	C_{IN}	E_{INH}	C_{INH}	WAVEFORM TYPE
1	X_n to C_R or X_n to C_p	2	2	1	2	1	2	1	2	1	2	2	2	A,B C,D
2	Y_n to C_R or Y_n to C_p	2	1	2	1	2	1	2	1	2	2	2	2	A,B C,D
3	X_n, Y_n to f_n	2	1	1	1	1	1	1	1	1	1	1	1	A,B
4	C_{IN} to C_R	2	2	2	2	2	2	2	2	2	2	2	2	A,B
5	C_{IN} to f_n	2	1	2	1	2	1	2	1	2	2	2	2	C,D

AC TEST FIGURE



NOTE: Scope terminals to be ≤ ½" from Package Pins

VOLTAGE WAVEFORM



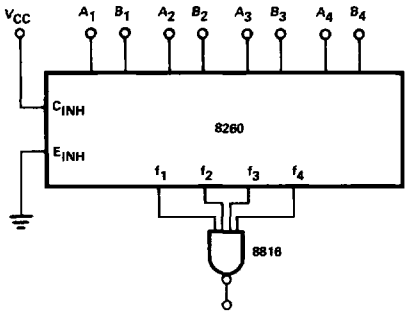
TYPICAL APPLICATIONS

The 8260 contains the control logic necessary to allow operation as a general purpose arithmetic logic device. Below, the internal carries are inhibited to effect Exclusive-NOR or coincidence operation. The 87260 may also be operated as four independent AND gates to implement masking and similar requirements of micro-programming.

The Ripple Adder System is the simplest but also the slowest application of the 8260. The typical total addition time (input to sum output for 12-bit ripple adder is 42ns).

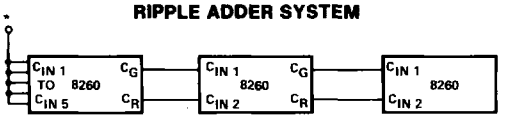
The Fast Adder System provides complete carry look-ahead addition for words to 24 bits in length and is the fastest application of the 8260 units. The typical total addition time for a 24 bit fast adder is 42ns.

FOUR-BIT COMPARATOR



"0" = A B

RIPPLE ADDER SYSTEM



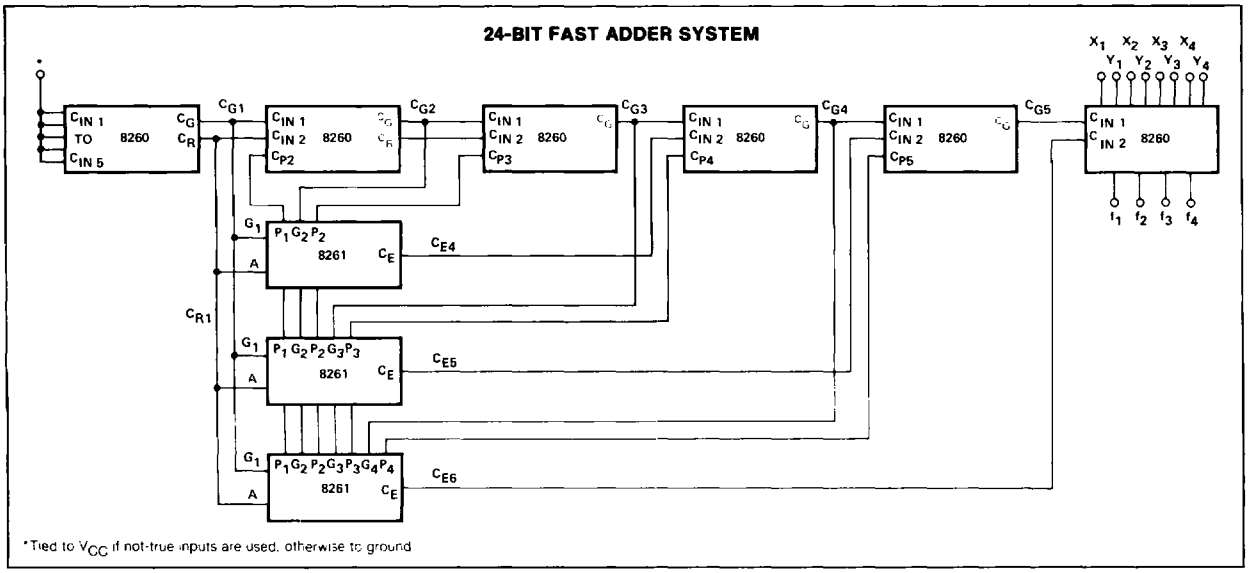
*Tied to VCC if not-true inputs are used, otherwise to ground

LOGIC

ARITHMETIC LOGIC ELEMENT 8260

8260-N,F,Q

TYPICAL APPLICATIONS



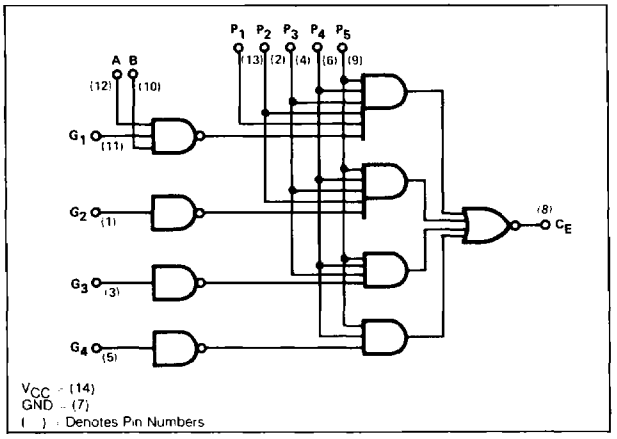
FAST CARRY EXPANDER 8261

8261-A,F,W

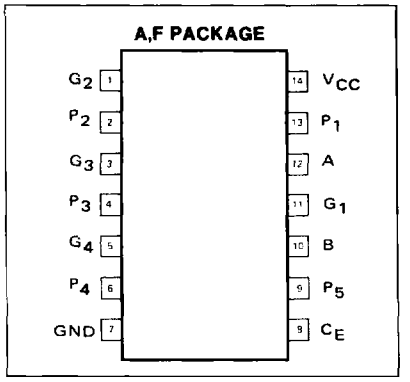
DESCRIPTION

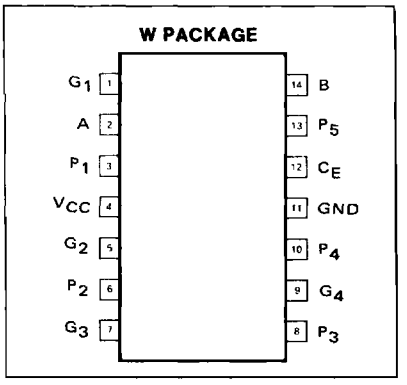
The 8261 Fast Carry Extender is a monolithic gate array designed specifically to be used in conjunction with the 8260 Arithmetic Logic element. A 8260/8261 combination facilitates the implementation of the look-ahead technique in adder systems, thus considerably improving propagation times. The circuit structure of this array is of the familar TTL type.

LOGIC DIAGRAM



PIN CONFIGURATION





8261-A,F,W

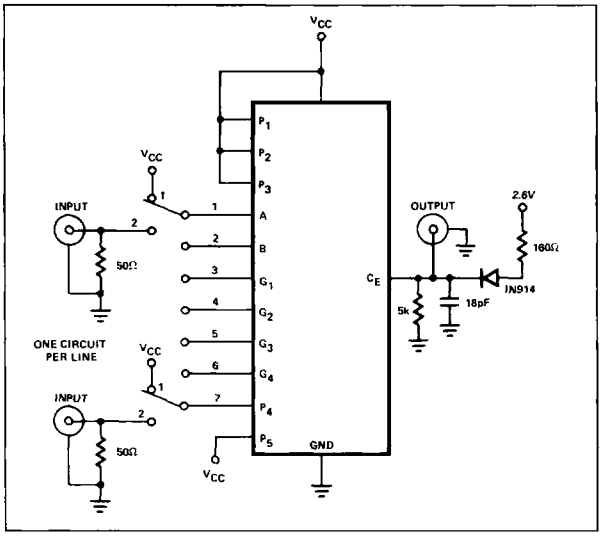
SWITCHING CHARACTERISTICS T_A = 25°C, V_{CC} = 5V

PARAMETER		LIMITS TYP	LIMITS MAX	UNIT
t_{on}	Turn-on delay			
	G to C_E	16	25	ns
	P to C_E	13	25	
t_{off}	Turn-off delay			
	G to C_E	16	23	ns
	P to C_E	9	15	

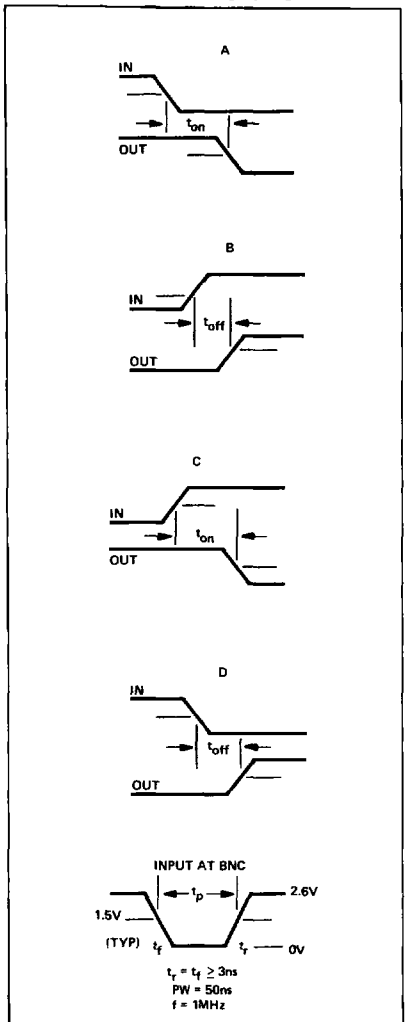
AC TEST TABLE

PIN DESIGNATION	INPUT A	B	G_1	G_2	G_3	G_4	P_4	WAVEFORM
1	PULSE	1	1	1	1	1	1	A,B
2	1	PULSE	1	1	1	1	1	
3	1	1	PULSE	1	1	1	1	
4	1	1	1	PULSE	1	1	1	
5	1	1	1	1	PULSE	1	1	
6	1	1	1	1	1	PULSE	1	
7	2	2	2	2	2	2	PULSE	C,D

AC TEST FIGURE

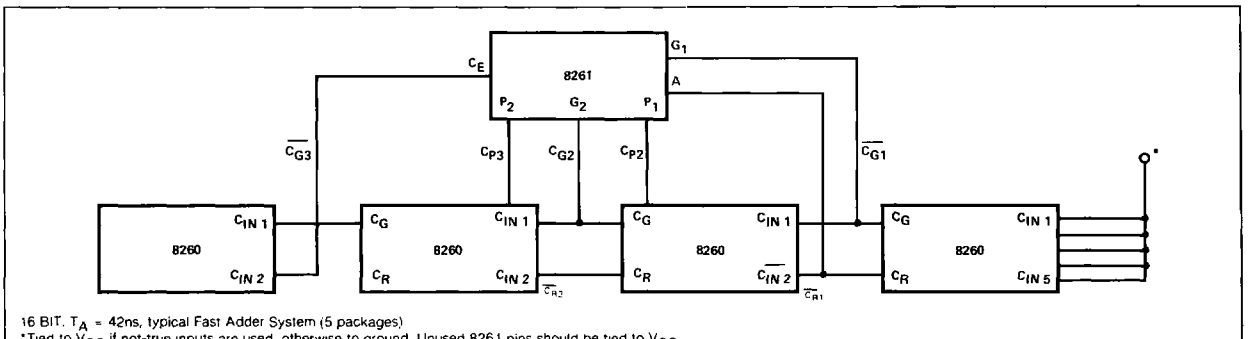


VOLTAGE WAVEFORMS



NOTES:
A. Position 1 on all switches provides a logical "1". Position 2 on all switches provides a logical "0" when input signal is not present.
B. All measurements are made at 1.5 volts level.

TYPICAL APPLICATION



16 BIT, T_A = 42ns, typical Fast Adder System (5 packages)
*Tied to V_{CC} if not-true inputs are used, otherwise to ground. Unused 8261 pins should be tied to V_{CC}.

LOGIC