FEATURES

- Complies with ANSI, Bellcore and ITU-T specifications
- Supports STS-12/STM-4 to STS-48/STM-16 Mux/Demux functions
- 8-bit LVDS data path for STS-48/STM-16 data
- 8-bit LVTTL data path with parity for each STS-12/STM-4 data stream
- Optionally calculates even or odd parity over parallel data bus or data and frame pulse
- Compatible with AMCC S3041/S3042 Mux/Demux chipset
- Compatible with PMC PM5355 User Network Interface device and PMC PM5312 STTX
- Optionally calculates and inserts Byte Interleaved Parity (B1)
- Receive side Byte Interleave parity (B1) compare, insertion, and error indication (B1ERR)
- Optionally calculates and inserts M1 Bytes, and recalculates and inserts the B2 parity bytes due to the M1 insertions
- Optionally inserts section-trace bytes (J0/Z0) in the transmit path
- Diagnostic Loopback Mode
- Out of Frame (OOF) monitor and alarm indication
- Loss of Frame (LOF) monitor and alarm indication
- Loss of Signal (LOS) monitor and alarm indication
- Squelch Mode: Provides downstream clock during Clock Recovery Failure
- Receive J0 Frame Pulse (J0FP) indicator
- Performs optional Frame synchronous scrambling and descrambling
- Provides synchronization signal to STS-12/STM-4 Network Interface Processors
- Single 3.3V supply
- 5 Volt tolerant input
- 208-pin TEP PQFP package

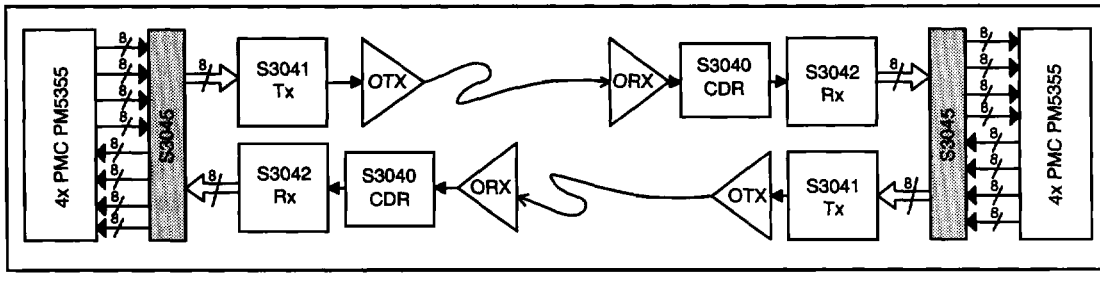
APPLICATIONS

- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add drop multiplexers
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment
- ATM Switch Backbones

GENERAL DESCRIPTION

The S3045 SONET/SDH byte interleave chip is a fully integrated STS-12/STM-4 to STS-48/STM-16 Mux/Demux device. The S3045 performs all necessary byte interleave and byte de-interleave functions for multiplexing and de-multiplexing of four STS-12/STM-4 data streams into/from a single STS-48/STM-16 data stream. The S3045 functions in conformance with SONET/SDH transmission standards and is suitable for SONET-based ATM applications. Figure 1 shows a typical network application. Byte Interleave parity (B1) is calculated and inserted for the transmit path and calculated, compared and inserted for the receive path. Optional frame synchronous scrambling and descrambling are performed, and an STS-12/STM-4 framing signal is provided to the STS-12/STM-4 interface processors to allow synchronization of the receive STS-12/STM-4 data streams.

Figure 1. System Block Diagram



S3045 OVERVIEW

The S3045 byte interleave chip implements SONET/SDH byte interleave functions required to multiplex/demultiplex four STS-12/STM-4 data streams into a single STS-48/STM-16 data stream. Each of the four STS-12/STM-4 transmit/receive data streams uses an 8-bit parallel LVTTL interface with parity to maintain compatibility with industry standard network interface processors. The STS-48/STM-16 data stream uses an 8-bit parallel LVDS data path to be compatible with the S3041/S3042 Mux/Demux chipset. The block diagram in Figure 2 shows the basic operation of the chip. This chip can be used with the S3041 and S3042 to implement the front end of SONET equipment. The chip includes byte interleave circuitry along with B1 calculation, M1 calculation, J0/Z0 insertion, and B1 verification circuitry. STS-48/STM-16 data stream is monitored in the receive path for OOF, LOF, and LOS, and alarm outputs are generated.

The S3045 is divided into a transmitter section and a receiver section. The sequence of operation is as follows:

Transmitter Operations

1. 32-bit LVTTL parallel input from four 8-bit STS-12/ STM-4 data streams (PIN A, B, C, D) with parity (PARIN A, B, C, D).
2. Four Byte interleave conversion Mux.
3. Section-trace insertion (J0/Z0).
4. M1 calculation (addition of four STS-12/STM-4 M1 values) and insertion into the number one STS-12/STM-4 location.
5. M1 insertion of zero into STS-12/STM-4 number two, three, and four locations.
6. Four B2 parity byte calculations and insertions for STS-1 frames after M1 insertions.
7. Frame synchronous scrambling.
8. B1 calculation and insertion.
9. STS-48/STM-16 compatible 8-bit wide 311 MHz LVDS output (311DATOUT).

Receiver Operations

1. STS-48/STM-16 compatible 8-bit wide 311 MHz LVDS input (311DATIN).
2. OOF, LOF, and LOS states are monitored and alarms are generated.
3. B1 extraction and calculation of the STS-48/STM-16 frame.
4. B1 calculation of the number one STS-12/STM-4 frame.
5. Frame synchronous descrambling.
6. B1 compare and error indication (B1ERR) generation for the STS-48/STM-16 frame.
7. Insert the number one STS-12/STM-4 B1 parity byte into the number one STS-12/STM-4 frame and insert errors if any found in the STS-48/STM-16 B1 parity byte.
8. 32-bit (4 x 8 bit) parallel output of four STS-12/STM-4 data streams (POUT A, B, C, D) with parity output (PAROUT A, B, C, D).

Suggested Interface Devices

AMCC	S3040/S3047	Clock Recovery Device
AMCC	S3041	OC-48 Mux
AMCC	S3042	OC-48 Demux
PMC	PM5312	STTX Device
PMC	PM5355	SUNI Device

S3045 Acronym List

BER	–	Bit Error rate	**OTX**	–	Optical Transmitter
CDR	–	Clock and Data Recovery	**SDH**	–	Synchronous Digital Heirarchy
LOF	–	Loss Of Frame	**SEF**	–	Severely Errored Frame
LOS	–	Loss Of Signal	**SONET**	–	Synchronous Optical Network
OOF	–	Out Of Frame	**STM**	–	Synchronous Transport Module
ORX	–	Optical Receiver\	**STS**	–	Synchronous Transport Signal

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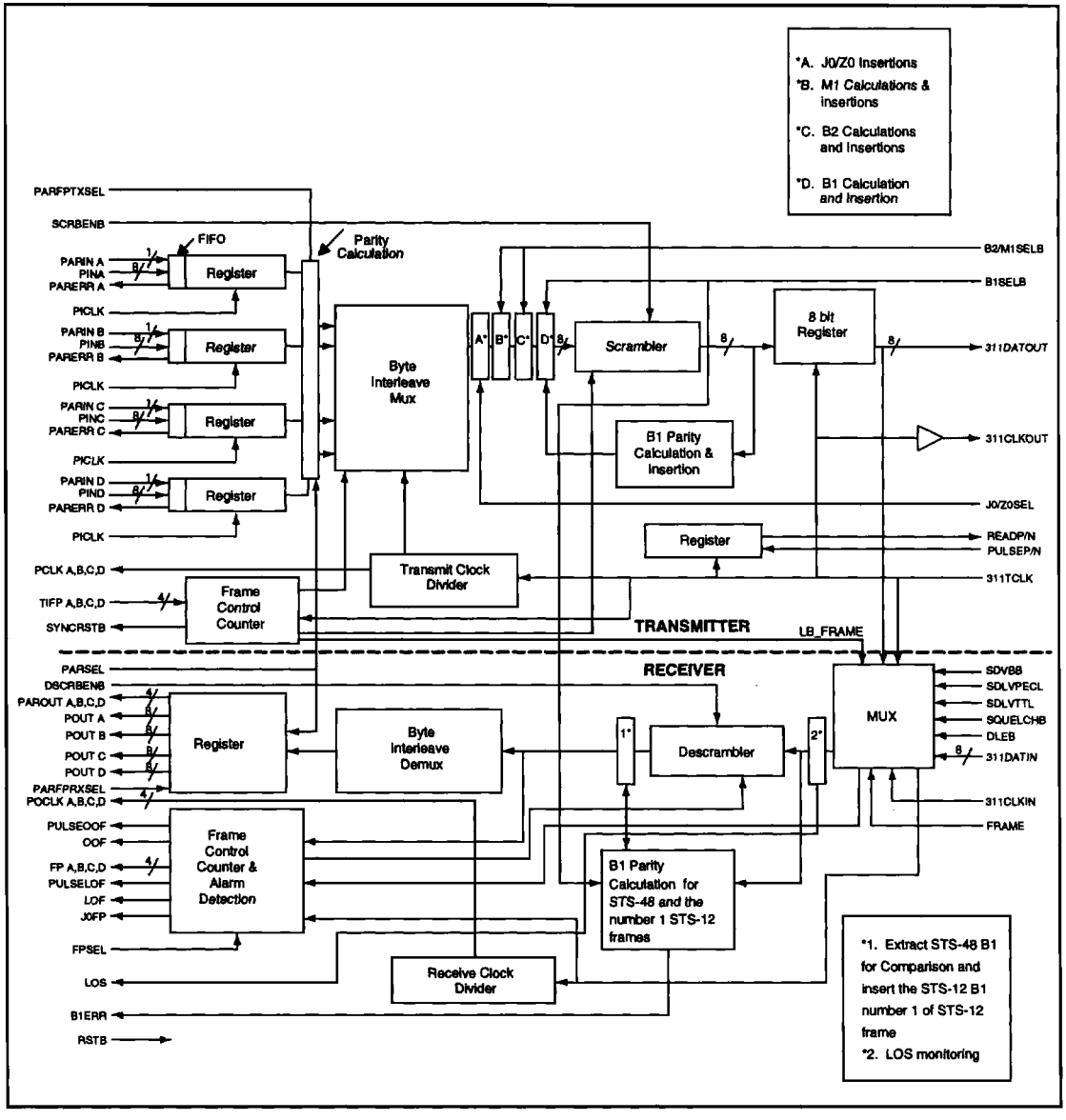
Figure 2. Functional Block Diagram



ARCHITECTURE/FUNCTIONAL DESIGN

Transmit Operation

The S3045 transmit section performs the byte interleaving stage in the processing of a transmit SONET/SDH STS-48/STM-16 byte wide data stream. It converts four byte wide STS-12/STM-4 data streams into a single byte serial STS-48/STM-16 data stream. The byte interleaved parity (B1) is calculated over the entire STS-48/STM-16 frame and inserted into the appropriate B1 location. In each STS-48/STM-16 frame there is one B1 byte located in the first STS-1 frame. The M1 byte is calculated (addition of four STS-12/STM-4 M1 bytes) and inserted into the number one STS-12/STM-4 M1 position. Zero is inserted into the number two, three, and four STS-12/STM-4 M1 positions. The section-trace bytes (J0/Z0) can be optionally inserted by setting the J0/Z0SEL high. The SONET/SDH scrambler can be enabled or disabled by the SCRBENB input.

STS-48/STM-16 Byte Interleave Multiplexing

The byte interleave mux shown in Figure 2 takes in the four byte wide STS-12/STM-4 data streams four bytes at a time and outputs byte wide STS-48/STM-16 data stream. The byte interleave mux inputs are registered on the STS-12/STM-4 interface. The mux first takes four bytes from the A input, followed by four from B, four from C, and four from D. The pattern is repeated as data on the A, B, C, and D inputs are registered and passed into a four word deep pipeline register. Each of the four data words are then latched into holding registers. A counter at the STS-48/STM-16 byte rate (311 MHz) controls a mux that loads data into a register at the STS-48/STM-16 byte rate and is then transmitted. STS-48/STM-16 byte interleaving must be done four bytes at a time, where as STS-3/STM-1 and STS-12/STM-4 is accomplished one byte at a time.

Scrambler

The scrambler can be utilized in order to guarantee a suitable bit pattern, which prevents a long sequence of 1's or 0's. The frame synchronous scrambler can be optionally used to scramble the STS-48/STM-16 data stream. The SONET scrambling generator polynomial of $1 + x^6 + x^7$ with a sequence length of 127 is used. The scrambler will be reset to "1111111" on the most significant bit of the byte following the last byte of the first row (last C1 byte) of the STS-12/STM-4 section overhead. This bit and all subsequent bits to be scrambled will be added modulo 2 to the output from the X^7 position of the scrambler (A1, A2, or C1 bytes are not scrambled). The scrambler will run continuously throughout the complete STS-48/STM-16 frame. A set of signals from the frame control counter block controls when the scrambler is on, off, or reset.

Frame Synchronization

The four STS-12/STM-4 input data streams from the four controllers must be frame aligned before this data is fed into the S3045 since the S3045 does not have any data buffering. The four controllers each output an active high framing position signal that is input into the TIFP inputs of the S3045 that marks the frame alignment on the output bus. This signal goes high for a single 77.76 MHz clock period during the first synchronous payload envelope byte immediately following the C1 bytes. The TIFP A, B, C, D inputs associated with each of the four STS-12/STM-4 data streams must be high at the same time so as to indicate frame alignment of all four data streams. These frame pulses will indicate frame alignment with the first payload byte of the STS-12/STM-4 frames. When frame alignment occurs, valid data will start to be output by the next valid frame. Valid B1 and B2 parity bytes will be output on the following frame. Otherwise random data will be clocked out of the 311DATOUT[7:0] output. In the event that all four pulses are not high at the same time (frames are not exactly aligned), a reset sequence will be generated by the S3045 to re-synchronize the four data streams.

In order to guarantee the synchronization of the four controllers, a reset sequence will be applied by the S3045. This reset will align the four STS-12/STM-4 inputs for multiplexing. Note that parity errors may be erroneously generated during this reset sequence. Figure 3 depicts the following synchronization sequence.

1. The SYNCRSTB will be asserted low to reset the four controllers upon a misalignment of the four TIFP pulses and will be held low for 16 PCLK A, B, C, D clock cycles (77.76 MHz).
2. The transmitter data clock (PCLK A, B, C, D) will stop for 16 clock cycles while the SYNCRSTB is asserted low.

3. The SYNCRSTB will be removed (de-asserted high) from the four controllers for 16 PCLK A, B, C, D clock cycles.
4. The transmit data clock (PCLK A, B, C, D) will continue to be stopped for 16 clock cycles after reset is de-asserted and then start clocking.
5. STS-12/STM-4 data out of the four controllers will start to flow into the S3045. The S3045 will search for a high pulse on the TIFP input pulses on all four channels. If the four controllers are not frame aligned in 250us this sequence will restart.

Frame Control Counter

The frame counter receives the TIFP signals indicating the frame boundaries and counts 38,880 bytes (9 rows x 90 columns x 48 STS-1) to ensure that the transmitter is receiving synchronous TIFP pulses. The frame counter keeps track of the overhead bytes so that proper location and insertion of bytes is accomplished.

The frame control block outputs a frame synchronous reset signal (SYNCRSTB) that frame aligns the STS-12/STM-4 network interface processors. The Transmit Input Frame Pulse (TIFP) signal indicates to the frame counter the frame position of the input data channel. If the transmitter does not get four simultaneous TIFP signals after 250us the SYNCRSTB pin is asserted low. The frame counter controls the output mux on the scrambler to allow scrambling, parity byte (B1) generation and insertion, M1 calculations and insertions, Z0 calculations insertions, and parity byte (B2) generations and insertions.

Clock Generation

The clock generation circuitry generates the 77.76 MHz PCLK A, B, C, D clock required for the byte wide STS-12/STM-4 interface from the 311 MHz clock (311TCLK) required for the byte wide STS-48/STM-16 interface.

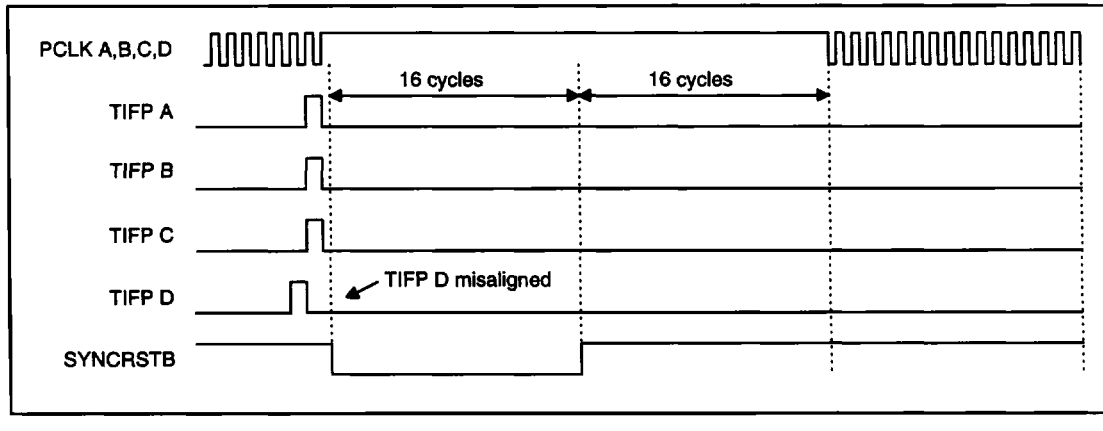
Bit Interleaved Parity - N

Bit Interleaved Parity-N (BIP-N) is a method of error monitoring. Even parity is used for the BIP-8 calculation. The transmitting equipment generates an N-bit code over a specified portion of the signal in such a manner that the first bit of the code provides even parity over the first bit of all N-bit sequences on the covered portion of the signal, the second bit provides even parity over the second bit of all N-bit sequences within the specified portion, etc. Even parity is generated by setting the BIP-N bits so that there are an even number of ones in each of all N-bit sequences including the BIP-N.

B1 Parity Calculation

This byte is allocated for regeneration section error monitoring. This byte will be calculated using even parity. Even parity is generated by setting the bit interleaved parity bits so that there is an even number of ones in each monitored partition of the signal. The interleaved even parity byte B1 is calculated over the entire scrambled STS-48/STM-16 frame and inserted into the B1 location of the next frame before going through the scrambling process. The computed bit interleaved parity is only placed in the B1 byte of the first STS-1 signal of the STS-48/STM-16 frame before scrambling (one B1 byte is valid in a

Figure 3. S3045 Synchronous Reset Functional Timing Diagram



single STS-48/STM-16 frame). The B1 parity byte is calculated after the M1 bytes are inserted, the section-trace J0/Z0 bytes are inserted, and the B2 parity bytes are inserted.

B2 Parity Calculation

The B2 byte is allocated in each STS-1 frame for a line error monitoring function. The interleave even parity byte B2 is calculated and inserted only over the four STS-1 frames that the four M1 bytes were inserted (the B2 byte will not be calculated for all 48 STS-1's). These four B2 bytes are calculated over the STS-1 frames of the previous STS-48/STM-16 frame except for the first three rows of the section overhead (computed over all bits of the line overhead and capacity envelope of the previous STS-1 frame before scrambling) and is inserted into the appropriate B2 locations (locations of the B2 bytes are found by control from the frame counter block) of the current frame before scrambling. These bytes will be inserted within a STS-48/STM-16 signal (48 B2 bytes are contained in a single STS-48/STM-16 frame). These parity bytes are calculated and inserted after the M1 bytes are inserted into the STS-48/STM-16 and before the B1 is calculated and inserted.

M1 Byte (B2 Parity Error Count)

The STS-48/STM-16 M1 byte is calculated by extracting each of the four M1 bytes of the STS-12/STM-4 frames and adding them together and inserting this new M1 byte into the STS-48/STM-16 M1 byte. For STS-48/STM-16 rate the M1 count will truncate at 255 (never report more than 255 errors). The STS-48/STM-16 M1 byte will only be transmitted over the number one STS-12/STM-4 data stream. The other 3 STS-12/STM-4 M1 bytes will be inserted with the value of zero.

Section-trace Insertion (J0/Z0) Bytes

The section-trace bytes (J0/Z0) can optionally be filled by setting J0/Z0SEL as indicated below in Table 1.

Table 1. Section-Trace Insertion (J0/Z0) Bytes

J0/Z0SEL	Description
0	Transparent Operation - J0/Z0 bytes are passed through with no modification.
1	Byte 1 of 48 (J0 byte) is passed through with no modification (transparent) and bytes 2 through 48 (Z0 bytes) are filled with the values of 02hex to 30hex (48 decimal) respectively.

RECEIVER OPERATION

The S3045 byte interleave receive section converts the byte wide STS-48/STM-16 LVDS data stream into four byte wide STS-12/STM-4 LVTTL data streams with parity. The B1 parity byte is calculated over the STS-48/STM-16 frame and over the number one STS-12/STM-4 frame. The STS-48/STM-16 B1 parity byte is compared to the one received, if an error exists then B1ERR will be asserted and the STS-12/STM-4 parity B1 will be inserted with the same number of bit errors found in the STS-48/STM-16 B1 parity byte. Also, if no errors exist then the calculated STS-12/STM-4 B1 will be inserted into the number one STS-12/STM-4 frame. A frame synchronous descrambler can be optionally disabled by the DSCRBENB input. The input data stream is monitored for Loss of Signal (LOS), Loss of Frame (LOF), and Out of Frame (OOF) and alarms are generated for each one.

Descrambling

The byte wide STS-48/STM-16 data stream is optionally descrambled using the SONET frame synchronous descrambler with a generator polynomial of $1 + x^6 + x^7$ with a sequence length of 127. The descrambler algorithm is identical to the scrambler algorithm. The descrambler will be reset to "1111111" on the most significant bit of the byte following the last byte of the first row of the STS-12/STM-4 section overhead. This bit and all subsequent bits to be descrambled will be added modulo 2 to the output from the X^7 position of the descrambler (A1, A2, or C1 bytes are not descrambled). The descrambler will run continuously throughout the complete STS-48/STM-16 frame. A signal from the frame counter block controls when the descrambler is on, off, or reset.

Receive Frame Counter

The frame counter receives the FRAME signal indicating the frame boundaries and counts 38,880 bytes (9 rows x 90 columns x 48 STS-1) to ensure that the receiver is receiving synchronous FRAME pulses. The frame counter keeps track of the overhead bytes so that proper location and insertion of bytes is accomplished. In diagnostic loopback mode, a loopback frame (LB_FRAME) signal is generated internally and the FRAME input is disabled.

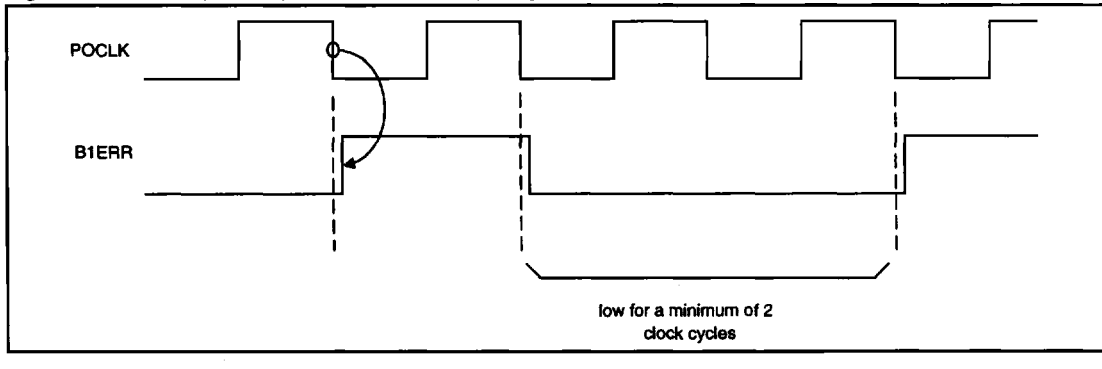
Clock Generation

The clock generation circuitry generates the 77.76 MHz POCLK clock required for the byte wide STS-12/STM-4 interface from the 311 MHz clock (311CLKIN) required for the byte wide STS-48/STM-16 interface.

B1 Parity Calculation and Compare

The B1 byte is allocated for regeneration section error monitoring. This byte will be calculated using even parity. The section bit interleaved parity (BIP-8) error detection code B1 will be calculated for every STS-48/STM-16 frame and for the number one STS-12/STM-4 frame before descrambling. The B1 value is compared to the extracted value of the STS-48/STM-16 B1 parity byte after descrambling in the following frame. B1 errors will be shown at the B1ERR output. The calculated STS-12/STM-4 B1 parity byte will be inserted after descrambling into the number one STS-12/STM-4 frame if there are no errors found on the STS-48/STM-16 B1 parity byte. If there are errors found with the STS-48/STM-16 B1 parity byte, the number of bit errors (1 to 8) will be passed onto the STS-12/STM-4 B1 parity byte for insertion into the number one STS-12/STM-4 frame. The number one STS-12/STM-4 frame is output on the POUT[7:0]A data bus. The following timing diagram depicts the B1ERR timing.

Figure 4. B1 Error (B1ERR) Functional Timing Diagram



FRAMER (In-frame, going out-of-frame)

The frame acquisition algorithm determines whether the receiver is in-frame or out-of-frame. In-frame is defined as the state where the frame boundaries are known. Out-of-Frame (OOF) is defined as the state where the frame boundaries of the incoming signal are unknown. OOF is also referred to as the Severely Errored Frame (SEF) in the SONET standards. The frame pulse (FRAME) input of the S3045 indicates if the frame boundaries are known (in-frame) or unknown (out-of frame).

An Out-of-Frame (OOF) also known as an SEF condition on an STS-48/STM-16 signal will be declared when a minimum of four consecutive errored framing patterns have been received. The maximum SEF detection time will be 625 us for a random signal. The framing algorithm used to check the alignment is such that 10^{-3} BER does not cause an SEF more than once every 6 minutes. This algorithm examines the 48th A1 (F6h) byte and the first four bits of the first A2 (28h) byte for a total of 12 bits to guarantee this requirement.

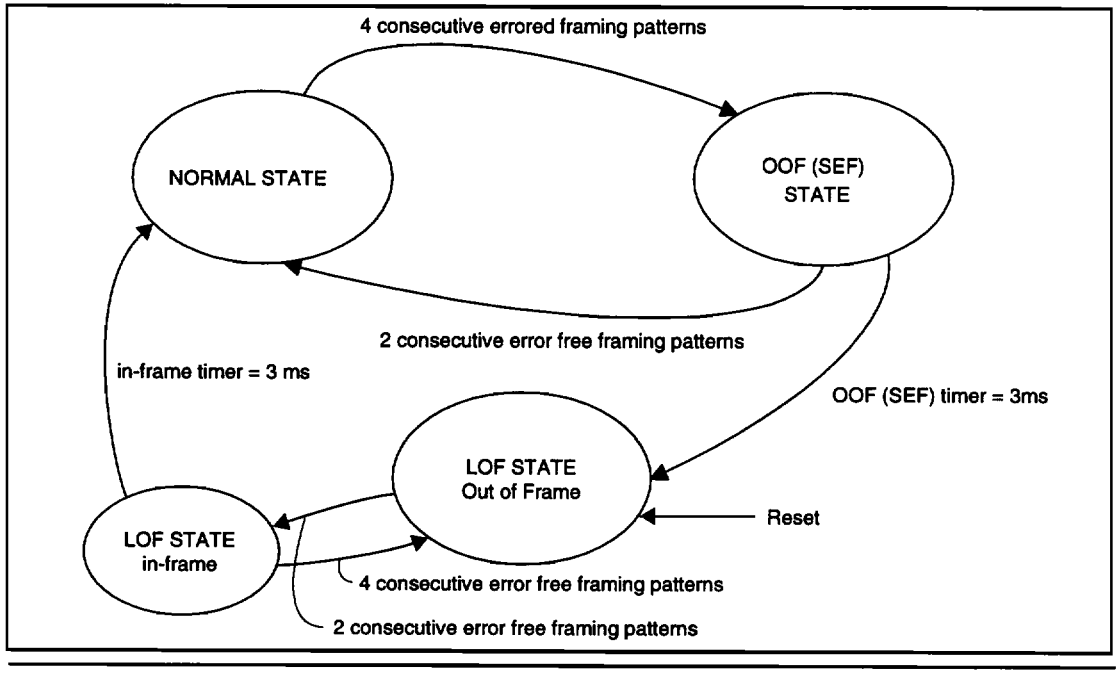
When in an SEF condition the S3045 will assume the frame has been recovered and declare an in-frame condition on detecting two successive error-free framing patterns. This implementation of the frame recovery circuit achieves realignment following a declared SEF within 250-us. Failure to obtain a frame within 3 ms (SEF persists for 3 ms) results in a Loss of Frame (LOF).

The LOF state is implemented by using a 3 ms integration timer to deal with intermittent SEF's when monitoring for LOF. The 3 ms integration timer consists of an SEF timer and an in-frame timer that operates as follows:

1. The in-frame timer is activated (accumulates) when in-frame is present. It stops accumulating and is reset to zero when SEF is present.
2. The SEF timer is activated (accumulates) when SEF is present. It stops accumulating when the signal goes-in-frame. It is reset to zero when the signal remains in-frame continuously for 3 ms (i.e., the in-frame-timer reaches 3 ms).

The LOF state will be entered if the accumulated SEF timer reaches the 3 ms threshold. Once in the LOF state, the LOF state will be exited when the in-frame timer reaches 3 ms. Once in the LOF state, the S3045 will exit the LOF state within 3 ms of a continuous in-frame signal in the incoming signal. Figure 5 is a state diagram of the OOF (SEF) and LOF state machine implementation.

Figure 5. OOF, LOF State Machine



Loss of Signal (LOS)

The Loss of Signal (LOS) block monitors the scrambled NRZ data of the complete STS-48/STM-16 data stream for all zero's. When a minimum of 27 µsec of all zero's are detected, a loss of signal (LOS) is declared (high signal). LOS is deactivated (low signal) when two valid frames are detected and no LOS condition is detected in between. LOS is updated on the falling edge of POCLKA,B,C,D.

J0 Frame Pulse

The J0 Frame Pulse output will be active high when the J0 byte is presented on the POUT[7:0]A data bus. Figure 6 depicts the functional timing of this signal.

FP Frame Pulse

The FP output indicates frame boundaries in the incoming data stream. FP pulses high for one POCLK cycle when the third A2 byte of the framing sequence is valid on the POUT[7:0]A data bus. Figure 7 depicts the functional timing of this signal.

STS-48/STM-16 Byte Interleave Demux

The byte interleave demux shown in Figure 2 converts the byte wide STS-48/STM-16 data stream into four byte wide STS-12/STM-4 data streams. The data is byte deinterleaved using four bytes at a time. The data is output with a 77.76 MHz clock.

OTHER OPERATING MODES

Diagnostic Loopback

When the Diagnostic Loopback Enable (DLEB) input is low, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes. In loopback mode the STS-48/STM-16 transmitter outputs (311DATOUT[7:0], 311CLKOUT and an internally generated Frame pulse on the third A2 byte (that is not accessible to the outside of the chip)) are internally connected to the STS-48/STM-16 receiver inputs (311DATIN[7:0], 311CLKIN, and FRAME). In loopback mode the STS-48/STM-16 transmitter outputs (311DATOUT[7:0] and 311CLKOUT) are still active.

"Squelched Clock" Operation

Some integrated optical receiver/clock recovery modules force their recovered serial receive clock output to the logic zero state (squelched clock) if the optical signal is removed or reduced below a fixed threshold. This condition is accompanied by the expected deassertion of the Signal Detect (SD) output.

The S3045 has been designed for operation with clock recovery devices that provide continuous serial clock for seamless down stream clocking in the event of optical signal loss. For operation with an optical transceiver that provides the "squelched clock" behavior as described above, the S3045 can be operated in the "squelched clock mode" using the SQUELCHB input.

In squelch mode, the 311CLKIN is used for all receiver timing when the SDLVPECL or SDLVTTL inputs are in the active state. (SDLVPECL and SDLVTTL are in opposite logical states.) When the SDLVPECL or SDLVTTL inputs are placed in the inactive state (usually by the de-assertion of the Signal Detect [SDLVPECL and SDLVTTL are in the same logical state] from the optical transceiver/clock recovery unit) the transmitter serial clock (311TCLK) will be used to maintain timing in the receiver section. This will allow the POCLK A, B, C, D to continue to run and the parallel outputs to flush out the last received characters and assume the all zero state imposed at the serial data input.

It is important to note that in squelch mode there may be up to 3.2 nsec shortening or lengthening of the POCLK A, B, C, D cycle, resulting in an apparent phase shift in the POCLK at the de-assertion of the SD condition. Another similar phase shift will occur when the SD condition is reasserted. Figure 8 depicts this operation.

In the normal operating mode with SQUELCHB input inactive (high), there will be no phase discontinuities at the POCLK A, B, C, D output during signal loss or reacquisition (assuming operation with continuous clock from the CRU device such as the AMCC S3040 or S3047). Figure 9 depicts this operation.

Byte wide Parity Calculation

Odd parity or even parity can be calculated using the PIN A, B, C, D and POUT A, B, C, D data busses by setting the PARSEL line high for even parity or low for odd parity. Even parity is generated by setting the parity bit so that there are an even number of ones throughout the 9 bits. Odd parity is generated by setting the parity bit so that there is an odd number of ones throughout the 9 bits.

Reset Operation

The RESET (RST) input forces all the internal logic of the S3045 to its deasserted state. All of the sequential logic inside the S3045 will remain static for as long as reset is asserted. The RESETB input is implemented using a schmitt type receiver. The RESETB input is asynchronous to the input clock. RESETB should be asserted for at least one PCLK cycle. RESETB should be asserted after power up for proper operation. During reset PCLK A, B, C, D and POCLK A, B, C, D will stop, and SYNCRSTB will remain high.

Figure 6. J0 Frame Pulse Functional Timing Diagram

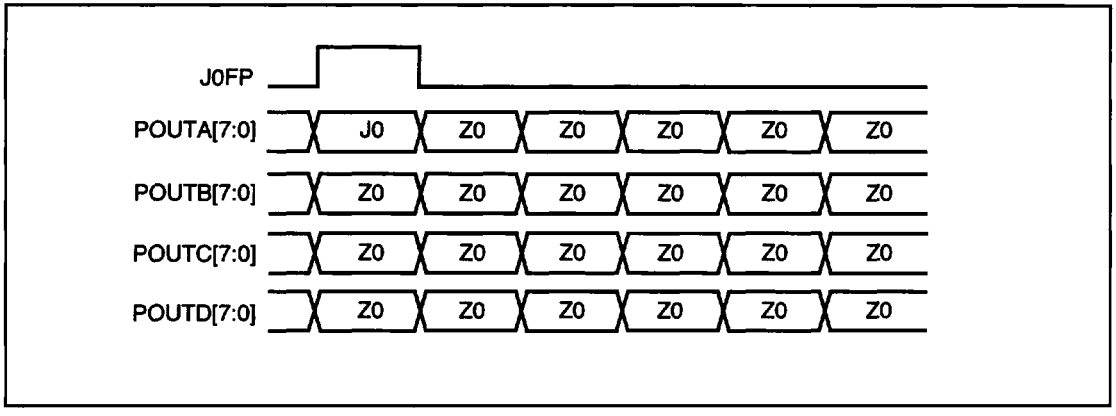


Figure 7. FP Frame Pulse Functional Timing Diagram

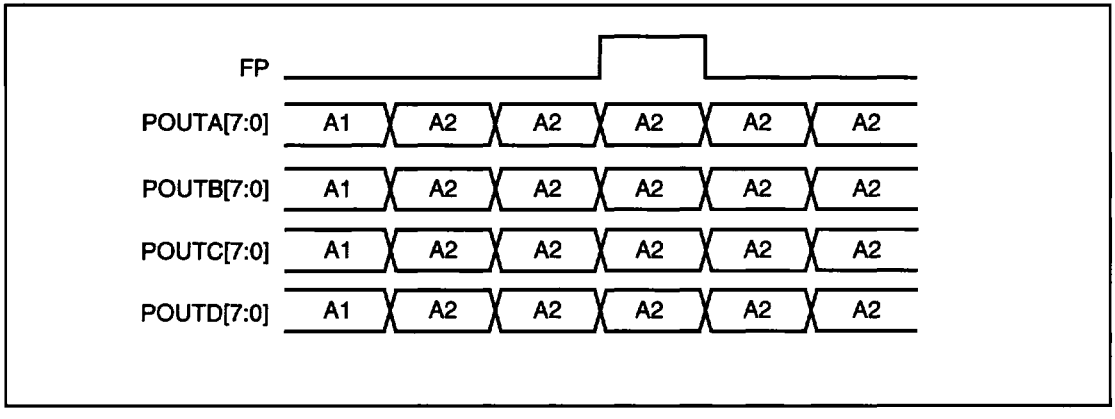


Figure 8. Functional Operation of SQUELCH Mode

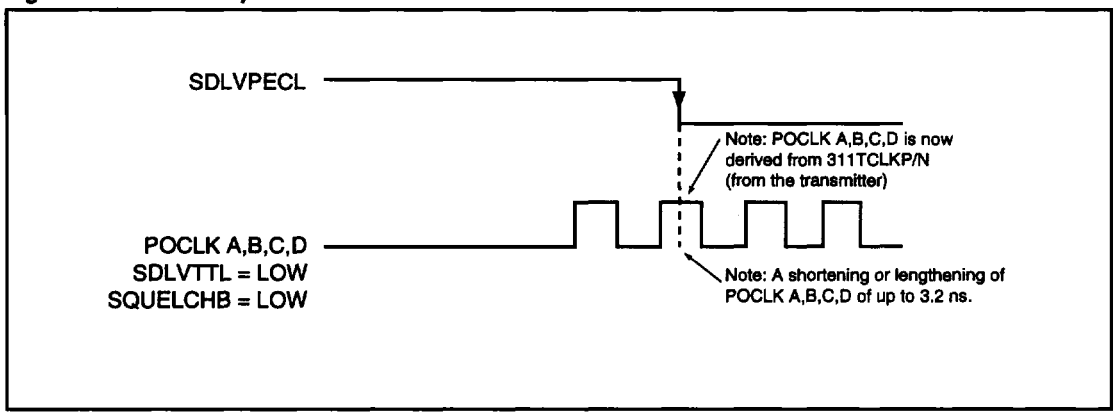


Figure 9. Functional Operation of Non-SQUELCH Mode

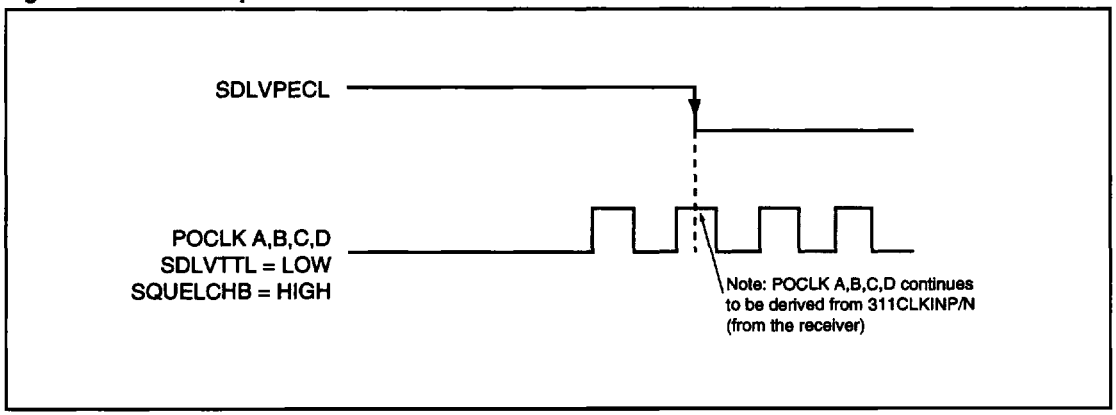


Table 2. Transmitter Input Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
PICLK	LVTTL	I	129	Parallel Input Clock. PICLK is a 77.76 MHz input clock which PIN[7:0] is aligned. PICLK is used to transfer the data on the PIN inputs into a holding register. The rising edge of PICLK samples PIN A, B, C, D[7:0].
PINA[7:0] PINB[7:0] PINC[7:0] PIND[7:0]	LVTTL	I	180–173, 156–149, 121–117, 115–113, 94–91, 89–86	Parallel Data Input. A 77.76 Mbytes/sec word, aligned to the PICLK parallel input clock. PIN[7] is the most significant bit (corresponding to bit 1 of each word, the first bit transmitted). PIN[0] is the least significant bit (corresponding to bit 8 of each word, the last bit transmitted). PIN[7:0] is sampled on the rising edge of PICLK.
SCRBENB	LVTTL	I	198	Scramble Enable. Active low. When active, the frame synchronous scrambler is enabled. When inactive, the scrambler is disabled. This signal is static and must not be changed in normal operation.
311TCLKN 311TCLKP	LVDS	I	30 31	311 MHz Transmit Clock. Used by the transmitter to generate the 77.76 MHz clocks and retime the STS-48/STM-16 byte wide data.
TIFPA TIFPB TIFPC TIFPD	LVTTL	I	172 148 112 85	Transmit Input Frame Pulse. Active high. When active, it indicates the frame position of the transmit data (PIN[7:0]). TIFP goes high for a single PCLK A, B, C, D (77.76 MHz) period during the first synchronous payload envelope byte after 12 C1 bytes. TIFP is clocked in on the rising edge of PICLK.
PARINA PARINB PARINC PARIND	LVTTL	I	181 146 111 84	Parity Input. Odd or even parity depending on the input of parity select (PARSEL) for the 8 bit PIN[7:0] A, B, C, D data bus. PARIN is clocked in on the rising edge of PICLK.
B2/M1SELB	LVTTL	I	200	B2/M1 Parity Byte and Parity Count Select. Active low. When inactive the B2/M1 byte calculations and insertions are disabled. When active, normal operation occurs (B2 and M1 calculations and insertions are enabled). This signal is static and must not be changed in normal operation.
J0/Z0SEL	LVTTL	I	205	Section-Trace Insertion Select. Select pin, select section-trace bytes J0/Z0 options. When low the J0/Z0 bytes are passed through with no modification. When high, byte 1 of 48 (J0 byte) is passed though with no modification (transparent) and bytes 2 through 48 (Z0 bytes) are filled with the values of 02hex to 30hex (48 decimal) respectively. (See Table 1.) This signal is static and must not be changed in normal operation.
PULSEP PULSEN	LVDS	I	52 51	PULSE Input. This input is used to generate the READP/N output by synchronizing the PULSEP/N input to the 311TCLK input clock through a register. (Required for operation with the AMCC S3041 OC-48 TX Mux).
PARFPTXSEL	LVTTL		208	Parity Frame Pulse Select. When low, parity is calculated over the data bus PIN[7:0] A, B, C, D. When high, parity is calculated over the PIN[7:0] A, B, C, D data bus and the Transmit Input Frame Pulse (TIFP A, B, C, D). This signal is static and must not be changed in normal operation.

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Table 3. Transmitter Output Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
PCLKA PCLKB PCLKC PCLKD	LVTTL	O	128 127 126 125	Parallel Clock. A 77.76 MHz clock generated by dividing the internal 311TCLK by four. It is normally used to coordinate byte wide transfers between the STS-12/STM-4 overhead processors and the S3045 device.
311DATOUT-P/N[7:0]	LVDS	O	48–41 39–32	311 Mbit Data. STS-48/STM-16 byte wide data path. A 311 Mbytes/sec word, aligned to the 311 MHz parallel output clock (311CLKOUT). 311DATOUT [7] is the most significant bit (corresponding to bit 1 of each word, the first bit transmitted). 311DATOUT[0] is the least significant bit (corresponding to bit 8 of each word, the last bit transmitted). 311DATAOUT [7:0] is transmitted on the falling edge of the 311CLKOUT.
311CLKOUTP 311CLKOUTN	LVDS	O	27 26	311 MHz Clock. 311 CLKOUT is a clock for the transmit STS-48/STM-16 byte wide data path. A 311 MHz output clock, which 311DATAOUT [7:0] is aligned.
SYNCRSTB	LVTTL	O	122	Synchronous Reset. Active low. When active, the Network Interface Processors are reset to synchronize the four STS-12/STM-4 incoming data streams. Figure 3 shows the S3045 synchronous reset timing diagram.
PARERRA PARERRB PARERRC PARERRD	LVTTL	O	182 145 110 83	Parity Error Output. Active high. Indicates to the controller that a parity error has been detected on the PIN[7:0] A, B, C, D data bus on a previous byte of data. When active, a parity error has been received. When inactive, PIN[7:0] A, B, C, D data has been received without parity errors. PARERR output can be delayed by one to five PCLK cycles due to the internal data FIFO. See Figure 10. Note that during a sync reset condition, parity errors may erroneously be generated.
READP READN	LVDS	O	54 53	Read Output. This output is the result of synchronizing the PULSEP/N input to the 311TCLK input clock through a register. (Required for operation with the AMCC S3041.)

Table 4. Receiver Input Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
311DATINN/P [7:0]	LVDS	I	21–14, 11–4	311 Mbit Data Inputs. Parallel STS-48/STM-16 data bus, a 311 Mbyte/sec word aligned to the parallel input [311CLKIN]. 311DATAIN [7] is the most significant bit (corresponding to bit 1 of each word, the first bit received). 311DATAIN [0] is the least significant bit (corresponding to bit 8 of each word, the last bit received). 311DATAIN [7:0] is latched on the rising edge of 311CLKIN.
311CLKINN 311CLKINP	LVDS	I	25 24	311 MHz Clock. 311CLKIN is a 311 MHz byte rate input clock that is aligned to 311DATAIN [7:0] byte serial input data. 311DATIN [7:0] and FRAME are clocked in on the rising edge of the 311CLKIN.
FRAMEN FRAMEP	LVDS	I	2 1	Frame. Active high. When active, it indicates that the third A2 byte of the framing sequence is valid on the 311DATIN<7:0> pins. Therefore it indicates frame boundaries in the incoming data stream (311DATIN[7:0]).
DSCRBENB	LVTTL	I	199	Descrambler Enable. Active low. When active, the frame synchronous descrambler is enabled. When inactive the frame synchronous descrambler is disabled. This signal is static and must not be changed in normal operation.
SQUELCHB	LVTTL	I	201	Squelch Clock Mode. Active low. Set inactive when a clock recovery device used provides a continuous clock during signal loss or re-acquisition. Set active when the clock recovery device used does not provide a continuous clock during signal loss or signal acquisition. When active and SDLVPECL/SDLVTTL is inactive (SDLVPECL and SDLVTTL are in the same logical states) the transmitter serial clock (311TCLK) will be used to maintain timing in the receiving section. This signal is static and must not be changed in normal operation.
SDLVTTL	LVTTL	I	192	Signal Detect. Active High when SDLVPECL is tied to logic 0. Active Low when SDLVPECL is held at logic 1. A single-ended LVTTL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDLVTTL is inactive, the data on the 311DATIN[7:0] pins will be internally forced to a constant zero with the descrambler bypassed. When SDLVTTL is active, data on the 311DATIN[7:0] pins will be processed normally.
SDLVPECL	LVPECL	I	191	Signal Detect. Active High when SDLVTTL is held at logic 0. Active Low when SDLVTTL is held at logic 1. A single-ended LVPECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDLVPECL is inactive, the data on the Serial Data in 311DATIN[7:0] pins will be internally forced to a constant zero with the descrambler bypassed. When SDLVPECL is active, data on the 311DATIN[7:0] pins will be processed normally. When SDLVTTL is to be connected to the optical receiver module instead of SDLVPECL, then SDLVPECL should be tied High to implement an active low Signal Detect.

Table 4. Receiver Input Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
SDVBB		I	190	Signal Detect. Bias pin for the SDLVPECL input. Biased internally to VDD -1.3V.
FPSEL	LVTTL	I	204	Frame Pulse Select. When low the FRAME input is used to generate the FP A, B, C, D pulse when the third A2 byte is output. When high, the FP A, B, C, D output is internally generated using the A1A2 frame boundary. The FP A, B, C, D is asserted high when the third A2 (28h) byte is output. For normal operation set high. This signal is static and must not be changed in normal operation.
PARFPRXSEL	LVTTL	I	207	Parity Frame Pulse Receive Select. When low, parity is calculated over the data POUT[7:0] A, B, C, D. When high, parity is calculated over the data POUT[7:0] A, B, C, D and the frame pulse (FP A, B, C, D) output. This signal is static and must not be changed in normal operation.

Table 5. Receiver Output Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
POUTA[7:0] POUTB[7:0] POUTC[7:0] POUTD[7:0]	LVTTL	O	168–161 140–133 106–99 79–72	Parallel Data Output. Parallel data bus, a 77.76 Mbyte/sec word, aligned to the parallel output clock (POCLK). POUT[7] is the most significant bit (corresponding to bit 1 of each word, the first bit received). POUT[0] is the least significant bit (corresponding to bit 8 of each word, the last bit received). POUT[7:0], LOS, LOF, PAROUT A, B, C, D, B1ERR, FP A, B, C, D and OOF are updated on the falling edge of POCLK.
POCLKA POCLKB POCLKC POCLKD	LVTTL	O	169 141 107 80	Parallel Output Clock. POCLKA, B, C, D are 77.76 MHz byte rate output clocks that are aligned to POUT[7:0]A, B, C, D byte serial output data. POUT[7:0] is updated on the falling edge of POCLK.
FPA FPB FPC FPD	LVTTL	O	157 130 95 69	Frame Pulse. Indicate frame boundaries in the incoming data stream. FP pulses high for one POCLK cycle when the third A2 byte of the framing sequence is valid on the POUTA[7:0] data. FP is updated on the falling edge of POCLK.
OOF	LVTTL	O	185	Out of Frame. The Out of Frame (OOF) signal is active when the S3045 has detected an out of frame condition. The OOF is inactive when the S3045 is in frame. An OOF declaration occurs when four consecutive errored framing patterns are received. OOF is used to enable upstream framing pattern detector to search for the framing pattern. Figure 13 depicts the functional timing of this signal.

Table 5. Receiver Output Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
PULSEOOF	LVTTL	O	186	Pulse Out of Frame. Active high. The Out of Frame (OOF) signal will pulse when the S3045 is out of frame and when the A1A2 boundary is not received. The PULSEOOF is inactive when the S3045 is in frame. An OOF declaration occurs when four consecutive errored framing patterns are received. OOF is used to enable upstream framing pattern detector to search for the framing pattern. Figure 13 depicts the functional timing of this signal.
LOF	LVTTL	O	187	Loss of Frame. Active high. When active, indicates that the Out-of-Frame (OOF) condition has persisted for a period of 3 ms. LOF is de-activated when an in-frame condition (as indicated by a low level on the OOF output) persists for a period of 3ms. Figure 14 depicts the functional timing of this signal.
PULSELOF	LVTTL	O	189	Pulse Loss of Frame. Active high. When active, indicates that the Out-of-Frame (OOF) condition has persisted for a period of 3 ms. LOF is de-activated when an in-frame condition (as indicated by a low level on the OOF output) persists for a period of 3ms. PULSELOF signal will pulse when the S3045 is Out-of-Frame (OOF is high) in LOF (high) and the A1A2 boundary is not received. Figure 14 depicts the functional timing of this signal.
J0FP	LVTTL	O	206	J0 Frame Pulse. Active high. Active when the J0 byte is presented on the POUTA[7:0] data bus.
B1ERR	LVTTL	O	183	B1 Parity Error. Active high. Indicates that a B1 bit error has been detected when high for a minimum of 12ns. B1ERR is updated on the falling edge of POCLK. For each frame B1ERR will pulse a maximum of 8 times. In between pulses (bit errors) the B1ERR will be low for a minimum of 24ns.
PAROUTA PAROUTB PAROUTC PAROUTD	LVTTL	O	158 144 96 68	Parity Output. Odd or even parity depending on the input of parity select (PARSEL) for the 8 bit POUT[7:0] A, B, C, D and FP A, B, C, D (optional) data bus. PAROUT A, B, C, D, (FP A, B, C, D optional) is updated on the falling edge of POCLK.
LOS	LVTTL	O	184	Loss of Signal. Active high. When active, LOS indicates that a consecutive zero pattern for a minimum of 27usec of all zeros is detected on the incoming scrambled STS-48/STM-16 signal before descrambling. LOS is deactivated when two valid framing words are detected and no LOS is detected in between. LOS is updated on the falling edge of POCLK.

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Table 6. Common Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
B1SELB	LVTTL	I	203	B1 Parity Byte Select. Active low. When active, B1 calculation and insertion is enabled. When inactive, the B1 calculation and insertion is disabled. This signal is static and must not be changed in normal operation.
PARSEL	LVTTL	I	197	Parity Select. When high selects even parity. When low selects odd parity. This signal is static and must not be changed in normal operation.
RSTB	LVTTL	I	193	Reset. Active low. Asyncronous reset input for the device. During reset PCLK A, B, C, D does not toggle and frame synchronization with SYNCRST will be activated.
DLEB	LVTTL	I	196	Diagnostic Loopback Enable. Active low. When DLEB is inactive, the S3045 uses the primary data 311DATIN[7:0] and clock 311CLKIN inputs. When active, the S3045 selects diagnostic loopback mode. In loopback mode the STS-48/STM-16 transmitter outputs (311DATOUT[7:0] and 311CLKOUT) are internally connected to the STS-48/STM-16 receiver inputs (311DATIN[7:0] and 311CLKIN). This signal is static and must not be changed in normal operation.
VDD			202, 194, 159, 143, 123, 116, 109, 97, 82, 66, 58, 56, 55, 50, 28, 22, 12	Power Pins. VDD pins must be tied to 3.3V.
VSS			195, 188, 170, 160, 147, 142, 132, 124, 108, 98, 90, 81, 71, 67, 63, 62, 61, 60, 59, 57, 49, 40, 29, 23, 13, 3	Ground Pins. VSS pins must be tied to ground.
VDD5			171, 131, 70	TTL I/O Power Pins. There are three power pins that may be connected to 3.3 volts or 5 volts. When these pins are connected to 3.3 volts, the TTL interface is a 3.3 volt LVTTL interface. When these pins are connected to 5 volts, the TTL inputs are 5 volt TTL tolerant. All three pins must be connected to the same voltage level.
TEST_EN[0:1]	LVTTL		64, 65	TEST Enable. For factory test. For normal operation tie low.

Figure 10. Parity Error (PARERR) Output Functional Timing Diagram

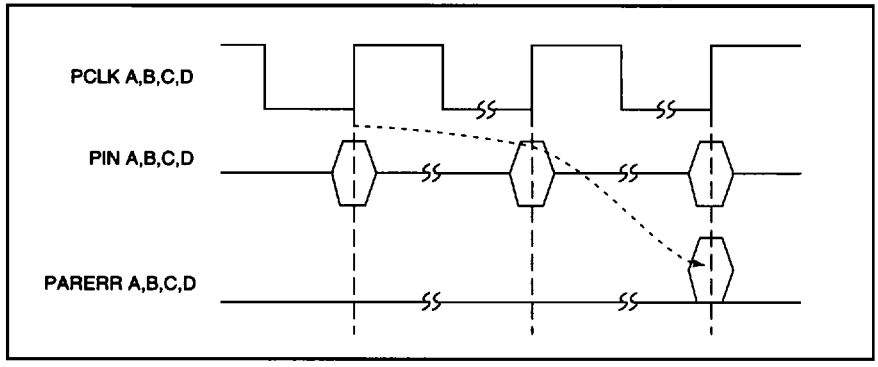

Figure 11. S3045 LVDS Inputs

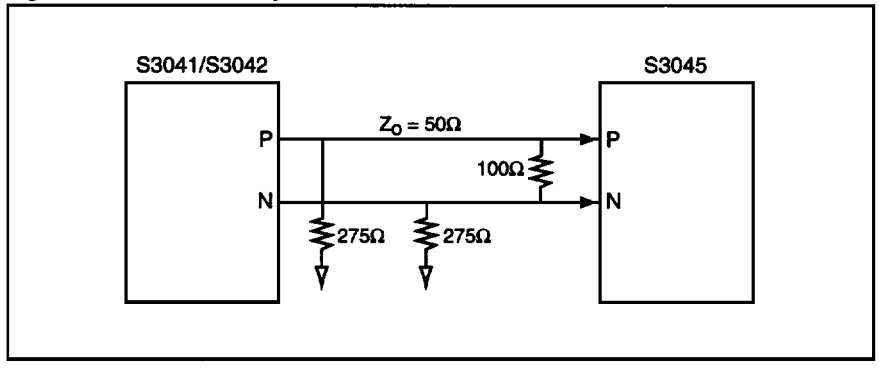

Figure 12. S3045 LVDS Outputs

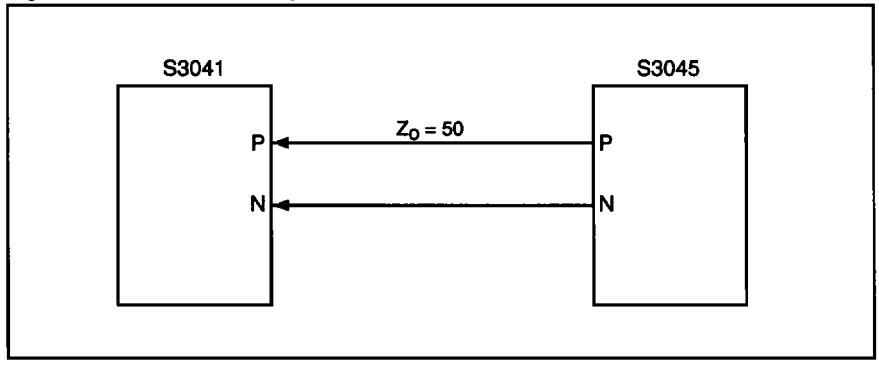

Figure 13. OOF and PULSEOOF Functional Timing Diagram

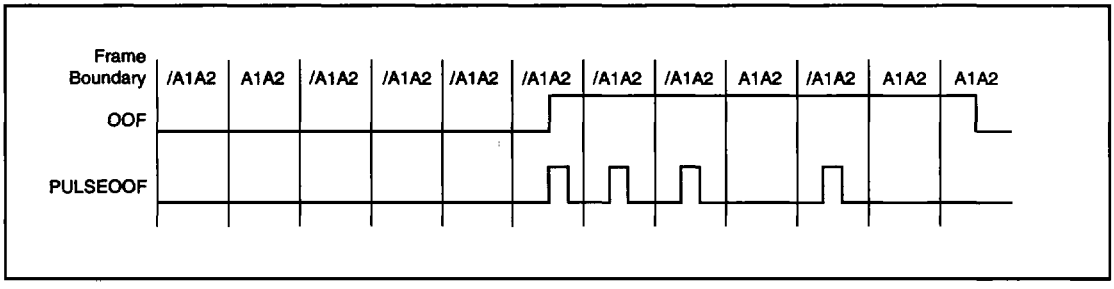

Figure 14. OOF, LOF, and PULSELOF Timing Diagram

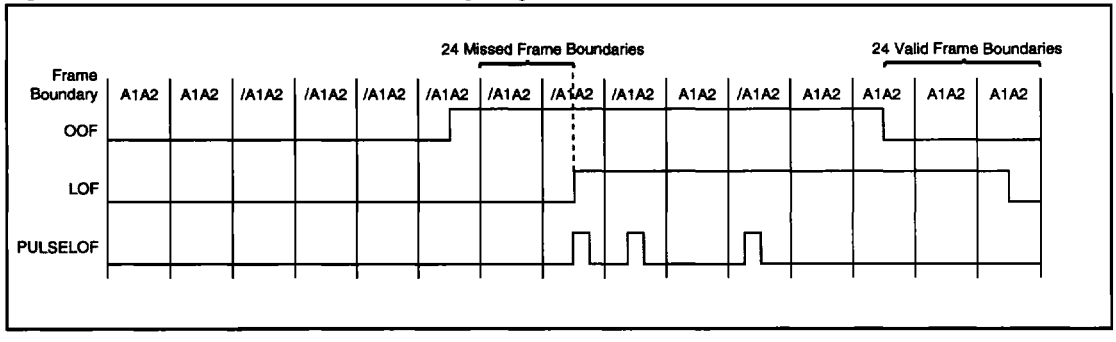

Figure 15. S3045 Pinout

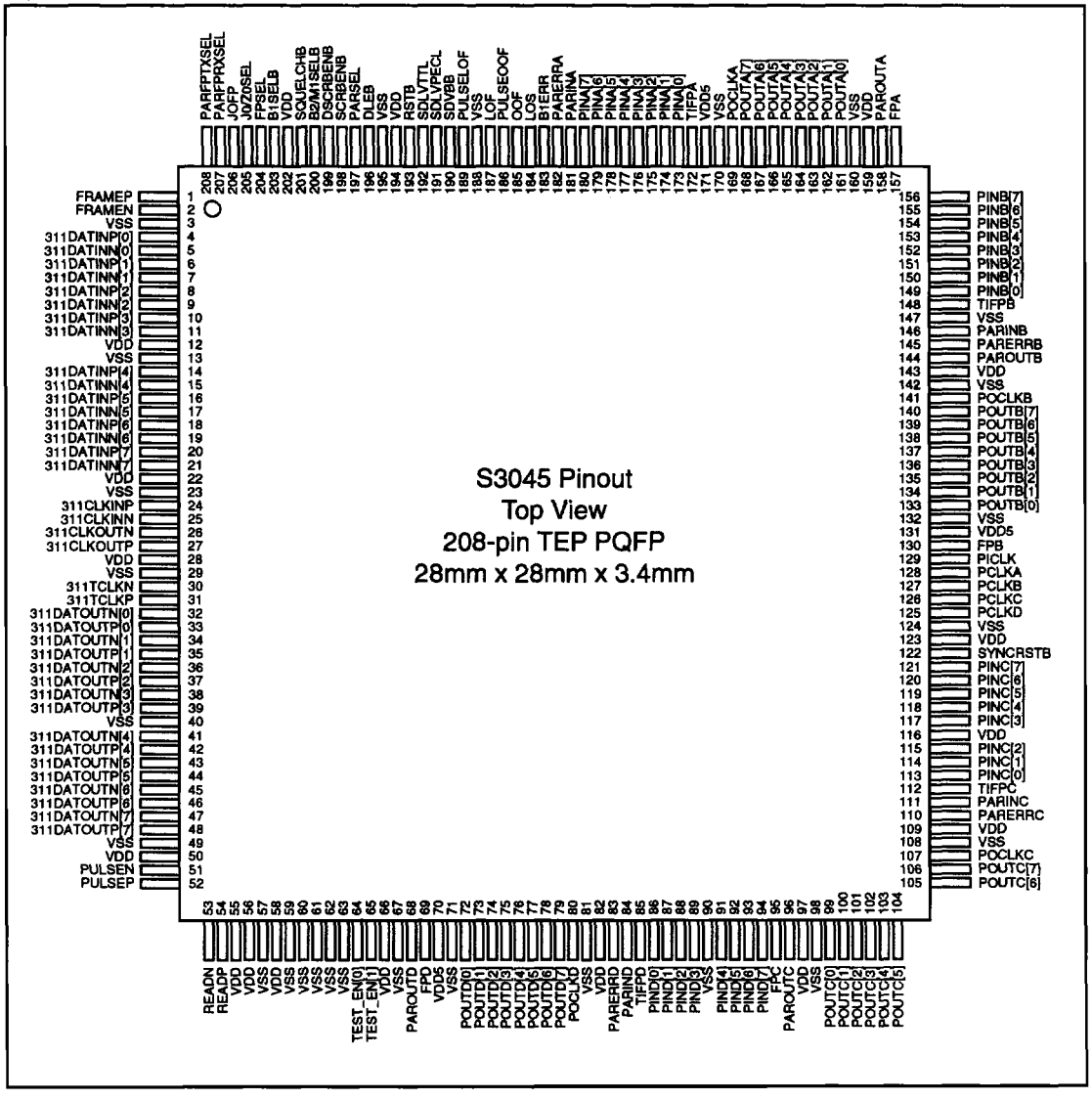

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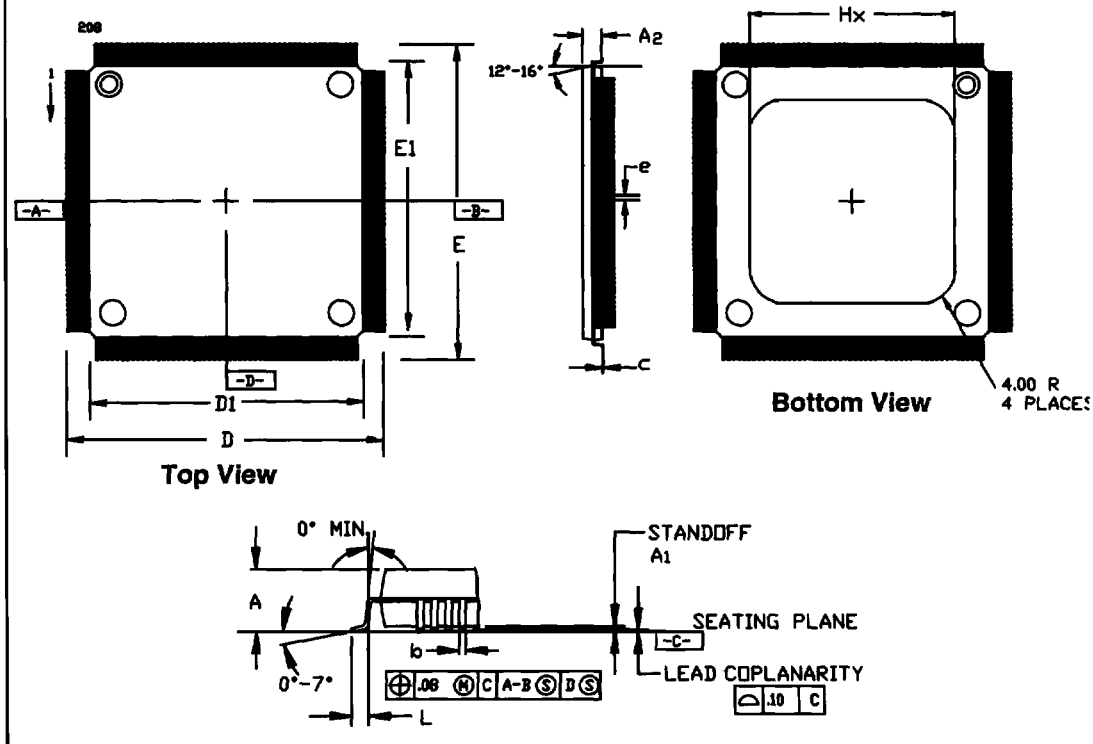
Figure 16. S3045 208 PQFP TEP (28 x 28 x 3.40mm) - Plastic Quad Flat Pack



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b	c	Hx
MIN		0.25	3.17	30.60 BSC.	28.00 BSC.	30.60 BSC.	28.00 BSC.	0.46	0.50 BSC.	0.17	0.13	21.00 REF.
NOM	3.70	0.33	3.37					0.56		0.22		
MAX	4.07		3.67					0.66		0.27	0.23	

Note: The S3045 package is equipped with an embedded conductive heatsink on the bottom (board side). Active circuitry and vias should not appear in the area immediately under the package.

Thermal Management

Device	Θja (Still Air)	Θjc
S3045	18 ° C/W	0.3 ° C/W

Table 7. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Case Temperature Under Bias	-55		125	°C
Junction Temperature Under Bias	-55		150	°C
Storage Temperature	-65		150	°C
Voltage on Vdd with respect to GND	-0.5		+5.0	V
Voltage on any LVPECL Input Pin	0		+5.0	V
Voltage on any LVTTL Input Pin	-0.5		VDD5 +0.5	V
LVTTL Output sink current			8	mA
LVTTL Output source current			8	mA
Static Discharge Voltage			2000	V

Table 8. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	0		+70	°C
Junction Temperature Under Bias			+125	°C
Voltage on Vdd with respect to GND	3.14	3.3	3.47	V
Voltage on any LVPECL Input Pin	VDD -2.00		VDD -0.4	V
Voltage on any LVTTL Input Pin	0		VDD5 +0.5V	V
Power Dissipation			2	W

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Table 9. LVPECL Input DC Characteristics

Parameters	Description	Min	Max	Units	Conditions
V_{IL}	Input LOW Voltage	V_{dd}-2.0	V_{dd}-1.6	V	
V_{IH}	Input HIGH Voltage	V_{dd}-1.0	V_{dd}-0.4	V	
I_{IH}	Single-ended input HIGH current	-20	20	µA	$V_{IN} = V_{dd}$ -0.4V
I_{IL}	Single-ended input LOW current	-20	20	µA	$V_{IN} = V_{dd}$ -2.0V
V_{OUT}	SDVBB pin	1.8	2.2	V	$I_{OUT} = 0$, $V_{dd} = 3.47V$

Table 10. LVTTL Input/Output DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	2.4			V	$V_{dd} = 3.14V$, $I_{OH} = -2.4mA$
V_{OL}	Output LOW Voltage			.5	V	$V_{dd} = 3.14V$, $I_{OL} = 2.4mA$
V_{IH}	Input HIGH Voltage	2.0		VDD5 +0.5	V	
V_{IL}	Input LOW Voltage	0		0.8	V	
I_I	Input HIGH Current			1	mA	$V_{IN} = V_{dd}5 = 5.5V$
I_{IH}	Input HIGH Current	-50	2	50	µA	$V_{IN} = 2.4V$
I_{IH}	Input HIGH Current with pulldowns TEST_EN0, TEST_EN1	10	25	50	µA	$V_{IN} = 2.4V$
I_{IL}	Input LOW Current	-500		0	µA	$V_{IN} = 0.5V$
I_{IL}	Input LOW Current with pulldowns TEST_EN0, TEST_EN1	1	10	50	µA	$V_{IN} = 0.5V$
I_{OS}	Output short circuit current	-95	-20	-5	mA	$V_{OUT} = 0.5V$
V_{IK}	Input Clamp Voltage	-1.2	-0.8	-0.2	V	$I_{IN} = -18mA$

Table 11. LVDS Input/Output Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
I_{IH}	Input High Current	-10		10	µA	V_{IN} = 2.4V
I_{IL}	Input Low Current	-10		10	µA	V_{IN} = 0.0V
V_{DIFF}	Input Voltage Differential	100		400	mV	V_{IN} Common Mode Range .9 to 1.9V
VIS	Input Offset Voltage	0.92	1.2	1.62	V	
Ro	Output Impedence Single ended	57		117	Ohm	
Delta Ro	Ro mismatch between differential outputs		1		%	
V_{OS}	Output Offset Voltage	1.1	1.30	1.40	V	100 Ohms across diff. pair
V_{OH}	Output High Voltage	1.2	1.45	1.55	V	100 Ohms across diff. pair
V_{OL}	Output Low Voltage	0.93	1.15	1.25	V	100 Ohms across diff. pair
V_{OUT} (diff)	Output Differential Voltage	250	300	400	mV	100 Ohms across diff. pair
V_{dim}	Input Differential Threshold	-100		+100	mV	

Figure 17. AC Transmitter Parallel Input Data Timing Diagram

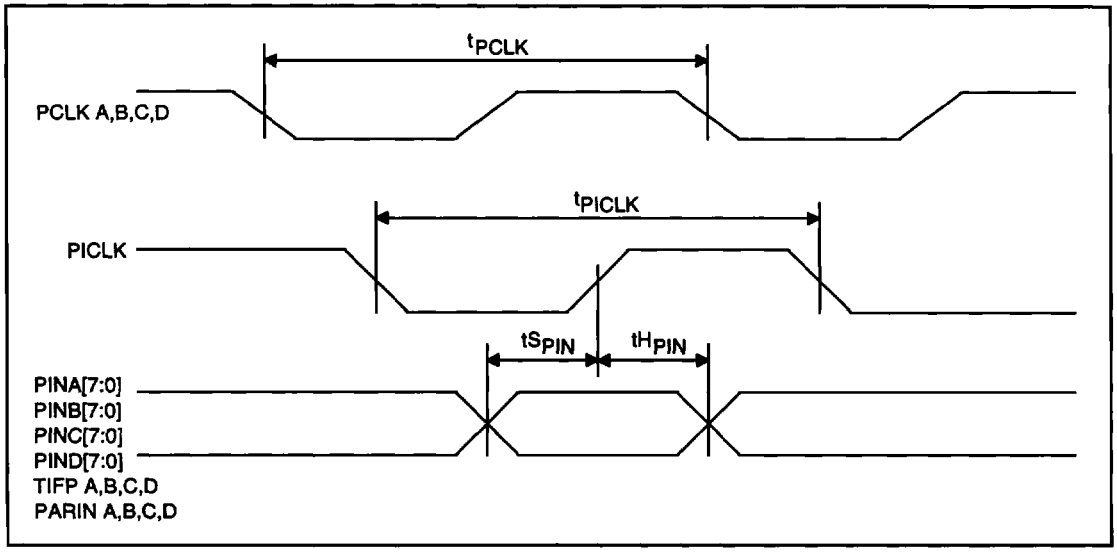


Table 12. AC Transmitter Parallel Data Input Timing Characteristics

Parameters	Characteristics	Min	Typ	Max	Units
t_{PCLK}	PCLK A, B, C, D 77.76 MHz Output Clock		12.86		ns
	PCLK A, B, C, D 77.76 MHz Output Clock duty cycle	40		60	%
t_{PICLK}	Parallel Input Clock (PICLK) period		12.86		ns
	Parallel Input Clock (PICLK) duty cycle	40		60	%
tS_{PIN}	PINA[7:0], PINB[7:0], PINC[7:0], PIND[7:0] PARIN A, B, C, D and TIFP A, B, C, D, data setup time with respect to rising edge of PICLK	0.75			ns
tH_{PIN}	PINA[7:0], PINB[7:0], PINC[7:0], PIND[7:0] PARIN A, B, C, D and TIFP A, B, C, D, data hold time with respect to rising edge of PICLK	0.85			ns

Figure 18. AC Parity Error Timing Diagram

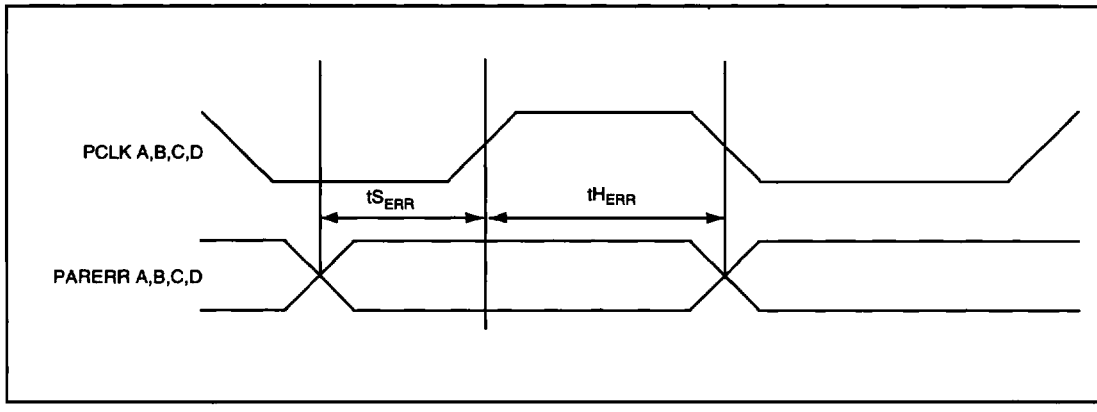
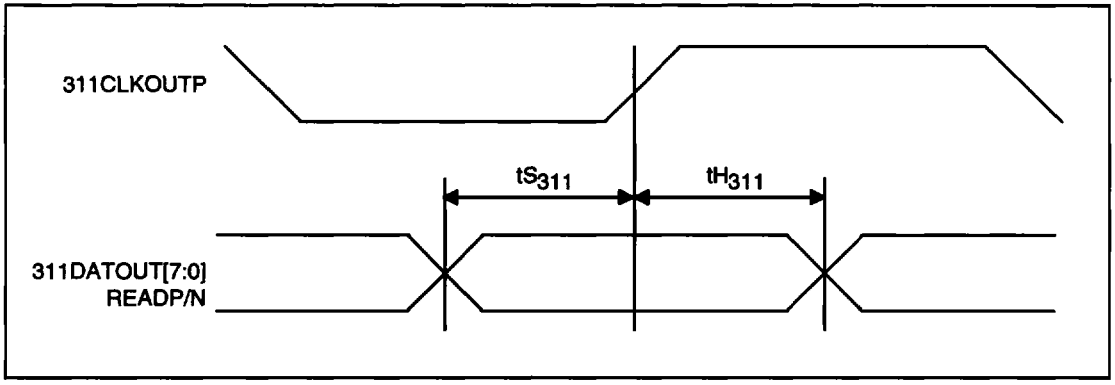


Table 13. Parity Error Timing Characteristics

Symbol	Description	Min	Max	Units
tS_{ERR}	Parity Error Output Set-up Time w.r.t. PCLK	4		ns
tH_{ERR}	Parity Error Output Hold Time w.r.t. PCLK	3.5		ns

Figure 19. AC Transmitter Output Timing Diagram



Notes:
1. When a set-up time is specified on differential LVDS signals between an input and a clock, the set-up time is the time in nanoseconds from the cross-over point of the input to the cross-over point of the clock.
2. When a hold time is specified on differential LVDS signals between an input and a clock, the hold time is the time in nanoseconds from the cross-over point of the clock to the cross-over point of the input.

Table 14. Transmitter Output Timing Characteristics

Symbol	Description	Min	Max	Units
	311CLKOUT Duty Cycle	33	67	%
tS_{311}	311DATOUT[7:0] Set-up Time w.r.t. 311CLKOUTP	0.65		ns
tH_{311}	311DATOUT[7:0] Hold Time w.r.t. 311CLKOUTP	0.55		ns
tP_{CLK}	Transmit Clock Input (311TCLK) to Transmit Output Clock (311CLKOUT) propagation delay		3.0	ns

Figure 20. Transmitter Clock Input (311TCLK) to Output Clock (311CLKOUT) Propagation Delay

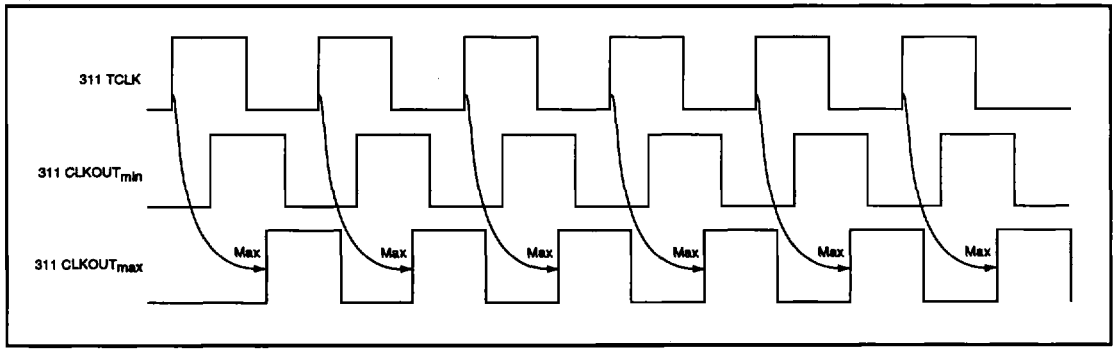
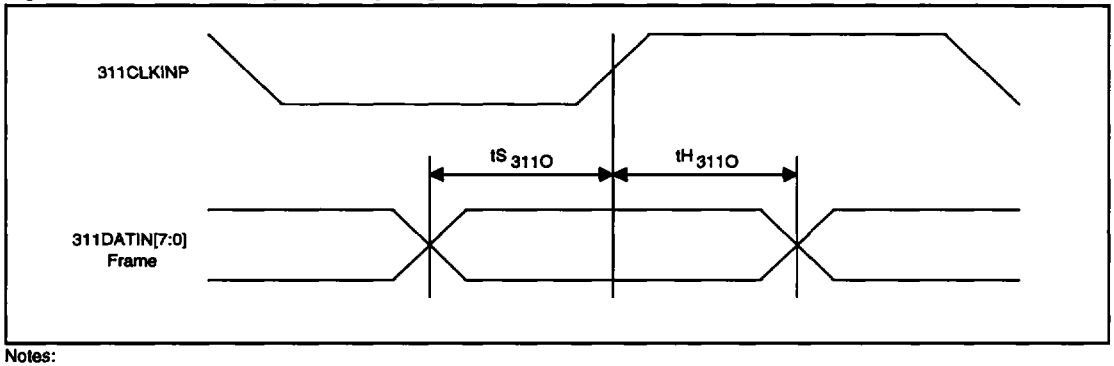


Figure 21. AC Receiver Input Timing Diagram



Notes:
1. When a set-up time is specified on differential LVDS signals between an input and a clock, the set-up time is the time in nanoseconds from the cross-over point of the input to the cross-over point of the clock.
2. When a hold time is specified on differential LVDS signals between an input and a clock, the hold time is the time in nanoseconds from the cross-over point of the clock to the cross-over point of the input.

Table 15. AC Receiver Input Timing Characteristics

Symbol	Description	Min	Max	Units
	311CLKIN Duty Cycle	40	60	%
tS_{311O}	311DATIN[7:0] and Frame Set-up Time w.r.t. 311CLKINP	0.5		ns
tH_{311O}	311DATIN[7:0] and Frame Hold Time w.r.t. 311CLKINP	0.9		ns

Table 16. AC Receiver Output Timing Characteristics

Symbol	Description	Min	Max	Units
	POCLK Frequency (nominally 77.76MHz)		78	MHz
	POCLK Duty Cycle	40	60	%
tS_{POUT}	POUT[7:0] Set-up Time to POCLK	4		ns
tH_{POUT}	POUT[7:0] Hold Time to POCLK	3.5		ns

Figure 22. AC Receiver Output Timing Diagram

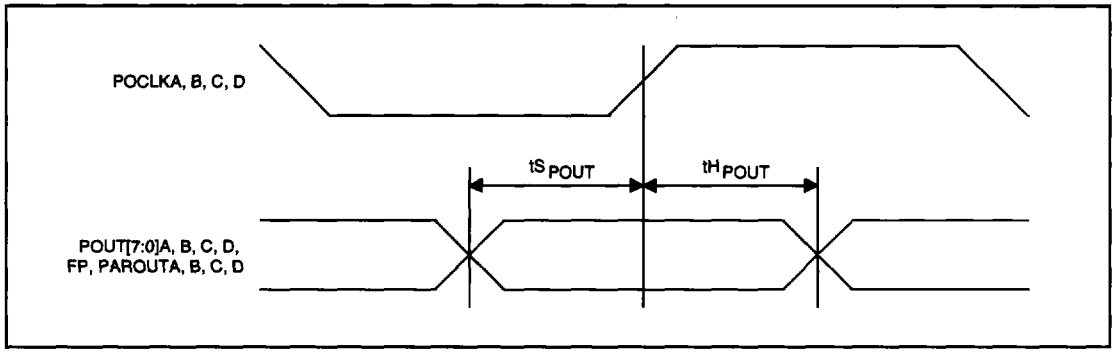
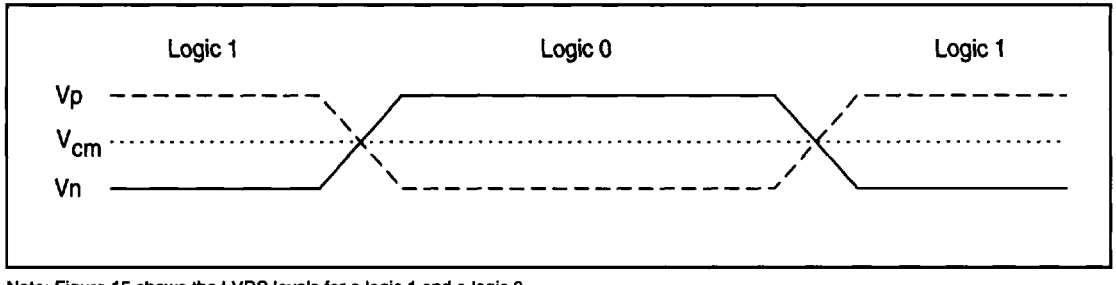


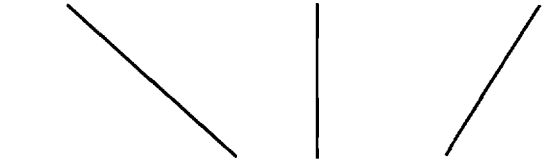
Figure 23. LVDS Input/Output Signaling



Note: Figure 15 shows the LVDS levels for a logic 1 and a logic 0.

Ordering Information

GRADE	TRANSCEIVER	PACKAGE
S—Commercial	3045	A-208 TEP PQFP



X XXXX X
Grade Part Number Package