FEATURES

- 64 bit/66 MHz PCI Bus Master Rev 2.2
- 32 bit/66 MHz PCI Target Rev 2.2
- Single 3.3V Core w/5V Tolerant User Interface
- Asynchronous 75 MHz User Bus
- 4 DMA Engines with 512 QWORD Buffers
- DMA Block Mode and Demand Mode Transfers
- 2 Pass-Thru Data Channels
- 128 QWORD PCI R/W Buffers for 128 QWORD BURST
- Independent PCI & User Write Posting Buffers
- Support for Type 0 & 1 Configuration Cycles and PCI Bridge Configuration Space
- *Compact*PCI® Hot Swap Friendly
- PCI SIG Hot Plug Compliant
- I_2O Messaging
- PCI Power Management Compliant
- JTAG Support
- Dual Bus DMA Chaining (Scatter/Gather)
- Mailboxes - Doorbells - Message Queuing
- Add-On Bus Parity
- User-Definable General Purpose I/O Pins
- Three User Definable Timers
- Expansion BIOS and POST Code Support
- Support for Unaligned Data Transfers
- Multiple DMA Transfers can be Linked Including Scatter/Gather
- Prefetch Capability
- Programmable Bus Utilization for 2nd Channel Based on PCI Bus Usage
- Bootload via Serial or Parallel ROM/FLASH
- Programmable Add-On Bus Register Offsets
- Small 256 PBGA Footprint

APPLICATIONS

- Intel® 80960Jx™
- Motorola® MPC603, PowerPC™ Family
- Motorola® QUICC™
- Video Frame Grabbers
- Data Communication Controllers
- Memory Controllers
- Bridge Interface
- High Speed Data Acquisition
- Intelligent I/O Controller
- Data Encryption/Decryption

DESCRIPTION

The S5964 is a high-performance PCI interface designed to easily connect user applications to the PCI Local Bus. It includes a rich set of features to make it the premier choice for interfacing microprocessors, microcontrollers, RISCs, DSPs, communications chips and much more to the PCI Local Bus. The S5964 is capable of performing as a PCI Target, Bus Master or a PCI Bridge. The PCI Bridge functions include generation of special PCI Local Bus configuration cycles required for a user Host processor to configure other PCI devices. Additional design flexibility allows connection as either a 32 bit or a 64 bit PCI Local Bus Device with clock frequencies from 0 to 66 MHz. The S5964 logic core is powered from a single 3.3 volt supply and accommodates both 3.3 and 5 volt signal inputs from the user application.

The S5964 is compliant with the PCI Local Bus Specification Revision 2.2, and includes the specification's optional Power Management registers, JTAG, Expansion ROM and parity features. Features included from other industry specifications are the *Compact*PCI® Hot Swap registers, CompactPCI I/O signals, I_2O Messaging registers and Scatter Gather capabilities via DMA chain descriptors. The S5964 also includes three user definable timers with interrupt capability and user-definable general purpose I/O signal pins.

An advanced AMCC technology is utilized to achieve low system power consumption while maintaining superior performance at PCI clock speeds up to 66 MHz. AMCC's new proven S5920 design methodology has been utilized in the S5964 for design ease, reliability and trouble free operation.

Figure 1.

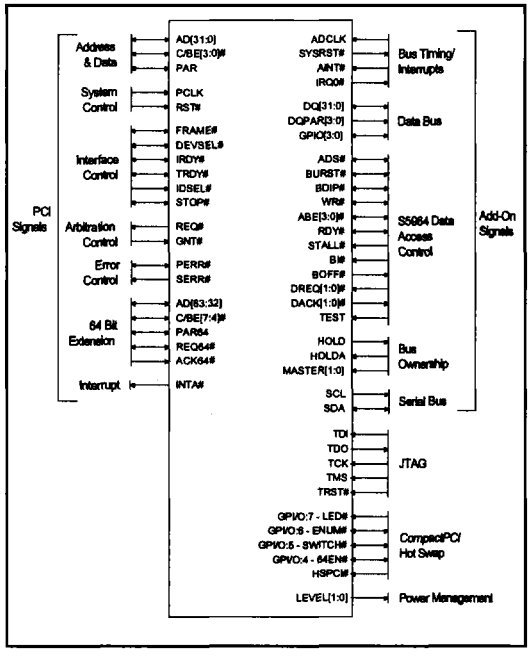
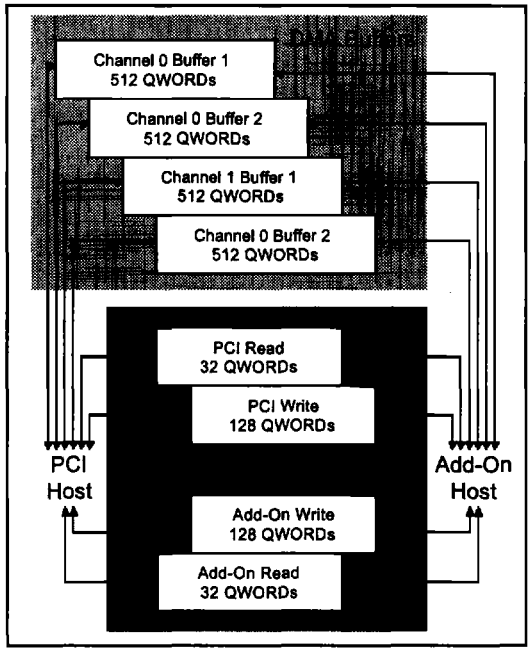


Figure 2.



The S5964 signal pins are shown in Figure 1. The left side details the PCI Local Bus signals and other industry standard signals supported. The right side details the Add-On Local Bus signal pins which is the user application interface.

The S5964 provides two independent DMA data channels containing four DMA engines for low-latency, high data rate data transfers. Two engines are dedicated to 32 and 64 bit PCI Local Bus data transfers and two engines are dedicated to 32 bit Add-On Local Bus data transfers. Each DMA channel incorporates two 512 QWORD deep buffers. PCI and Add-On data transfer overlapping is provided due to extended buffer capability. A PCI bus DMA transfer to one data channel's buffer can overlap with an Add-On bus DMA transfer from the same channel's second buffer. The S5964 supports DMA data transfers utilizing Demand Mode and Block Mode protocols.

Maximal DMA transfer flexibility is provided with the S5964 DMA Chain Descriptor feature. A Chain Descriptor is a 'command packet' which instructs a DMA Engine what operations to perform. The DMA engine executes each chain descriptor command from either Host or user memory. Multiple Chain descriptors can be created to move data from one location to multiple address destinations, or from different locations to one final linear location. This type of transfer is commonly known as Scatter/Gather and is supported by the S5964.

The S5964 design has been optimized for today's high transfer rate requirements. Multiple data buffers, shown in Figure 2, have been incorporated for each data channel. Programmable pre-fetch capabilities have also been incorporated in the S5964 to further optimize performance. Special non-DMA buffers allow Host bursting when the S5964 functions as a PCI or Add-On Target.

The Add-On Local Bus or user bus is a 32 bit synchronous data bus. An external Add-On clock input pin is provided to synchronize S5964 internal operation with Add-On user designs. The clock input frequency is user definable to a maximum rate of 75 MHz. The Add-On Bus contains multiplexed address/data to significantly reduces PCB trace space and layout requirements.

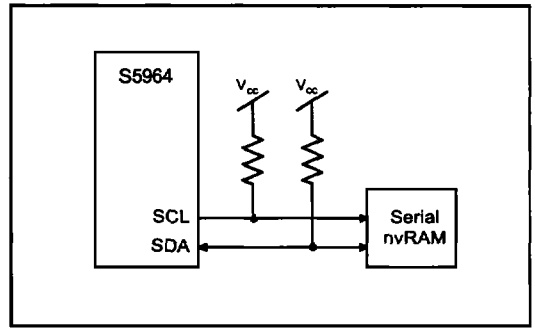
The S5964 has a built-in, bidirectional aligner allowing data to be aligned on any byte boundary. Data transfers from the PCI Bus to the Add-On Bus may be read with a different byte alignment than an Add-On address requires. Add-On Bus data read by a DMA engine from an Add-On Local Bus address is aligned based on the PCI address requirement. Non-DMA data transfers are performed without alignment modifications.

The S5964 supports boot loading of configuration data, Expansion BIOS and Power On Self Test code options via an external nonvolatile serial memory device. The serial nvRAM may be programmed with user defined configuration information which is loaded into the S5964 during power up initialization. Programming or reading the nvRAM may be done any time from dedicated S5964 operation registers. The S5964 provides a programmable SCL clock divider to support multiple speed serial nvRAMs. Serial nvRAM connections are shown in Figure 3.

The S5964 contains three user-definable 32-bit timers: two Add-On Local Bus timers and one PCI Local Bus timer. All timers are driven at the Add-On bus speed preventing time variations due to various motherboard PCI bus clock speeds.

Each timer contains a programmable prescale clock divider of 1, 2, 4, or 8. It is also programmable for single-shot mode and continuous mode operation with interrupt capability support.

Figure 3.



The S5964 supports three PCI to Add-On messaging mechanisms via a messaging unit. The messaging unit is composed of mailboxes, doorbells and I_2O Message Queuing registers required to implement the I_2O protocol. The S5964 supports the full I_2O specification. Table 1 summarizes the S5964 messaging registers and register interrupt capabilities.

Many of today's new systems are required to implement a power management feature. The S5964 supports both PCI Specification Revision 2.2 Power Management features and the *Compact*PCI specification Hot Swap feature.

Table 2 shows the S5964 PCI Configuration registers and all additional register sets implemented for both specifications. The I/O power control signal pins required by the *Compact*PCI specification for external circuit control are supported through the general purpose I/O pins.

During power up initialization, the S5964 configuration information loaded from the external nvRAM is placed in a set of embedded configuration registers. Table 3 shows the S5964 embedded configuration registers. A special embedded Base address size register set allows the user to relocate the Add-On bus Pass-Thru data channel regions and S5964 operation registers.

9

Table 1.

Register Type	Description	PCI Interrupt Capable	Add-On Interrupt Capable
Mailbox	Inbound	No	Opt. when full
Mailbox	Outbound	Opt. when full	No
Doorbell	Inbound	No	Opt. per bit
Doorbell	Outbound	Opt. per bit	No
Message	Inbound	Optional	Optional
Message	Outbound	Optional	Optional

Table 2.

Byte 3	Byte 2	Byte 1	Byte 0	Address
Device ID Register		Vendor ID Register		00h
PCI Status Register		PCI Command Register		04h
Class Code Register			Revision ID Register	08h
Built-In Self Test	Header Type Register	Latency Timer Register	CacheLine Size	0Ch
Base Address Register 0				10h
Base Address Register 1				14h
Base Address Register 2				18h
Reserved Space				1Ch
Reserved Space				20h
Reserved Space				24h
Cardbus CIS Pointer Register				28h
Subsystem ID Register		Subsystem Vendor ID Register		2Ch
Expansion ROM Base Address Register				30h
Reserved Space			Capabilities Pointer	34h
Reserved Space				38h
Max. Latency Register	Min. Grant Register	Interrupt Pin Register	Interrupt Line Register	3Ch
Reserved	PCISSTS Register	PCICTRL Register	SPECIAL Register	40h
CompactPCI Hot Swap Control/Status Register				44h
Power Management Capabilities Register		Next Item Pointer	Capability ID	48h
PMD Register	PMCSR_BSE Register	PMCSR Register		4Ch
Not Used				50h-FFh

Table 3.

Byte 3	Byte 2	Byte 1	Byte 0	Address
S5964 Control Key Register				00h
Base Address Size Register 0				04h
Base Address Size Register 1				08h
Base Address Size Register 2				0Ch
PCI Retry Counter Register		Expansion ROM Size Register		10h

The S5964 contains three groups of operation registers to control data flow and the S5964 functions. These registers contain user status, flow control and operation information. The three register groups are defined as PCI accessible only (Table 4), Add-On accessible only (Table 5) and PCI/Add-On accessible or common registers (Table 6) shown below.

Table 4.

PCI Local Bus Registers	Size (bytes)
PCI Control and Status Register (PCSR)	4
Outbound Status Register (OSR)	4
Outbound Interrupt Mask Register (OIMR)	4
Inbound Queue FIFO	4
Outbound Queue FIFO	4
PCI Timer Mode Register (PTMR)	4
PCI Timer Count Register (PTCR)	4
PCI Timer Reload Register (PTRR)	4

Table 5.

Add-On Local Bus Registers	Size (bytes)
Add-On Timer Mode Register 0 (ATMR0)	4
Add-On Timer Count Register 0 (ATCR0)	4
Add-On Timer Reload Register 0 (ATRR0)	4
Add-On Timer Mode Register 1 (ATMR1)	4
Add-On Timer Count Register 1 (ATCR1)	4
Add-On Timer Reload Register 1 (ATRR1)	4
Add-On Operation Decode Register (AODR)	2
Reserved Space	2
Queue Base Address Register (QBAR)	2
Messaging Unit Control Register (MUCR)	1
Reserved Space	1
Inbound Free Head Pointer Register (IFHPR)	4
Inbound Free Tail Pointer Register (IFTPR)	4
Inbound Post Head Pointer Register (IPHPR)	4
Inbound Post Tail Pointer Register (IPTPR)	4
Outbound Free Head Pointer Register (OFHPR)	4
Outbound Free Tail Pointer Register (OFTPR)	4
Outbound Post Head Pointer Register (OPHPR)	4
Outbound Post Tail Pointer Register (OPTPR)	4
Inbound Status Register (ISR)	4
Inbound Interrupt Mask Register (IIMR)	4
Memory Window Add-On Address Register (MWAAR)	2
Memory Window Size Register (MWSR)	2
Memory Window PCI Address Register Low (MWPARL)	4
Memory Window PCI Address Register High (MWPARH)	4
I/O Window PCI Address Register (IOWPAR)	2
I/O Window Add-On Address Register (IOWAAR)	2
Outbound ATU Control Register (OACR)	4

Table 6.

Common Bus Registers	Size (bytes)
Add-On Control/Status Register (ACSR)	2
GPIO Register (GPIOR)	2
Inbound Doorbell Register (IDR)	4
Outbound Doorbell Register (ODR)	4
Memory Address Register (MAR)	4
Memory Control/Data Register (MCDR)	2
Reserved Space	2
DMA Control Register (DMACR)	1
Reserved	3
S5964 Control Key Register (64CTRL)	4
Power Management Options Register (PMOR)	1
Reserved	3
Inbound Mailbox Register (IMR)	4
Reserved - Inbound Mailbox Register 1 (IMR1)	4
Outbound Mailbox Register (OMR)	4
Reserved - Outbound Mailbox Register 1 (OMR1)	4
Add-On Master 0 Registers	8
Add-On Master 1 Registers	8
Add-On Master 2 Registers	8
DMA Channel 0 Registers	36
DMA Channel 1 Registers	36

S5964 Pin Descriptions

AD[31:0] t/s *Address/Data Bus.* The PCI Local Bus data and address information are multiplexed on these signal lines. Each PCI Bus transaction starts with an address/command phase followed by one or more data phases. An address phase occurs on a PCI Bus CLK cycle rising edge in which FRAME# is seen asserted. The following data phases occur on each subsequent CLK rising edges in which both IRDY# and TRDY# are seen asserted. The AD lines contain address information in an address/command phase and 8, 16, 32 or 64 bit data in data phases.

C/BE[3:0]# t/s *Command/Byte Enable.* Both the PCI Bus transaction command and Byte Enables are multiplexed on these signal lines. During a PCI Bus transaction start or address/command phase, the Bus Master requested transaction type command is driven onto these lines. A list of each valid command is shown below. During subsequent data phases, these lines are driven with Byte Enable data to indicate which bytes of the AD[32:0] bus DWORD are valid for that data phase. C/BE[0]# = LSB valid, C/BE[3]# = MSB valid.

C/BE# [3	2	1	0]	Description
0	0	0	0	Interrupt Acknowledge
0	0	0	1	Special Cycle
0	0	1	0	I/O Read
0	0	1	1	I/O Write
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Memory Read
0	1	1	1	Memory Write
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Configuration Read
1	0	1	1	Configuration Write
1	1	0	0	Memory Read Multiple
1	1	0	1	Dual Address Cycle
1	1	1	0	Memory Read Line
1	1	1	1	Memory Write and Invalidate

PAR t/s *Parity.* Parity is always driven as even using all AD[31:0] and C/BE[3:0]# signals. The PAR signal is valid one clock following the address phase. During a data phase for write transactions, the Bus Master drives this signal on the clock following IRDY# active. During a data phase for read transactions, this signal is driven by the Target and is valid on the clock following TRDY# active.

PCLK input *PCI Clock.* The rising edge of this signal is the reference upon which all PCI Bus signals are based except for RST# and INTA#. The maximum PCLK frequency for the S5964 is 66 MHz and the minimum is DC (0 Hz).

RST# input *Reset.* Reset is used to bring the S5964 registers, signals and internal logic to a known state.

FRAME#	s/t/s	*Frame.* This signal is driven by an active Bus Master to indicate the start and the duration of a bus transaction. When FRAME# is first asserted, it initiates a bus transaction and a valid AD[31:0] address is present and a valid C/BE[3:0] command is present. Data transfers continue while FRAME# is asserted. The de-assertion of FRAME# indicates the transaction is in a final data phase or has completed.
DEVSEL#	s/t/s	*Device Select.* This signal is driven by the Target responding to the AD[63:0] address information and indicates ownership of the address. This signal informs the Bus Master an agent has decoded the address and is responding to a current bus cycle. The S5964 is a medium DEVSEL device.
IRDY#	s/t/s	*Initiator Ready.* This signal is driven by the active Bus Master to indicate its readiness to transfer data in the current data phase. During a write transaction, IRDY# indicates the AD[63:0] lines contain valid data.
TRDY#	s/t/s	*Target Ready.* This signal is driven by the Target to indicate the target's readiness to transfer data in a data phase. During a read transaction, TRDY# indicates the AD[63:0] lines contain valid data. Data transfer wait states occur until both TRDY# and IRDY# are asserted on the same PCLK rising edge.
IDSEL	input	*Initialization Device Select.* This pin is used during power up as a chip select. The PCI BIOS executes special commands to read or write configuration information during the motherboard initialization process.
STOP#	s/t/s	*Stop.* The Stop signal is driven by the active Target to convey a request to the Bus Master to stop a data transaction.
REQ#	t/s	*Request.* This signal is sourced by an agent wishing to become a Bus Master for a data transfer. It is a point-to-point signal between the system arbiter and each Bus Master.
GNT#	t/s	*Grant.* This signal is sourced by the system arbiter. Grant indicates to a requesting Bus Masters permission to acquire the bus is granted. It is a point-to-point signal between the system arbiter and each Bus Master
PERR#	s/t/s	*Parity Error.* This signal reports data parity errors for all bus transactions except for Special Cycles. It is driven by the agent receiving data two clock cycles after the parity was detected as an error. This signal is driven inactive (high) for one clock cycle prior to returning to the tri-state condition.
SERR#	o/d	*System Error.* Used to report address and data parity errors on Special Cycle commands and any other error condition having a catastrophic system impact. Special Cycle commands are not supported by the S5964.
AD[63:32]	t/s	*Address/Data Bus.* The PCI Bus data and address information is multiplexed on these signal lines and provides 32 additional bits. The upper 32 bits of a 64-bit address are transferred during an address phase, otherwise, these bits are reserved but are stable and indeterminate. When REQ64# and ACK64# are both asserted, an additional 32 bits of data are transferred.
C/BE[7:4]#	t/s	*Command/Byte Enable.* These bits are reserved and indeterminate until an address request is asserted. The bus command is transferred on C/BE[7:4]#. When REQ64# and ACK64# are both asserted, C/BE[7:4]# are Byte Enables that indicate which byte lanes carry meaningful data. C/BE[4] applies to byte 4; C/BE[7] to byte 7.
PAR64	t/s	*Parity.* Parity is always driven as even using all AD[63:32] and C/BE[7:4]# signals. The parity is valid one clock following the second address phase when REQ64# is asserted and the Dual Address Cycle command is indicated on the C/BE[3:0] lines. During a data phase for write transactions, the Bus Master sources this signal; during a data phase for read transactions, the Target drives this signal.

REQ64#	s/t/s	*Request 64-bit Transfer.* This signal is sourced by the Bus Master to request a 64-bit data transfer. This signal has the same timing as FRAME#. REQ64# is also used during system reset to identify devices connected to the 64-bit data path and devices not connected.
ACK64#	s/t/s	*Acknowledge 64-bit Transfer.* This signal is sourced by the active Target to indicate willingness to transfer data using 64 bits. ACK64# has the same timing as DEVSEL#.
INTA#	o/d	*Interrupt A.* This signal is level sensitive. Driving it low will interrupt to the host. The INTA# interrupt is to be used for any single function device requiring interrupt capability.
TDI	input	*Test Data Input.* This is used to test instructions and shift test data into the S5964 during Test Access Port operation.
TDO	output	*Test Output.* This signal is used to test instructions and shift test data out of the S5964 during Test Access Port operation.
TCK	input	*Test Clock.* This is used to clock state information and test data into and out of the S5964 during operation of the Test Access Port
TMS	input	*Test Mode Select.* This is used to control the state of the Test Access Port controller in the S5964.
TRST#	input	*Test Reset.* This provides an asynchronous initialization of the Test Access Port controller.
LED#	o/d in	*CompactPCI LED Output*, or GPIO[7].
ENUM#	bi-dir	*CompactPCI ENUM# Output*, or GPIO[6]
SWITCH#	bi-dir	*CompactPCI SWITCH Input*, or GPIO[5].
64EN#	bi-dir	*Compact PCI 64EN# Input*, or GPIO[4].
HSPCI#	input	*Hot Swap PCI.* Low when the S5964 is used in a Compact PCI Hot Swap system. This signal controls use of 64EN# and other signals, as well as enabling reporting Hot Swap Support. When high, the four Hot Swap signals become GPIO[7:4].
LEVEL[1:0]	output	*Power Level Control.*
ADCLK	input	*Add-On Clock.* All internal Add-On Bus logic and timers are driven and synchronous to this clock input. Driving this signal from application logic allows the S5964 Add-On Bus to be asynchronous to the PCI Bus.
SYSRST#	output	*System Reset.* This output signal is an active low buffered form of the PCI Bus RST# signal. May be also activated through software writing to a S5964 Operation register. This signal is used to bring Add-On application logic to a known state.
AINT#	input	*Add-On Interrupt.* The AINT# input is enabled and disabled through writing to an S5964 operation register. The assertion of this signal from Add-On logic will assert the PCI Bus signal INTA# low. This signal is level sensitive allowing it to be driven by multiple sources.
IRQ#	output	*Interrupt Request.* Interrupt request to the Add-On Local Bus. An interrupt output is de-asserted by clearing the source of the interrupt. Interrupts may be generated from several sources, which are arranged into interrupt "groups" (each interrupt source is specified as belonging to a group rather than a specific pin).
DQ[31:0]	bi-dir	*Data Bus.* The Add-On data and address information is multiplexed on these signal lines. Each data transaction starts with an address phase followed by one or more data phases. During an address phase, the ADS# signal is asserted to indicate a valid address is on the DQ Bus. This is then followed by valid data on each subsequent ADCLK rising edge. When used for address, DQ[1:0] is only valid for byte-wide ROM accesses.

DQPAR[3:0]	output	*Data Bus Parity.* One parity bit is generated for each of the DQ Bus bytes. DQPAR[0] for DQ[7:0], DQPAR[1] for DQ[15:8], etc.
GPIO[3:0]	bi-dir	*General Purpose Input/Output.* GPIO[1:0] may be used as IRQ2# / IRQ1#.
ADS#	bi-dir	*Address Strobe.* This signal is sourced by the Add-On Bus Master. Assertion indicates the initiation of an Add-On to PCI data transfer phase requiring the valid address on the DQ[31:0] bus be latched. As a target, ADS# must be driven only during the address phase since the S5964 always decodes an access when ADS# is low. The S5964 allows ADS# to be driven the cycle immediately following a data transfer (if a turnaround is required, it is up to the master to enforce the turnaround itself). As a master, the S5964 will not drive ADS# on the cycle immediately after a read data transaction because it requires a cycle to change the DQ inputs over to the address.
BURST#	bi-dir	When the S5964 is the master of the Add-On bus, BURST# is asserted with ADS# (if the cycle is a burst), and it is held asserted through the last data transfer. This signal has the same function in both BDIP and BLAST modes. When the S5964 is a target in BDIP mode, BURST# is used to determine if the external Add-On master is requesting a burst transfer.
BDIP#/ BLAST#	bi-dir	Driven by the bus master, this signal indicates how much data will be transferred. In BLAST mode it is driven active during the last data transaction. When the S5964 is the target of an Add-On Master, this signal can be programmed to work in one of two modes: BLAST or BDIP. In BLAST mode, BLAST# is asserted with the last data transfer. When BLAST# is inactive during a data transfer it indicates that the transfer should continue. Once BLAST# is asserted, it must remain asserted until the transfer completes with RDY#. BURST# is not used in this mode. In BDIP mode, BDIP# is used to indicate the last data transfer - the last transfer is complete when BDIP# is sampled high with the data (RDY# active). When the S5964 is the master of the Add-On Bus, BLAST or BDIP mode may be used. For BDIP mode, BDIP goes high at the leading edge of the last DWORD transfer. In BLAST mode, BLAST# goes active at the leading edge of the last DWORD transfer.
WR#	bi-dir	*Write.* The write signal is driven by the Add-On Bus Master to indicate the current data phase is a read or write to the DQ[31:0] Bus.
ABE[3:0]#	bi-dir	*Add-On Byte Enable.* During Add-On data transfers, these signal lines are driven with byte enable data to indicate which bytes on the DQ[31:0] pins are valid during the data phase. BE0# = DQ[7:0] valid, BE1# = DQ[15:8] valid, etc. These are S5964 driven outputs during PCI writes and Add-On logic driven inputs driven during PCI reads. For slave accesses, these pins are inputs indicating byte lane validity as shown below: The BEs for the first access of a transfer are valid with the address. This is done so that SIZE bits can be created for embedded CPU devices that use the address and transfer size rather than BEs. During ROM accesses, BE[1:0] presents the byte address for the access with the same timing as ADR.

ABE0# 0 = Byte 0 is valid

ABE1# 0 = Byte 1 is valid

ABE2# 0 = Byte 2 is valid

ABE3# 0 = Byte 3 is valid

RDY#	bi-dir	*Ready.* Data transfers occur on ADCLK rising clock edges. The ready signal is an output during PCI writes indicating valid data. The Add-On logic drives this signal during PCI reads to indicate valid data on the DQ[31:0] Bus.When the S5964 is a slave, RDY# is only driven active during the actual data portion of the transfer. At the end of the transfer, RDY# is actively de-asserted on the cycle following the last data transfer, and tri-stated the following cycle.
STALL#	input	*Stall.* When the S5964 is a target, this signal can be used to extend data cycles. It is sampled with RDY# during a data phase. STALL# de-asserted with RDY# asserted completes a data transfer. During a read of the S5964, STALL# may be used to keep read data valid on the bus longer. During a write of the S5964, it may be used to delay the S5964 from accepting data. When the S5964 is master, STALL# may be used to postpone driving ADS#. On the clock edge which ADS# would normally be asserted, STALL# must be high or ADS# is delayed. This functionality can be used with devices that have slow output buffers so that the address for the new transfer will not be driven while the buffers are still enabled.
BI#	input	*Burst Inhibit.* Assertion of this signal prevents the S5964 from performing Add-On burst operations when a Bus Master. Asserting BI# with RDY# active causes the S5964 to complete the current data phase and present a new address phase for the next data transfer. This signal can be used to force single data phases with an address phase for each transfer to reduce design complexity.
BOFF#	output	*Backoff.* This output is used to retry an Add-On read or write to the S5964. BOFF# is asserted instead of RDY# to tell the Add-On Master to relinquish the bus and retry his access. BOFF# is a sustained tri-state signal that will be actively de-asserted for one cycle then tri-stated.
DREQ[1:0]#	input	*DMA Request.* This signal enables a DMA transfer for Channel 0 and 1.
DACK[1:0]#	output	*DMA Acknowledge.* Is asserted to indicate the associated DMA channel is busy. It is always driven when a DMA address occurs, whether or not in demand mode. DMAACK0# = Channel 0, DMAACK1 = Channel 1. This signal is valid with the first ADS# until the end of the transaction.
TEST	input	*Factory test signal.* This signal must be left open.
HOLD	output	Asserted by the S5964 to request bus ownership. Once driven, HOLD will be held active until HOLDA occurs. Master Bus Request to Add-On arbiter.
HOLDA	input	*Hold Acknowledge.* Asserted to grant bus ownership to the S5964. HOLDA must be de-asserted one cycle after HOLD is de-asserted unless HOLDA is always asserted. Master Bus acknowledge from Add-On arbiter.
MASTER[1:0]	input	*Add-On Master.* These signals indicate which DMA Engine currently owns the bus, and which set of DMA Engine control/status registers to use. Is used to determine which register set controls S5964 response to the master.
SCL	o/d t/s	*Serial Clock.* This output is intended to drive a two-wire Serial Interface and functions as the Bus's Master. It is intended that this signal be directly connected to one or more serial non-volatile RAMs.
SDA	bi-dir o/d	*Serial Data/Address.* This bi-directional pin is used to transfer addresses and data to and from an external serial nvRAM. It is an open drain output and intended to be wire-ORed with all other devices on the serial bus using a 4.7K external pull-up resistor.

Absolute Maximum Ratings

Supply Voltage Range (VCC Core) ..... 3 V to +3.3 V

Input Pin Voltage Range ..... -0.5 V to VCC + 0.5 V

Storage Temperature Range ..... -55 to 125 °C

Operating Ambient Temperature Range ..... 0 to 70 °C

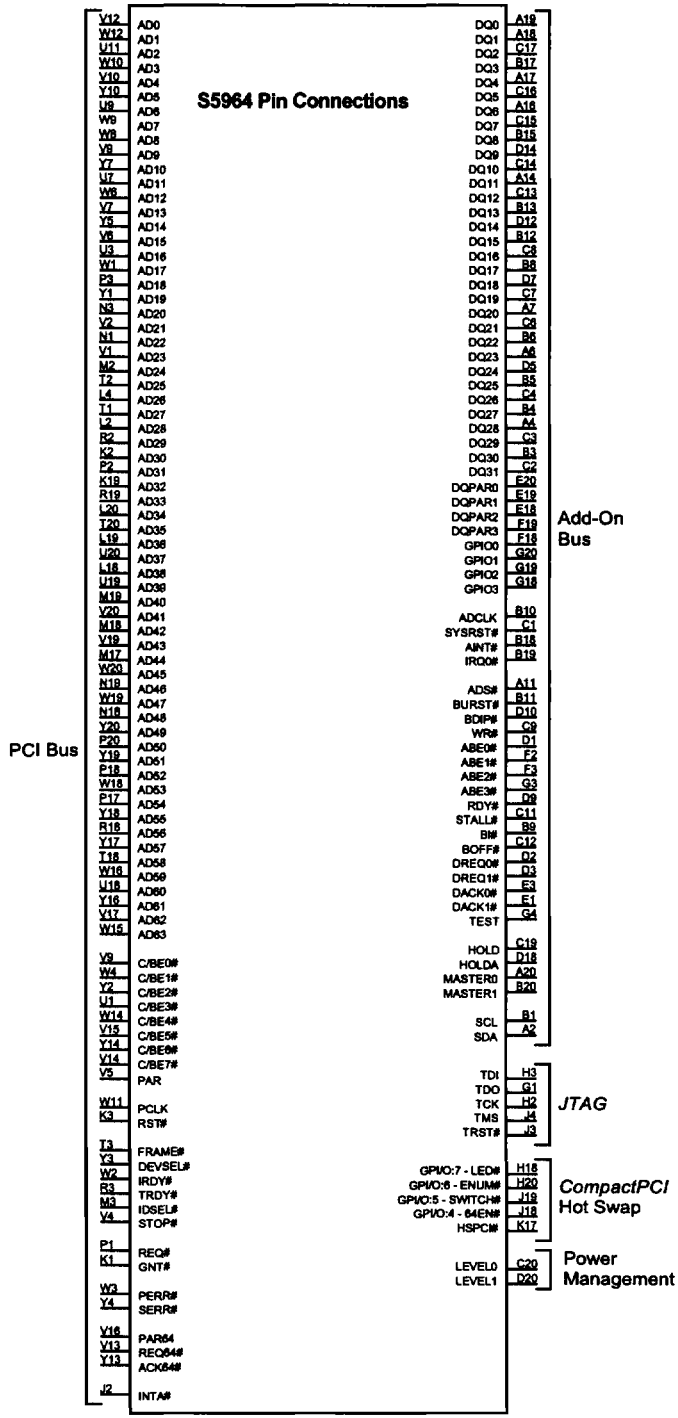
Virtual Junction Temperature ..... 150 °C

Soldering Lead Temperature ..... 300 °C 10 Seconds

* Stresses beyond those listed under absolute maximum ratings may cause permanent damage to this device. These are stress ratings only.

Recommended Operating Conditions

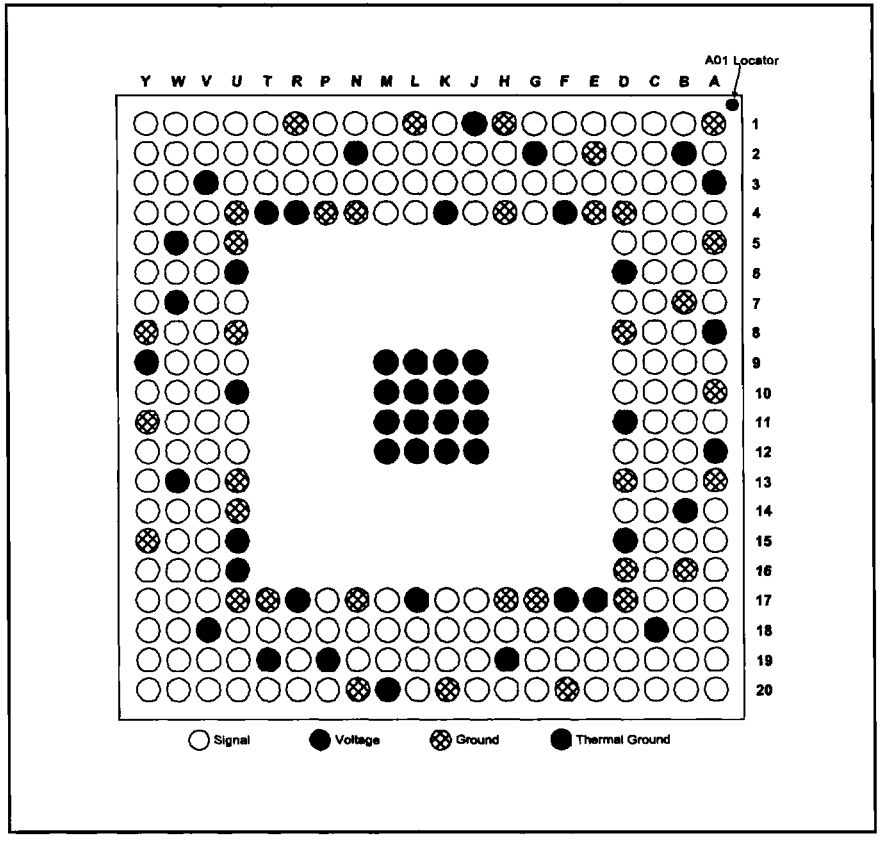
Symbol	Parameter	Min	NOM	Max	Units	Test Conditions	Notes
V_{CC}	PCI Supply Voltage (core)	3	3.3	3.6	Volts	To PCI Spec 2.2	
V_I	Input Voltage	0	-	3.6	Volts	Add-On 5 V tolerant	
V_O	Output Voltage	0	-	3.6	Volts		
V_{ih}	High Level Input Voltage	0.7	-	V_{CC}	Volts		
V_{il}	Low Level Input Voltage		-	0.3	Volts		
V_{oh}	High Level Output Voltage	0.9	-	-	Volts	I_{oh} = TBD	
V_{ol}	Low Level Output Voltage	-	-	0.1	Volts	I_{ol} = TBD	
T_c	PCLK Cycle Time	15	-	30	ns		
T_w	PCLK High/Low Time	6			ns		
T_r	Rise/Fall Time	-	-	25	ns		
T_a	Ambient Temperature	0	-	70	°C		
T_{JA}	Thermal Resistance	TBD	-	-	°C/W		
P_{DD}	Power Dissipation	-	TBD	TBD	Watts		


S5964 Pin Connections
PCI Bus
V12 AD0
W12 AD1
U11 AD2
W10 AD3
V10 AD4
Y10 AD5
U9 AD6
W9 AD7
W8 AD8
V8 AD9
Y7 AD10
U7 AD11
W6 AD12
V7 AD13
Y5 AD14
V6 AD15
U3 AD16
W1 AD17
P3 AD18
Y1 AD19
N3 AD20
V2 AD21
N1 AD22
V1 AD23
M2 AD24
T2 AD25
L4 AD26
T1 AD27
L2 AD28
R2 AD29
K2 AD30
P2 AD31
K19 AD32
R19 AD33
L20 AD34
T20 AD35
L19 AD36
U20 AD37
L18 AD38
U19 AD39
M19 AD40
V20 AD41
M18 AD42
V19 AD43
M17 AD44
W20 AD45
N19 AD46
W19 AD47
N18 AD48
Y20 AD49
P20 AD50
Y19 AD51
P18 AD52
W18 AD53
P17 AD54
Y18 AD55
R18 AD56
Y17 AD57
T18 AD58
W16 AD59
U18 AD60
Y16 AD61
V17 AD62
W15 AD63
V9 C/BE0#
W4 C/BE1#
Y2 C/BE2#
U1 C/BE3#
W14 C/BE4#
V15 C/BE5#
Y14 C/BE6#
V14 C/BE7#
V5 PAR
W11 PCLK
K3 RST#
T3 FRAME#
Y3 DEVSEL#
W2 IRDY#
R3 TRDY#
M3 IDSEL#
V4 STOP#
P1 REQ#
K1 GNT#
W3 PERR#
Y4 SERR#
V16 PAR64
V13 REQ64#
Y13 ACK64#
J2 INTA#
DQ0 A19
DQ1 A18
DQ2 C17
DQ3 B17
DQ4 A17
DQ5 C16
DQ6 A16
DQ7 C15
DQ8 B15
DQ9 D14
DQ10 C14
DQ11 A14
DQ12 C13
DQ13 B13
DQ14 D12
DQ15 B12
DQ16 C6
DQ17 B6
DQ18 D7
DQ19 C7
DQ20 A7
DQ21 C8
DQ22 B8
DQ23 A8
DQ24 D5
DQ25 B5
DQ26 C4
DQ27 B4
DQ28 A4
DQ29 C3
DQ30 B3
DQ31 C2
DQPAR0 E20
DQPAR1 E19
DQPAR2 E18
DQPAR3 F19
GPIO0 F18
GPIO1 G20
GPIO2 G19
GPIO3 G18
ADCLK B10
SYSRST# C1
AINT# B18
IRQ0# B19
ADS# A11
BURST# B11
BDIP# D10
WR# C9
ABE0# D1
ABE1# F2
ABE2# F3
ABE3# G3
RDY# D9
STALL# C11
BI# B9
BOFF# C12
DREQ0# D2
DREQ1# D3
DACK0# E3
DACK1# E1
TEST G4
HOLD C19
HOLDA D18
MASTER0 A20
MASTER1 B20
SCL B1
SDA A2
Add-On Bus
TDI H3
TDO G1
TCK H2
TMS J4
TRST# J3
JTAG
GPIO:7 - LED# H18
GPIO:6 - ENUM# H20
GPIO:5 - SWITCH# J19
GPIO:4 - 64EN# J18
HSPCI# K17
CompactPCI Hot Swap
LEVEL0 C20
LEVEL1 D20
Power Management

Package Information - 256 PBGA

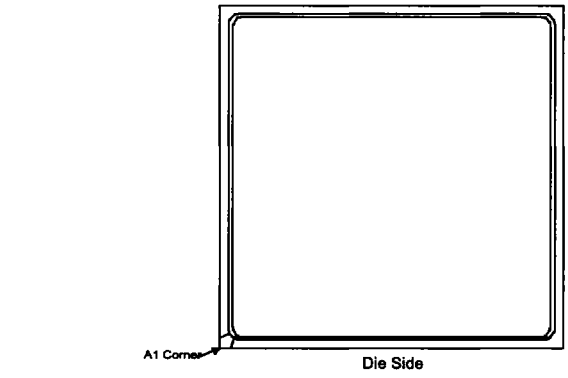
- Copper conductor
- 0.40 W/m-°C Thermal conductivity

256 PBGA Package Leads

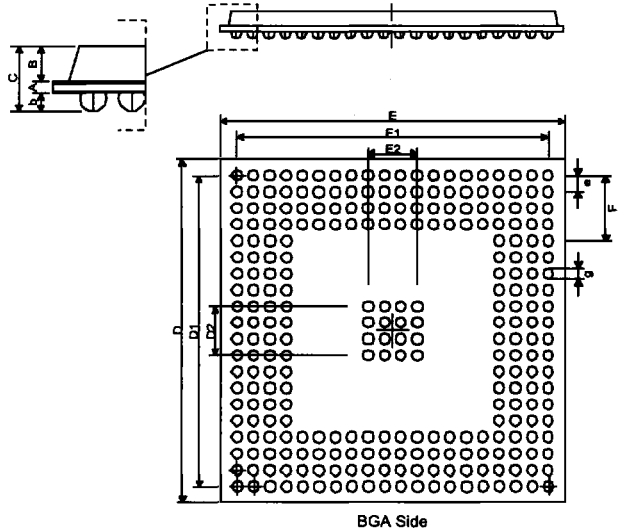


9

Mechanical Data 256 PBGA



Die Side



BGA Side

Dimensions	Tolerance +/-	256 PBGA Package
A	0.109	0.67
B	0.100	1.20
b	0.100	0.60
C, max	-	2.65
D and E	0.203	27.00
D1 and E1	0.051	24.13
e	Nom	1.27
g	Nom	0.75
D2 and E2	0.051	3.81
I/O Matrix		20 x 20
Populated Rows (F)		4