1,048,576 WORD × 1 BIT DYNAMIC RAM

PRELIMINARY

DESCRIPTION

The TC511002BP/BJ/BZ/BFT is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511002BP/BJ/BZ/BFT utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC511002BP/BJ/BZ/BFT to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ, 20/19 pin plastic ZIP, 24/20 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

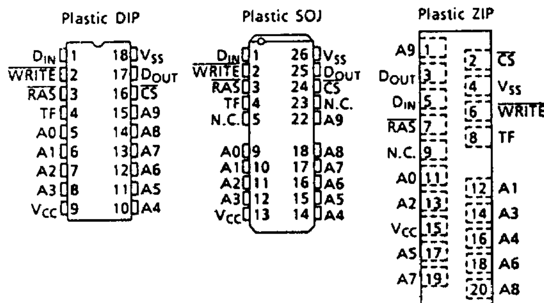
FEATURES

- 1,048,576 word by 1bit organization
- Fast access time and cycle time

	TC511002BP/BJ/BZ/BFT – 60
t_{RAC} $\overline{\text{RAS}}$ Access Time	60ns
t_{AA} Column Address Access Time	30ns
t_{CAC} $\overline{\text{CS}}$ Access Time	20ns
t_{RC} Cycle Time	110ns
t_{SC} Static Column Mode Cycle Time	35ns

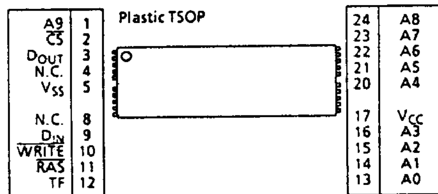
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  - 495mW MAX. Operating
  - 5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability
- Read-Modify-Write, $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only refresh, Hidden refresh, Static Column Mode and Test Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- Package
  - TC511002BP : DIP18-P-300C
  - TC511002BJ : SOJ26-P-300
  - TC511002BZ : ZIP20-P-400
  - TC511002BFT : TSOP24-P-0616

PIN CONNECTION

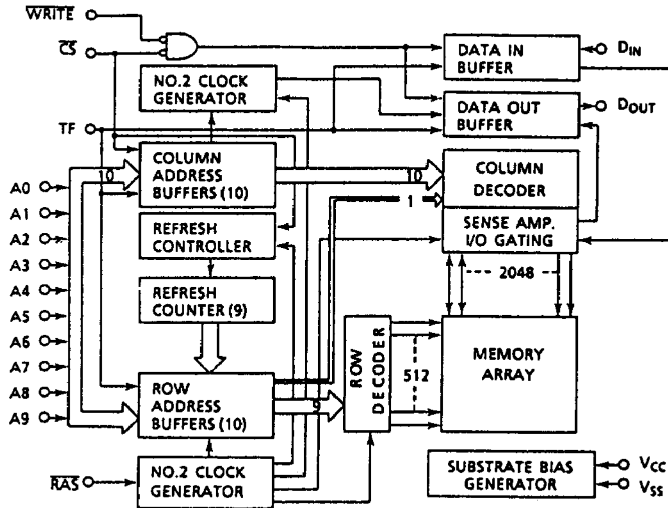


PIN NAMES

A0~A9	Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{\text{CS}}$	Chip Select Input
$\overline{\text{WRITE}}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
TF	Test Function
N.C.	No Connection



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1~7	V	1
Test Function Input Voltage	$V_{IN(TF)}$	-1~10.5	V	1
Output Voltage	V_{OUT}	-1~7	V	1
Power Supply Voltage	V_{CC}	-1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2
$V_{IH(TF)}$	Test Enable Input High Voltage	V_{CC}+4.5	-	10.5	V	2
$V_{IL(TF)}$	Test Disable Input Low Voltage	-1.0		V_{CC}+1.0	V	2

DC ELECTRICAL CHARACTERISTICS (VCC = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	TC511002BP/BJ/ BZ/BFT-60	-	90	mA	3, 4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CS} = V_{IH}$)		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	TC511002BP/BJ/ BZ/BFT-60	-	90	mA	3, 5
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode ($\overline{RAS} = \overline{CS} = V_{IL}$, Address Cycling: $t_{SC} = t_{SC}$ MIN.)	TC511002BP/BJ/ BZ/BFT-60	-	70	mA	3, 4
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CS} = V_{CC} - 0.2V$)		-	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	TC511002BP/BJ/ BZ/BFT-60	-	90	mA	3
$I_{I(L)}$	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input ($0V \leq V_{IH} \leq 6.5V$, All Other Pins Not Under Test = 0V)		- 10	10	µA	
$I_{ITF(L)}$	INPUT LEAKAGE CURRENT (only TF) ($0V \leq V_{IN\ (TF)} \leq V_{CC} + 0.5V$, All Other Pins Not Under Test = 0V)		- 10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq +5.5V$)		- 10	10	µA	
I_{TF}	TEST FUNCTION INPUT CURRENT ($V_{CC} + 4.5V \leq V_{IN\ (TF)} \leq 10.5V$)		-	1	mA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage ($I_{OUT} = -5mA$)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage ($I_{OUT} = 4.2mA$)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(VCC = 5V ± 10%, Ta = 0~70°c)(Notes 6, 7, 8)

SYMBOL	PARAMETER	TC511002BP/BJ/BZ/BFT-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	135	-	ns	
t_{SC}	Static Column Mode Cycle Time	35	-	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cycle Time	60	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	ns	9, 14
t_{CAC}	Access Time from $\overline{CS}$	-	20	ns	9, 14
t_{AA}	Access Time from Column Address	-	30	ns	9, 15
t_{ALW}	Access Time from Last Write	-	55	ns	9, 16
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	0	-	ns	9
t_{OFF}	Output Buffer Turn-Off Delay	0	20	ns	10
t_{AOH}	Output Data Hold Time from Column Address	5	-	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	-	20	ns	
t_{WOH}	Output Data Hold Time from $\overline{WRITE}$	0	-	ns	
t_T	Transition Time (Rise and Fall)	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	60	100,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	20	-	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	60	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	20	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	20	100,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	20	40	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	15
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	5	-	ns	
t_{CP}	$\overline{CS}$ Precharge Time	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	ns	
t_{AWR}	Column Address Hold Time referenced to $\overline{RAS}$ (WRITE CYCLE)	50	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$ (READ CYCLE)	70	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	-	ns	
t_{AH}	Column Address Hold Time referenced to $\overline{RAS}$ Rise	5	-	ns	17
t_{CWL}	Write Command to $\overline{CS}$ Lead Time	20	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC511002BP/BJ/BZ/BFT-60 MIN.	MAX.	UNITS	NOTES
t_{LWAD}	Last Write to Column Address Delay Time	20	25	ns	16
t_{AHLW}	Last Write to Column Address Hold Time	55	-	ns	
t_{RCS}	Read Command Set-up Time referenced to $\overline{CS}$	0	-	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CS}$	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	-	ns	
t_{WP}	Write Command Pulse Width	10	-	ns	
t_{WI}	Write Command Inactive Time	10	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	ns	12
t_{DH}	Data-In Hold Time	15	-	ns	12
t_{DHR}	Data-In Hold Time referenced to $\overline{RAS}$	50	-	ns	
t_{REF}	Refresh Period	-	8	ms	
t_{WCS}	Write Command Set-UP Time	0	-	ns	13
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time	20	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	60	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	30	-	ns	13
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$)	5	-	ns	
t_{CHR}	$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$)	15	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	0	-	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test)	30	-	ns	
t_{TES}	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	-	ns	
t_{TEHR}	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	-	ns	
t_{TEHC}	Test Mode Enable Hold Time referenced to $\overline{CS}$	0	-	ns	

CAPACITANCE (VCC = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

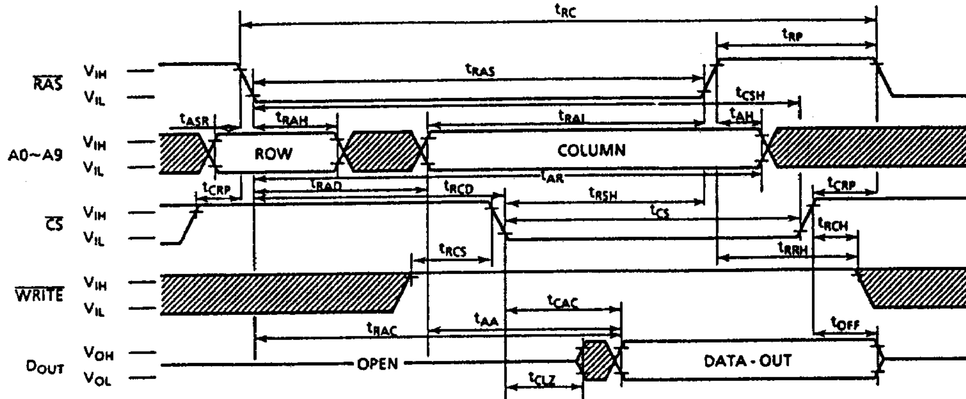
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$, TF)	-	7	
C_O	Output Capacitance (D_{OUT})	-	7	

NOTES:

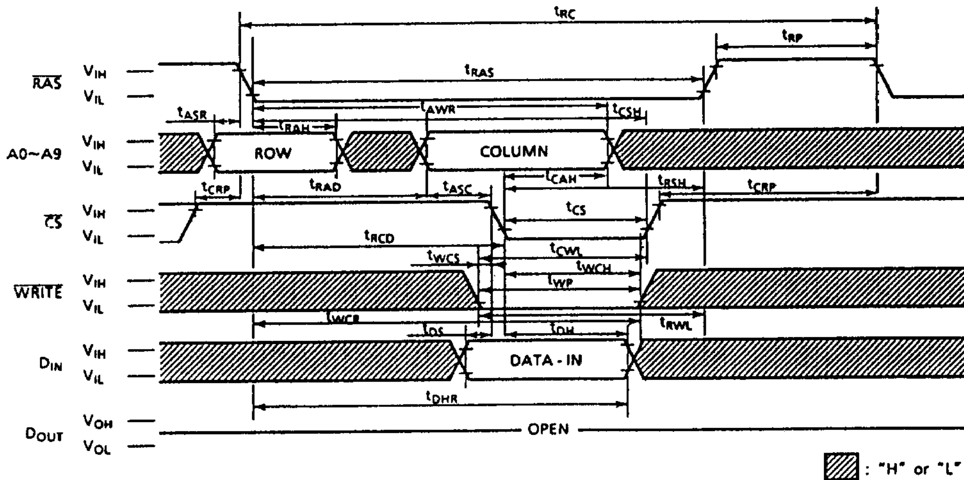
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less While $\overline{RAS}=V_{IL}$.
6. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T=5$ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (min.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
16. Operation within the t_{LWAD}(max.) limit insures that t_{ALW}(max.) can be met.
    t_{LWAD}(max.) is specified as a reference point only: If t_{LWAD} is greater than the specified t_{LWAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
17. t_{AH} is the condition to latch column address when $\overline{RAS}$ has risen up.

TIMING WAVEFORMS

READ CYCLE

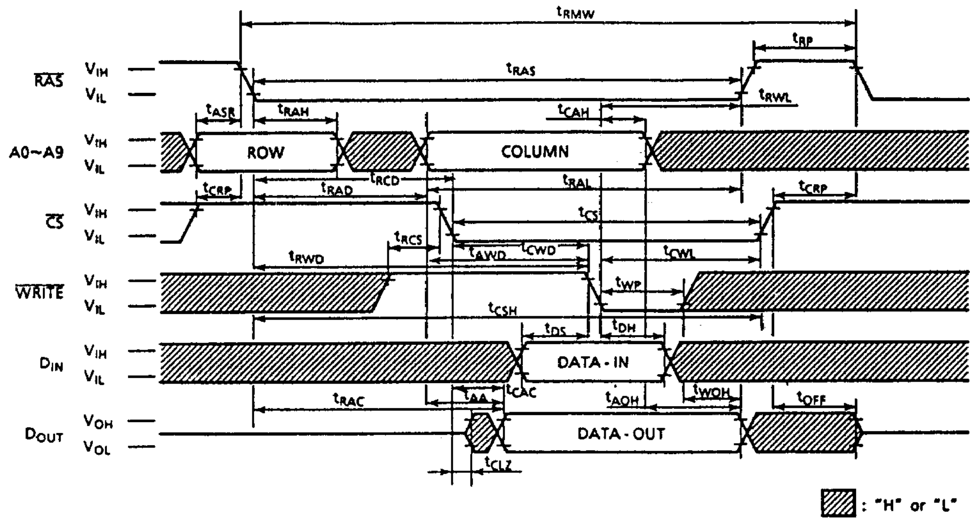


WRITE CYCLE (EARLY WRITE)



Note: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

READ-MODIFY-WRITE CYCLE



Note: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

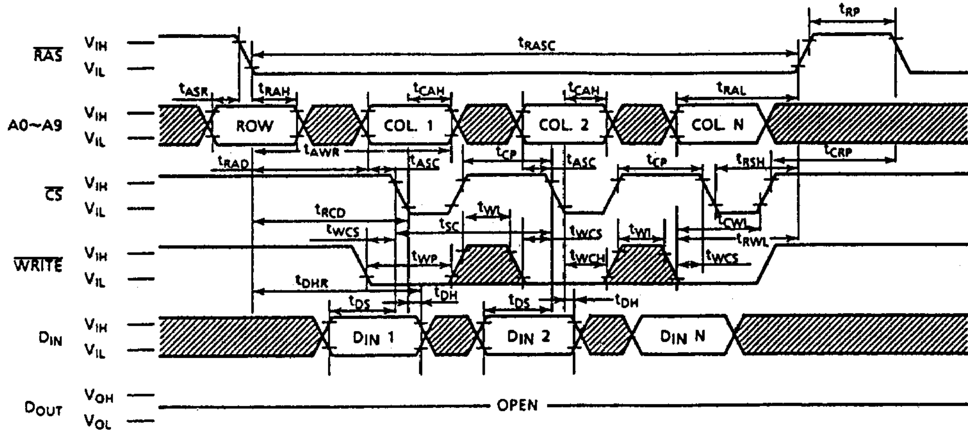
STATIC COLUMN MODE READ CYCLE

RAS VIH VIL
tRASC tRP tASR tRAH tSC tSC tRAL tAH
A0~A9 VIH VIL ROW COL. 1 COL. 2 COL. N
tRAD tAR tCP tRSH tCRP
CS VIH VIL
tCSC tCSC tRCS tRCH tRRH tRCD tCSH tRCS tRCH
WRITE VIH VIL
tCAC tAA tAA tAA tOFF tCAC tAOH tOFF tRAC
DOUT VOH VOL DOUT 1 DOUT 2 DOUT N
tCLZ tCLZ

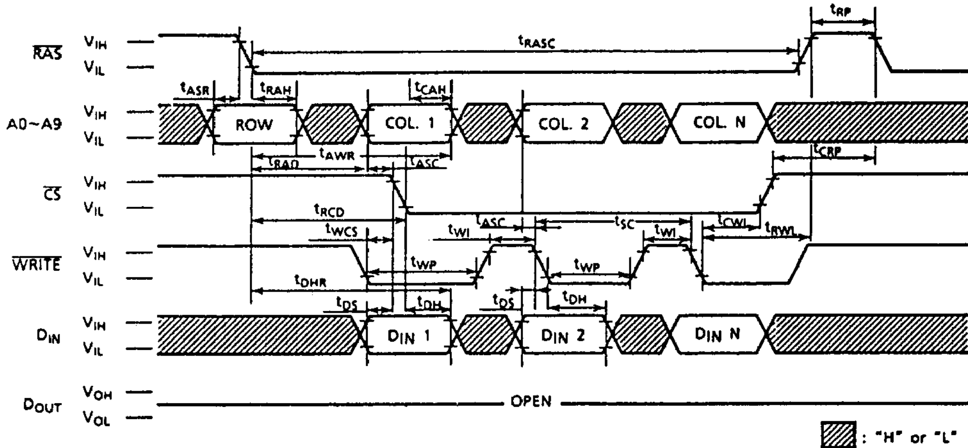
: "H" or "L"

Note: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



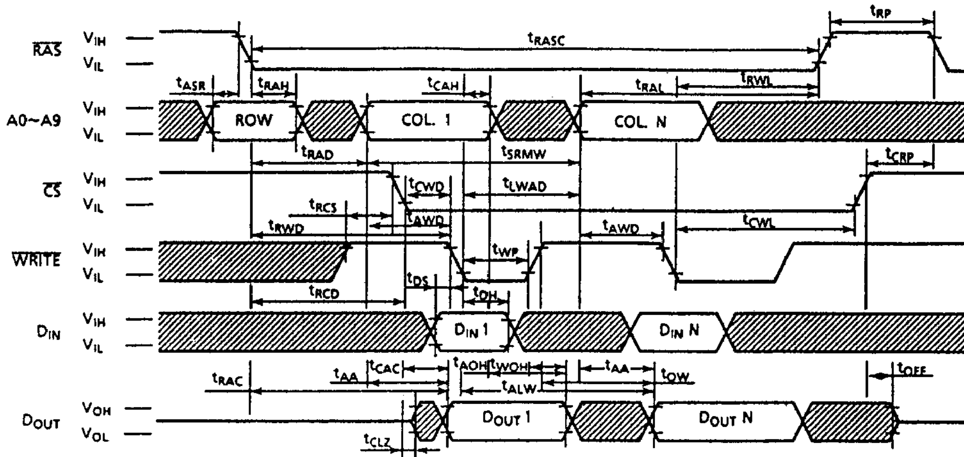
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



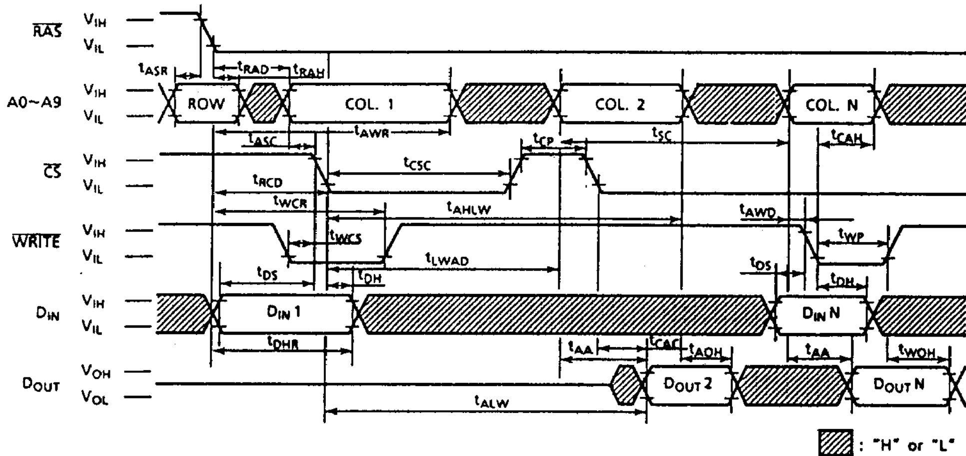
: "H" or "L"

Note: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE

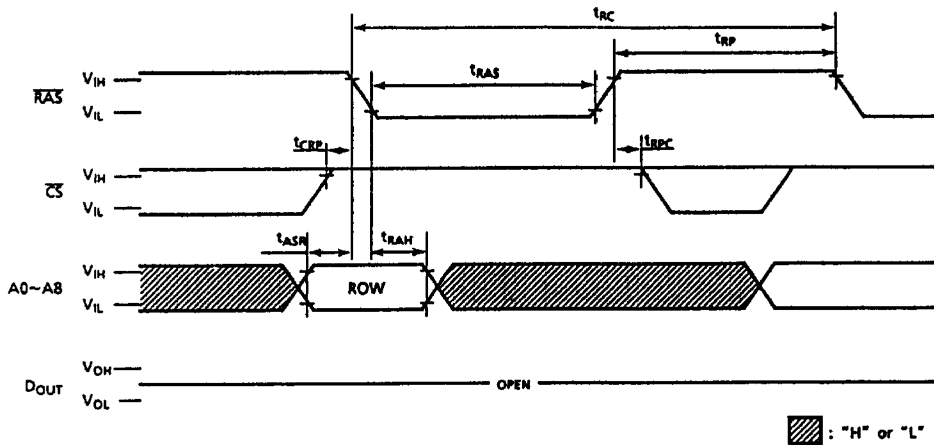


STATIC COLUMN MODE READ/WRITE MIXED CYCLE



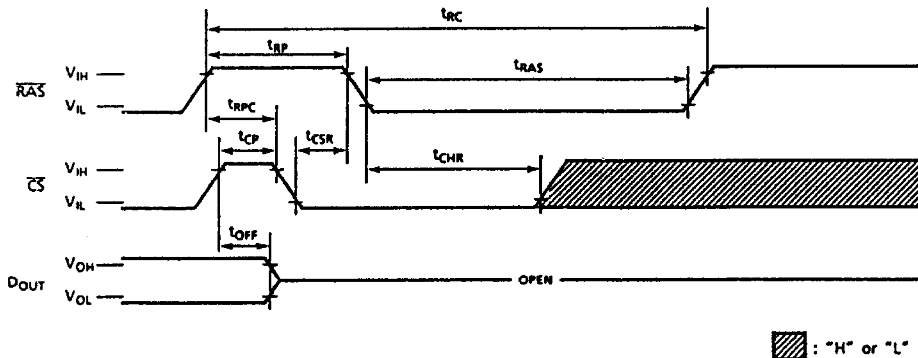
Note: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

RAS ONLY REFRESH CYCLE



Note: $\overline{WRITE}$ = "H" or "L", A9 = "H" or "L"

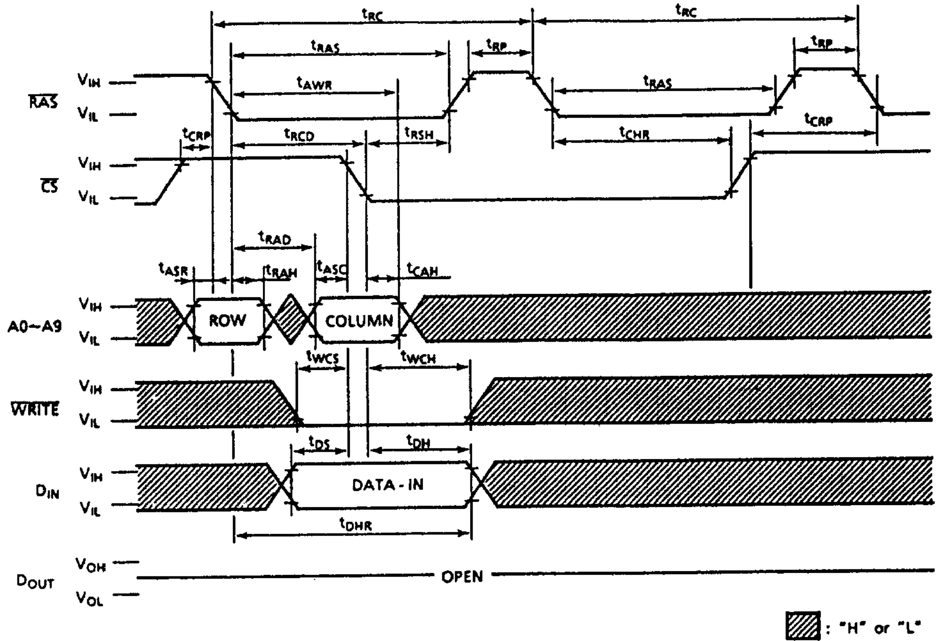
$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: $\overline{WRITE}$ = "H" or "L", A0~A9 = "H" or "L"
"TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

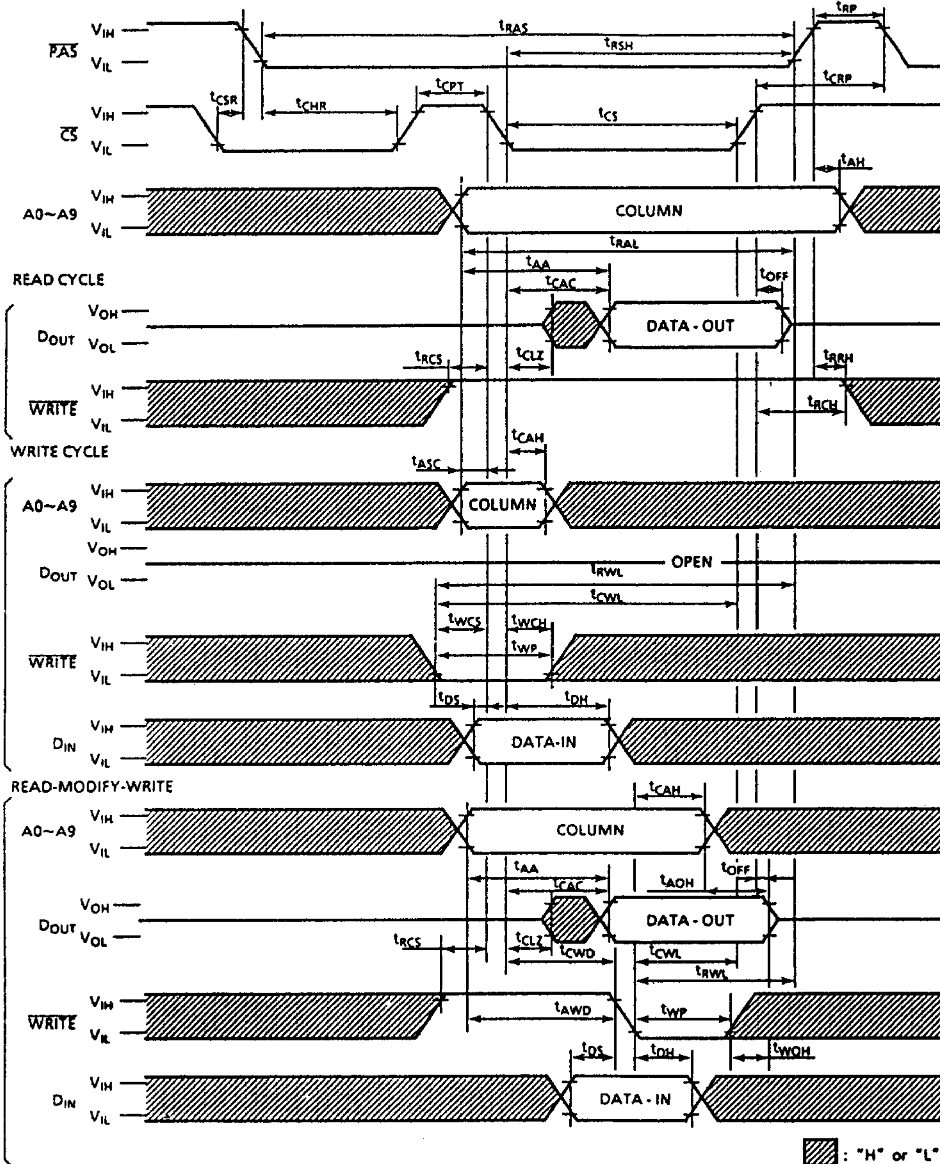
HIDDEN REFRESH CYCLE (READ)

HIDDEN REFRESH CYCLE (WRITE)



Note: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



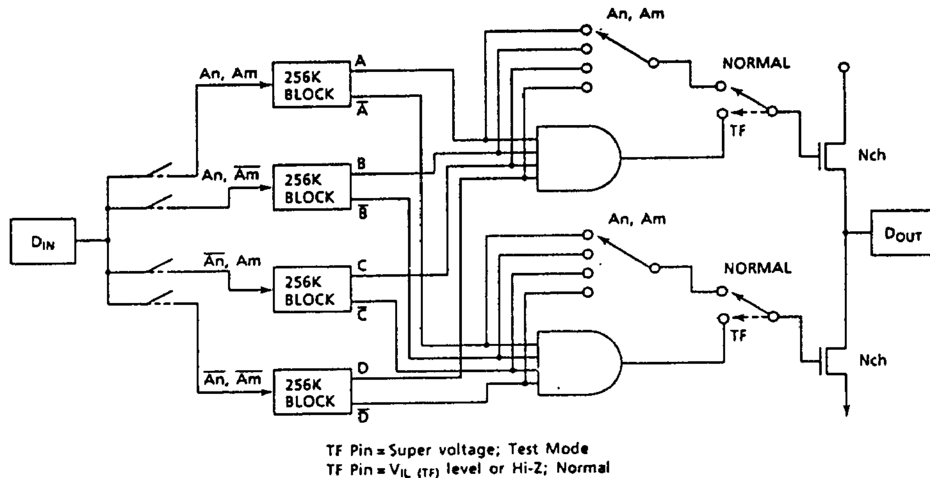
Note: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

TEST MODE

The TC511002BP/BJ/BZ/BFT is the RAM organized 1,048,576 words by 1 bit, it is internally organized 262,144 words by 4 bits. In "Test Mode", data is written into a number of sectors (4 sectors) in parallel and retrieved the same way. If, upon reading, all bits are equal (all "H" or "L"), the data output pin indicates a same data as all bits. In this case, the data output pin indicates an expected data for good parts, the data output pin indicates a complementary data for bad parts. And also, if any of the bits differed, the data output pin would indicate a high impedance state for bad parts. Fig. 1 shows the block diagram of TC511002BP/BJ/BZ/BFT including its truth table when "Test Mode" is used.

In test mode, 1MDRAM can be tested as if it were 256K DRAM by the following method.

Block Diagram in Test Mode



Truth Table in Test Mode Function

A	B	C	D	DOUT
0	0	0	0	0
1	1	1	1	1
Otherwise				Hi - Z

Fig. 1

"Test Mode" function is performed on any of the timing cycles including Static Column Mode when "TF" pin is held on "super voltage (V_{CC} + 4.5V (V_{CC} = 5V ± 10%), max. voltage = 10.5V)" for the specified period (t_{TES}, t_{TEHR} and t_{TEHC}; see Fig. 2). The address input of A9 is ignored in the "Test Mode".

On the other hand, normal operation requires the "TF" pin be connected to $V_{IL\,(TF)}$ level, or left unconnected on the printed wiring board.

The "Test Mode" function reduces test times (1/4; in case of using N test pattern).

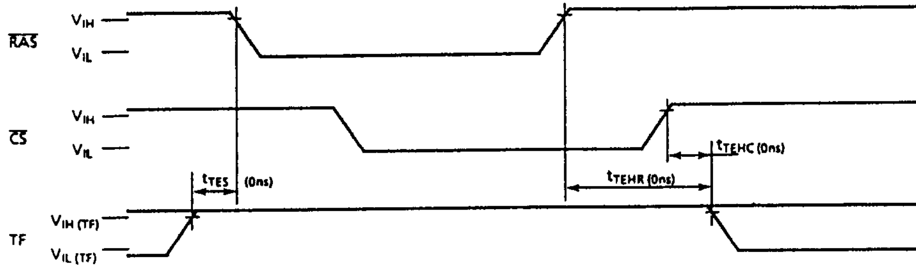


Fig. 2 Test Mode Cycle