DATEL

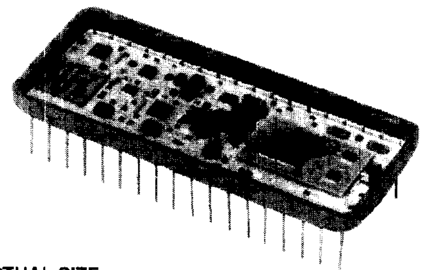
HRD1066
HSD1066

High Quality Bipolar Velocity Pin Programmable Output Resolution Microprocessor Compatible, 16-bit Hybrid **Synchro (Resolver)-to-Digital Converter**

HRD1066
HSD1066

Features

- **Programmable Resolution** (10, 12, 14 or 16-bit)
- **1.3 Arc-minute Accuracy**
- **BIT (Built-In-Test)**
- **Reference Synthesizer**
- **No 180° false lock-up**
- **Analog Velocity Output** (±10V full scale output)
- **3-State Latched Output** (inhibit does not interrupt tracking)
- **Very High Tracking Rate** (1800°/second for high frequency option)
- **High Input Impedance** (solid-state differential input)
- **8- and 16-bit microprocessor compatible**
- **Hermetic 36-pin DDIP package**
- **MIL-STD-883 Processing Available**



ACTUAL SIZE

Applications

Avionics systems
Antenna monitoring
Servo systems
Coordinate conversion
Fire control systems
Axis rotation
Engine controllers
Industrial control systems
Simulation
Robotics
Machine tool control systems
Solar Panel control systems

Description

The **HSD1066 (HRD1066)**, a 10-, 12-, 14-, or 16-bit Programmable Synchro (Resolver)-to-Digital Converter, packaged in a 36-pin DDIP hybrid, offers a high accuracy of ±1.3 arc-minutes, both 8- and 16-bit microprocessor compatibility and excellent dynamic performance. Additional superior features provided in the **Model 1066** include Built-in-Test, anti-180° false lock-up circuit and a reference synthesizer. Requiring a ±15 V-dc main supply and +5 V-dc logic supply for its operation, the converter maintains both static and dynamic accuracy over a wide range of power supply and temperature variations. Unique features include digitally programmable output resolution, providing faster settling/tracking rates with reduced resolution. The **Model 1066** also provides a velocity output signal with a full-scale swing of ±10 V-dc.

Using a high-accuracy differential signal conditioner for the resolver input and a resistive scott-tee for the synchro-input, the converter provides common mode rejection in excess of 70 dB. The input impedance remains constant and balanced independent of dc power to the converter. This feature prevents loading of the synchro and reference input lines when the converter is not powered. This technique also permits resistor programming for non-standard input voltages.

Model 1066 is a Type-II tracking converter with zero velocity lag error. An internal reference synthesizer permits improved dynamic accuracy by reducing the effects of "speed voltages," at high rotational speeds. The accuracy of the converter is maintained with signal-to-reference phase shifts up to ±45 degrees. An anti-180 degree false lock-up circuit is used to assure that the converter does not get locked into an angle 180 degrees from the true angle when a step function of 180 degrees is applied. Transferring data from the **1066** is eased through the use of a transparent latch with three-state outputs configured as two independently enabled 8-bit bytes. Not only does this allow data to be read without interrupting converter tracking, it also permits memory-mapped data interface and control with the most popular 8- and 16-bit microprocessors and single-board computers.

A built-in-test (BIT) feature provides a Logic "0" when the tracking error exceeds ±50 LSBs. Monitoring of converter dynamics is facilitated through the availability of analog signals corresponding to converter tracking velocity and instantaneous tracking error. The analog outputs are "bipolar" outputs which are referenced to power supply Gnd.

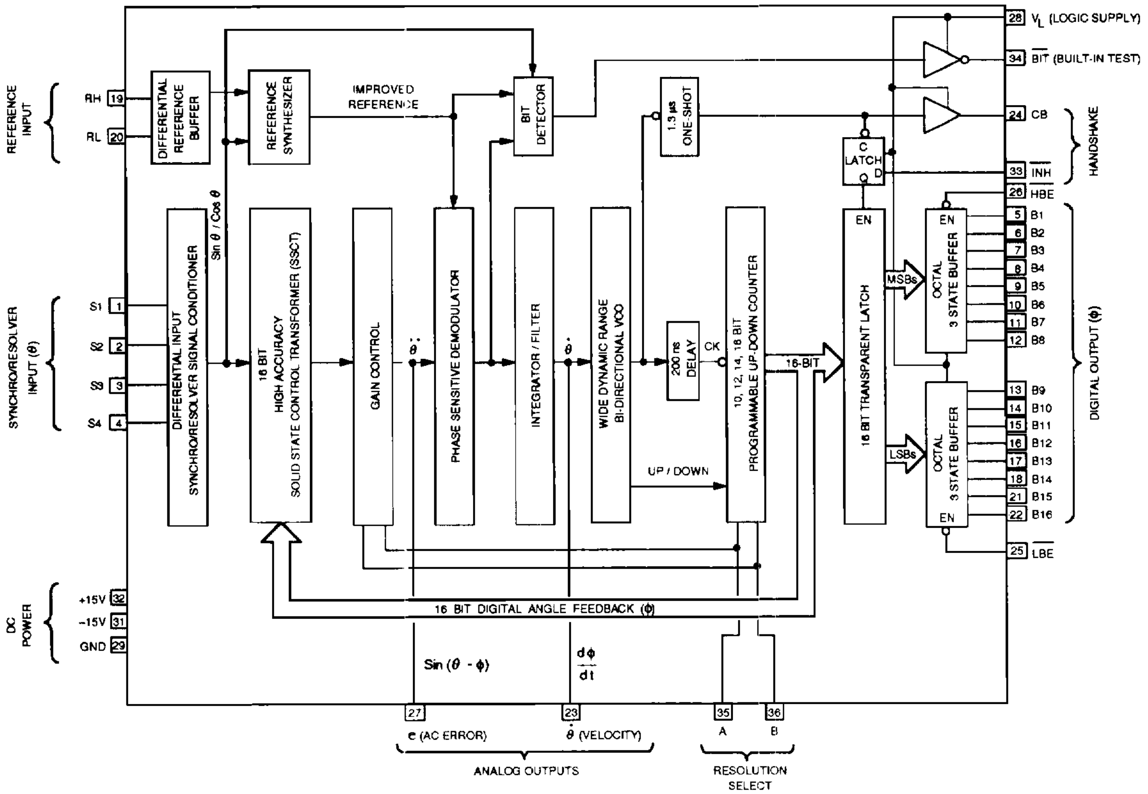


FIGURE 1 1066 Functional Block Diagram

The operation of the **Model 1066** is illustrated in the functional block diagram of Figure 1. The **1066** is a high-gain Type II tracking converter exhibiting zero error for a constant velocity input. The basic conversion process consists of continuously comparing the digital output angle (ϕ) and the synchro (or resolver) input angle (θ). An up-down counter, containing the feed-back angle, is changed (increased or decreased) until the feed-back angle equals the input angle. The input and feed-back signals are combined in a solid state control transformer to obtain an error voltage (e), according to the following trigonometric identity:

$$\text{"e"} = \sin(\theta - \phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

When the error voltage goes to null, sin ($\theta - \phi$) is zero, which makes the angle θ equal to the angle ϕ. Thus, the digital output represents the input shaft angle. Once synchronized, the digital output angle always tracks the input shaft angle without any lag error for constant velocity input.

The input "signal conditioner" accepts either a synchro or a resolver input and converts it into low level signals sin θ and cos θ, which are applied to the "solid state control transformer" (SSCT) discussed above. Output of SSCT goes to "gain control", which adjusts for external programming of converter resolution. The output is applied to a "phase sensitive demodulator" that is used to determine the polarity (phase) of the error signal "e" with respect to reference signal. Instead of using the external reference signal (RH, RL) as applied to the converter, **Model 1066** generates an improved reference internally. The "reference synthesizer" obtains this improved reference from sin θ and cos θ signals and uses the external reference for coarse phase determination only. Use of the improved reference for demodulation allows the **Model 1066** to better reject quadrature components in the error signal "e". The demodulated error signal is applied to an "integrator/filter" which, in addition to ripple and noise filtering, provides the first integration required for the Type II servo loop. The integrator/filter is also used for appropriate gain and phase compensation for loop stability (optimized for low overshoot and fast settling time). The "wide dynamic range bi-directional VCO" performs a voltage-to-frequency conversion whose pulses or counts are accumulated in the "10, 12, 14, 16 bit programmable up-down counter". The up-down counter performs the second integration in the Type II loop. The input to the VCO inherently provides an analog indication of the digital output rate of change (velocity).

The "16-bit transparent latch" provides a means of holding the digital output steady during data transfer, while allowing the converter to continuously track the input angle. The "1.3 µs one shot" provides an output pulse (CB) for every LSB of output change. It is also used as a clock or gate for the inhibit $\overline{\text{INH}}$ "latch" to prevent attempted "data read" commands during an up-down counter output transition. The "200ns delay" is used to prevent a race condition between the CB (Converter Busy) output and $\overline{\text{INH}}$ input.

The "3-state buffer" output is split into two 8-bit bytes to allow interfacing on both 8- and 16-bit data bus systems. The "BIT detector" provides a fault indication as well as help in eliminating false 180 degree digital output readings. The "$\overline{\text{BIT}}$" output provides a logic "0" for fault conditions.

Specifications

PARAMETER	VALUE		REMARKS
Digital Output Resolution			
	10-, 12-, 14- or 16-bits		Programmable
Accuracy			
	± 4.0 arc-minutes (Option S) ±1 LSB ± 2.0 arc-minutes (Option H) ±1 LSB ± 1.0 arc-minutes (Option V) ±1 LSB		Accuracy applies over the full operating temperature range, ±10% frequency variation from nominal and includes hysteresis
Reference Input			
Voltage	4 to 130 V-rms		
Frequency	700 to 3000 Hz (Option 8) 360 to 1000 Hz (Option 4) 47 to 1000 Hz (Option 6)		800 Hz (Nominal) 400 Hz (Nominal) 60 Hz (Nominal)
Input Impedance (Minimum)	250 KΩ Single Ended 500 KΩ Differential		
Common Mode Range	±250 V peak maximum		dc plus recurrent ac peak
Synchro/Resolver Inputs			
Input Voltages (line-to-line)	11.8 V-rms (Option 1) 26.0 V-rms (Option 2) 90.0 V-rms (Option 9)		Accuracy of the converter is maintained with ±10% variation in signal voltages.
Input Impedance (Minimum)	Differential	Line-to-GND	
	60 KΩ 150 KΩ 500 KΩ	30 KΩ 75 KΩ 250 KΩ	11.8 V-rms L-L Models 26.0 V-rms L-L Models 90.0 V-rms L-L Models
Impedance Unbalance	0.2% maximum		For all Models
Common Mode Range	± 25 V peak ± 55 V peak ±180 V peak		11.8 V-rms Models 26.0 V-rms Models 90.0 V-rms Models
Common Mode Rejection Ratio	70 dB minimum		dc to 1000 Hz
Harmonic Distortion	10% maximum		Without degradation in accuracy specification
Digital Inputs			CMOS transient protected
$\overline{INH}$	Logic "1" Logic "0"		Digital output follows analog input signals Output data latched in holding register (Does not interrupt converter tracking loop.)
$\overline{HBE}$	Logic "1" Logic "0"		8 MSBs are in high impedance state of 3-state output 8 MSBs are enabled
$\overline{LBE}$	Logic "1" Logic "0"		8 LSBs are in high impedance state of 3-state output 8 LSBs are enabled
Resolution Select A B	<u>10-bit</u> <u>12-bit</u> <u>14-bit</u> <u>16-bit</u> 0 1 0 1 0 0 1 1		
Voltage Levels Logic "0" Logic "1"	–0.3 V-dc to +0.8 V-dc +2.4 V-dc to +5.0 V-dc		For V_L = 5 V-dc
Input Currents $\overline{INH}$, A, B	–15 µA typical (–30 µA max), pull-up to power supply (V_L)		When not used, may be left unconnected
$\overline{HBE}$, $\overline{LBE}$	+15 µA typical (30 µA max), pull-down to ground (GND)		When not used, may be left unconnected
Digital Outputs			CMOS Outputs
Data Bits (B1-B16)	Natural Binary Angle		Positive logic B1 = 180° B16 = 0.0055°
CB	Logic "0" Logic "1" (Nominal 1.3 µsec pulse for every LSB change)		Output angle not changing Output angle changing (leading edge initiates output change --- see Figure 2.)

PARAMETER	VALUE	REMARKS
Digital Outputs (cont'd.)		**CMOS Outputs**
$\overline{BIT}$	Logic "1" Logic "0"	Digital output tracking analog input Fault indication (tracking error > 50 LSBs typical)
Drive Capability Data Bits (B1-B16), CB, $\overline{BIT}$ "0" Sink Current "1" Source Current	 1 Standard TTL minimum +1.6 mA (min) @ 0.4 V-dc –0.4 mA (min) @ 2.8 V-dc	 For V_L = 4.5 V-dc and over operating temperature range
Hi-Z Output Leakage Data Bits (B1-B16)	±10 µA maximum	Output Capacitance ≈ 5 pf
Analog Outputs	**Typical, unless specified**	**Analog outputs referenced to GND**
e (AC error) mV-rms/LSB	10-bit 12-bit 14-bit 16-bit 50 25 12.5 6.3	 Nominal (for all models)
Drive Capability	±1 mA minimum	All analog outputs
$\dot{\theta}$ (Velocity Output)	**Typical, unless specified**	
Scale Factor (Gain) mV/deg/sec (Nominal)	10-bit 12-bit 14-bit 16-bit 0.087 0.347 1.389 5.556 0.174 0.694 2.778 11.111 0.694 2.778 11.111 44.444	 800 Hz Models 400 Hz Models 60 Hz Models
Scale Factor Tolerance @ 25°C	±15% (±30%) ±10% (±20%) ±10% (±20%)	800 Hz Models (full-temp limits) 400 Hz Models (full-temp limits) 60 Hz Models (full-temp limits)
Full Scale Output Voltage	±10 V-dc	
Linearity @ 25°C	±8% (±15%) of full scale (maximum) ±2% (± 4%) of full scale (maximum) ±1% (± 2%) of full scale (maximum)	800 Hz Models (full-temp limits) 400 Hz Models (full-temp limits) 60 Hz Models (full-temp limits)
Output Offset	± 2 mV-dc typical ±10 mV-dc maximum	Static output voltage
Polarity	Positive output for increasing angle	
ΔGain vs Polarity (Gain Differential)	10% maximum 20% maximum (800 Hz Model)	Between positive and negative outputs (reversal error)
Dynamic Characteristics	**Typical, unless specified**	**Specified for Main Power Supply = ±15 V-dc**
Maximum Tracking Rate Revolutions/Second (minimum)	10-bit 12-bit 14-bit 16-bit 320.0 80.0 20.0 5.000 160.0 40.0 10.0 2.500 40.0 10.0 2.5 .625	 800 Hz Models 400 Hz Models 60 Hz Models
Velocity Constant (K_V)	∞	Type II Servo loop
Acceleration Constant (K_A)	50,000/sec^2 (nominal) 12,500/sec^2 (nominal) 780/sec^2 (nominal)	800 Hz Models 400 Hz Models 60 Hz Models
Setting Time to 1 LSB (for 179 degree step) milliseconds (max.)	10-bit 12-bit 14-bit 16-bit 45 70 110 250 90 135 220 500 400 600 950 2000	 800 Hz Models 400 Hz Models 60 Hz Models
Settling Time to 1 LSB (for <1.4 degree step) milliseconds (max.)	10-bit 12-bit 14-bit 16-bit 30 40 45 50 60 80 90 100 270 360 400 450	 800 Hz Models 400 Hz Models 60 Hz Models
Converter Bandwidth	108 Hz typical 54 Hz typical 14 Hz typical	800 Hz Models 400 Hz Models 60 Hz Models
Reference Synthesizer		
Phase-shift allowed between Input signals and Input reference	± 45° guaranteed ± 65° typical	Without any degradation of converter accuracy

PARAMETER	VALUE	REMARKS
Power Supplies		
Main Power Supply (±15V)		
Voltage	13.5 V-dc to 16.5 V-dc	Without any degradation of converter accuracy
Current (+15V) (−15V)	12 mA typical, 20 mA maximum 10 mA typical, 15 mA maximum	
Logic Power Supply (V_L)		
Voltage	4.5 V-dc to 5.5 V-dc	
Current	3 mA maximum	For V_L = 5 V-dc
Thermal Characteristics		
Junction Temperature Rise Above Case	4°C typical, 10°C maximum	For component with highest temperature rise
Case Temperature Rise Above Ambient	10°C typical, 20°C maximum	Without any heat sink
Power Dissipation	345 mW typical, 540 mW maximum	For V_L = 5 V-dc and Main Power Supply = ±15 V-dc
Physical Characteristics		
Type	36 PIN Hermetic Double DIP	
Size	0.78 x 1.9 x 0.21 inch (20 x 48 x 5.3 mm)	3 Standoffs are added to the package to insulate it from printed circuit board traces (Standoffs included in 0.21 inch height dimension).
Weight	0.6 oz (17 g.) maximum	

Absolute Maximum Ratings

Signal Inputs .... Twice Normal Voltage
Reference Input .... 200 V-rms
Main Power Supply (±15V) .... ±18 V-dc
Logic Voltage (V_L) .... −0.3 V-dc to +6.5 V-dc
Digital Inputs .... − 0.3 V-dc to V_L
Storage Temperature .... − 65°C to +135°C

When installing or removing the converter from printed circuit boards or sockets, it is recommended that the power supplies and input signals be turned off. Decoupling capacitors are recommended on the main power supply (±15V) as well as logic voltage (V_L). A 1µF tantalum capacitor in parallel with 0.01 µF ceramic capacitor should be mounted as close to the supply pins (28, 31 and 32) as possible.

Velocity Output

The Model **1066** is a True "Dual Supply" (±15 V-dc) type S/D converter, using +5 V-dc for digital I/O only. All internal analog circuits are referenced to power supply ground (GND), including the AC error and Velocity Output signals. No internal analog "level shifting" is used on the Velocity Output (or AC error out), resulting in very low output DC offset and excellent power supply rejection ratio.

The full scale velocity output level is ±10 V-dc at the specified maximum tracking rate, (which depends on the model and resolution setting ... specifications are on page 4). The output polarity is positive for increasing angle and negative for decreasing angle. The output can sink or source 1 mA-dc minimum (10K load). If a ±10 V-dc velocity output swing (with respect to Gnd) is not a necessity, see **Model HSRD1056** .

Programmable Output Resolution

A unique feature of the model **1066** is the programmable output resolution control. One of four possible operating modes can be selected: 10, 12, 14, or 16-bit. The resolution control function allows a single converter to be "programmed" for an optimum compromise between converter tracking rate/settling time and output accuracy. The output resolution is controlled by two TTL/CMOS compatible inputs (labeled A and B).

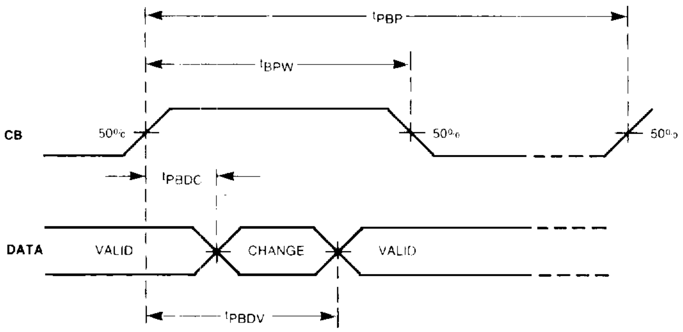
For the best converter accuracy, select the highest resolution allowable which will meet the required tracking rate and/or large signal settling time requirements. If required, the output resolution can be changed "on the fly", allowing the converter to be optimized for varying modes of operating conditions. (Low resolution during large angle changes and high resolution during smaller changes.)

It should be noted that the converter "Bandwidth" and "K_A" will not change with different output resolution selected. It remains constant from 10-bit to 16-bit mode. If higher bandwidth and/or K_A is required, see **Model HSRD1056.**

Digital I/O Characteristics and Timing

$T_a = 25°C$ $R_L = 200\ k\Omega$ Input $t_r\ t_f = 20\ ns$ $V_L = 5\ V\text{-}dc$ $C_L = 50\ pF$

CHARACTERISTIC	LIMITS MIN	TYP	MAX	UNITS	FIGURE
BUSY PULSE WIDTH (t_{BPW})	0.8	1.3	2.0	µs	2
BUSY PERIOD (t_{PBP})	2.0	NOTE 1	∞	µs	2
BUSY TO DATA CHANGE (t_{PBDC})	100	500	—	ns	2
BUSY TO DATA VALID (t_{PBDV})	—	600	800	ns	2
INHIBIT TO DATA STABLE (t_{PIDS})	0	—	1.0	µs	3,4
INHIBIT TO DATA UP-DATE (t_{PIDU})	100	—	—	ns	3,4
INHIBIT UPDATE PULSE WIDTH (t_{IPW})	2.0	—	—	µs	4
HIGH Z TO LOW Z (t_{PHZL})	30	150	250	ns	5
LOW Z TO HIGH Z (t_{PLZH})	30	100	200	ns	5
TRANSITION HIGH TO LOW (t_{THL}) 90%-10%	—	45	75	ns	6
TRANSISTION LOW TO HIGH (t_{LHT}) TTL 10%-50%	—	60	100	ns	6
(t_{TLH}) CMOS 10%-90%	—	120	200	ns	



NOTE 1: Busy Period (t_{PBP}) $= \dfrac{K \cdot 10^6}{2^N \cdot R}$ (μs)

For Reference

Busy Frequency $= \dfrac{2^N \cdot R}{K}$ (Hz)

Rate (R) $= \dfrac{K \cdot \text{Busy Frequency}}{2^N}$

Where

N = Converter Resolution (10, 12, 14 or 16)

K = 360 (For Degrees) or = 2π (For Radians) and

R = Rate (Degrees / Second) or = Rate (Radians / Second)

FIGURE 2 Converter Busy and Data Timing

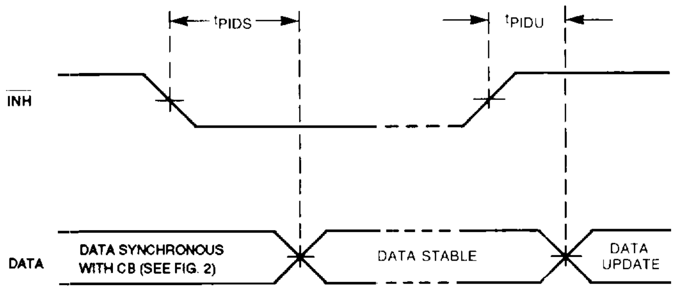


FIGURE 3 Inhibiting Output Data Update

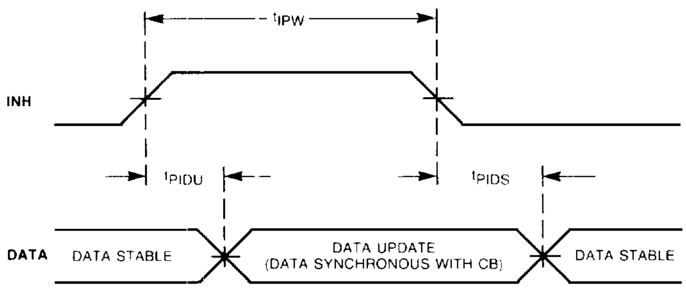


FIGURE 4 Enabling Output Data Update

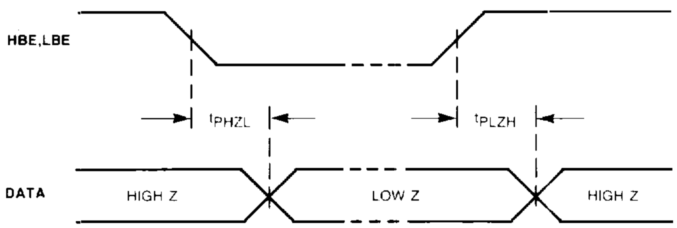


FIGURE 5 3-State Output Timing

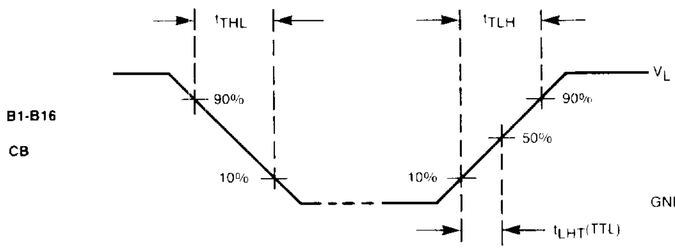


FIGURE 6 Transition Times

Transfer Function

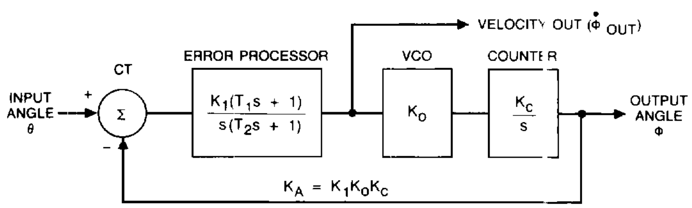


FIGURE 7 Detailed Transfer Function Model

POSITION GAIN (OPEN LOOP) $\dfrac{\Phi_{OUT}}{\theta_{IN}} = \dfrac{K_A(T_1 s + 1)}{s^2(T_2 s + 1)}$

POSITION GAIN (CLOSED LOOP) $\dfrac{\Phi_{OUT}}{\theta_{IN}} = \dfrac{T_1 s + 1}{\dfrac{T_2 s^3}{K_A} + \dfrac{s^2}{K_A} + T_1 s + 1}$

VELOCITY GAIN (OPEN LOOP) $\dfrac{\dot{\Phi}_{OUT}}{\theta_{IN}} = \dfrac{K_1(T_1 s + 1)}{s(T_2 s + 1)}$

VELOCITY GAIN (CLOSED LOOP) $\dfrac{\dot{\Phi}_{OUT}}{\theta_{IN}} = \dfrac{T_1 s^2 + s}{\dfrac{T_2 s^3}{K_1} + \dfrac{s^2}{K_1} + T_1 K_O K_C s + K_O K_C}$

Transfer Function Parameters

PARAMETER	UNITS	60 Hz OPTION				400 Hz OPTION				800 Hz OPTION			
		RESOLUTION MODE				RESOLUTION MODE				RESOLUTION MODE			
		10 BIT	12 BIT	14 BIT	16 BIT	10 BIT	12 BIT	14 BIT	16 BIT	10 BIT	12 BIT	14 BIT	16 BIT
K_A	sec^{-2}	780	780	780	780	12,500	12,500	12,500	12,500	50,000	50,000	50,000	50,000
K_O	$\frac{Counts}{Volt \cdot Sec}$	4,096	4,096	4,096	4,096	16,384	16,384	16,384	16,384	32,768	32,768	32,768	32,768
K_C	$\frac{Radians}{Count}$	6.136×10^{-3}	1.534×10^{-3}	3.835×10^{-4}	9.587×10^{-5}	6.136×10^{-3}	1.534×10^{-3}	3.835×10^{-4}	9.587×10^{-5}	6.136×10^{-3}	1.534×10^{-3}	3.835×10^{-4}	9.587×10^{-5}
K_1	$\frac{Volts}{Radians \cdot Sec}$	31.0	124	497	1,986	124	497	1,989	7,958	249	995	3,979	15,915
T_1	ms	80	80	80	80	20	20	20	20	10	10	10	10
T_2	ms	8	8	8	8	2	2	2	2	1	1	1	1
K_OK_C	$\frac{Radians}{Volt \cdot Sec}$	25.13	6.283	1.571	0.3927	100.5	25.13	6.283	1.571	201.1	50.27	12.57	3.142

FIGURE 8 Transfer Function Parameters (Typical Values)

Pin Designations

+15V, −15V — Main Power Supply –
±15 V-dc ±10%

V_L — Logic Voltage –
5 V-dc ±10%

GND — Power Supply Ground, Digital Ground

B1-B16 — Parallel Output Data Bits –

B1 is MSB. Bit weight = 180 degrees
B16 is LSB. Bit weight = 0.0055 degrees

S1, S2, S3, S4 — Input Analog Signals –
Leave S4 unconnected for synchro-input

RH, RL — Reference Voltage Input

$\overline{BIT}$ — Built-in-Test –
A Logic "low" indicates that output is not tracking the input analog signal within ±50 LSB's nominal

e — Unfiltered ac null error –

$\dot{\theta}$ — Velocity Output –
dc analog voltage proportional to rotational speed of the input shaft angle.

A, B — Resolution Select –

	A	B
10 Bit	0	0
12 Bit	1	0
14 Bit	0	1
16 Bit	1	1

$\overline{INH}$ — Inhibit Function –
A logic "low" freezes the digital angular output. Internal loop keeps tracking the analog input. All other outputs keep following the input. For continuous operation this pin may be left unconnected. Internal active pull-up will apply V_L to the pin.

S1	1	36	B
S2	2	35	A
S3	3	34	$\overline{BIT}$
S4	4	33	$\overline{INH}$
B1	5	32	+15V
B2	6	31	−15V
B3	7	30	NC
B4	8	29	GND
B5	9	28	V_L
B6	10	27	e
B7	11	26	$\overline{HBE}$
B8	12	25	$\overline{LBE}$
B9	13	24	CB
B10	14	23	$\dot{\theta}$
B11	15	22	B16
B12	16	21	B15
B13	17	20	RL
B14	18	19	RH

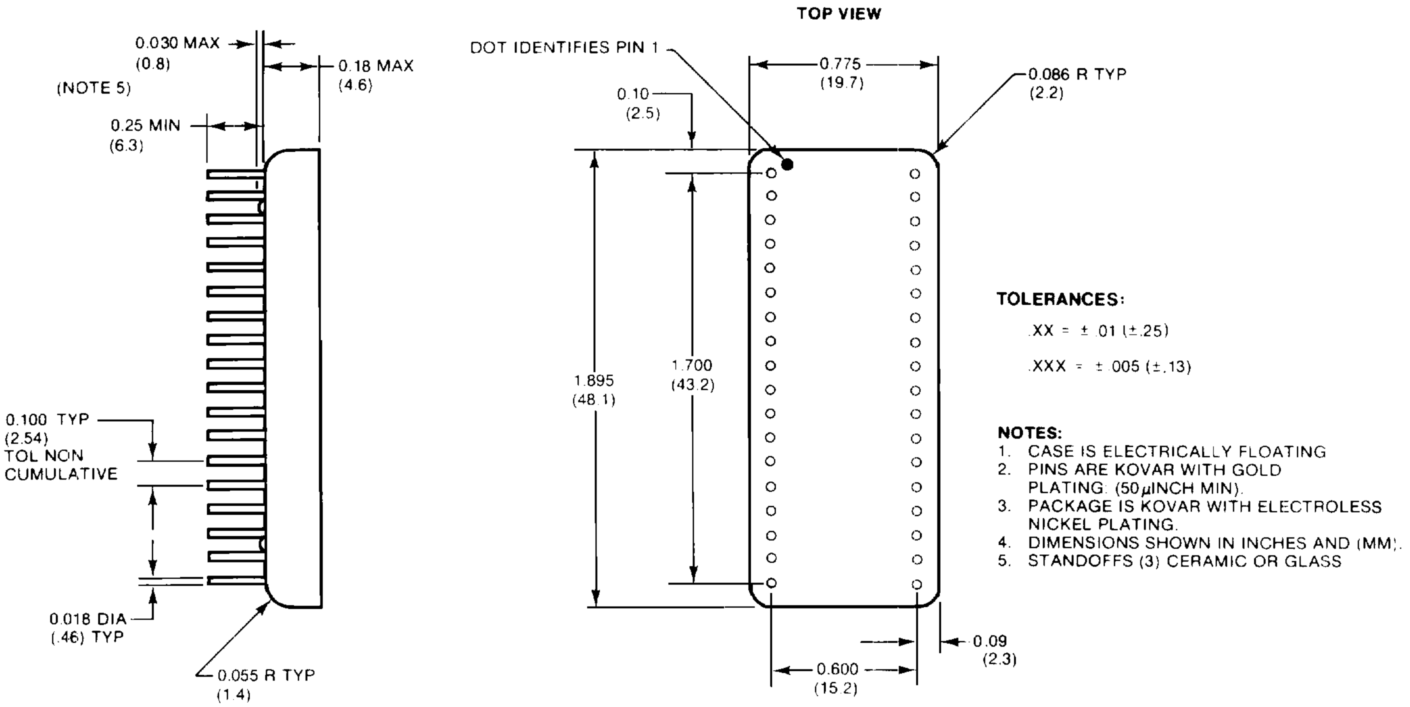
FIGURE 9 HSD1066/HRD1066 Pin Assignments

CB — Converter Busy –
A 1.3 us pulse which occurs during each converter update. Output data can be transferred at the trailing edge of the CB pulse. When the converter output is not changing CB is at logic "low."

$\overline{HBE}$ — High Byte Enable –
Data bits B1 through B8 are enabled (low-impedance state of 3-state output) when $\overline{HBE}$ is set to a logic "low." When $\overline{HBE}$ is set to a logic "high," the data bits B1 through B8 are disabled (high-impedance state of 3-state output).

$\overline{LBE}$ — Low Byte Enable –
Data bits B9 through B16 are enabled when $\overline{LBE}$ is set to a logic "low." When $\overline{LBE}$ is set to a logic "high," the data bits B9 through B16 are disabled.

Note: For continuous 16-bit parallel output $\overline{HBE}$ and LBE may be left open. Internal active pulldown to ground will apply logic "low" to these pins thus enabling all data bits B1 through B16.



MECHANICAL OUTLINE (36 PIN DOUBLE DIP)

Ordering Information

HSD1066 - T F I A

Temperature Range (T)
- 1 = 0° C to + 70° C
- 2 = –25° C to + 85° C
- 3 = –55° C to + 125° C

Frequency (F)
- 4 = 400 Hz
- 6 = 60 Hz
- 8 = 800 Hz

Input Signal (I)
- 1 = 11.8 V-rms
- 2 = 26 V-rms
- 9 = 90 V-rms
- 0 = Ext. Signal XFMRS
- 5 = Ext. Signal and Reference XFMRS

Accuracy (±1 LSB) (A)
- S = 4 arc-minutes
- H = 2 arc-minutes
- V = 1 arc-minutes

SPECIFY HRD1066 FOR RESOLVER INPUT

MIL-STD-883 COMPLIANT HYBRIDS AVAILABLE
Contact Natel Engineering for Delivery

Other products available from NATEL

- **3 arc-second accurate**, Programmable Dynamic Angle Simulator that includes 4 Related Instruments and is totally A.T.E. Programmable (L200).
- Hybrid (36-pin DDIP size) Synchro(Resolver)-to-Digital converters that operate from a **single +5V power supply** and offer excellent features such as BIT, AGC, low power dissipation and more (Models 1006, 1056, 1046 and 1044).
- 1.3 arc-minute accuracy, high power, Digital-to-Synchro converters that **do not require any DC power supplies** (Models 5031 and 5131).
- 1-inch square, **single +5V powered**, 16-bit R/D converter with built-in **Reference Oscillator** (HRD1416).
- **2-channel** Digital-to-Sin/Cos Converter in a single 36-pin hybrid (HDSC2036).
- **2-speed**, 22-Bit Synchro(Resolver)-to-Digital Converter, 0.0004° accuracy in a single 40-pin TDIP (HRD/HSD1626).
- **3-channel** Resolver-to-Digital Converter in a single 40-pin TDIP (HRD1346).
- Resolver Control Differential Transmitter in a single 36-pin package (HCDX3106).

A wide range of applications assistance is available from Natel. Application notes can be requested when available . . . and Natel's applications engineers are at your disposal for solving specific problems.

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