ADM7008/X

8-port 10/100 PHY controller

Communications

Never stop thinking.

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Previous Version:

Page/Date	Subjects (major changes since last revision)
2003-01-23	Rev. 1.0, First release of ADM7008
2003-10-28	Rev. 1.1, Updated Chapters 2, 3, 4
2003-11-27	Rev. 1.2, Updated Chapter 2
2005-09-12	Rev. 1.21 when changed to the new Infineon format
2005-11-28	Minor change. Included Green package information

Trademarks

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1 Product Overview

Features and Block Diagram.

1.1 Overview

The ADM7008/X is a single chip eight port 10/100M PHY, which is designed for today's low cost and low power dual speed application. The ADM7008X is the environmentally friendly "green" package version.

It supports eight auto sensing 10/100 Mbit/s ports with on-chip clock recovery and base line wander correction including integrated MLT-3 functionality for 100 Mbit/s operation. It also supports Manchester Code Converter with on chip clock recovery circuitry for 10 Mbit/s functionality, provides Reduced MII (RMII), Serial MII (SMII) and Source Synchronous MII (SS_SMII) interface to facilitate high port count switch system application and reduce the pin number simultaneously.

For today's Information Application (IA), ADM7008/X also supports "Auto Cross Over Detection" function to eliminate the technical barrier between networking and the end user. With the aid of this auto cross over detection function, Plug-n-Play features can be easily applied to IA relative products.

The major design goal for ADM7008/X is to reduce the power consumption and system radiation for the whole system. With the aid of this low power consumption and low radiation chip, fan and on-system power supply can be removed to save the total manufacture cost and make SOHO application achievable.

1.1.1 Package Information

Product Name	Product Type	Package	Ordering Number
ADM7008/X	ADM7008/X	P-QFP-128-1	Q67801H 1A[1)]

1) contact Infineon for the updated ordering information.

1.2 Features

Main features:

- IEEE 802.3 compatible (2000 edition) 10Base-T and 100Base-T physical layer interface and ANSI X3.263 TP-PMD compatible transceiver.
- Eight-port, single chip, integrated physical layer and transceivers for 10Base-T and 100BASE-TX function.
- Reduced MII (RMII), Serial MII (SMII) and Source Synchronous MII (SS_SMII) for high port count switch.
- Built-in 10 Mbit transmit filter.
- 10 Mbit PLL, exceeding tolerances for both preamble and data jitter.
- 100 Mbit PLL, combined with the digital adaptive equalizer and performance exceeds 140 meters for UTP 5.
- 125 MHz Clock Generator and Timing Recovery.
- Integrated Base Line Wander Correction.
- Carrier Integrity Monitor function supported.
- Supports Auto Cross Over Detection function for Plug-and-Play.
- IEEE 802.3u Clause 28 compliant auto negotiation for full 10 Mbit/s and 100 Mbit/s control.
- Supports programmable LED for different Switch Application and Power On LED Self Test.
- Supports PECL interface for fiber connection.
- Built-in 3.3 V to 1.8 V Regulator Control Signal.
- Built-in Clock Generator and Power On Reset Signal to save system cost.
- 128 P-QFP with 1.8 V/3.3 V Power Supply.
- Support Power saving function.
- Support Parallel/Serial LED output.

1.3 Block Diagram

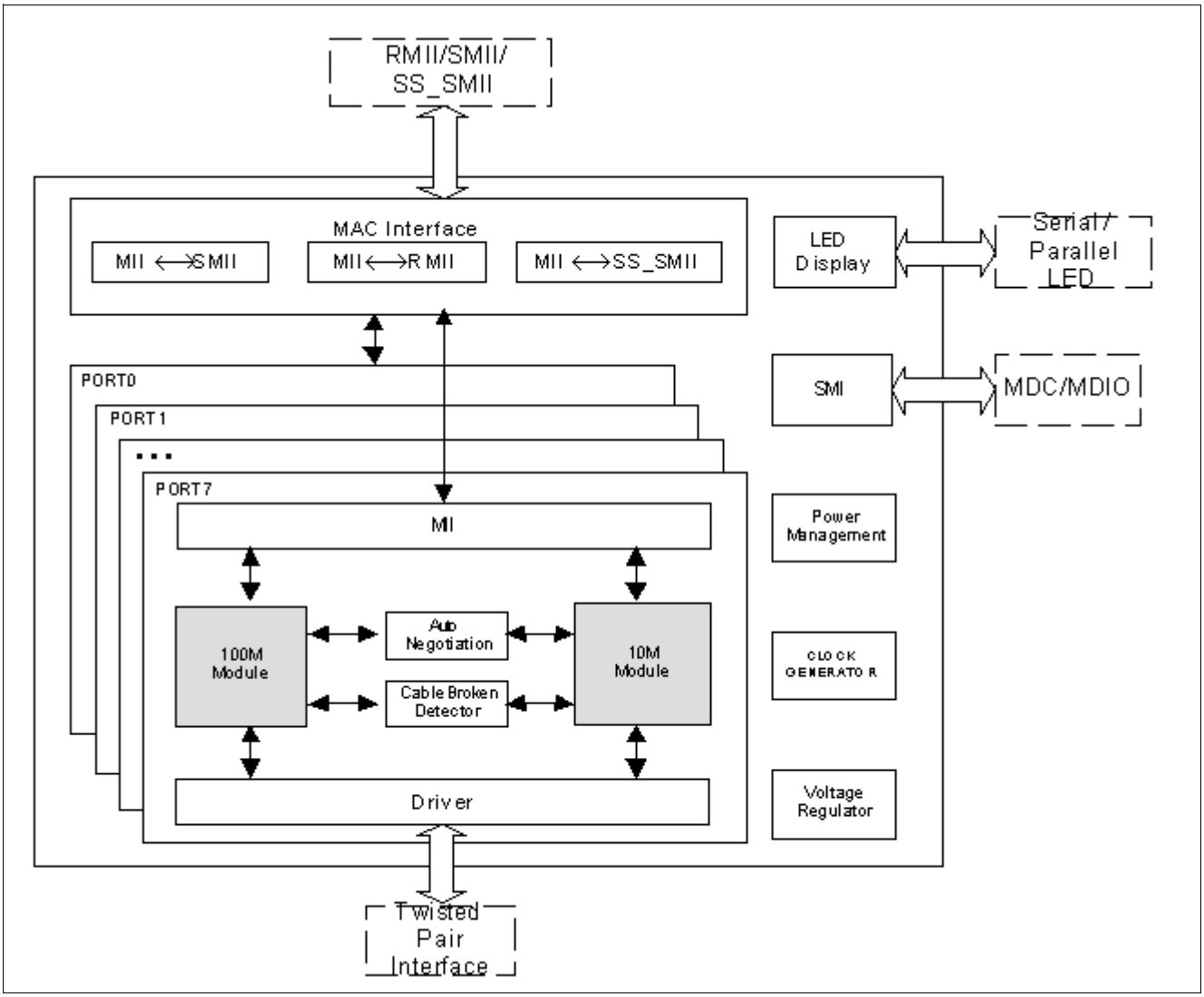


Figure 1 ADM7008/X Block Diagram

2 Interface Description

2.1 Pin Diagram

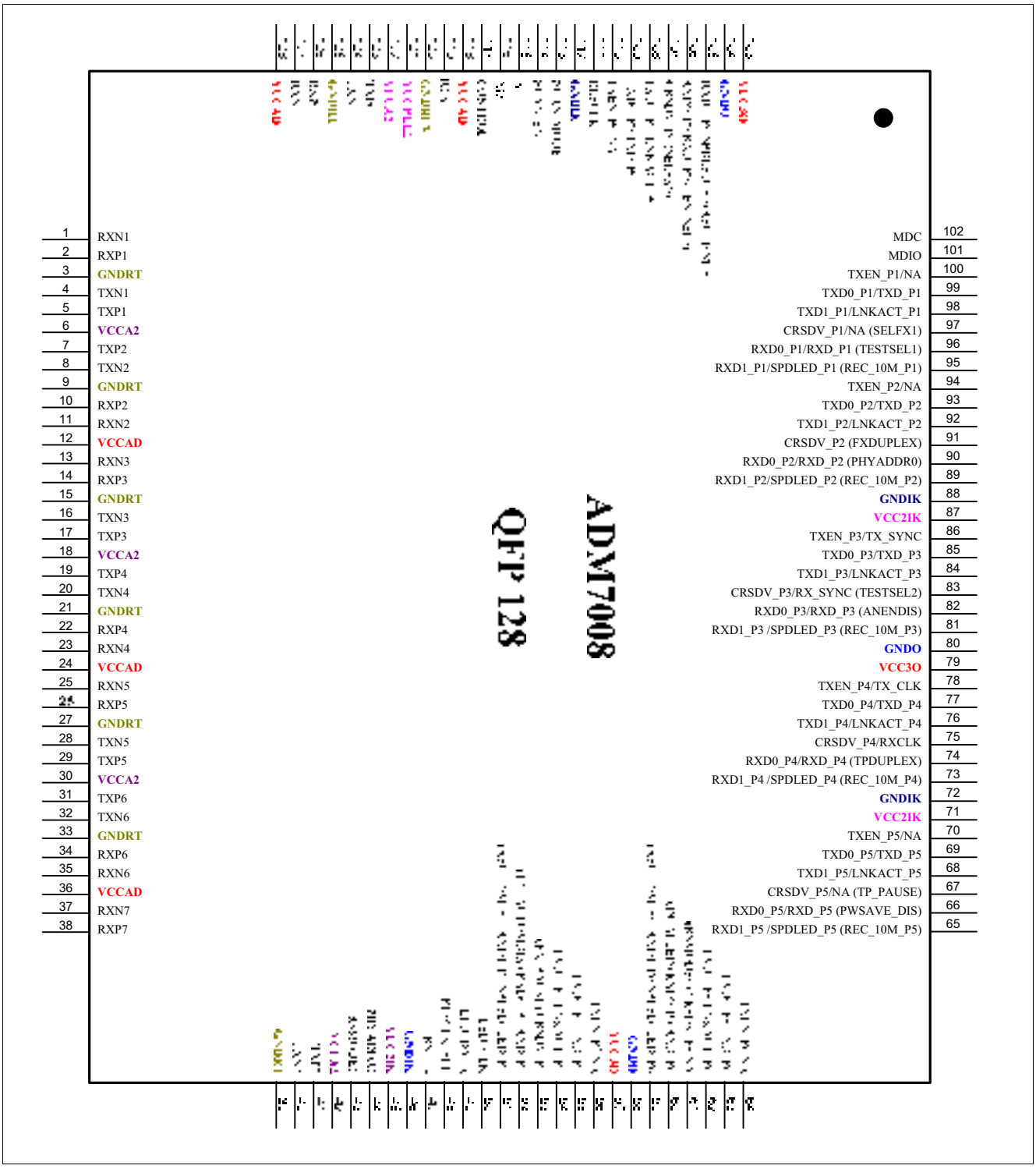


Figure 2 Pin Diagram

2.2 Pin Description

If not specified, all signals are default to digital signals.

Table 1 Abbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or Output. Analog levels.
PWR	Power
GND	Ground
MCL	Must be connected to Low (JEDEC Standard)
MCH	Must be connected to High (JEDEC Standard)
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 2 Abbreviations for Buffer Type

Abbreviations	Description
Z	High impedance
PU1	Pull up, 10 kΩ
PD1	Pull down, 10 kΩ
PD2	Pull down, 20 kΩ
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
OC	Open Collector
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).
OD/PP	Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute.
ST	Schmitt-Trigger characteristics
TTL	TTL characteristics

2.2.1 Twisted Pair Interface, 32 Pins

Table 3 Twisted Pair Interface, 32 Pins

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
123	TXP0	AO		**Twisted Pair Transmit Output Positive 7:0**
5	TXP1			
7	TXP2			
17	TXP3			
19	TXP4			
29	TXP5			
31	TXP6			
41	TXP7			
124	TXN0			**Twisted Pair Transmit Output Negative 7:0**
4	TXN1			
8	TXN2			
16	TXN3			
20	TXN4			
28	TXN5			
32	TXN6			
40	TXN7			
126	RXP0	I		**Twisted Pair Receive Input Positive 7:0**
2	RXP1			
10	RXP2			
14	RXP3			
22	RXP4			
26	RXP5			
34	RXP6			
38	RXP7			
127	RXN0			**Twisted Pair Receive Input Negative 7:0**
1	RXN1			
11	RXN2			
13	RXN3			
23	RXN4			
25	RXN5			
35	RXN6			
37	RXN7			

2.2.2 Ground and Power, 20 Pins

Table 4 Ground and Power, 20 Pins

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
125, 3, 9, 15, 21, 27, 33, 39	GNDRT	A, GND		**Analog Ground Pad**
118, 128, 12, 24, 36	VCCAD	A, PWR		**Analog 3.3 V Power**
122, 6, 18, 30, 42	VCCA2	A, PWR		**Analog 1.8 V Power**
120	GNDRCV	A, GND		**Analog Ground used by Clock Generator Module**
121	VCCPLL2	A, PWR		**Analog 1.8 V Power used by Clock Generator Module**
58, 80, 104	GNDO	D, GND		**Ground used by 3.3 V I/O.**
46, 72, 88, 112	GNDIK	D, GND		**Ground used by Core**
57, 79, 103	VCC3O	D, PWR		**3.3 V Power used by I/O**
45, 71, 87	VCC2IK	D, PWR		**1.8 V Power used by Core**

2.2.3 Mode Setting

Table 5 Mode Setting

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
43	RSMODE1	I	PD	**RMII and SMII/SS_SMII Mode Select Signal** Dedicated input provided by ADM7008/X to determine the interface. 0_B , SMII or SS_SMII interface (See CRSDV_P6 power on setting for more detail) 1_B , RMII interface

2.2.4 Clock Input Select

Table 6 Clock Input Select

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
48	REFCLK_SEL	I	PD	**XI/XO and REFCLK Clock Select Signal** Dedicated input provided by ADM7008/X to determine the clock source for ADM7008/X. *Note: That when RSMODE1 is set to 1 (RMII mode), the input of REFCLK should be 50 MHz; when RSMODE1 is set to 0 (SMII or SS_SMII mode) the clock input on REFCLK should be 125 MHz* 0_B , ADM7008/X will use XI/XO as clock source for internal clock generator. In this mode, REFCLK (pin 111) will output 50 MHz clock in RMII mode (RSMODE1 is set to 1) and 125 MHz clock in either SMII or SS_SMII mode (RSMODE1 is set to 0) 1_B , ADM7008/X will use the input of REFCLK (pin 111) as the clock source for internal clock generator.

2.2.5 Clock Input, 3 Pins

Table 7 Clock Input, 3 pins

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
115	XI	I	CTL	**Crystal Input** 0_B **REFCLK_SEL**, 25M Crystal/Oscillator Input 1_B **REFCLK_SEL**, Leave unconnected
	OSCI			**Oscillator Input**
116	XO	O	CTL	**Crystal Output** When 25M Oscillator is used, this pin should be left unconnected. See XI/OSCI description above.
111	REFCLK	I/O	16 mA LVTTL	**Reference Clock** Function on this pin is highly depended upon the setting on REFCLK_SEL and RSMODE1. REFCLK_SEL RSMODE1 REFCLK (Direction/Frequency) 0 0 Output/125 MHz 0 1 Output/50 MHz 1 0 Input/125 MHz with max 100 ppm 1 1 Input/50 MHz with max 100 ppm

2.2.6 RMII/SMII Interface, 48 Pins

Table 8 RMII/SMII Interface, 48 Pins

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
51	REC_10M_P7	I/O	8 mA, PD/PU	**Power On Setting** REC_10M: Value on RXD1_P7 will be latched by ADM7008/X during power on reset as Port 7 10M Re-command value. 0_B **REC_10M_P70**, Recommend Port 7 to operate in 100M Mode 1_B **REC_10M_P71**, Recommend Port 7 to operate in 10M Mode
	RXD1_P7	I/O	8 mA, PD/PU	**RMII Mode** Port 7: RXD[1] is the port 7 output di-bit synchronously to REFCLK. Upon assertion of CRSDV_P7, RXD0 and RXD1 remain at '00' until valid data is output from the FIFO onto RXD. '01' on RXD1 and RXD0 indicates the start of valid data. If a false carrier or a symbol error is detected, RXD1 and RXD0 are set to '10' for the duration of the activity. Note that in 100Mb /s mode RXD can change once per REFCLK cycle, whereas in 10Mb/s mode RXD must be held steady for 10 consecutive REFCLK cycles.
	SPDLED_P7	I/O	8 mA, PD/PU	**SMII Receive Data** Port 7: RXD0 for the designated port outputs data or in-band management information synchronously to TX_CLK (pin 78). In 100Mb/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10Mbit/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 7.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
52	EN_AUTOMDIX	I/O	8 mA, PD/PU	**Power On Setting: Auto MDIX Enable Signal** Value on RXD0_P7 will be latched by ADM7008/X during power on reset as Auto MDX function control signal 0_B **EN_AUTOMDIX0**, Disable all ports' Auto MDIX function. 1_B **EN_AUTOMDIX1**, Enable all ports' Auto MDIX function.
	RXD0_P7	I/O	8 mA, PD/PU	**RMII: RMII Mode** Port 7: RXD[0] is the port 7 output di-bit synchronously to REFCLK. Upon assertion of CRSDV_P7, RXD0 and RXD1 remain at '00' until valid data is output from the FIFO onto RXD. '01' on RXD1 and RXD0 indicates the start of valid data. If a false carrier or a symbol error is detected, RXD1 and RXD0 are set to '10' for the duration of the activity. Note that in 100 Mbit /s mode RXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode RXD must be held steady for 10 consecutive REF-CLK cycles.
	SMII_RXD_P7	I/O	8 mA, PD/PU	**SMII: SMII Receive Data** Port 7: RXD0 for the designated port outputs data or in-band management information synchronously to TX_CLK (pin 78). In 100Mb/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 7.
	SS_SMII_RXD_P7	I/O	8 mA, PD/PU	**SMII: SS_SMII Receive Data** Port 7 RXD0 for the designated port outputs data or in-band management information synchronously to RXCLK (pin 75). In 100 Mbit/s mode, RXD0 outputs a new 10 bits segment starting with SYNC. In 10Mb/s mode, RXD must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 7.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
53	FX_PAUSE	I	LVTTL, PD	**Power On Setting: Fiber PAUSE Recommend Value** Value on this pin will be latched by ADM7008/X during power on reset as Fiber port (See SELFX power on setting for more detail) pause capability control signal. 0_B **FXP0**, Pause off for all fiber ports 1_B **FXP1**, Pause on for all fiber ports
	CRSDV_P7	O	8 mA	**RMII: Carrier Sense/Receive Data Valid** Port 7. CRSDV_P7 asserts when the receive medium is non-idle. The assertion of CRSDV_P7 is asynchronous to REFCLK. At the de-assertion of carrier, CRSDV_P7 de-asserts synchronously to REFCLK only on the first di-bit of RXD. If there is still data in the FIFO not yet presented onto RXD, then on the second di-bit of RXD, CRSDV_P7 is asserted synchronously to REFCLK. The toggling of CRSDV_P7 on the first and second di-bit continues until all the data in the FIFO is presented onto RXD. CRSDV_P7 is asserted for the duration of carrier activity for a false carrier event.
	N/A	O	8 mA	**SMII/SS_SMII: N/A** Not used in SMII/SS_SMII Mode
54	TXD1_P7	I	TTL, PD	**RMII: RMII Transmit Data[1]** Transmit data for port 7 input the di-bits that re transmitted and are driven synchronously to REFCLK. Note: that in 100 Mbit/s mode, TXD can change once per REFCLK cycle, whereas in 10Mb/s mode, TXD must be held steady for 10 consecutive REFCLK cycles.
	LNKACT_P7	I	TTL, PD	**SMII: Link and Activity LED** See LED Description for more detail.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
55	TXD0_P7	I	TTL, PD	**RMII: RMII Transmit Data[0]** Transmit data for port 7 input the di-bits that re transmitted and are driven synchronously to REFCLK. Note: that in 100 Mbit/s mode, TXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode, TXD must be held steady for 10 consecutive REFCLK cycles.
	SMII_TXD_P7	I	TTL, PD	**SMII: SMII Transmit Data** Inputs the data that is transmitted and is driven synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, TXD0 inputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, TXD0 must repeat each 10-bit segment 10 times. TXD1_P7 acts as Port 7 Link/Activity LED in both SMII and SS_SMII Mode.
	SS_SMII_TXD_P7	I	TTL, PD	**SMII: SS_SMII Transmit Data** Inputs the data that is transmitted and is driven synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, TXD0 inputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, TXD0 must repeat each 10-bit segment 10 times.
56	TXEN_P7	I	TTL	**RMII: Transmit Enable** Transmit Enable for port 7 indicates that the di-bit on TXD is valid and it is driven synchronously to REFCLK.
	SMII/SS_SMIILOW	I	TTL	**SMII: SMII/SS_SMII LOW** TIED TO LOW. TXEN_P7 should be tied to low for normal operation.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
59	REC_10M_P6	IPD	PD,	**Power On Setting: REC_10M** Value on RXD1_P6 will be latched by ADM7008/X during power on reset as Port 6 10M Re-command value. 0_B **REC_10M0**, Recommend Port 6 to operate in 100M Mode 1_B **REC_10M1**, Recommend Port 6 to operate in 10M Mode
	RXD1_P 6	O	8 mA	**RMII: RMII Receive Data[1]** RXD[1] is the port 6 output di-bit synchronously to REFCLK. Upon assertion of CRSDV_P 6, RXD0 and RXD1 remain at ' 00 ' until valid data is output from the FIFO onto RXD. The start of valid data is indicated by '01' on RXD1 and RXD0. If a false carrier or a symbol error is detected, RXD1 and RXD0 are set to '10' for the duration of the activity. Note that in 100Mb/s mode RXD can change once per REFCLK cycle, whereas in 10Mb/s mode RXD must be held steady for 10 consecutive REFCLK cycles.
	SPDLED_P6	O	8 mA	**SMII: SMII Receive Data** Port 6: RXD0 for the designated port outputs data or in-band management information synchronously to TX_CLK (pin 78). In 100Mb/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10Mb/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 6.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
60	DUALLED	IPD	PD,	**Power On Setting: DUALLED** Dual Color LED Mode. Value on RXD0_P6 will be latched by ADM7008/X during power on reset to form LED control signal. Value on this pin will affect the output value on Serial LED output. 0_B **DUALLED0**, Single Color 3 bits/port serial stream (Default Value) 1_B **DUALLED1**, Dual Color 3 bits/port serial stream
	RXD0_P 6	O	8 mA	**RMII: RMII Receive Data[0]** RXD[0] is the port 6 output di-bit synchronously to REFCLK. Upon assertion of CRSDV_P 6, RXD0 and RXD1 remain at '00' until valid data is output from the FIFO onto RXD. The start of valid data is indicated by '01' on RXD1 and RXD0. If a false carrier or a symbol error is detected, RXD1 and RXD0 are set to '10' for the duration of the activity. Note that in 100Mb/s mode RXD can change once per REFCLK cycle, whereas in 10Mb/s mode RXD must be held steady for 10 consecutive REFCLK cycles.
	SMII_RXD_P	O	8 mA	**SMII: SMII Receive Data** Port 6: RXD0 for the designated port outputs data or in-band management information synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 6.
	SS _SMII_RXD_P6	O	8 mA	**SMII: SS_SMII Receive Data** Port 6: RXD0 for the designated port outputs data or in-band management information synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 6.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
61	RSMODE0	I	LVTTL,PD	**Power On Setting: RSMODE0** RMII/SMII/SS_SMII Configuration bit 0. Value on this pin will be latched by ADM7008/X during power on reset as interface configuration bit 0. Combined with RSMODE1 (pin 43), three possible interfaces are provided by ADM7008/X RSMODE[1:0] Interface 00_B **SMII**, SMII 01_B **SS_SMII**, SS_SMII $1x_B$ **RMII**, 1x RMII
	CRSDV_P6	O	8 mA	**Power On Setting: Carrier Sense/Receive Data Valid** Port 6: CRSDV_P6 asserts when the receive medium is non-idle. The assertion of CRSDV_P6 is asynchronous to REFCLK. At the de-assertion of carrier, CRSDV_P6 de-asserts synchronously to REFCLK only on the first di-bit of RXD. If there is still data in the FIFO not yet presented onto RXD, then on the second di-bit of RXD, CRSDV_P6 is asserted synchronously to REFCLK. The toggling of CRSDV_P6 on the first and second di-bit continues until all the data in the FIFO is presented onto RXD. CRSDV_P6 is asserted for the duration of carrier activity for a false carrier event.
	N/A	O	8 mA	**SMII/SS_SMII: N/A** Not used in SMII/SS_SMII Mode
62	TXD1_P6	I	LVTTL,PD, PD	**RMII: RMII Transmit Data[1:0]** Port 6: Transmit data for port 6 input the di-bits that re transmitted and are driven synchronously to REFCLK. Note that in 100 Mbit/s mode, TXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode, TXD must be held steady for 10 consecutive REFCLK cycles.
	LNKACT_P6	I	LVTTL,PD, PD	**SMII: Link and Activity LED** See LED Description for more detail.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
63	TXD0_P6	I	LVTTL,PD, PD	**RMII: RMII Transmit Data[1:0]** Port 6: Transmit data for port 6 input the di-bits that re transmitted and are driven synchronously to REFCLK. Note that in 100 Mbit/s mode, TXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode, TXD must be held steady for 10 consecutive REFCLK cycles.
	SMII_TXD_P6	I	LVTTL,PD, PD	**SMII: SMII Transmit Data** Port 6: TXD0 for port 6 inputs the data that is transmitted and is driven synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, TXD0 inputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, TXD0 must repeat each 10-bit segment 10 times. TXD1_P6 acts as Port 6 Link/Activity LED in both SMII and SS_SMII Mode.
	SS _S MII_TXD_P6	I	LVTTL,PD, PD	**SS_SMII: SS_SMII Transmit Data** Port 6: TXD0 for port 6 inputs the data that is transmitted and is driven synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, TXD0 inputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, TXD0 must repeat each 10-bit segment 10 times.
64	TXEN_P6	I	TTL	**RMII: Transmit Enable** Port 6: Transmit Enable for port 6 indicates that the di-bit on TXD is valid and it is driven synchronously to REFCLK.
	SMII/SS_SMIILOW	I	TTL	**SMII and SS_SMII Mode** TIED TO LOW. TXEN_P6 should be tied to low for normal operation in both SMII and SS_SMII Mode.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
65	REC_10M_P5	I	PD,PD	**Power On setting: REC_10M** Value on RXD1_P5 will be latched by ADM7008/X during power on reset as Port 5 10M Re-command value. 0_B **REC_10M0**, Recommend Port 5 to operate in 100M Mode (Default) 1_B **REC_10M1**, Recommend Port 5 to operate in 10M Mode
	RXD1_P 5	O	8 mA	**RMII: RMII Receive Data** Port 5 RMII Receive Data, RXD[1:0]. RXD[1:0] are the port 5 output di-bits synchronously to REFCLK. Upon assertion of CRSDV_P 5, RXD0 and RXD1 remain at '00' until valid data is output from the FIFO onto RXD. '01' on RXD1 and RXD0 indicates the start of valid data. If a false carrier or a symbol error is detected, RXD1 and RXD0 are set to '10' for the duration of the activity. Note that in 100 Mbit/s mode RXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode RXD must be held steady for 10 consecutive REFCLK cycles.
	SPDLED_P5	O	8 mA	**SMII: SMII Receive Data** Port 5: RXD0 for the designated port outputs data or in-band management information synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 5.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
66	PWSAVE_ DIS	I	PD, PD	**Power On Setting: Lower power Link Pulse Function Disable** (Power Saving, LLP) Value on RXD1 will be latched by ADM7008/X during power on reset as power saving disable signal. (See Lower Power Link Pulse Function description for more detail) 0_B **PWSAVE0**, Power Saving Enable 1_B **PWSAVE1**, Power Saving disable (Default)
	RXD0_P 5	O	8 mA	**RMII: RMII Receive Data** Port 5 RMII Receive Data, RXD[1:0]. RXD[1:0] are the port 5 output di-bits synchronously to REFCLK. Upon assertion of CRSDV_P 5, RXD0 and RXD1 remain at '00' until valid data is output from the FIFO onto RXD. '01' on RXD1 and RXD0 indicates the start of valid data. If a false carrier or a symbol error is detected, RXD1 and RXD0 are set to '10' for the duration of the activity. Note that in 100 Mbit/s mode RXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode RXD must be held steady for 10 consecutive REFCLK cycles.
	SMII_RXD_P5	O	8 mA	**SMII: SMII Receive Data** Port 5: RXD0 for the designated port outputs data or in-band management information synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 5.
	SS _S MII_RXD_P5	O	8 mA	**SMII: SS_SMII Receive Data** Port 5: RXD0 for the designated port outputs data or in-band management information synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 5.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
67	TP_PAUSE	I	LVTTL, PU	**Power On Setting: Twisted Pair PAUSE Recommend Value** Value on this pin will be latched by ADM7008/X during power on reset as twisted pair port (See SELFX power on setting for more detail) pause capability control signal. 0_B **TP_PAUSE0**, Pause off for all twisted pair ports 1_B **TP_PAUSE1**, Pause on for all twisted pair ports
	CRSDV_P5	O	8 mA	**Power ON Setting: Carrier Sense/Receive Data Valid** Port 5: CRSDV_P5 asserts when the receive medium is non-idle. The assertion of CRSDV_P5 is asynchronous to REFCLK. At the de-assertion of carrier, CRSDV_P5 de-asserts synchronously to REFCLK only on the first di-bit of RXD. If there is still data in the FIFO not yet presented onto RXD, then on the second di-bit of RXD, CRSDV_P5 is asserted synchronously to REFCLK. The toggling of CRSDV_P5 on the first and second di-bit continues until all the data in the FIFO is presented onto RXD. CRSDV_P5 is asserted for the duration of carrier activity for a false carrier event.
	N/A	O	8 mA	**SMII/SS_SMII: SMII/SS_SMII** Not used in SMII/SS_SMII Mode
68	LNKACT_P5	I	TTL, PD	**SMII: Link and Activity LED** See LED Description for more detail.
	TXD1_P5	I	TTL, PD	**RMII: RMII Transmit Data[1:0]** Port 5: Transmit data for port 5 inputs the di-bits that re transmitted and are driven synchronously to REFCLK. Note that in 100 Mbit/s mode, TXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode, TXD must be held steady for 10 consecutive REFCLK cycles.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
69	TXD0_P5	I	TTL, PD	**RMII: RMII Transmit Data[1:0]** Port 5: Transmit data for port 5 inputs the di-bits that re transmitted and are driven synchronously to REFCLK. Note that in 100 Mbit/s mode, TXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode, TXD must be held steady for 10 consecutive REFCLK cycles.
	SMII_TXD_P5	I	TTL, PD	**SMII: SMII Transmit Data** Port 5: TXD0 for port 5 inputs the data that is transmitted and is driven synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, TXD0 inputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, TXD0 must repeat each 10-bit segment 10 times. TXD1_P5 acts as Port 5 Link/Activity LED in both SMII and SS_SMII Mode.
	SS_SMII_TXD_P5	I	TTL, PD	**SS_SMII: SS_SMII Transmit Data** Port 5: TXD0 for port 5 inputs the data that is transmitted and is driven synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, TXD0 inputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, TXD0 must repeat each 10-bit segment 10 times.
70	TXEN_P5	I	TTL	**RMII: Transmit Enable** Port 5: Transmit Enable for port 5 indicates that the di-bit on TXD is valid and it is driven synchronously to REFCLK.
	SMII/SS_SMIILOW	I	TTL	**SMII/SS_SMII: SMII/SS_SMII Mode** Keep LOW for normal operation.
73	REC_10M_P4	I/O	8 mA, PD/PU	**Power On Setting: REC_10M** Value on RXD1_P4 will be latched by ADM7008/X during power on reset as Port 4 10M Re-command value. 0_B **REC_10M0**, Recommend Port 4 to operate in 100M Mode 1_B **REC_10M1**, Recommend Port 4 to operate in 10M Mode

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
74	TP_DUPLEX	I/O	8 mA, PD/PU	**Power On Setting: Twisted Pair Duplex Recommend Value** Twisted Pair Duplex Recommend Value. Value on RXD1 will be latched by ADM7008/X during power on reset as duplex recommend value for twisted pair interface. 0_B **TP_DUPLEX0**, Half Duplex for all twisted pair ports 1_B **TP_DUPLEX1**, Full Duplex for all twisted pair ports
	RXD0_P 4	I/O	8 mA,PD/PU	**RMII: RMII Receive Data[1:0]** Port 4 RXD[0] is the port 4 output di-bit synchronously to REFCLK. Upon assertion of CRSDV_P 4, RXD0 and RXD1 remain at '00' until valid data is output from the FIFO onto RXD. '01' on RXD1 and RXD0 indicates the start of valid data. If a false carrier or a symbol error is detected, RXD1 and RXD0 are set to '10' for the duration of the activity. Note that in 100 Mbit/s mode RXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode RXD must be held steady for 10 consecutive REFCLK cycles.
	SMII_RXD_P4	I/O	8 mA,PD/PU	**SMII: SMII Receive Data** Port 4: RXD0 for the designated port outputs data or in-band management information synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 4.
	SS _ SMII_RXD_P4	I/O	8 mA, PD/PU	**SS_SMII: SS_SMII Receive Data** Port 4: RXD0 for the designated port outputs data or in-band management information synchronously to RX_CLK (pin 75). In 100 Mbit/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 4.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
73	RXD1_P4	I/O	8 mA, PD/PU	**RMII: RMII Receive Data[1:0]** Port 4 RXD[1] is the port 4 output di-bit synchronously to REFCLK. Upon assertion of CRSDV_P 4, RXD0 and RXD1 remain at '00' until valid data is output from the FIFO onto RXD. '01' on RXD1 and RXD0 indicates the start of valid data. If a false carrier or a symbol error is detected, RXD1 and RXD0 are set to '10' for the duration of the activity. Note that in 100 Mbit/s mode RXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode RXD must be held steady for 10 consecutive REFCLK cycles.
	SPDLED_P4	I/O	8 mA, PD/PU	**SMII: SMII Receive Data** Port 4: RXD0 for the designated port outputs data or in-band management information synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 4.
75	CRSDV_P4	I	LVTTL, PDO, 8 mA	**RMII: Carrier Sense/Receive Data Valid** Port 4: CRSDV_P4 asserts when the receive medium is non-idle. The assertion of CRSDV_P4 is asynchronous to REFCLK. At the de-assertion of carrier, CRSDV_P4 de-asserts synchronously to REFCLK only on the first di-bit of RXD. If there is still data in the FIFO not yet presented onto RXD, then on the second di-bit of RXD, CRSDV_P4 is asserted synchronously to REFCLK. The toggling of CRSDV_P4 on the first and second di-bit continues until all the data in the FIFO is presented onto RXD. CRSDV_P4 is asserted for the duration of carrier activity for a false carrier event.
	N/A	I	LVTTL, PDO, 8 mA	**SMII: N/A** Not used in SMII Mode
	RXCLK	I	LVTTL, PDO, 8 mA	**SS_SMII: RXCLK** 125 MHz Receive Clock. This pin acts as 125 MHz receive clock when ADM7008/X is programmed to SS_SMII mode. All SS_SMII_RXD are synchronous to the rising edge of this clock. *Note: That clock on this pin will not be active during power on reset due to power on setting.*

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
76	TXD1_P4	I	TTL, PD	**RMII: RMII Transmit Data[1]** Port 4 Transmit data for port 4 inputs the di-bits that re transmitted and are driven synchronously to REFCLK. Note that in 100 Mbit/s mode, TXD can change once per REFCLK cycle, whereas in 10 Mb/its mode, TXD must be held steady for 10 consecutive REFCLK cycles.
	LNKACT_P4	I	TTL, PD	**SMII: Link and Activity LED/** See LED Description for more detail.
77	TXD0_P4	I	TTL, PD	**RMII: RMII Transmit Data[0]** Port 4 Transmit data for port 4 inputs the di-bits that re transmitted and are driven synchronously to REFCLK. Note that in 100 Mbit/s mode, TXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode, TXD must be held steady for 10 consecutive REFCLK cycles.
	SMII_TXD_P4	I	TTL, PD	**SMII: SMII Transmit Data** Port 4 TXD0 for port 4 inputs the data that is transmitted and is driven synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, TXD0 inputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, TXD0 must repeat each 10-bit segment 10 times. TXD1_P4 acts as Port 4 Link/Activity LED in both SMII and SS_SMII Mode. See LED Description for more detail.
	SS_SMII_TXD_P4	I	TTL, PD	**SS_SMII: SS_SMII Transmit Data** Port 4 TXD0 for port 4 inputs the data that is transmitted and is driven synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, TXD0 inputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, TXD0 must repeat each 10-bit segment 10 times.
78	TXEN_P4	I	TTL	**RMII: Transmit Enable** Port 4 Transmit Enable for port 4 indicates that the di-bit on TXD is valid and it is driven synchronously to REFCLK.
	TX_CLK	I	TTL	**SMII: SMII Reference Clock** SMII 125 MHz Reference Clock. In SMII Mode, this pin acts as 125 MHz reference clock for all ports. All transmit and receive data (include transmit enable and receive data valid) should be synchronous to the rising edge of this clock.
	TXCLK	I	TTL	**SS_SMII: SS_SMII Transmit Clock** SS_SMII 125 MHz Transmit Clock. In SS_SMII Mode, this pin acts as 125 Hz transmit clock for all ports. TXD and TXEN should be synchronous to the rising edge of this clock.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
81	REC_10M_P3,	I/O	8 mA, PD	**Power On Setting: REC_10M** Value on RXD1_P3 will be latched by ADM7008/X during power on reset as Port 3 10M Re-command value. 0_B , Recommend Port 3 to operate in 100M Mode 1_B , Recommend Port 3 to operate in 10M Mode
	RXD1_P3		PD	**RMII: RMII Receive Data[1]** Port 3 RXD[1] is the port 3 output di-bits synchronously to REFCLK. Upon assertion of CRSDV_P 3, RXD0 and RXD1 remain at '00' until valid data is output from the FIFO onto RXD. The start of valid data is indicated by '01' on RXD1 and RXD0. If a false carrier or a symbol error is detected, RXD1 and RXD0 are set to '10' for the duration of the activity. Note that in 100 Mbit/s mode RXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode RXD must be held steady for 10 consecutive REF-CLK cycles.
	SPDLED_P3		PD	**SMII: Speed Status LED** Port 3:RXD0 for the designated port outputs data or in-band management information synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 3.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
82	ANENDIS		PD	**Twisted Pair Duplex Recommend Value** Value on RXD1 will be latched by ADM7008/X during power on reset as auto negotiation disable recommend value for twisted pair interface. 0_B , Auto-negotiation Enable for all twisted pair ports. 1_B , Auto-negotiation Disable for all twisted pair ports
	RXD0_P3		PD	**RMII: RMII Receive Data[0]** Port 3 RXD[1:0] are the port 3 output di-bits synchronously to REFCLK. Upon assertion of CRSDV_P 3, RXD0 and RXD1 remain at '00' until valid data is output from the FIFO onto RXD. The start of valid data is indicated by '01' on RXD1 and RXD0. If a false carrier or a symbol error is detected, RXD1 and RXD0 are set to '10' for the duration of the activity. Note that in 100 Mbit/s mode RXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode RXD must be held steady for 10 consecutive REF-CLK cycles.
	SMII_RXD_P3		PD	**SMII: SMII Receive Data** Port 3: RXD0 for the designated port outputs data or in-band management information synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 3.
	SS _ SMII_RXD_P3		PD	**SS_SMII: SS_SMII Receive Data** Port 3: RXD0 for the designated port outputs data or in-band management information synchronously to RXCLK (pin 75). In 100 Mbit/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 3.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
83	TESTSEL2	I	PD	**Power On Setting: Industrial Test Mode Select 2** Value on this pin will be latched by ADM7008/X during power on reset as industrial test mode select bit 2. Pull down for normal operation. For Test Mode, See test select 0 for more detail
	CRSDV_P3	O	8 mA	**RMII: Carrier Sense/Receive Data Valid** Port 3 CRSDV_P3 asserts when the receive medium is non-idle. The assertion of CRSDV_P3 is asynchronous to REFCLK. At the de-assertion of carrier, CRSDV_P3 de-asserts synchronously to REFCLK only on the first di-bit of RXD. If there is still data in the FIFO not yet presented onto RXD, then on the second di-bit of RXD, CRSDV_P3 is asserted synchronously to REFCLK. The toggling of CRSDV_P3 on the first and second di-bit continues until all the data in the FIFO is presented onto RXD. CRSDV_P3 is asserted for the duration of carrier activity for a false carrier event.
	N/A	O	8 mA	**SMII: N/A** Not used in SMII Mode
	RX_SYNC	O	8 mA	**SS_SMII: SS_SMII Receive Synchronization Signal** In SS_SMII Mode, this pin sets the bit stream alignment of SS_SMII_RXD for all ports.
84	TXD1_P3	I	TTL, PD	**RMII: RMII Transmit Data[1]** Port 3: Transmit data for port 3 inputs the di-bit that re transmitted and are driven synchronously to REFCLK. Note that in 100 Mbit/s mode, TXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode, TXD must be held steady for 10 consecutive REFCLK cycles.
	LNKACT_P3	I	TTL, PD	**SMII: Link and Activity LED** See LED Description for more detail.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
85	TXD0_P3	I	TTL, PD	**RMII: RMII Transmit Data[0]** Port 3: Transmit data for port 3 inputs the di-bit that re transmitted and are driven synchronously to REFCLK. Note that in 100 Mbit/s mode, TXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode, TXD must be held steady for 10 consecutive REFCLK cycles.
	SMII_TXD_P3	I	TTL, PD	**SMII: SMII Transmit Data** Port 3: TXD0 for port 3 inputs the data that is transmitted and is driven synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, TXD0 inputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, TXD0 must repeat each 10-bit segment 10 times. TXD1_P3 acts as Port 3 Link/Activity LED in both SMII and SS_SMII Mode. See LED Description for more detail.
	SS _ SMII_TXD_P3	I	TTL, PD	**SS_SMII: SS_SMII Transmit Data** Port 3: TXD0 for port 3 inputs the data that is transmitted and is driven synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, TXD0 inputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, TXD0 must repeat each 10-bit segment 10 times.
86	TXEN_P3	I	TTL	**RMII: Transmit Enable** Port 3: Transmit Enable for port 3 indicates that the di-bit on TXD is valid and it is driven synchronously to REFCLK.
	SMII_SYNC	I	TTL	**SMII: SMII Synchronization Signal** In SMII Mode, this pin sets the bit stream alignment of SMII_TXD and SMII_RXD for all ports.
	TX_SYNC	I	TTL	**SS_SMII: SS_SMII Transmit Synchronization Signal** In SS_SMII Mode, this pin sets the bit stream alignment of SS_SMII_TXD for all ports.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
89	REC_10M_P2	I	PD	**Power On Setting: REC_10M** Value on RXD1_P2 will be latched by ADM7008/X during power on reset as Port 2 10M Re-command value. 0_B **REC_10M0**, Recommend Port 2 to operate in 100M Mode 1_B **REC_10M1**, Recommend Port 2 to operate in 10M Mode
	RXD1_P 2	O	8 mA	**RMII: RMII Receive Data[1]** Port 2: RXD[1] is the port 2 output di-bit synchronously to REFCLK. Upon assertion of CRSDV_P 2, RXD0 and RXD1 remain at '00' until valid data is output from the FIFO onto RXD. The start of valid data is indicated by '01' on RXD1 and RXD0. If a false carrier or a symbol error is detected, RXD1 and RXD0 are set to '10' for the duration of the activity. Note that in 100 Mbit/s mode RXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode RXD must be held steady for 10 consecutive REF-CLK cycles.
	SPDLED_P2	O	8 mA	**SMII: Speed Status LED** Port 2: RXD0 for the designated port outputs data or in-band management information synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 2.
	SS _ SMII_RXD_P2	O	8 mA	**SS_SMII: SMII Receive Data** Port 2: RXD0 for the designated port outputs data or in-band management information synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 2.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
90	PHYADDR0	I	PD	**Power On Setting: PHYADDR0** PHY Address Bit 0. Value on RXD1 will be latched by ADM7008/X during power on reset as PHY address bit 0. Combined with PHYADDR1 (pin 44) to form PHY address for ADM7008/X. See PHYADDR1 description for more detail
	RXD0_P 2	O	8 mA	**RMII: RMII Receive Data[1:0]** Port 2: RXD[0] is the port 2 output di-bit synchronously to REFCLK. Upon assertion of CRSDV_P 2, RXD0 and RXD1 remain at '00' until valid data is output from the FIFO onto RXD. The start of valid data is indicated by '01' on RXD1 and RXD0. If a false carrier or a symbol error is detected, RXD1 and RXD0 are set to '10' for the duration of the activity. Note that in 100 Mbit/s mode RXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode RXD must be held steady for 10 consecutive REF-CLK cycles.
	SMII_RXD_P2	O	8 mA	**SMII: SMII Receive Data** Port 2: RXD0 for the designated port outputs data or in-band management information synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 2.
91	FX_DUPLEX	I/ O	8 mA, PU	**Power On Setting: Duplex Recommend Value** Duplex Recommend Value for Fiber Port. Value on this pin will be latched by ADM7008/X during power on reset as duplex recommend value for all fiber ports. 0_B , Half duplex for all fiber ports. 1_B , Full duplex for all fiber ports.
	CRSDV_P2	I/ O	8 mA, PU	**RMII: Carrier Sense/Receive Data Valid** Port 2: CRSDV_P2 asserts when the receive medium is non-idle. The assertion of CRSDV_P2 is asynchronous to REFCLK. At the de-assertion of carrier, CRSDV_P2 de-asserts synchronously to REFCLK only on the first di-bit of RXD. If there is still data in the FIFO not yet presented onto RXD, then on the second di-bit of RXD, CRSDV_P2 is asserted synchronously to REFCLK. The toggling of CRSDV_P2 on the first and second di-bit continues until all the data in the FIFO is presented onto RXD. CRSDV_P2 is asserted for the duration of carrier activity for a false carrier event.
	N/A	I/ O	8 mA, PU	**SMII/SS_SMII** Not used in SMII and SS_SMII Mode

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
92	TXD1_P2	I	TTL,PD	**RMII: RMII Transmit Data[1]** Port 2: Transmit data for port 2 inputs the di-bits that re transmitted and are driven synchronously to REFCLK. Note that in 100 Mbit/s mode, TXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode, TXD must be held steady for 10 consecutive REFCLK cycles.
	LNKACT_P2	I	TTL, PD	**SMII: Link and Activity LED** See LED Description for more detail.
93	TXD0_P2	I	TTL, PD	**RMII: RMII Transmit Data[0]** Port 2: Transmit data for port 2 inputs the di-bits that re transmitted and are driven synchronously to REFCLK. Note that in 100 Mbit/s mode, TXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode, TXD must be held steady for 10 consecutive REFCLK cycles.
	SMII_TXD_P2	I	TTL, PD	**SMII: SMII Transmit Data** Port 2: TXD0 for port 2 inputs the data that is transmitted and is driven synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, TXD0 inputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, TXD0 must repeat each 10-bit segment 10 times. TXD1_P2 acts as Port 2 Link/Activity LED in both SMII and SS_SMII Mode.
	SS _ SMII_TXD_P2	I	TTL, PD	**SS_SMII: SS_SMII Transmit Data** Port 2: TXD0 for port 2 inputs the data that is transmitted and is driven synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, TXD0 inputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, TXD0 must repeat each 10-bit segment 10 times.
94	TXEN_P2	I	TTL	**RMII: Transmit Enable** Port 2: Transmit Enable for port 2 indicates that the di-bit on TXD is valid and it is driven synchronously to REFCLK.
	SMII/SS_SMIILOW	I	TTL	**SMII/SS_SMIILOW** Not Used. Tied to LOW for normal operation in SMII/SS_SMII mode.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
95	REC_10M_P1,	I/O	8 mA, PD	**Power On Setting: REC_10M** Value on RXD1_P1 will be latched by ADM7008/X during power on reset as Port 1 10M Re-command value. 0_B **REC_10M0**, Recommend Port 1 to operate in 100M Mode 1_B **REC_10M1**, Recommend Port 1 to operate in 10M Mode
	SPDLED_P1		PD	**SMII: Speed Status LED** Port 1 SMII Receive Data. RXD0 for the designated port outputs data or in-band management information synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 1.
	RXD1_P 1		PD	**RMII: RMII Receive Data[1]** Port 1: RXD[1] is the port 1 output di-bit synchronously to REFCLK. Upon assertion of CRSDV_P 1, RXD0 and RXD1 remain at '00' until valid data is output from the FIFO onto RXD. The start of valid data is indicated by '01' on RXD1 and RXD0. If a false carrier or a symbol error is detected, RXD1 and RXD0 are set to '10' for the duration of the activity. Note that in 100 Mbit/s mode RXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode RXD must be held steady for 10 consecutive REFCLK cycles.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
96	TESTSEL1		PD	**Industrial Test Mode Select 1** Value on RXD0_P1 will be latched by ADM7008/X during power on reset as industrial test mode select bit 1. Pull down for normal operation. For Test Mode, See test select 0 for more detail
	RXD0_P 1		PD	**RMII: RMII Receive Data[0]** Port 1: RXD[0] is the port 1 output di-bit synchronously to REFCLK. Upon assertion of CRSDV_P 1, RXD0 and RXD1 remain at '00' until valid data is output from the FIFO onto RXD. The start of valid data is indicated by '01' on RXD1 and RXD0. If a false carrier or a symbol error is detected, RXD1 and RXD0 are set to '10' for the duration of the activity. Note that in 100 Mbit/s mode RXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode RXD must be held steady for 10 consecutive REF-CLK cycles.
	SMII_RXD_P1		PD	**SMII:** SMII Receive Data Port 1: RXD0 for the designated port outputs data or in-band management information synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 1.
	SS _ SMII_RXD_P1		PD	**SS_SMII: SS_SMII Receive Data** Port 1: RXD0 for the designated port outputs data or in-band management information synchronously to RXCLK (pin 75). In 100 Mbit/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 1.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
97	SELFX1	I/O	8 mA, PD	**Power On Setting: Fiber/Twisted Pair Configuration** Fiber/Twisted Pair Configuration bit 1. Value on RXD1 will be latched by ADM7008/X during power on reset as fiber/twisted pair interface configuration bit 1. Combined with SELFX0 (Power On setting value on CRSDV _P0) to program ADM7008/X into 4 different modes. port 00_B **SELFX00**, all ports are twisted ports 01_B **SELFX01**, only port 7 is fiber port, and all the other ports are twisted ports. 10_B **SELFX10**, only port 7 and port 6 are fiber ports, and all the other port are twisted 11_B **SELF11**, all ports are fiber ports.
	CRSDV_P1	I/O	8 mA, PD	**RMII: Carrier Sense/Receive Data Valid** Port 1: CRSDV_P1 asserts when the receive medium is non-idle. The assertion of CRSDV_P1 is asynchronous to REFCLK. At the de-assertion of carrier, CRSDV_P1 de-asserts synchronously to REFCLK only on the first di-bit of RXD. If there is still data in the FIFO not yet presented onto RXD, then on the second di-bit of RXD, CRSDV_P1 is asserted synchronously to REFCLK. The toggling of CRSDV_P1 on the first and second di-bit continues until all the data in the FIFO is presented onto RXD. CRSDV_P1 is asserted for the duration of carrier activity for a false carrier event.
	N/A	I/O	8 mA, PD	**SMII/SS_SMII: N/A** Not used in SMII and SS_SMII Mode
98	TXD1_P1	I	TTL, PD	**RMII: RMII Transmit Data[1]** Port 1: Transmit data for port 1 inputs the di-bit that re transmitted and is driven synchronously to REFCLK. Note that in 100 Mbit/s mode, TXD can change once per REF-CLK cycle, whereas in 10 Mbit/s mode, TXD must be held steady for 10 consecutive REFCLK cycles.
	LNKACT_P1	I	TTL, PD	**SMII: Link and Activity LED** See LED Description for more detail.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
99	TXD0_P1	I	TTL, PD	**RMII: RMII Transmit Data[0]** Port 1: Transmit data for port 1 inputs the di-bit that re transmitted and is driven synchronously to REFCLK. Note that in 100 Mbit/s mode, TXD can change once per REF-CLK cycle, whereas in 10 Mbit/s mode, TXD must be held steady for 10 consecutive REFCLK cycles.
	SMII_TXD_P1	I	TTL, PD	**SMII: SMII Transmit Data** Port 1: TXD0 for port 1 inputs the data that is transmitted and is driven synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, TXD0 inputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, TXD0 must repeat each 10-bit segment 10 times. TXD1_P1 acts as Port 1 Link/Activity LED in both SMII and SS_SMII Mode. See LED Description for more detail.
	SS _ SMII_TXD_P1	I	TTL, PD	**SS_SMII: SS_SMII Transmit Data** Port 1: TXD0 for port 1 inputs the data that is transmitted and is driven synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, TXD0 inputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, TXD0 must repeat each 10-bit segment 10 times.
100	TXEN_P1	I	TTL	**RMII: Transmit Enable. Transmit Enable** Port 1 Transmit Enable. Transmit Enable for port 1 indi-cates that the di-bit on TXD is valid and it is driven syn-chronously to REFCLK.
	SMII/SS_SMIILOW	I	TTL	**SMII/SS_SMIILOW** Not Used. Tied to LOW for normal operation in SMII/SS_SMII mode.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
105	REC_10M_P0	I/O	8 mA, PD, PD	**Power On Setting: REC_10M** Value on RXD1_P0 will be latched by ADM7008/X during power on reset as Port 0 10M Re-command value. 0_B **REC_10M0**, Recommend Port 0 to operate in 100M Mode 1_B **REC_10M1**, Recommend Port 0 to operate in 10M Mode
	RXD1_P0	I/O	8 mA, PD, PD	**RMII: RMII Receive Data[1]** Port 0: RXD[1] is the port 0 output di-bit synchronously to REFCLK. Upon assertion of CRSDV_P 0, RXD0 and RXD1 remain at '00' until valid data is output from the FIFO onto RXD. The start of valid data is indicated by '01' on RXD1 and RXD0. If a false carrier or a symbol error is detected, RXD1 and RXD0 are set to '10' for the duration of the activity. Note that in 100 Mbit/s mode RXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode RXD must be held steady for 10 consecutive REFCLK cycles.
	SPDLED_P0	I/O	8 mA, PD, PD	**SMII: Speed Status LED** Port 0: RXD0 for the designated port outputs data or in-band management information synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 7.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
106	RXD0_P0	I/O	8 mA, PD, PD	**RMII: RMII Receive Data[0]** Port 0: RXD[0] is the port 0 output di-bit synchronously to REFCLK. Upon assertion of CRSDV_P 0, RXD0 and RXD1 remain at '00' until valid data is output from the FIFO onto RXD. The start of valid data is indicated by '01' on RXD1 and RXD0. If a false carrier or a symbol error is detected, RXD1 and RXD0 are set to '10' for the duration of the activity. Note that in 100 Mbit/s mode RXD can change once per REFCLK cycle, whereas in 10 Mbit/s mode RXD must be held steady for 10 consecutive REFCLK cycles.
	TESTSEL0	I/O	8 mA, PD, PD	**Power On Setting: Industrial Test Mode Select 0** Industrial Test Mode Select 0. Value on RXD0_P1 will be latched by ADM7008/X during power on reset as industrial test mode select bit 0. Pull down TESTSEL[2:0] for normal operation. 000_B **TESTSEL**, Normal Mode
	SMII_RXD_P0	I/O	8 mA, PD, PD	**SMII: SMII Receive Data** Port 0: RXD0 for the designated port outputs data or in-band management information synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 0.
	SS _ SMII_RXD_P0	I/O	8 mA, PD, PD	**SS_SMII: SS_SMII Receive Data** Port 0 RXD0 for the designated port outputs data or in-band management information synchronously to TX_CLK (pin 75). In 100 Mbit/s mode, RXD0 outputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, RXD0 must repeat each 10 bits segment 10 times. RXD1 for the designated port is acted as Speed Status LED for port 0.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
107	SELFX0	I/O	8 mA, PD	**Power On Setting: Fiber/Twisted Pair Configuration** Fiber/Twisted Pair Configuration bit 0. Value on RXD1 will be latched by ADM7008/X during power on reset as fiber/twisted pair interface configuration bit 1. Combined with SELFX1 (Power On setting value on CRSDV _P1) to program ADM7008/X into 4 different modes. See SELFX1 for more detail
	CRSDV_P0	I/O	8 mA, PD	**RMII: Carrier Sense/Receive Data Valid** Port 0 CRSDV_P0 asserts when the receive medium is non-idle. The assertion of CRSDV_P0 is asynchronous to REFCLK. At the de-assertion of carrier, CRSDV_P0 de-asserts synchronously to REFCLK only on the first di-bit of RXD. If there is still data in the FIFO not yet presented onto RXD, then on the second di-bit of RXD, CRSDV_P0 is asserted synchronously to REFCLK. The toggling of CRSDV_P0 on the first and second di-bit continues until all the data in the FIFO is presented onto RXD. CRSDV_P0 is asserted for the duration of carrier activity for a false carrier event.
	N/A	I/O	8 mA, PD	**SMII/SS_SMII: N/A** Not used in SMII and SS_SMII Mode
108	TXD1_P0	I	TTL, PD	**RMII: RMII Transmit Data[1]** Port 0: Transmit data for port 1 inputs the di-bit that re transmitted and is driven synchronously to REFCLK. Note that in 100 Mbit/s mode, TXD can change once per REF-CLK cycle, whereas in 10 Mbit/s mode, TXD must be held steady for 10 consecutive REFCLK cycles.
	LNKACT_P0	I	TTL, PD	**SMII: Link and Activity LED** See LED Description for more detail.

Table 8 RMII/SMII Interface, 48 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
109	TXD0_P0	I	TTL, PD	**RMII: RMII Transmit Data[0]** Port 0: Transmit data for port 1 inputs the di-bit that re transmitted and is driven synchronously to REFCLK. Note that in 100 Mbit/s mode, TXD can change once per REF-CLK cycle, whereas in 10 Mbit/s mode, TXD must be held steady for 10 consecutive REFCLK cycles.
	SMII_TXD_P0	I	TTL, PD	**SMII: SMII Transmit Data.** Port 0: TXD0 for port 0 inputs the data that is transmitted and is driven synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, TXD0 inputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, TXD0 must repeat each 10-bit segment 10 times. TXD1_P0 acts as Port 0 Link/Activity LED in both SMII and SS_SMII Mode. See LED Description for more detail.
	SS _ SMII_TXD_P0	I	TTL, PD	**SS_SMII: SS_SMII Transmit Data** Port 0: TXD0 for port 1 inputs the data that is transmitted and is driven synchronously to TX_CLK (pin 78). In 100 Mbit/s mode, TXD0 inputs a new 10-bit segment starting with SYNC. In 10 Mbit/s mode, TXD0 must repeat each 10-bit segment 10 times.
110	TXEN_P0	I	TTL	**RMII: Transmit Enable** Port 0: Transmit Enable for port 0 indicates that the di-bit on TXD is valid and it is driven synchronously to REFCLK.
	SMII/SS_SMIILOW	I	TTL	**SMII/SS_SMIILOW** Not Used. Tied to LOW for normal operation in SMII/SS_SMII mode.

2.2.7 ATPG Signals, 2 Pins

Table 9 ATPG Signals, 2 Pins

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
114	SCAN_EN	I	LVTTL	**Scan Enable** Scan enable for test 0: Normal mode Pull Low for normal operation
113	SCAN_MODE	I	LVTTL	**Scan Mode Select** Scan mode select for test 0: Normal mode Pull Low for normal operation

2.2.8 Reset Pin

Table 10 Reset Pin

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
47	$\overline{\text{RESET}}$	I	SCHE	**Reset Signal** Active low to bring ADM7008/X into reset condition. Recommend keeping low for at least 100 ms to ensure the stability of the system after power on reset.

2.2.9 Control Signals, 3 Pins

Table 11 Control Signals, 3 Pins

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
101	MDIO	I/O	LV TTL	**Management Data** Management Data MDIO transfers management data in and out of the device synchronous to MDC.
102	MDC	I	LV TTL	**Management Data Reference Clock** A non-continuous clock input for management usage. ADM7008/X will use this clock to sample data input on MDIO and drive data onto MDIO according to rising edge of this clock.
44	PHYADDR1	I	LV TTL	**PHY Address Bit 1** Pure input of ADM7008/X. Combined with PHYADDR0 to form the Most Significant 2 bits of PHY address for ADM7008/X. The LSB 3 bits will be assigned by ADM7008/X automatically according to port number 000_B **PORT0**, Port 0 001_B **PORT1**, Port 1 010_B **PORT2**, Port 2 011_B **PORT3**, Port 3 100_B **PORT4**, Port 4 101_B **PORT5**, Port 5 110_B **PORT6**, Port 6 111_B **PORT7**, Port 7

2.2.10 LED Interface, 2 Pins

Table 12 LED Interface, 2 Pins

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
50	LED_CLK	I/O	4 mA, PD	**LED Clock** Non-Continuous Clock for Serial Output LED status. The clock high duration is 40 ns and low for 600 ns. This 640 ns period forms one clock cycle and 24 clocks form one LED burst. The first clock output is used to latch the first bit on LED_DATA (See LED_DATA for more detail) and the final clock is used to latch the last data on LED_DATA. LED_CLK will be kept low for 40 ms before next LED stream data is output.
49	LED_DATA	I/O	4 mA, PD	**LED Data** 8 port Status Output with difference sequence according to different interface. DATA_LED is driven out by ADM7008/X at the falling edge of CLK_LED. System design should use the rising edge of LED_CLK to latch the data on LED_DATA. The output sequence is: DUPCOL0 (First Bit Output) DUPCOL1 … DUPCOL7 SPEED0 SPEED1 … SPEED7 LNKACT0 LNKACT1 … LNKACT7 (Last Bit Output)

2.2.11 Regulator Control, 2 Pins

Table 13 Regulator Control, 2 Pins

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
117	CONTROL	AO		**Regulator Control** Voltage Control to external 1.8 V Regulator. See 4.2.9 for more function description.
119	RTX	AI		**Constant Voltage Reference** External 1.1 kΩ 1% resistor connection to ground.

3 Function Description

ADM7008/X/X integrates eight 100Base-X physical sublayer (PHY), 100Base-TX physical medium dependent (PMD) transceivers, eight complete 10Base-T modules into a single chip for both 10 Mbits/s and 100 Mbits/s Ethernet operation. It also supports 100Base-FX operation through external fiber-optic transceivers. The device is capable of operating in either full-duplex mode or half-duplex mode in either 10 Mbits/s or 100 Mbits/s operation. Operational modes can be selected by hardware configuration pins, software settings of management registers, or determined by the on-chip auto negotiation logic.

The 10Base-T section of the device consists of the 10 Mbits/s transceiver module with filters and a Manchester ENDEC module.

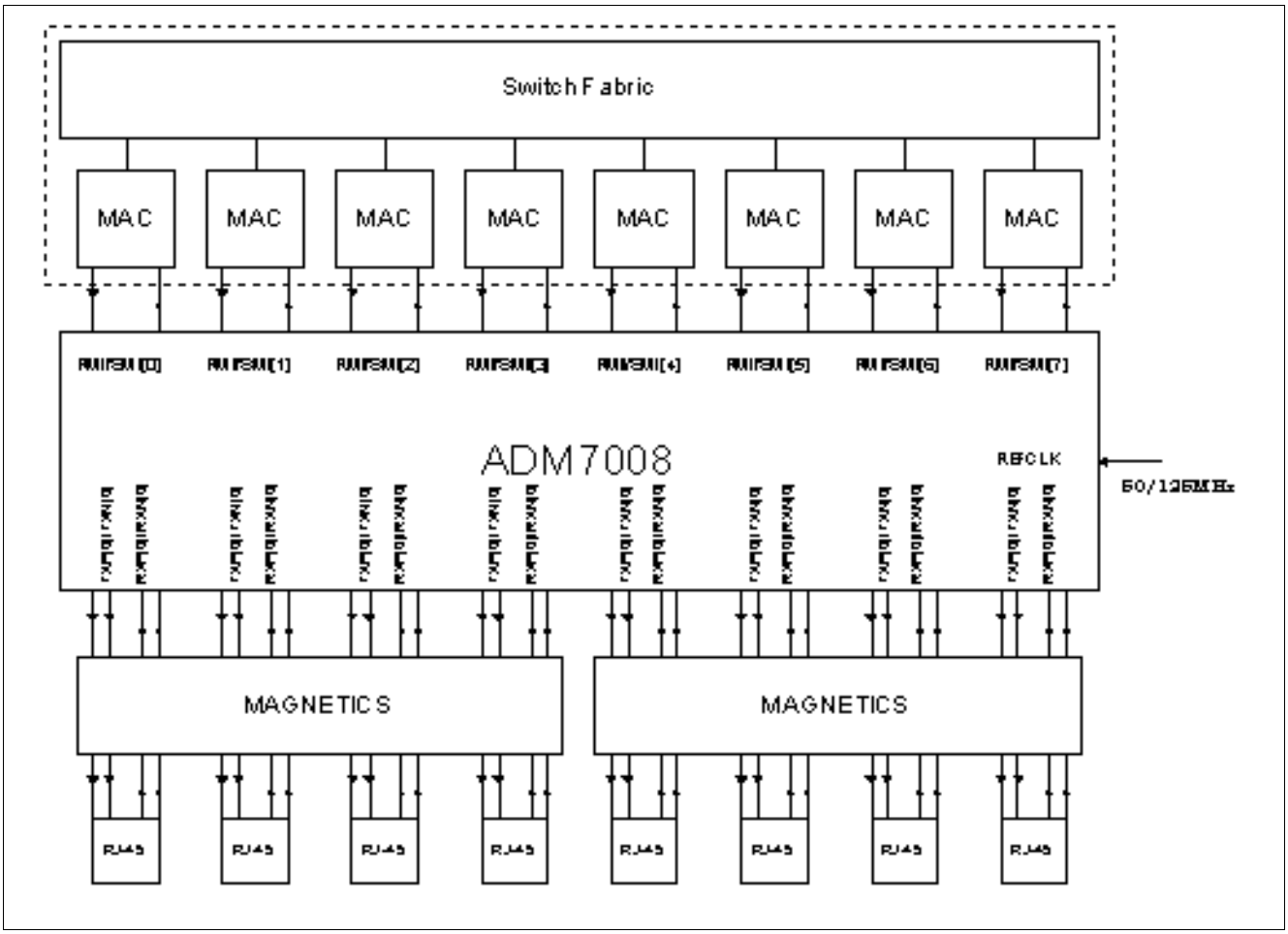


Figure 3 ADM7008/X Switch Application (10/100M TP Mode)

ADM7008/X consists of eight kinds of major blocks:

- Eight 10/100M PHY Blocks
- MAC Interface
- LED Display
- SMI
- Power Management
- Clock Generator
- Voltage Regulator

Each 10/100M PHY block contains:

- 10M PHY block
- 100M PHY block

- Auto-negotiation
- Cable Broken Detector
- Other Digital Control Blocks

3.1 10/100M PHY Block

The 100Base-X section of the device implements he following functional blocks:

- 100Base-X physical coding sub-layer (PCS)
- 100Base-X physical medium attachment (PMA)
- Twisted-pair PMD (TP-PMD) transceiver

The 100Base-X and 10Base-T sections share the following functional blocks:

- Clock synthesizer module
- MII Registers
- IEEE 802.3u auto negotiation

The interfaces used for communication between PHY block and switch core is MII interface.

3.1.1 100Base-X Module

ADM7008/X implements 100Base-X compliant PCS and PMA and 100Base-TX compliant TP-PMD as illustrated in **Figure 4**. Bypass options for each of the major functional blocks within the 100Base-X PCS provides flexibility for various applications. 100 Mbit/s PHY loop back is included for diagnostic purpose.

3.1.2 100Base-TX Receiver

For 100Base-TX operation, the on-chip twisted pair receiver that consists of a differential line receiver, an adaptive equalizer and a base-line wander compensation circuits detects the incoming signal.

ADM7008/X uses an adaptive equalizer that changes filter frequency response in accordance with cable length. The cable length is estimated based on the incoming signal strength. The equalizer tunes itself automatically for any cable length to compensate for the amplitude and phase distortions incurred from the cable.

The 100Base-X receiver consists of functional blocks required to recover and condition the 125 Mbit/s receive data stream. The ADM7008/X implements the 100Base-X receiving state machine diagram as given in ANSI/IEEE Standard 802.3u, Clause 24. The 125 Mbit/s receive data stream may originate from the on-chip twisted-pair transceiver in a 100Base-TX application. Alternatively, the receive data stream may be generated by an external optical receiver as in a 100Base-FX application.

The receiver block consists of the following functional sub-blocks:

- A/D Converter
- Adaptive Equalizer and Timing Recovery Module
- NRZI/NRZ and Serial/Parallel Decoder
- De scrambler
- Symbol Alignment Block
- Symbol Decoder
- Collision Detect Block
- Carrier Sense Block
- Stream Decoder Block

A/D Converter

High performance A/D converter with 125M sampling rate converts signals received on RXP/RXN pins to 6-bits data streams; besides it possess auto-gain-control capability that will further improve receive performance especially under long cable or harsh detrimental signal integrity. Due to high pass characteristic on transformer, built in base-line-wander correcting circuit will cancel it out and restore its DC level.

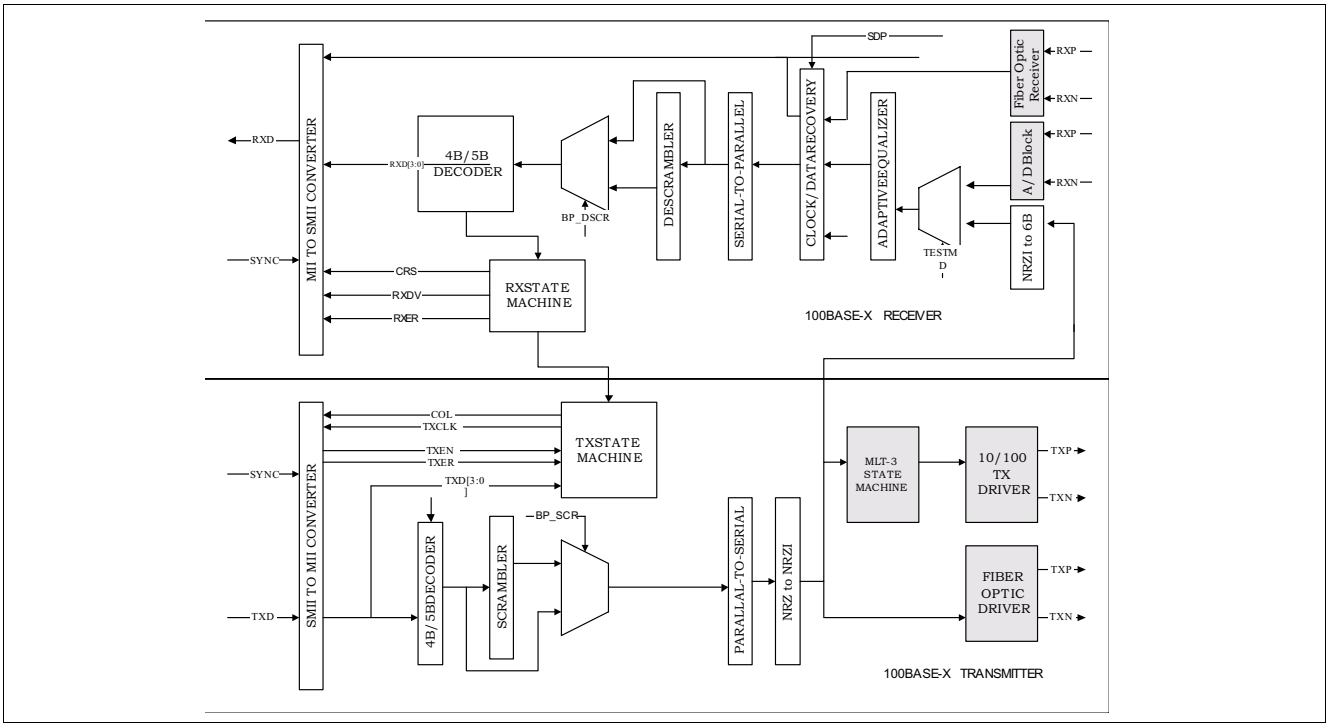


Figure 4 100Base-X Block Diagram and Data Path

Adaptive Equalizer and Timing Recovery Module

All digital design is especial immune from noise environments and achieves better correlations between production and system testing. Baud rate Adaptive Equalizer/Timing Recovery compensates line loss induced from twisted pair and tracks far end clock at 125M samples per second. Adaptive Equalizer implemented with Feed forward and Decision Feedback techniques meet the requirement of BER less than 10-12 for transmission on CAT5 twisted pair cable ranging from 0 to 140 meters.

NRZI/NRZ and Serial/Parallel Decoder

The recovered data is converted from NRZI to NRZ. The data is not necessarily aligned to 4B/5B code group's boundary.

Data Descrambling

The de scrambler acquires synchronization with the data stream by recognizing idle bursts of 40 or more bits and locking its deciphering Linear Feedback Shift Register (LFSR) to the state of the scrambling LFSR. Upon achieving synchronization, the incoming data is XORed by the deciphering LFSR and de scrambled.

In order to maintain synchronization, the de scrambler continuously monitors the validity of the unscrambled data that it generates. To ensure this, a link state monitor and a hold timer are used to constantly monitor the synchronization status. Upon synchronization of the de scrambler the hold timer starts a 722 μs countdown. Upon detection of at least 6 idle symbols (30 consecutive 1) within the 722 μs period, the hold timer will reset and begin a new countdown. This monitoring operation will continue indefinitely given a properly operating network connection with good signal integrity. If the link state monitor does not recognize at least 6 unscrambled idle symbols within 722 μs period, the de scrambler will be forced out of the current state of synchronization and reset in order to re-acquire synchronization.

Symbol Alignment

The symbol alignment circuit in the ADM7008/X determines code word alignment by recognizing the /J/K delimiter pair. This circuit operates on unaligned data from the de scrambler. Once the /J/K symbol pair (11000 10001) is detected, subsequent data is aligned on a fixed boundary.

Symbol Decoding

The symbol decoder functions as a look-up table that translates incoming 5B symbols into 4B nibbles as shown in **Table 14**. The symbol decoder first detects the /J/K symbol pair preceded by idle symbols and replaces the symbol with MAC preamble. All subsequent 5B symbols are converted to the corresponding 4B nibbles for the duration of the entire packet. This conversion ceases upon the detection of the /T/R symbol pair denoting the end of stream delimiter (ESD). The translated data is presented on the internal RXD[3:0] signal lines with RXD[0] represents the least significant bit of the translated nibble.

Table 14 Look-up Table for Translating 5B Symbols into 4B Nibbles

PCS Code-Group[4:0]	Name	MII (TXD/RXD)<3:0>	Interpretation
11110	0	0000	Data 0
01001	1	0001	Data 1
10100	2	0010	Data 2
10101	3	0011	Data 3
01010	4	0100	Data 4
01011	5	0101	Data 5
01110	6	0110	Data 6
01111	7	0111	Data 7
10010	8	1000	Data 8
10011	9	1001	Data 9
10110	A	1010	Data A
10111	B	1011	Data B
11010	C	1100	Data C
11011	D	1101	Data D
11100	E	1110	Data E
11101	F	1111	Data F
11111	I	Undefined	IDLEused as inter-stream fill code
11000	J	0101	Start-of-Stream Delimiter, Part 1 of 2; always used in pairs with K
10001	K	0101	Start-of-Stream Delimiter, Part 2 of 2; always used in pairs with J
01101	T	Undefined	Start-of-Stream Delimiter, Part 1 of 2; always used in pairs with R
0111	R	Undefined	Start-of-Stream Delimiter, Part 2 of 2; always used in pairs with T

Table 14 Look-up Table for Translating 5B Symbols into 4B Nibbles (cont'd)

PCS Code-Group[4:0]	Name	MII (TXD/RXD)<3:0>	Interpretation
00100	H	Undefined	Transmit Error; used to force signaling errors
00000	V	Undefined	Invalid code
00001	V	Undefined	Invalid code
00010	V	Undefined	Invalid code
00011	V	Undefined	Invalid code
00101	V	Undefined	Invalid code
00110	V	Undefined	Invalid code
01000	V	Undefined	Invalid code
01100	V	Undefined	Invalid code
10000	V	Undefined	Invalid code
11001	V	Undefined	Invalid code

Valid Data Signal

The valid data signal (RXDV) indicates that recovered and decoded nibbles are being presented on the internal RXD[3:0] synchronous to receive clock, RXCLK. RXDV is asserted when the first nibble of translated /J/K is ready for transfer over the internal MII. It remains active until either the /T/R delimiter is recognized, link test indicates failure, or no signal is detected. On any of these conditions, RXDV is deasserted.

Receive Errors

The RXER signal is used to communicate receiver error conditions. While the receiver is in a state of holding RXDV asserted, the RXER will be asserted for each code word that does not map to a valid code-group.

100Base-X Link Monitor

The 100Base-X link monitor function allows the receiver to ensure that reliable data is being received. Without reliable data reception, the link monitor will halt both transmit and receive operations until such time that a valid link is detected.

The ADM7008/X performs the link integrity test as outlined in IEEE 100Base-X (Clause 24) link monitor state diagram. The link status is multiplexed with 10 Mbits/s link status to form the reportable link status bit in serial management register 1h, and driven to the LNKACT pin.

When persistent signal energy is detected on the network, the logic moves into a Link-Ready state after approximately 500 μs, and waits for an enable from the auto negotiation module. When receive, the link-up state is entered, and the transmission and reception logic blocks become active. Should auto negotiation be disabled, the link integrity logic moves immediately to the link-up state after entering the link-ready state.

Carrier Sense

Carrier sense (CRS) for 100 Mbits/s operation is asserted upon the detection of two non contiguous zeros occurring within any 10-bit boundary of the received data stream.

The carrier sense function is independent of symbol alignment. In switch mode, CRS is asserted during either packet transmission or reception. For repeater mode, CRS is asserted only during packet reception. When the idle symbol pair is detected in the received data stream, CRS is deasserted. In repeater mode, CRS is only asserted due to receive activity. CRS is intended to encapsulate RXDV.

Bad SSD Detection

A bad start of stream delimiter (Bad SSD) is an error condition that occurs in the 100Base-X receiver if carrier is detected (CRS asserted) and a valid /J/K set of code-group (SSD) is not received.

If this condition is detected, then the ADM7008/X will assert RXER and present RXD[3:0] = 1110 to the internal MII for the cycles hat correspond to received 5B code-groups until at least two idle code-groups are detected. Once at least two idle code groups are detected, RXER and CRS become deasserted.

Far-End Fault

Auto negotiation provides a mechanism for transferring information from the Local Station to the link Partner that a remote fault has occurred for 100Base-TX. As auto negotiation is not currently specified for operation over fiber, the far end fault indication function (FEFI) provides this capability for 100Base-FX applications.

A remote fault is an error in the link that one station can detect while the other cannot. An example of this is a disconnected wire at a station's transmitter. This station will be receiving valid data and detect that the link is good via the link integrity monitor, but will not be able to detect that its transmission is not propagating to the other station.

A 100Base-FX station that detects such a remote fault may modify its transmitted idle stream from all ones to a group of 84 ones followed by a single 0. This is referred to as the FEFI idle pattern.

The FEFI function is controlled by bit 3 of register 11h. It is initialized to 1 (encoded) if the SELFX pin is at logic high level during power on reset. If the FEFI function is enabled the ADM7008/X will halt all current operations and transmit the FEFI idle pattern when FOSD signal is de-asserted following a good link indication from the link integrity monitor. FOSD signal is generated internally from the internal signal detect circuit. Transmission of the FEFI idle pattern will continue until link up signal is asserted. If three or more FEFI idle patterns are detected by the ADM7008/X, then bit 4 of the Basic mode status register (address 1h) is set to one until read by management. Additionally, upon detection of far end fault, all receive and transmit MII activity is disabled/ignored.

3.1.3 100Base-TX Transmitter

ADM7008/X implements a TP-PMD compliant transceiver for 100Base-TX operation. The differential transmit driver is shared by the 10Base-T and 100Base-TX subsystems. This arrangement results in one device that uses the same external magnetics for both the 10Base-T and the 100Base-TX transmission with simple RC component connections. The individually wave-shaped 10Base-T and 100Base-TX transmit signals are multiplexed in the transmission output driver selection.

ADM7008/X 100Base-TX transmission driver implements MLT-3 translation and wave-shaping functions. The rise/fall time of the output signal is closely controlled to conform to the target range specified in the ANSI TP-PMD standard.

3.1.4 100Base-FX Receiver

Signal is received through PECL receiver inputs from fiber transceiver, and directly passed to clock recovery circuit for data/clock recovery. Scrambler/de-scrambler is bypassed in 100Base-FX.

Automatic "Signal_Detect" Function Block

Due to pin limitation, ADM7008/X doesn't support SDP/SDN in fiber mode, which is used to connect to fiber transceiver to indicate there is signal on the fiber. Instead, ADM7008/X use the data on RXP/RXN to detect consecutive 65 '1' on the receive data (Recovered from RXP/RXN) to determine whether "Signal" is detected or not. When the detect condition is true (Consecutive 65 bits '1'), internal signal detect signal will be asserted to inform receive relative blocks to be ready for coming receive activities.

3.1.5 100Base-FX Transmitter

In 100Base FX transmit, the serial data stream is driven out as NRZI PECL signals, which enters fiber transceiver in differential-pairs form. Fiber transceiver should be available working at 3.3 V environment.

3.1.6 10Base-T Module

The 10Base-T Transceiver Module is IEEE 802.3 compliant. It includes the receiver, transmitter, collision, heartbeat, loopback, jabber, waveshaper, and link integrity functions, as defined in the standard. Figure 3-3 provides an overview for the 10Base-T module.

The ADM7008/X 10Base-T module is comprised of the following functional blocks:

- Manchester encoder and decoder
- Collision detector
- Link test function
- Transmit driver and receiver
- Serial and parallel interface
- Jabber and SQE test functions
- Polarity detection and correction

3.1.7 Operation Modes

The ADM7008/X 10Base-T module is capable of operating in either half-duplex mode or full-duplex mode. In half-duplex mode, the ADM7008/X functions as an IEEE 802.3 compliant transceiver with fully integrated filtering. The COL signal is asserted during collisions or jabber events, and the CRS signal is asserted during transmit and receive. In full duplex mode the ADM7008/X can simultaneously transmit and receive data.

3.1.8 Manchester Encoder/Decoder

Data encoding and transmission begins when the transmission enable input (TXEN) goes high and continues as long as the transceiver is in good link state. Transmission ends when the transmission enable input goes low. The last transition occurs at the center of the bit cell if the last bit is a 1, or at the boundary of the bit cell if the last bit is 0.

A differential input receiver circuit accomplishes decoding and a phase-locked loop that separate the Manchester-encoded data stream into clock signals and NRZ data. The decoder detects the end of a frame when no more mid bit transitions are detected. Within one and half bit times after the last bit, carrier sense is deasserted.

3.1.9 Transmit Driver and Receiver

The ADM7008/X integrates all the required signal conditioning functions in its 10Base-T block such that external filters are not required. Only one isolation transformer and impedance matching resistors are needed for the 10Base-T transmit and receive interface. The internal transmit filtering ensures that all the harmonics in the transmission signal are attenuated properly.

3.1.10 Smart Squelch

The smart squelch circuit is responsible for determining when valid data is present on the differential receive. The ADM7008/X implements an intelligent receive squelch on the RXP/RXN differential inputs to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10Base-T standard) to determine the validity of data on the twisted-pair inputs.

The signal at the start of the packet is checked by the analog squelch circuit and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly, the opposite squelch level must then be exceeded within 150 ns. Finally, the signal must exceed the original squelch level within an additional 150 ns to ensure that the input waveform will not be rejected.

Only after all these conditions have been satisfied will a control signal be generated to indicate to the remainder of the circuitry that valid data is present.

Valid data is considered to be present until the squelch level has not been generated for a time longer than 200 ns, indicating end of packet. Once good data has been detected, the squelch levels are reduced to minimize the effect of noise, causing premature end-of-packet detection. The receive squelch threshold level can be lowered for use in longer cable applications. This is achieved by setting bit 7 of register address 10h.

3.1.11 Carrier Sense

Carrier Sense (CRS) is asserted due to receive activity once valid data is detected via the smart squelch function. For 10 Mbit/s half duplex operation, CRS is asserted during either packet transmission or reception. For 10 Mbit/s full duplex and repeater mode operations, the CRS is asserted only due to receive activity.

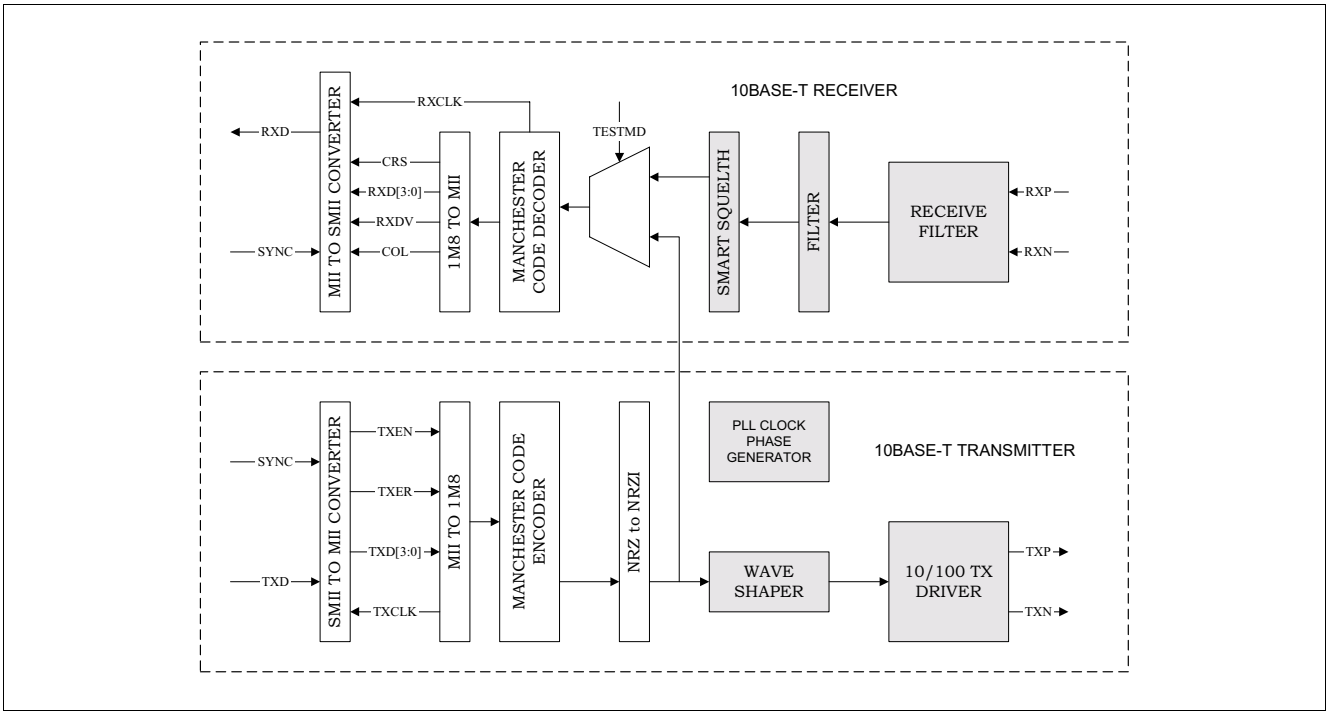


Figure 5 10Base-T Block Diagram and Data Path

3.1.12 Collision Detection

The SMII does not have a collision pin. Collision is detected internal to the MAC, which is generated by an AND function of TXEN and CRS derived from TXD and RXD, respectively. The internal MII will still generate the COL signal, but this information is not passed to the AMC via the SMII.

3.1.13 Jabber Function

The jabber function monitors the ADM7008/X output and disables the transmitter if it attempts to transmit a longer than legal sized packet. If TXEN is high for greater than 24 ms, the 10Base-T transmitter will be disabled. Once disabled by the jabber function, the transmitter stays disabled for the entire time that the TXEN signal is asserted. This signal has to be deasserted for approximately 408 ms (The un-jab time) before the jabber function re-enables the transmit outputs. The jabber function can be disabled by programming bit 0 of register address 10h to high.

3.1.14 Link Test Function

A link pulse is used to check the integrity of the connection with the remote end. If valid link pulses are not received, the link detector disables the 10Base-T twisted-pair transmitter, receiver, and collision detection functions.

The link pulse generator produces pulses as defined in IEEE 802.3 10Base-T standard. Each link pulse is nominally 100 ns in duration and is transmitted every 16 ms, in the absence of transmit data. Setting bit 10 of register 10h to high can disable link pulse check function.

3.1.15 Automatic Link Polarity Detection

ADM7008/X's 10Base-T transceiver module incorporates an "automatic link polarity detection circuit". The inverted polarity is determined when seven consecutive link pulses of inverted polarity or three consecutive packets are received with inverted end-of-packet pulses. If the input polarity is reversed, the error condition will be automatically corrected and reported in bit 13 of register 11h.

3.1.16 Clock Synthesizer

The ADM7008/X implements a clock synthesizer that generates all the reference clocks needed from a single external frequency source. The clock source must be a TTL level signal at 25 MHz $\pm$ 50ppm.

3.1.17 Auto Negotiation

The Auto Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices. Fast Link Pulse (FLP) Bursts provide the signaling used to communicate auto negotiation abilities between two devices at each end of a link segment. For further detail regarding auto negotiation, refer to Clause 28 of the IEEE 802.3u specification. The ADM7008/X supports four different Ethernet protocols, so the inclusion of auto negotiation ensures that the highest performance protocol will be selected based on the ability of the link partner.

The auto negotiation function within the ADM7008/X can be controlled either by internal register access or by the use of configuration pins are sampled. If disabled, auto negotiation will not occur until software enables bit 12 in register 0. If auto negotiation is enabled, the negotiation process will commence immediately.

When auto negotiation is enabled, the ADM7008/X transmits the abilities programmed into the auto negotiation advertisement register at address 04_H via FLP bursts. Any combination of 10 Mbits/s, 100 Mbits/s, half duplex and full duplex modes may be selected. Auto negotiation controls the exchange of configuration information. Upon successfully auto negotiation, the abilities reported by the link partner are stored in the auto negotiation link partner ability register at address 05_H.

The contents of the "auto negotiation link partner ability register" are used to automatically configure to the highest performance protocol between the local and far-end nodes. Software can determine which mode has been configured by auto negotiation by comparing the contents of register 04_H and 05_H and then selecting the technology whose bit is set in both registers of highest priority relative to the following list.

- 100Base-TX full duplex (highest priority)
- 100Base-TX half duplex
- 10Base-T full duplex
- 10Base-T half duplex (lowest priority)

The basic mode control register at address 0h provides control of enabling, disabling, and restarting of the auto negotiation function. When auto negotiation is disabled, the speed selection bit (bit 13) controls switching between 10 Mbits/s or 100 Mbits/s operation, while the duplex mode bit (bit 8) controls switching between full duplex operation and half duplex operation. The speed selection and duplex mode bits have no effect on the mode of operation when the auto negotiation enable bit (bit 12) is set.

The basic mode status register at address 1h indicates the set of available abilities for technology types (bit 15 to bit 11), auto negotiation ability (bit 3), and extended register capability (bit 0). These bits are hardwired to indicate the full functionality of the ADM7008/X. The BMSR also provides status on:

- Whether auto negotiation is complete (bit 5)
- Whether the Link Partner is advertising that a remote fault has occurred (bit 4)
- Whether a valid link has been established (bit 2)

The auto negotiation advertisement register at address 4_H indicates the auto negotiation abilities to be advertised by the ADM7008/X. All available abilities are transmitted by default, but writing to this register or configuring external pins can suppress any ability.

The auto negotiation link partner ability register at address 05_H indicates the abilities of the Link Partner as indicated by auto negotiation communication. The contents of this register are considered valid when the auto negotiation complete bits (bit 5, register address 1_H and bit 4, register 17_H) is set.

3.1.18 Auto Negotiation and Speed Configuration

The twelve sets of four pins listed in **Table 15** configure the speed capability of each channel of ADM7008/X. The logic state of these pins is latched into the advertisement register (register address 4_H) for auto negotiation purpose. These pins are also used for evaluating the default value in the base mode control register (register 0_H) according to **Table 15**.

3.2 MAC Interface

The ADM7008/X interfaces to eight 10/100 Media Access Controllers (MAC) via the RMII, SMII, or Source Synchronous SMII (SS_SMII) Interface. All ports on the device operate in the same interface mode that is selected.

3.2.1 Reduced Media Independent Interface (RMII)

The reduced media Independent interface (RMII) is compliant to the RMII consortium's RMII Rev. 1.2 specification. The REFCLK pin that supplies the 50 MHz reference clock to the ADM7008/X is used as the RMII REFCLK signal. All RMII signals with the exception of the assertion of CRSDV_P are synchronous to REFCLK. See **Figure 6**

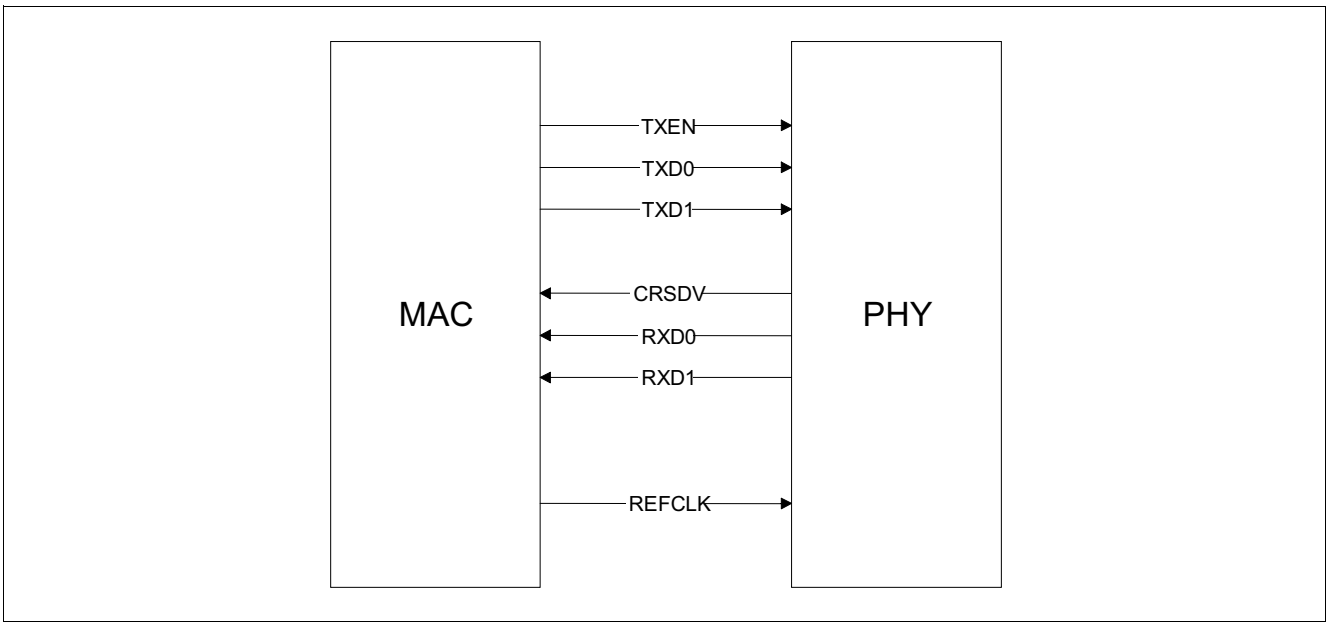


Figure 6 RMII Signal Diagram

3.2.2 Receive Path for 100M

Figure 7 shows the relationship among REFCLK, CRSDV_P, RXD0_P, RXD1_P and RXER_P while receiving a valid packet. Carrier sense is detected, which causes CRSDV_P to assert asynchronously to REFCLK. The received data is then placed into the FIFO for re synchronization. After a minimum of 12 bits are placed into the FIFO, the received data is presented onto RXD[1:0]_P synchronously to REFCLK. Note that while the FIFO is filling up RXD[1:0]_P is set to 00 until the first received di-bit of preamble (01) is presented onto RXD[1:0]_P. When carrier sense is de-asserted at the end of a packet, CRSDV_P is de-asserted when the first di-bit of a nibble is presented onto RXD[1:0]_P synchronously to REFCLK. If there is still data in the FIFO that has not yet been presented onto RXD[1:0]_P, then on the second di-bit of a nibble, CRSDV_P reasserts. This pattern of assertion and de-assertion continues until all received data in the FIFO has been presented onto RXD[1:0]_P.

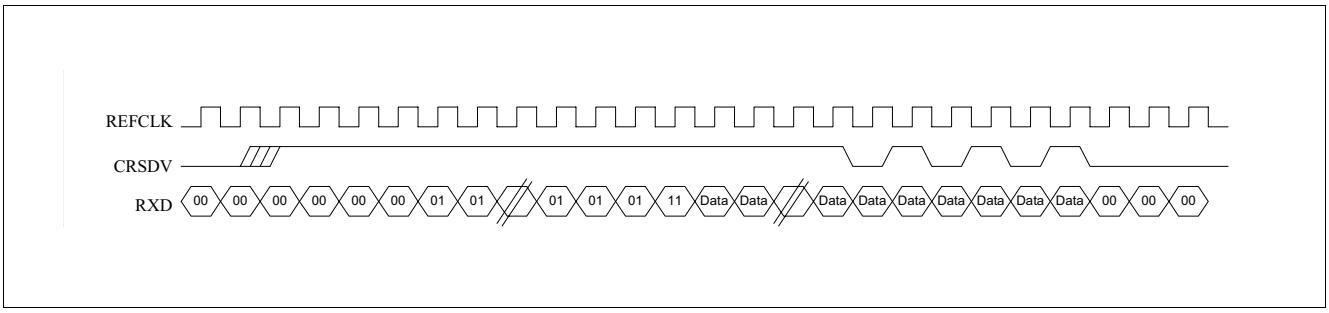


Figure 7 RMII Reception Without Error

3.2.3 Receive Path for 10M

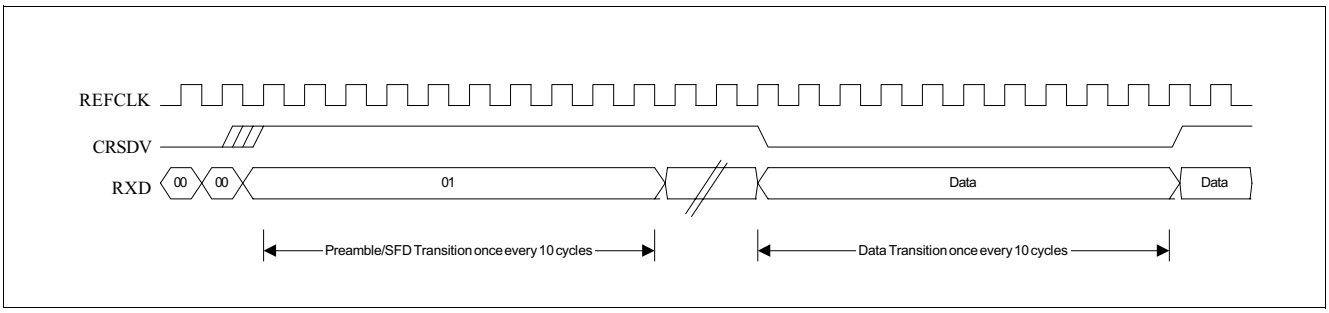


Figure 8 10M RMII Receive Diagram

In 10M Mode, RXER_P will maintain low all the time due to False Carrier and symbol error is not supported by 10M Mode. Different from 100M mode, RXD_P and CRSDV_P can transition once per 10 REFCLK cycles. After carrier sense is de-asserted yet the FIFO data is not fully presented onto RXD_P, the CRSDV_P de-assertion and re-assertion also follows this rule.

3.2.4 Transmit Path for 100M

Figure 9 shows the relationship among REFCLK, TXEN_P and TXD[1:0]_P during a transmit event. TXEN_P and TXD[1:0]_P are synchronous to REFCLK. When TXEN_P is asserted, it indicates that TXD[1:0]_P contains valid data to be transmitted. When TXEN_P is de-asserted, value on TXD[1:0]_P should be ignored. If an odd number of di-bits are presented onto TXD[1:0]_P and TXEN_P, the final di-bit will be discarded by AD2106.

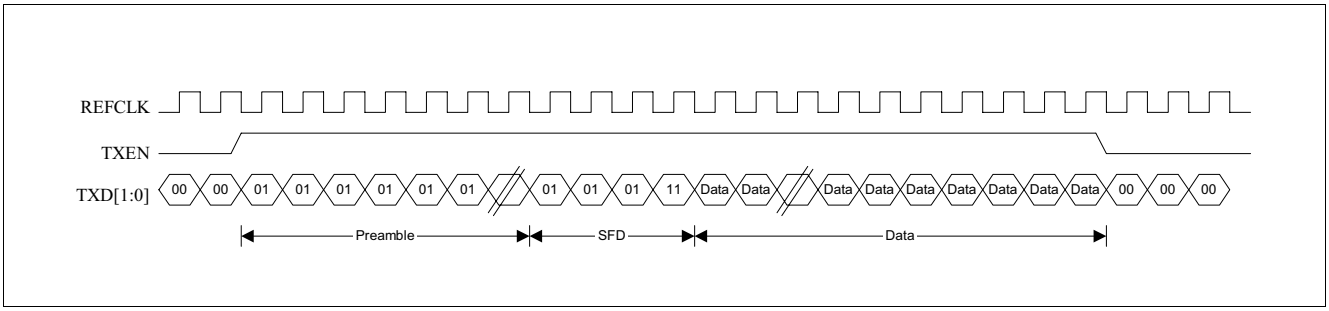


Figure 9 100M RMII Transmit Diagram

3.2.5 Transmit Path for 10M

In 10MBSE-T mode, each di-bit must be repeated 10 times by the MAC, TXEN_P and TXD[1:0]_P should be synchronous to REFCLK. When TXEN_P is asserted, it indicates that data on TXD[1:0]_P is valid for transmission.

In 10Base-T mode, it is possible that the number of preamble bits and the number of frame bits received are not integer nibbles. The preamble is always padded up such that the SFD appears on the RMII aligned to the nibble boundary. Extra bits at the end of the frame that do not complete a nibble are truncated by AD2106. **Figure 10** shows the timing diagram for 10M Transmission.

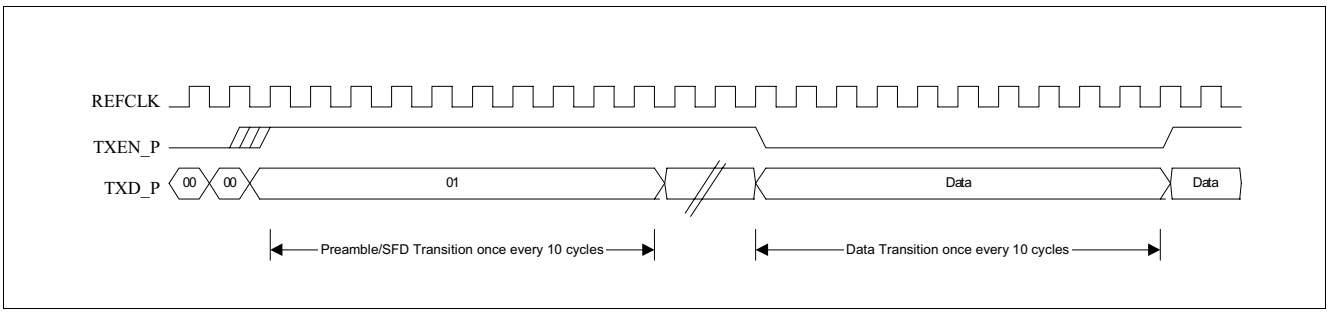


Figure 10 10M RMII Transmit Diagram

Table 15 Channel Configuration

Recommend Value			Auto Negotiation		Capability			
ANENDIS	REC_10M	TP_FULL DUPLEX	Enable	Disable	100 Full	100 Half	10 Full	10 Half
0	0	1	√		√	√	√	√
0	0	0	√			√		√
0	1	1	√				√	√
0	1	0	√					√
1	0	1		√	√			
1	0	0		√		√		
1	1	1		√			√	
1	1	0		√				√

3.2.6 Serial and Source Synchronous Media Independent Interface

The Synchronous Media Independent Interface (SMII) conforms to the SMII specification Rev. 2.1. The REFCLK pin that supplies the 125 MHz reference clock to the ADM7008/X is used as the SMII/Serial and Source Synchronous Media Independent Interface (SS_SMII) reference clock.

All SMII/SS_SMII signals are synchronous to REFCLK. The differences between SMII and SS_SMII are

1. SMII shares the same SYNC signal from MAC yet SS_SMII take TX_SYNC signal as synchronization input for transmission and output RX_SYNC to MAC for reception synchronization usage.
2. SMII use REFCLK (125 MHz) for both receive and transmit blocks. SS_SMII takes TXCLK as transmit block reference clock and output an 125 MHz RXCLK to MAC for receive usage. All signals output from ADM7008/X are synchronous to RXCLK.

In this mode, REFCLK will be divided by 5 to generate 25M clock before it is fed into ADM7008/X internal PLL block. SS_SMII mode is enabled by setting RSMODE1 (pin 43) to low and placing a pull up resistor on CRSDV_P6. In this mode, CRSDV_P[3] becomes RX_SYNC, CRSDV_P4 becomes RXCLK and TXEN_P4 acts as TX_SYNC.

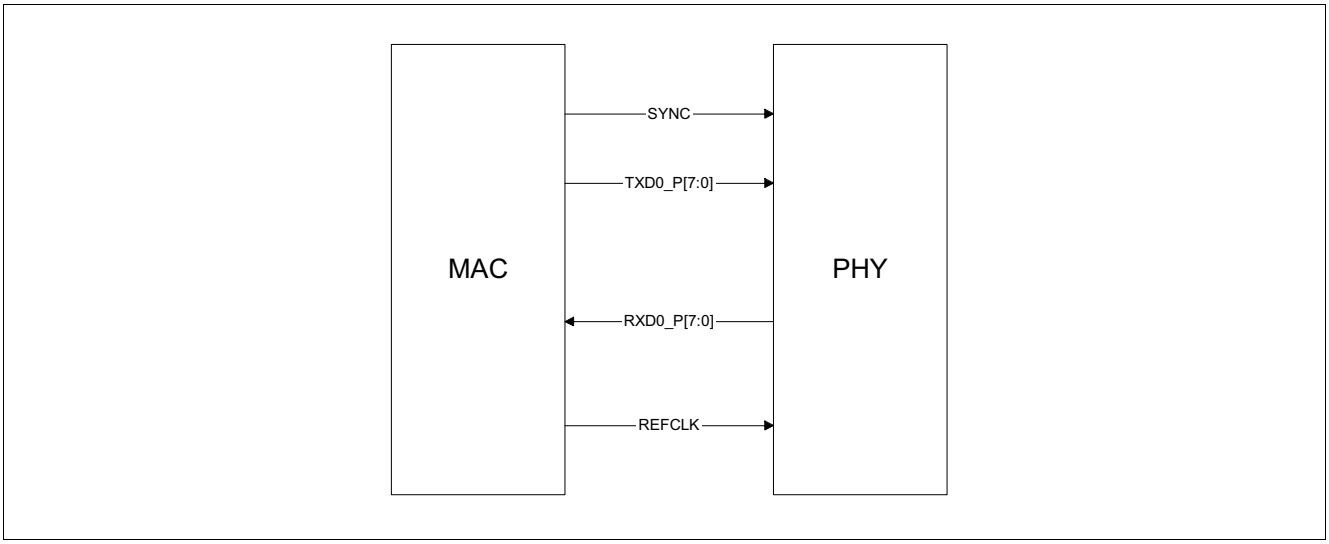


Figure 11 SMII Signal Diagram

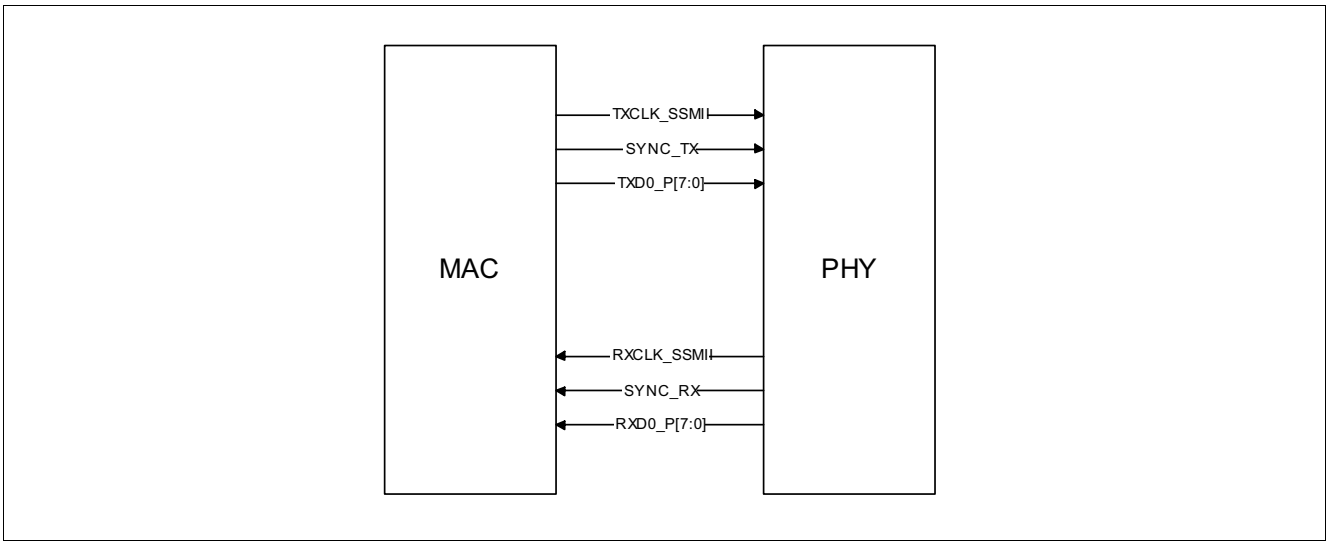


Figure 12 SS_SMII Signal Diagram

3.2.7 100M Receive Path

Received data and control information is grouped in 10-bit segments that are delimited by the SYNC signal in SMII mode (or SYNC_RX in SS_SMII mode) as shown in **Figure 13**. Each segment represents a new byte of data.

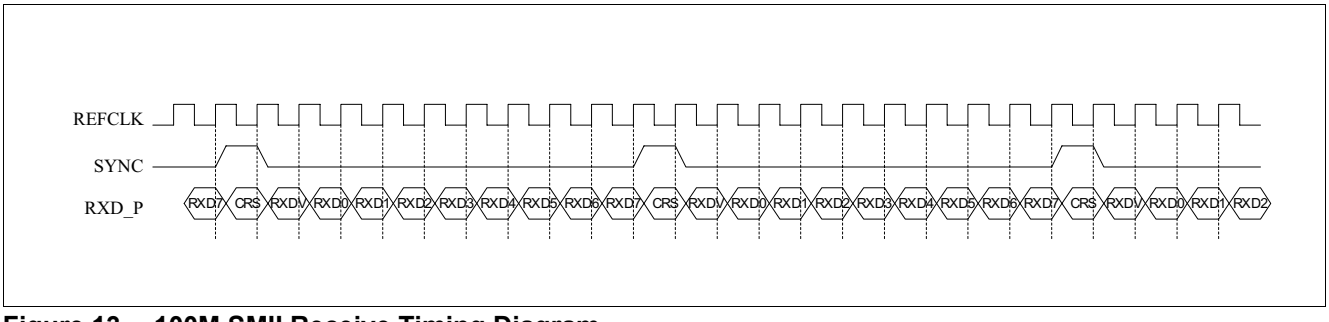


Figure 13 100M SMII Receive Timing Diagram

In SS_SMII mode, REFCLK and SYNC are no longer common for both transmit and receive blocks. They are renamed to RXCLK and RX_SYNC.

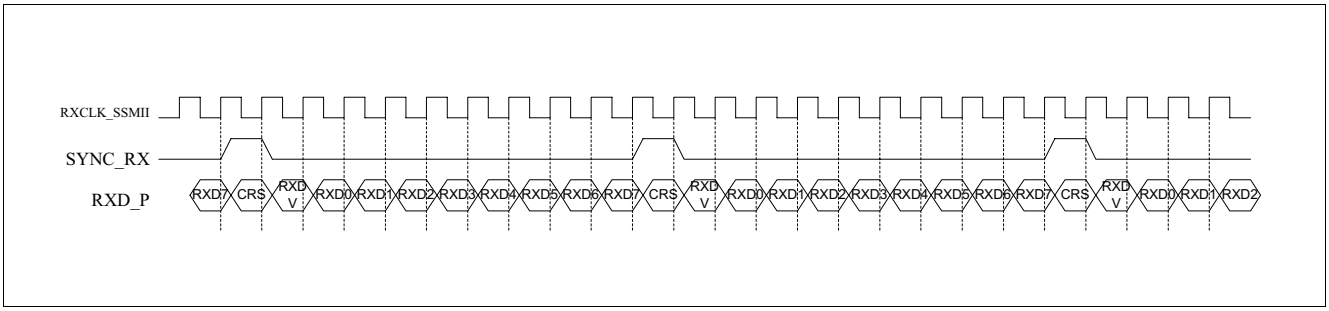


Figure 14 100M SS_SMII Receive Timing Diagram

In SMII mode, when RXDV bit is high, RXD[7:0] are used to convey packet data; when RXDV bit is low, RXD[7:0] are carrying PHY status. See **Table 16** for more detail.

Table 16 Receive Data Encoding for SMII/SS_SMII Mode

CRS	RXDV	RXD0	RXD1	RXD2	RXD3	RXD4	RXD5	RXD6	RXD7
X	0	RXER From Previous Frame	Speed 0 = 10 Mbit/s 1 = 100 Mbit/s	Duplex 0 = Half 1 = Full	Link 0 = Down 1 = Up	Jabber 0 = O.K. 1 = Error	Upper Nibble 0 = Invalid 1 = Valid	False Carrier 0 = NO 1 = Detected	1
X	1	One Data Byte (Two MII Data Nibble)							

3.2.8 10M Receive Path

Similar to 100M Receive path except that each segment is repeated 10 times. The MAC can sample any one of every 10 segments in 10Base-T mode. The MAC also has to generate a SYNC pulse once every 10 clock cycles.

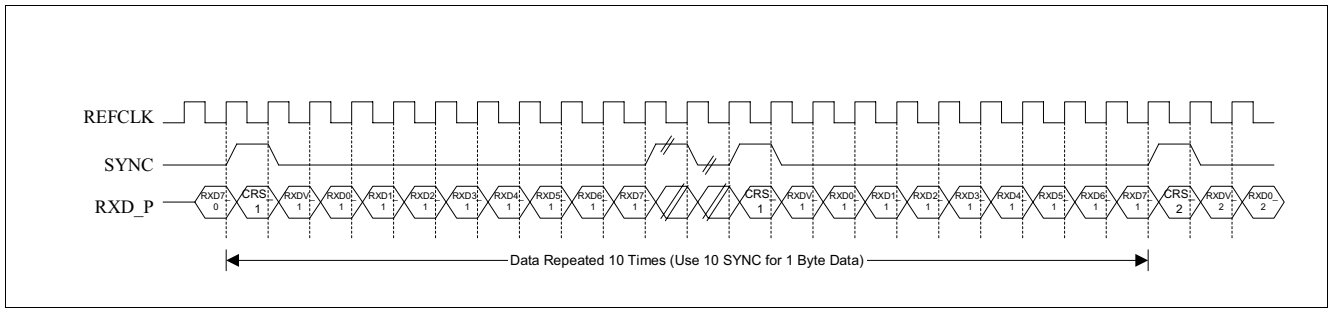


Figure 15 10M SMII Receive Timing Diagram

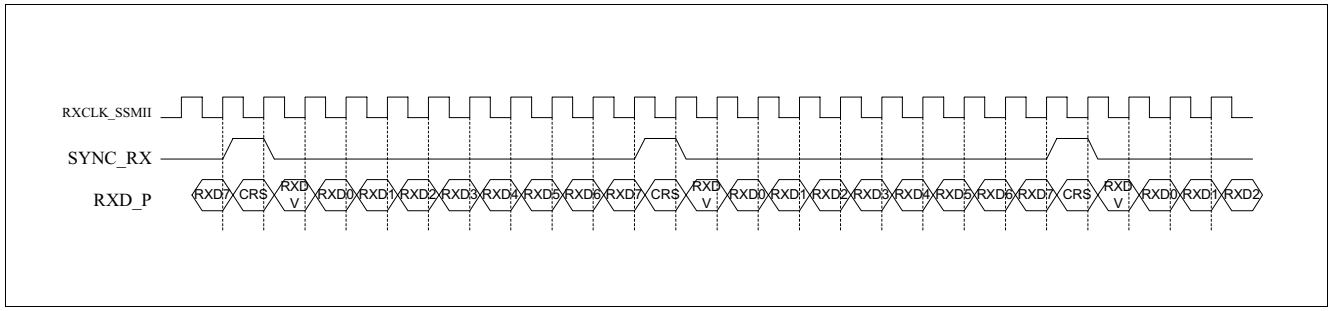


Figure 16 10M SS_SMII Receive Timing Diagram

3.2.9 100M Transmit Path

Similar to 100M Receive path, transmit data is grouped in 10-bit segments that are delimited by the SYNC signal (or TX_SYNC in SS_SMII mode), each segment represents a new byte of data. See **Figure 17** for 100M SMII transmit timing diagram and **Figure 18** for SS_SMII timing diagram.

In SS_SMII mode, REFCLK and SYNC are no longer commonly used for both transmit and receive blocks. They are renamed to TXCLK and TX_SYNC. When TXEN bit is low, data on TXD[7:0] will be ignored by ADM7008/X. See **Table 17** transmit data encoding for more detail.

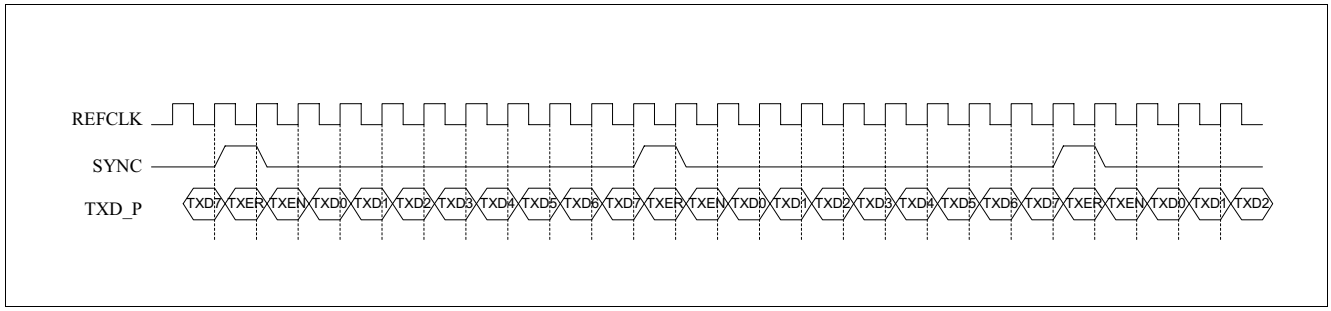


Figure 17 100M SMII Transmit Timing Diagram

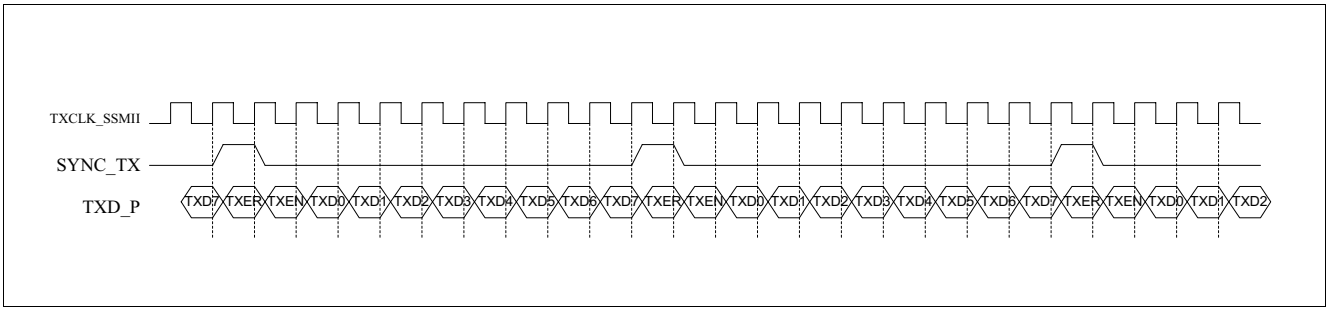


Figure 18 100M SS_SMII Transmit Timing Diagram

3.2.10 10M Transmit Path

In 10Base-T mode, each segment must be repeated 10 times by the MAC. In this mode, the MAC must generate the same data in each of the 10 segments. ADM7008/X will sample the incoming data at the 5th SYNC (or SYNC_TX) location.

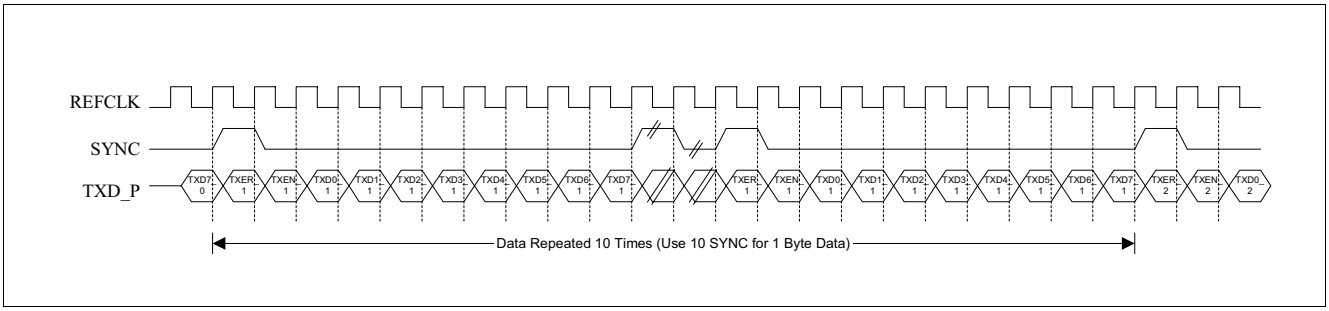


Figure 19 10M SMII Transmit Timing Diagram

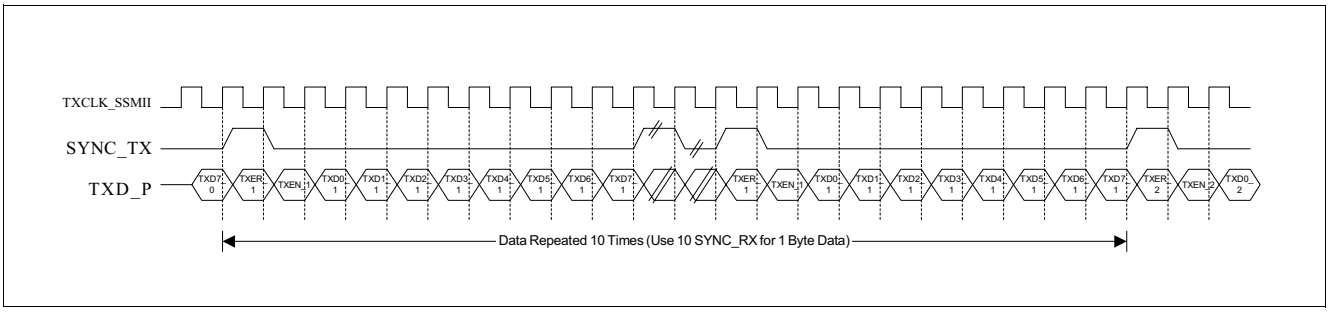


Figure 20 10M SS_SMII Transmit Timing Diagram

3.3 LED Display

Register 19 is used for different mode LED display. There are two kind of led display mechanisms provided by ADM7008/X: single and dual color LED mode, either mode provides power on LED self test to minimize and ease the system test LED cost.

3.3.1 Single Color LED

When Single Color LED is programmed (DUALLED is set to low during power on reset), all ports LED will be Off during power on reset (Output value same as recommend value on LED pins). After power on reset, all internal parallel LEDs will be On for 2 seconds, internal parallel LED status will be streamed out through LED_DATA and this signal is output by ADM7008/X at the falling edge of LED_CLK. Before describing the serial LED output data format, we tend to describe the meaning of internal parallel LEDs.

There are three types of LED supported by ADM7008/X internally. The first is LNKACT, which represents the status of Link and Transmit/Receive Activity; the second is SPDLED, which indicates the speed status and the last is DUPCOL, which shows pure duplex status in full duplex and duplex/collision combined status in half duplex. All these three LED can be controlled by Register 19 to change display contents.

After LED self test, **Table 17**, **Table 18** and **Table 19** show the On/Off polarity according to different recommended value setting for SPDLED, DUPCOL and LNKACT. When the recommend value is high, ADM7008/X will drive LED LOW; ADM7008/X will drive the LED HIGH when the recommend value is low, instead.

Table 17 Speed LED Display

SPEED	SPDLED
10M	1
100M	0
LINK FAIL	1

Table 18 Duplex LED Display

DUPLEX	DUPCOL	
	HALF	FULL
LINK UP	Blink (HIGH) When Collision	LOW All the Time
LINK FAIL	HIGH All the Time	HIGH All the Time

Table 19 Activity/Link LED Display

SPEED	Link/Activity	
	Link	Activity
LINK UP	LOW	Blink (HIGH) When RX/TX
LINK FAIL	HIGH All the Time	HIGH All the Time

3.3.2 Dual Color LED

When Dual Color LED is programmed (DUALLED is set to high during power on reset), all ports LED will be off during power on reset (Output high on LNKACT and SPDLED and output recommend value on DUPCOL). After power on reset, all LEDs will be on for 1 seconds to test 10M mode LNKACT/SPDLED connection and on for another 1 second to test 100M mode LNKACT/SPDLED wire connection. This period allow manufacture operator to check whether the LED wire connection on PCB board is correct or not.

After LED self-test, **Table 20** and **Table 21** show the On/Off polarity according to different speed detected by ADM7008/X. DUPCOL is always set to single color mode display no matter the value of DUALLED is.

Table 20 Speed LED Display

SPEED	SPDLED
10M	0
100M	1
LINK FAIL	0

Table 21 Activity/Link LED Display

SPEED	LNKACT	
	Link	Activity
100M LINK UP	LOW	Blink (HIGH) When RX/TX
10M LINK_UP	HIGH	Blink (LOW) When RX/TX
LINK FAIL	Low All the Time	Low All the Time

3.3.3 Serial Output LED Status

Internal LED status will be streamed output through two pins – LED_DATA and LED_CLK, where LED_DATA is used to indicate internal 8 port LED status and synchronous to LED_CLK.

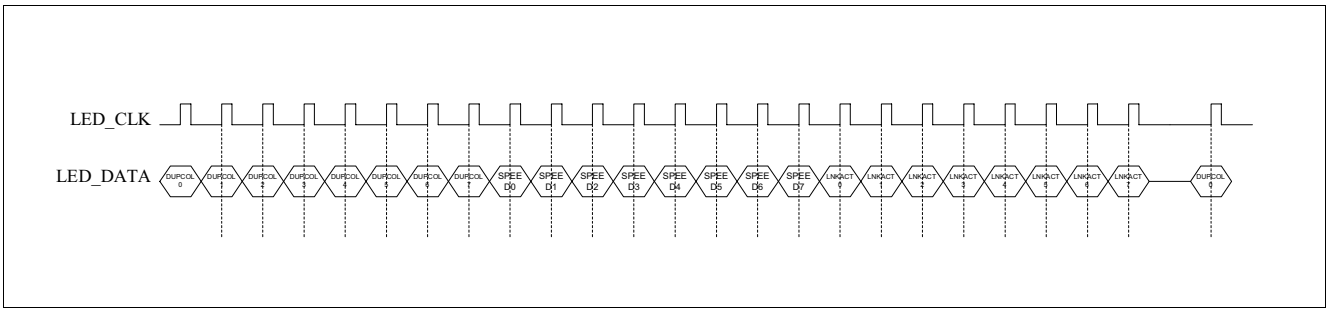


Figure 21 Stream LED under RMII Mode

The high duration for LED_CLK is 40 ns and the low duration is 600 ns to form 640 ns period clock. ADM7008/X will burst 24 bit status in one time in order to display internal LINK/Activity, Duplex/Collision and Speed status. When a burst is completed, LED_CLK will keep low for 40 ms and system can use it to distinguish between two bursts.

3.4 Management Register Access

The SMI consists of two pins, management data clock (MDC) and management data input/output (MDIO). The ADM7008/X is designed to support an MDC frequency specified in the IEEE specification of up to 2.5 MHz. The MDIO line is bi-directional and may be shared by up to 32 devices.

The MDIO pin requires a 1.5 kΩ pull-up which, during idle and turnaround periods, will pull MDIO to a logic one state. Each MII management data frame is 64 bits long. The first 32 bits are preamble consisting of 32 contiguous logic one bits on MDIO and 32 corresponding cycles on MDC. Following preamble is the start-of-frame field indicated by a <01> pattern. The next field signals the operation code (OP): <10> indicates read from MII management register operation, and <01> indicates write to MII management register operation. The next two fields are PHY device address and MII management register address. Both of them are 5-bits wide and the most significant bit is transferred first.

During Read operation, a 2-bit turn around (TA) time spacing between the register address field and data field is provided for the MDIO to avoid contention. Following the turnaround time, a 16-bit data stream is read from or written into the MII management registers of the ADM7008/X.

3.4.1 Preamble Suppression

The ADM7008/X supports a preamble suppression mode as indicated by an 1 in bit 6 of the basic mode status register (Register 1_H). If the station management entity (i.e. MAC or other management controller) determines that all PHYs in the system support preamble suppression by reading a 1 in this bit, then the station management entity needs not generate preamble for each management transaction. The ADM7008/X requires a single initialization sequence of 32 bits of preamble following powerup/hardware reset. This requirement is generally met by pulling-

up the resistor of MDIO. While the ADM7008/X will respond to management accesses without preamble, a minimum of one idle bit between management transactions is required as specified in IEEE 802.3u.

When ADM7008/X detects that there is physical address match, then it will enable Read/Write capability for external access. When neither physical address nor register address is matched, then ADM7008/X will tristate the MDIO pin.

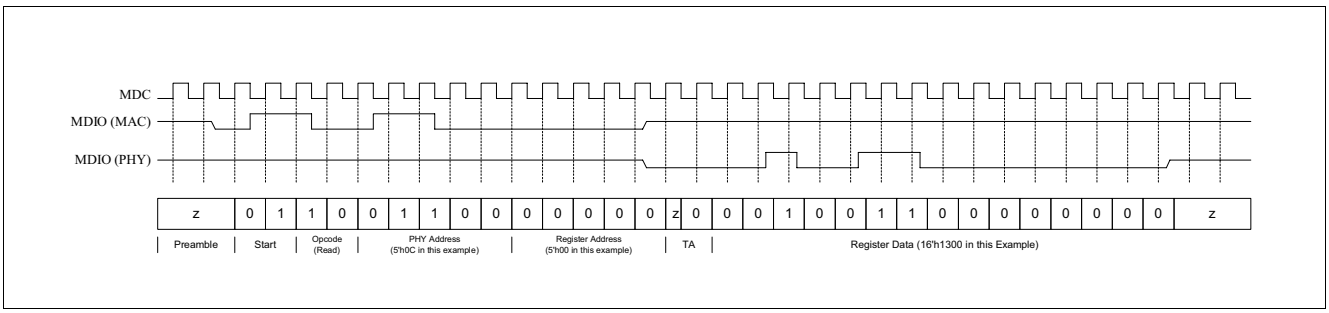


Figure 22 SMII Read Operation

3.4.2 Reset Operation

The ADM7008/X can be reset either by hardware or software. A hardware reset is accomplished by applying a negative pulse, with duration of at least 100 ms to the $\overline{RST}$ pin of the ADM7008/X during normal operation to guarantee internal Power On Reset Circuit is reset well. Software reset is activated by setting the reset bit in the basic mode control register (bit 15, register 0_H). This bit is self-clearing and, when set, will return a value of 1 until the software reset operation has completed, please note that internal SRAM will not be reset during software reset.

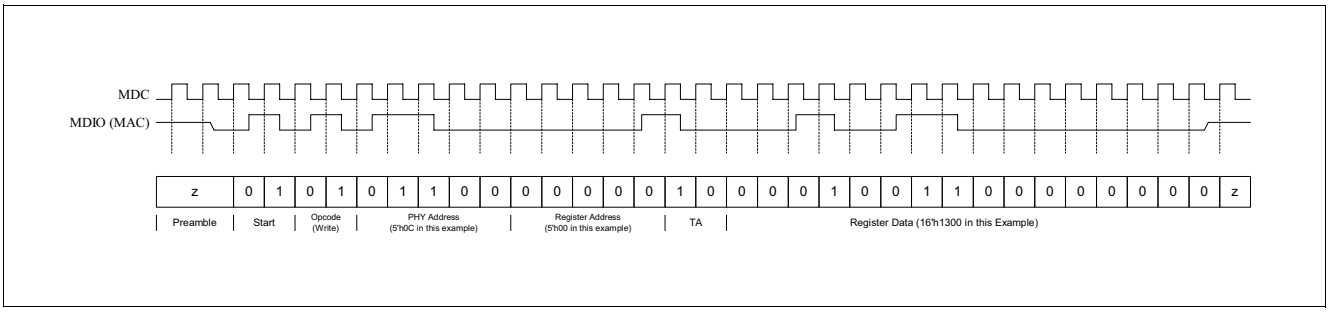


Figure 23 SMII Write Operation

Hardware reset operation samples the pins and initializes all registers to their default values. This process includes re-evaluation of all hardware configurable registers. A hardware reset affects all the eight PHYs in the device.

A software reset can reset an individual PHY and it does not latch the external pins nor reset the registers to their respective default value.

Logic levels on several I/O pins are detected during a hardware reset to determine the initial functionality of ADM7008/X. Some of these pins are used as output ports after reset operation.

Care must be taken to ensure that the configuration setup will not interfere with normal operation. Dedicated configuration pins can be tied to VCC or Ground directly. Configuration pins multiplexed with logic level output functions should be either weakly pulled up or weakly pulled down through resistors. Configuration pins multiplexed with LED outputs should be set up with one of the following circuits shown in **Figure 23**.

3.5 Power Management

There are two types of power saving mode provided by ADM7008/X: Receive Power Saving (So Called Medium Detect Power Saving) and Transmit Power Saving Mode (So Called Low Power Link Pulse power saving mode).

3.5.1 Medium Detect Power Saving

An analog block is designed for carrier sense detecting. When there is no carrier sense presented on medium (cable not attached), then “SIGNAL DETECT” will not be ON. Whenever cable is attached to ADM7008/X and the voltage threshold is above ± 50 mV, then SD will be asserted HIGH to indicate that there is cable attached to ADM7008/X. All internal blocks except Management block will be disabled (reset) before SD is asserted.

When SD is asserted, internal Auto Negotiation block will be turned on and the 10M transmit driver will also be turned on for auto negotiation process. Auto negotiation will issue control signals to control 10M receive and 100M A/D block according to different state in arbitration block diagram. During auto negotiation, all digital blocks except management and link monitor blocks will be disabled to reduce power consumption.

Whenever operating speed is determined (Either auto negotiation is On or Off), the non-active speed relative circuit will be disabled all the time to save more power. For example, when corresponding port is operating on 10M, then 100M relative blocks will be disabled and 10M relative blocks will be disabled whenever corresponding port is in 100M mode. Auto negotiation block will be reset when SD signal goes from high to low. See **Figure 24** for the state diagram for this algorithm.

3.5.2 Transmit Power Saving

In ADM7008/X, enabling TX Power Saving Feature could save transmit power before any link partner trying to link up. Two transmit power saving methods are applied to ADM7008/X by register 17.5 configuration. When setting register 17.5 to “0”, the transmit- driver will lower the driving current all the time to save power before the receiver detects signals coming in. When setting to “1”, ADM7008/X transmit Low-power Link Pulse (LLP) to the cable. The waveform of LLP is the same as NLP and FLP, the difference is the period of LLP is around 100 ms. Besides the longer period, ADM7008/X also lower the transmit-driving current between sending a pulse and a pulse. The TX Power Saving Feature is activated by setting ADM7008/X of N-way or 10M capabilities. See **Figure 25** for reference.

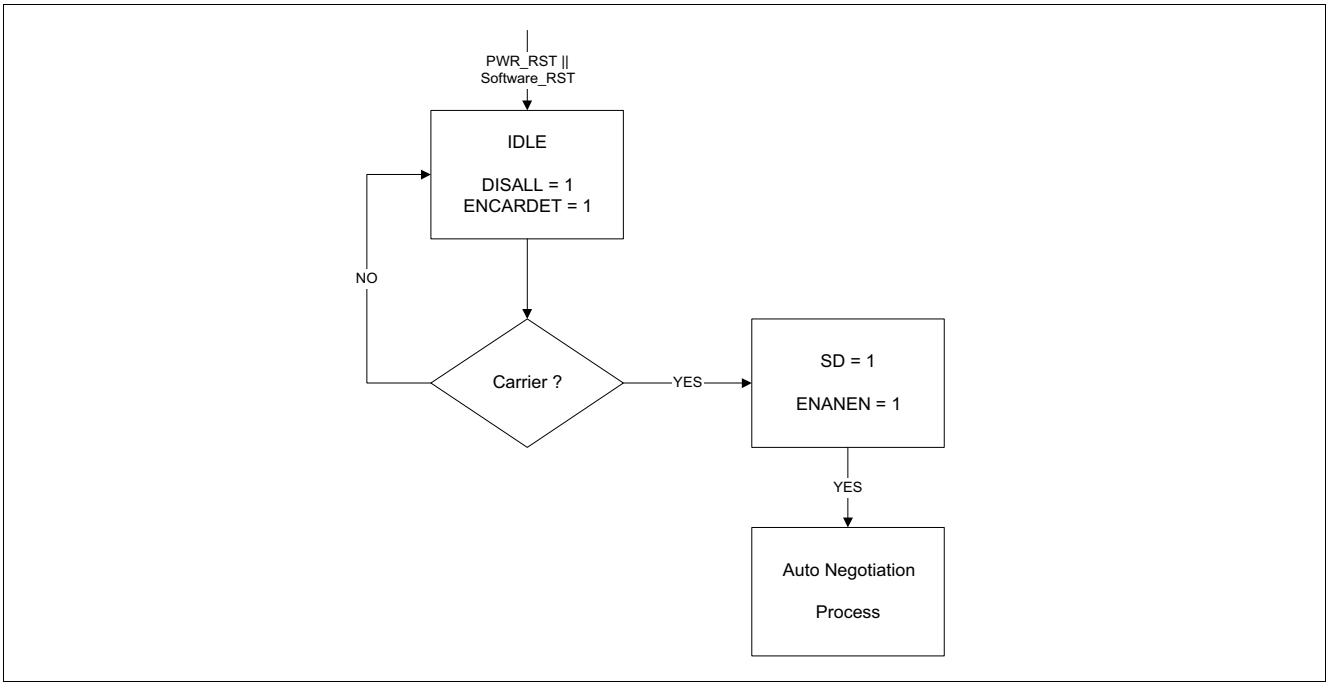


Figure 24 Medium Detect Power Management Flow Chart

Another way to reduce instant power is to separate the LED display period. All 24 LEDs will be divided into 24 time frame and each time frame occupies 1 us. One and only one LED will be driven at each time frame to reduce instant current consumed from LED.

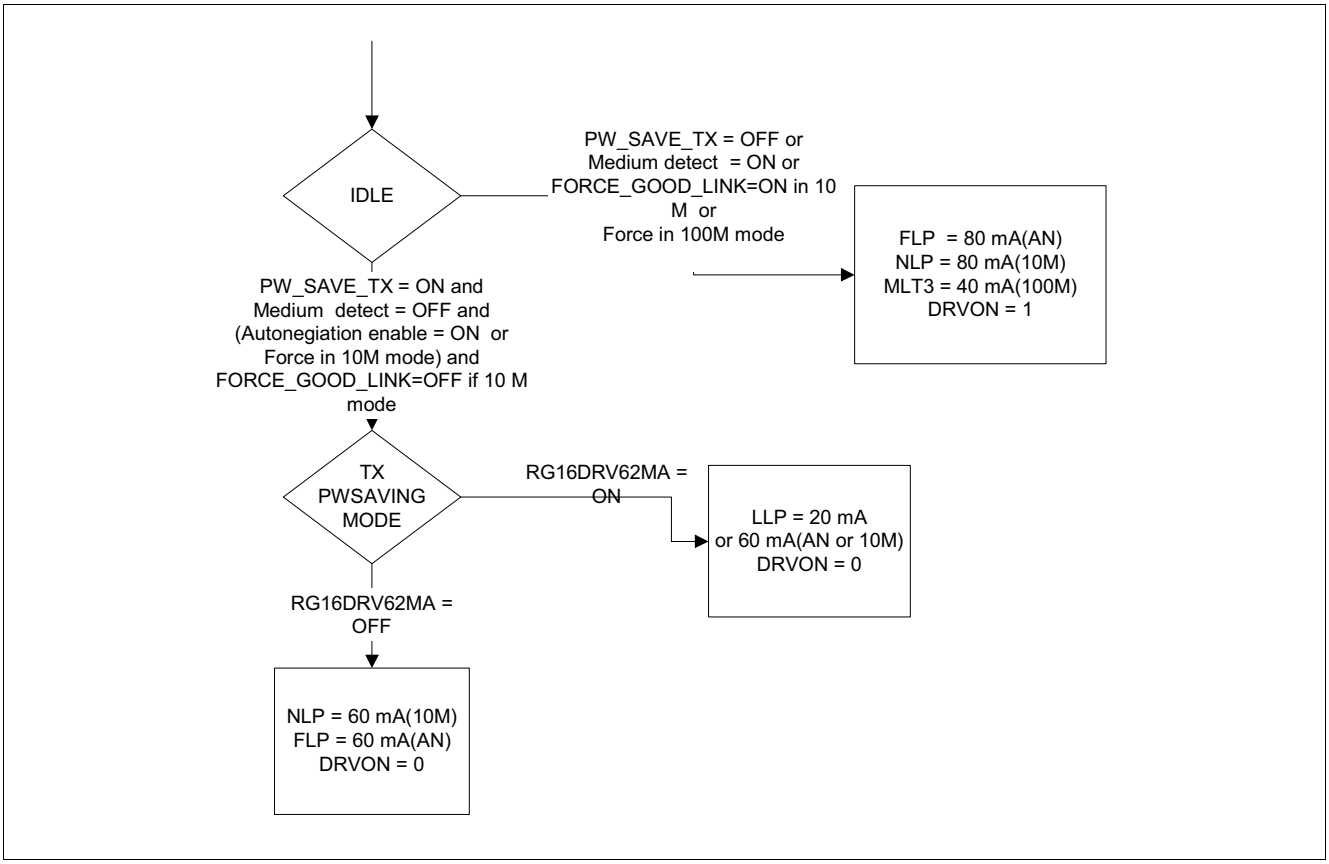


Figure 25 Low Power Link Pulse during TX for Power Management

3.5.3 Voltage Regulator

ADM7008/X requires two different levels, 3.3 V and 1.8 V, of voltage supply to provide the power to different parts of circuitry inside the chip. ADM7008/X has a build-in voltage regulator circuitry to generate the 1.8 V voltage from 3.3 V power source. Therefore, an external PNP power transistor is also needed and the block diagram of voltage regulator is shown as below.

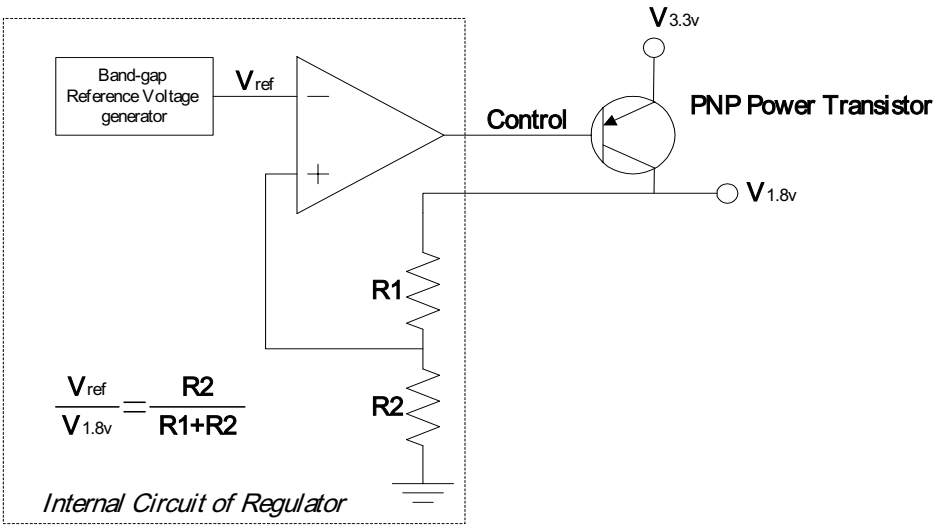


Figure 26 External PNP Power Transistor Diagram

4 Registers Descriptions

Table 22 Registers Address SpaceRegisters Address Space

Module	Base Address	End Address	Note
PHY	0000_H	$001F_H$	

Table 23 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
CR	Control Register	00_H	**73**
SR	Status Register	01_H	**75**
PHY_IR0	PHY Identifier Register 0	02_H	**77**
PHY_IR1	PHY Identifier Register 1	03_H	**77**
Advertisement	Advertisement	04_H	**78**
ANLPA	Auto Negotiation Link Partner Ability	05_H	**79**
ANER	Auto Negotiation Expansion Register	06_H	**80**
Res0	Reserved 0	07_H	**80**
Res1	Reserved 1	08_H	**81**
Res2	Reserved 2	09_H	**81**
Res3	Reserved 3	$0A_H$	**81**
Res4	Reserved 4	$0B_H$	**81**
Res5	Reserved 5	$0C_H$	**81**
Res6	Reserved 6	$0D_H$	**81**
Res7	Reserved 7	$0E_H$	**81**
Res8	Reserved 8	$0F_H$	**81**
GPCR	Generic PHY Configuration Register	10_H	**81**
P10_MCR	PHY 10M Module Configuration Register	11_H	**83**
P100_MCR	PHY 100M Module Control Register	12_H	**84**
LCR	LED Configuration Register	13_H	**84**
IER	Interrupt Enable Register	14_H	**87**
Res9	Reserved 9	15_H	**81**
PGSR	PHY Generic Status Register	16_H	**88**
PSSR	PHY Specific Status Register	17_H	**89**
PRVSR	PHY Recommend Value Status Register	18_H	**90**
ISR	Interrupt Status Register	19_H	**91**
Res10	Reserved 10	$1A_H$	**81**
Res11	Reserved 11	$1B_H$	**81**
Res12	Reserved 12	$1C_H$	**81**
RECR	Receive Error Counter Register	$1D_H$	**92**
PPIARIR	Per Port Interrupt and Revision ID Register	$1E_H$	**93**
CIR	Chip ID Register	$1F_H$	**93**

The register is addressed wordwise.

Table 24 Register Access Types

Mode	Symbol	Description HW	Description SW
read/write	rw	Register is used as input for the HW	Register is read and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latch high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latch high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latch high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latch high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiate the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiate the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiate the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiate the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is read and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is read and writable by SW.

Table 25 Registers Clock DomainsRegisters Clock Domains

Clock Short Name	Description

4.1 Registers Descriptions

Control Register

CR	Offset	Reset Value
Control Register	00_H	3100_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST	LPBK	SSL	ANEN	PDN	ISO	RAN	DPLX	CT	SSM	Res					
rwsc	rw	rw	rw	rw	rw	rwsc	rw	rw	ro	ro					

Field	Bits	Type	Description
RST	15	rwsc	**RESET** Setting this bit initiates the software reset function that resets the selected port, except for the phase-locked loop circuit. It will re-latch in all hardware configuration pin values. The software reset process takes 25 μ s to complete. This bit, which is self-clearing, returns a value of 1 until the reset process is complete. 0_B **RST_0**, Normal operation 1_B **RST_1**, PHY Reset
LPBK	14	rw	**Back Enable** This bit controls the PHY loop back operation that isolates the network transmitter outputs (TXP and TXN) and routes the MII transmit data to the MII receive data path. This function should only be used when auto negotiation is disabled (bit12 = 0). The specific PHY (10Base-T or 100Base-X) used for this operation is determined by bits 12 and 13. 0_B **LPBK_0**, Disable Loop back mode 1_B **LPBK_1**, Enable loop back mode
SSL	13	rw	**Speed Selection LSB** SPEED_LSB 0.60.13 Link speed is selected by this bit or by auto negotiation if bit 12 of this register is set (in which case, the value of this bit is ignored). 00_B **10M**, 10 Mbit/s 01_B **100M**, 100 Mbit/s 10_B **1000M**, 1000 Mbit/s 11_B **Res**, Reserved
ANEN	12	rw	**Auto Negotiation Enable** This bit determines whether the link speed should set up by the auto negotiation process or not. It is set at power up or reset if the PI_RECANEN pin detects a logic 1 input level in Twisted-Pair Mode. 0_B **ANEN_0**, Disable Auto negotiation process 1_B **ANEN_1**, Enable auto negotiation process

Field	Bits	Type	Description
PDN	11	rw	**Power Down Enable** Ored result with PI_PWRDN pin. Setting this bit high or asserting the PI_PWRDN puts the PHY841F into power down mode. During the power down mode, TXP/TXN and all LED outputs are tristated and the MII/RMII interfaces are isolated. 0_B **PDN_0**, Normal Operation 1_B **PDN_1**, Power Down
ISO	10	rw	**Isolate PHY841F from Network** Setting this control bit isolates the part from the RMII/MII, with the exception of the serial management interface. When this bit is asserted, the PHY841F does not respond to TXD, TXEN and TXER inputs, and it presents a high impedance on its TXC, RXC, CRSDV, RXER, RXD, COL and CRS outputs. 0_B **ISO_0**, Normal Operation 1_B **ISO_1**, Isolate PHY from MII/RMII
RAN	9	rwsc	**Restart Auto Negotiation** ANEN_RST. Setting this bit while auto negotiation is enabled forces a new auto negotiation process to start. This bit is self-clearing and returns to 0 after the auto negotiation process has commenced. 0_B **RAN_0**, Normal Operation 1_B **RAN_1**, Restart Auto Negotiation Process
DPLX	8	rw	**Duplex Mode** If auto negotiation is disabled, this bit determines the duplex mode for the link. 0_B **DPLX_0**, Half Duplex mode 1_B **DPLX_1**, Full Duplex mode
CT	7	rw	**Collision Test** When set, this bit will cause the COL signal of MII interface to be asserted in response to the assertion of TXEN. 0_B **CT_0**, Disable COL signal test 1_B **CT_1**, Enable COL signal test
SSM	6	ro	**Speed Selection MSB** SPEED_MSB. Set to 0 all the time indicate that the PHY841F does not support 1000 Mbit/s function.
Res	5:0	ro	**Reserved** Not Applicable

Status Register

SR	Offset	Reset Value
Status Register	01_H	7849_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T4	**TXF**	**TXH**	**TF**	**TH**	**T2**	Res			**SUPR**	**AN_C**	Res	**ANEG**	**LINK**	**JAB**	**XTND**
ro	ro	ro	ro	ro	ro	ro			ro	ro	ro	ro	ro, ll	ro, lh	ro

Field	Bits	Type	Description
T4	15	ro	**100Base-T4 Capable** Set to 0 all the time to indicate that the PHY841F does not support 100Base-T4.
TXF	14	ro	**100Base-X Full Duplex Capable** Set to 1 all the time to indicate that the PHY841F does support Full Duplex mode.
TXH	13	ro	**100Base-X Half Duplex Capable** Set to 1 all the time to indicate that the PHY841F does support Half Duplex mode
TF	12	ro	**10M Full Duplex Capable** TP: Set to 1 all the time to indicate that the PHY841F does support 10M Full Duplex mode. FX: Set to 0 all the time to indicate that the PHY841F does not support 10M Full Duplex mode
TH	11	ro	**10M Half Duplex Capable** TP: Set to 1 all the time to indicate that the PHY841F does support 10M Half Duplex mode. FX: Set to 0 all the time to indicate that the PHY841F does not support 10M Half Duplex mode
T2	10	ro	**100Base-T2 Capable** Set to 0 all the time to indicate that the PHY841F does not support 100Base-T2.
Res	9:7	ro	**Reserved** Not Applicable
SUPR	6	ro	**MF Preamble Suppression Capable** This bit is hardwired to 1 indicating that the PHY841F accepts management frame without preamble. Minimum 32 preamble bits are required following power-on or hardware reset. One idle bit is required between any two management transactions as per IEEE 802.3u specification.

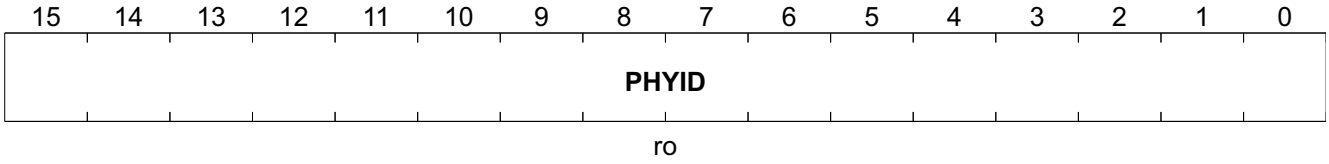
Field	Bits	Type	Description
AN_C	5	ro	**Auto Negotiation Complete** If auto negotiation is enabled, this bit indicates whether the auto negotiation process has been completed or not. Set to 0 all the time when Fiber Mode is selected. 0_B **AN_C_0**, Auto Negotiation process not completed 1_B **AN_C_1**, Auto Negotiation process completed
Res	4	ro	**Reserved** Not Applicable
ANEG	3	ro	**Auto Negotiation Ability** TP: This bit is set to 1 all the time, indicating that PHY841F is capable of auto negotiation. FX: This bit is set to 0 all the time, indicating that PHY841F is not capable of auto negotiation in Fiber Mode. 0_B **ANEG_0**, Not capable of auto negotiation 1_B **ANEG_1**, Capable of auto negotiation
LINK	2	ro, ll	**Link Status** This bit reflects the current state of the link -test-fail state machine. Loss of a valid link causes a 0 latched into this bit. It remains 0 until this register is read by the serial management interface. Whenever Linkup, this bit should be read twice to get link up status 0_B **LINK_0**, Link is down 1_B **LINK_1**, Link is up
JAB	1	ro, lh	**ll Jabber Detect** 0_B **JAB_0**, Jabber condition not detected 1_B **JAB_1**, Jabber condition detected
XTND	0	ro	**Extended Capability** This bit defaults to 1, indicating that the PHY841F implements extended registers. 0_B **XTND_0**, No extended register set 1_B **XTND_1**, Extended register set

PHY Identifier

PHY_IR0 — **PHY Identifier Register 0**

Offset 02_H

Reset Value $002E_H$



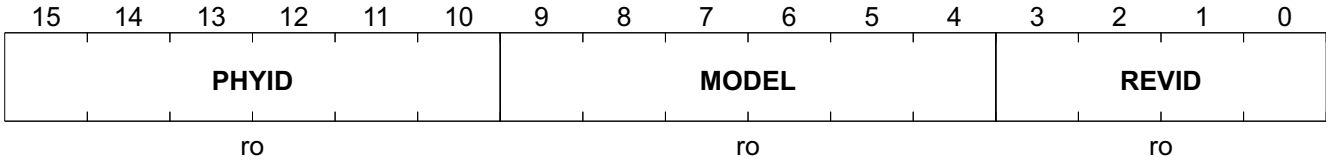
Field	Bits	Type	Description
PHYID	15:0	ro	**PHY-ID** IEEE Address

PHY Identifier Register 1

PHY_IR1 — **PHY Identifier Register 1**

Offset 03_H

Reset Value $CC23_H$



Field	Bits	Type	Description
PHYID	15:10	ro	**PHY-ID 15:0** IEEE Address/Model No./Rev. No.
MODEL	9:4	ro	**MODEL 5:0** ADMTEK PHY Revision ID.
REVID	3:0	ro	**REV-ID 3:0** ADMTEK PHY Revision ID.

Advertisement

Advertisement	Offset	Reset Value
Advertisement	04_H	$01E1_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NP	Res	**RF**	Res	**APD**	**PSE**	**T4**	**TXF**	**TXD**	**TF**	**TD**	**Sel**				
rw	ro	rw	ro	rw	rw	ro	rw	rw	rw	rw	ro				

Field	Bits	Type	Description
NP	15	rw	**Next Page** This bit is defaults to 1, indicating that PHY841F is next page capable.
Res	14	ro	**Reserved** Not Applicable
RF	13	rw	**Remote Fault** This bit is written by serial management interface for the purpose of communicating the remote fault condition to the auto negotiation link partner. 0_B **NRFD**, No remote fault has been detected 1_B **RFD**, Remote Fault has been detected
Res	12	ro	**Reserved** Not Applicable
APD	11	rw	**Asymmetric Pause Direction** Bit[11:10] Capability 00_B **NP**, No Pause 01_B **SP**, Symmetric PAUSE 10_B **AP**, Asymmetric PAUSE toward Link Partner 11_B **BSP**, Both Symmetric PAUSE and Asymmetric PAUSE toward local device
PSE	10	rw	**Pause Operation for Full Duplex** Value on PAUREC will be stored in this bit during power on reset.
T4	9	ro	**Technology Ability for 100Base-T4** Defaults to 0.
TXF	8	rw	**100Base-TX Full Duplex** 0_B **NCFDO**, Not capable of 100M Full duplex operation 1_B **CFDO**, Capable of 100M Full duplex operation
TXD	7	rw	**100Base-TX Half Duplex** 0_B **TXD_0**, Not capable of 100M operation 1_B **TXD_1**, Capable of 100M operation
TF	6	rw	**10Base-T Full Duplex** 0_B **TF_0**, Not capable of 10M full duplex operation 1_B **TF_1**, Capable of 10M Full Duplex operation

Field	Bits	Type	Description
TD	5	rw	**10Base-T Half Duplex** 0_B **TD_0**, Not capable of 10M operation 1_B **TD_1**, Capable of 10M operation
Sel	4:0	ro	**Selector Field** These 5 bits are hardwired to 00001b, indicating that the PHY841F supports IEEE 802.3 CSMA/CD.

Auto Negotiation Link Partner Ability

ANLPA	Offset	Reset Value
Auto Negotiation Link Partner Ability	**05_H**	**$01E1_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NPG	**ACK**	**RF**	Res	**LPAP**	**LPP**	**LPTA**	**TXF**	**TXD**	**TF**	**TD**	**Sel**				
ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro				

Field	Bits	Type	Description
NPG	15	ro	**Next Page** 0_B **NPG_0**, Not capable of next page function 1_B **NPG_1**, Capable of next page function
ACK	14	ro	**Acknowledge** 0_B **ACK_0**, Not acknowledged 1_B **ACK_1**, Link Partner acknowledges reception of the ability data word
RF	13	ro	**Remote Fault** 0_B **RF_0**, No remote fault has been detected 1_B **RF_1**, Remote Fault has been detected
Res	12	ro	**Reserved** Not Applicable
LPAP	11	ro	**Link Partner Asymmetric Pause Direction**
LPP	10	ro	**Link Partner Pause Capability** Value on PAUREC will be stored in this bit during power on reset.
LPTA	9	ro	**Link Partner Technology Ability for 100Base-T4** Defaults to 0.
TXF	8	ro	**100Base-TX Full Duplex** 0_B **TXF_0**, Not capable of 100M Full duplex operation 1_B **TXF_1**, Capable of 100M Full duplex operation
TXD	7	ro	**100Base-TX Half Duplex** 1_B **TXD_1**, Capable of 100M operation 0_B **TXD_2**, Not capable of 100M operation
TF	6	ro	**10Base-T Full Duplex** 1_B **TF_1**, Capable of 10M Full Duplex operation 0_B **TF_0**, Not capable of 10M full duplex operation

Field	Bits	Type	Description
TD	5	ro	**10Base-T Half Duplex** 1_B **TD_1**, Capable of 10M operation 0_B **TD_0**, Not capable of 10M operation
Sel	4:0	ro	**Encoding Definitions**

Auto Negotiation Expansion Register

ANER **Offset** **Reset Value**

Auto Negotiation Expansion Register **06_H** **0004_H**

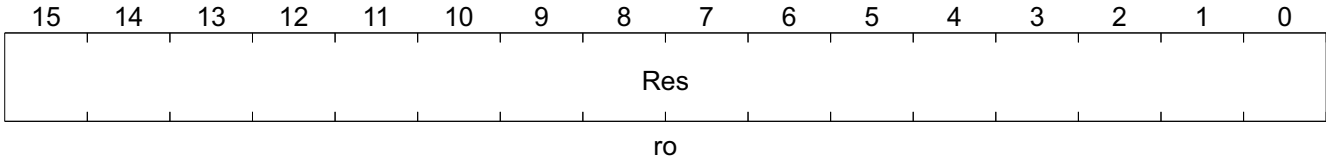
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res											PFLT	LPNP	NXPG	PRCV	LPAN
ro											ro, lh	ro	ro	ro, lh	ro

Field	Bits	Type	Description
Res	15:5	ro	**Reserved** Not Applicable
PFLT	4	ro, lh	**Parallel Detection Fault** 0_B **PFLT_0**, No Fault Detect 1_B **PFLT_1**, Fault has been detected
LPNP	3	ro	**Link Partner Next Page Able** 0_B **LPNP_0**, Link Partner is not next page capable 1_B **LPNP_1**, Link Partner is next page capable
NXPG	2	ro	**Next Page Able** 1_B **NXPG_1**, Next page Enable. 0_B **NXPG_0**, Next page Disable
PRCV	1	ro, lh	**Page Received** 0_B **PRCV_0**, No new page has been received 1_B **PRCV_1**, A new page has been received
LPAN	0	ro	**Link Partner Auto Negotiation Able** 0_B **LPAN_0**, Link Partner is not auto negotiable 1_B **LPAN_1**, Link Partner is auto negotiable

Reserved 0

Res0 **Offset** **Reset Value**

Reserved 0 **07_H** **$Reserved_H$**



Field	Bits	Type	Description
Res	15:0	ro	**Reserved** Not Applicable

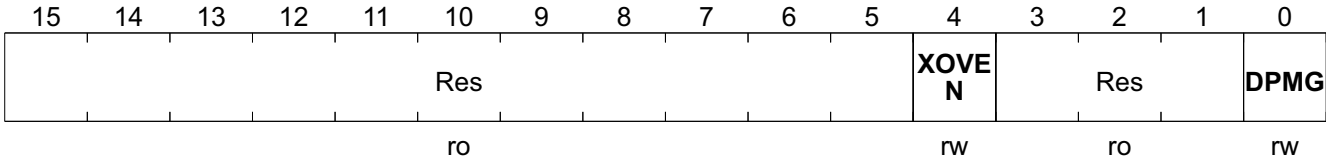
Table 26 Reserved Registers

Register Short Name	Register Long Name	Offset Address	Page Number
Res1	Reserved 1	08_H	
Res2	Reserved 2	09_H	
Res3	Reserved 3	$0A_H$	
Res4	Reserved 4	$0B_H$	
Res5	Reserved 5	$0C_H$	
Res6	Reserved 6	$0D_H$	
Res7	Reserved 7	$0E_H$	
Res8	Reserved 8	$0F_H$	
Res9	Reserved 9	15_H	
Res10	Reserved 10	$1A_H$	
Res11	Reserved 11	$1B_H$	
Res12	Reserved 12	$1C_H$	

Generic PHY Configuration Register

Note: PHY Control/Configuration Registers start from address 16 to 21.

GPCR	Offset	Reset Value
Generic PHY Configuration Register	**10_H**	**1000_H**

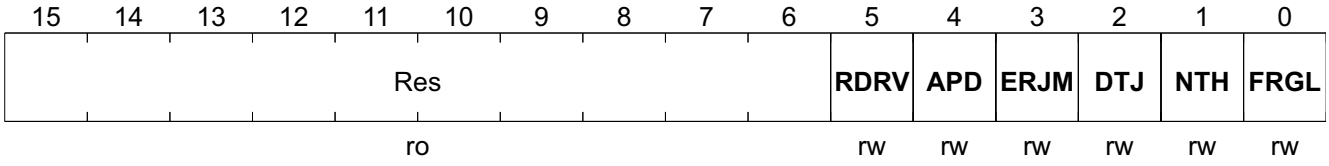


Field	Bits	Type	Description
Res	15:5	ro	**Reserved** Not Applicable

Field	Bits	Type	Description
XOVEN	4	rw	**Cross Over Auto Detect Enable** 0_B **XOAD_0**, Disable 1_B **XOAD_1**, Enable
Res	3:1	ro	**Reserved** Not Applicable
DPMG	0	rw	**Disable Power Management Feature** 0_B **DPMG_0**, Enable. Enable Medium Detect Function. 1_B **DPMG_1**, Disable. Medium_On is high all the time.

PHY 10M Module Configuration Register

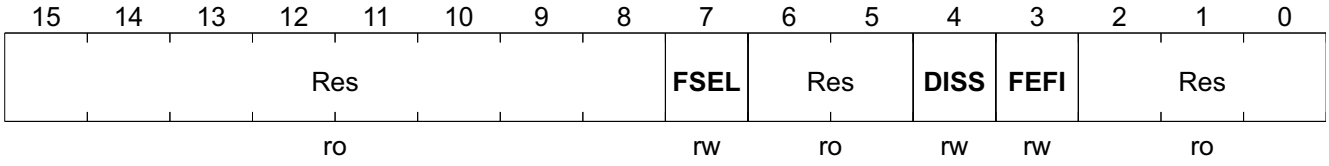
P10_MCR	Offset	Reset Value
PHY 10M Module Configuration Register	11_H	0008_H



Field	Bits	Type	Description
Res	15:6	ro	**Reserved** Not Applicable
RDRV	5	rw	**Reduce 10M Driver to 62 mA** 0_B **RDRV_0**, Normal 1_B **RDRV_1**, 62 mA
APD	4	rw	**Auto Polarity Disable** 0_B **APD_0**, Normal 1_B **APD_1**, Auto Polarity Function Disabled
ERJM	3	rw	**Enable Receive Jabber Monitor** 0_B **ERJM_0**, Disable 1_B **ERJM_1**, Enable
DTJ	2	rw	**Disable Transmit Jabber** 0_B **DTJ_0**, Enable Transmit Jabber Function 1_B **DTJ_1**, Disable Transmit Jabber Function
NTH	1	rw	**Normal Threshold** 0_B **NTH_0**, Lower 10Base-T Receive threshold 1_B **NTH_1**, Normal 10Base-T Receive threshold
FRGL	0	rw	**Force 10M Receive Good Link** 0_B **FRGL_0**, Normal Operation 1_B **FRGL_1**, Force Good Link

PHY 100M Module Control Register

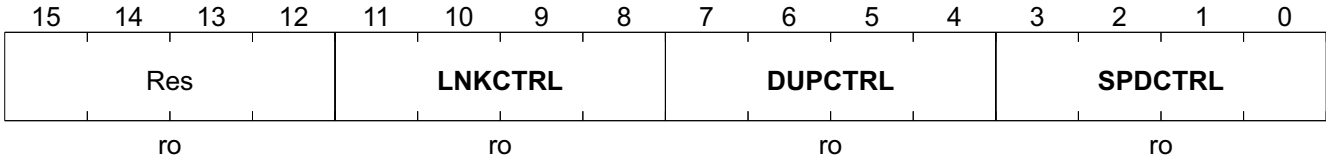
P100_MCR	Offset	Reset Value
PHY 100M Module Control Register	12_H	0022_H



Field	Bits	Type	Description
Res	15:8	ro	**Reserved** Not Applicable
FSEL	7	rw	**Fiber Select** 0_B **FSEL_0**, TP Mode 1_B **FSEL_1**, Fiber Mode
Res	6:5	ro	**Reserved** Not Applicable
DISS	4	rw	**Disable Scrambler** When set to fiber mode, this bit will be forced to 1 automatically. Write 0 to this bit in Fiber Mode has no effect. 0_B **DISS_0**, Enable Scrambler 1_B **DISS_1**, Disable Scrambler
FEFI	3	rw	**Enable FEFI** 0_B **FEFI_0**, Disable FEFI 1_B **FEFI_1**, Enable FEFI
Res	2:0	ro	**Reserved** Not Applicable

LED Configuration Register

LCR	Offset	Reset Value
LED Configuration Register	13_H	$0A34_H$



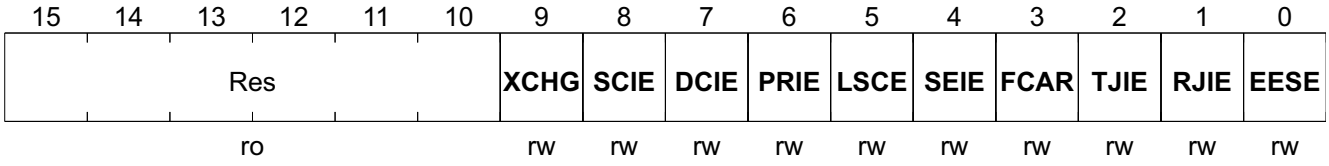
Field	Bits	Type	Description
Res	15:12	ro	**Reserved** Not Applicable

Field	Bits	Type	Description
LNKCTRL	11:8	ro	**Link/Act LED Control** 0000_B, Collision 0001_B, All Errors 0010_B, Duplex 0011_B, Duplex/Collision 0100_B, Speed 0101_B, Link 0110_B, Transmit Activity 0111_B, Receive Activity 1000_B, TX/RX Activity 1001_B, Link/Receive Activity 1010_B, Link and TX/RX Activity 1011_B, 100M False Carrier Error/10M Receive Jabber 1100_B, 100M Error End of Stream/10M Transmit Jabber 1101_B, 100M Symbol Error 1110_B, Distance (See LED Description for more detail) 1111_B, Cable Broken Distance
DUPCTRL	7:4	ro	**Duplex LED Control** 0000_B, Collision 0001_B, All Errors 0010_B, Duplex 0011_B, Duplex/Collision 0100_B, Speed 0101_B, Link 0110_B, Transmit Activity 0111_B, Receive Activity 1000_B, TX/RX Activity 1001_B, Link/Receive Activity 1010_B, Link and TX/RX Activity 1011_B, 100M False Carrier Error/10M Receive Jabber 1100_B, 100M Error End of Stream/10M Transmit Jabber 1101_B, 100M Symbol Error 1110_B, Distance (See LED Description for more detail) 1111_B, Cable Broken Distance

Field	Bits	Type	Description
SPDCTRL	3:0	ro	**Speed LED Control** 0000_B, Collision 0001_B, All Errors 0010_B, Duplex 0011_B, Duplex/Collision 0100_B, Speed 0101_B, Link 0110_B, Transmit Activity 0111_B, Receive Activity 1000_B, TX/RX Activity 1001_B, Link/Receive Activity 1010_B, Link and TX/RX Activity 1011_B, 100M False Carrier Error/10M Receive Jabber 1100_B, 100M Error End of Stream/10M Transmit Jabber 1101_B, 100M Symbol Error 1110_B, Distance (See LED Description for more detail) 1111_B, Cable Broken Distance

Interrupt Enable Register

IER	Offset	Reset Value
Interrupt Enable Register	14_H	$03FF_H$

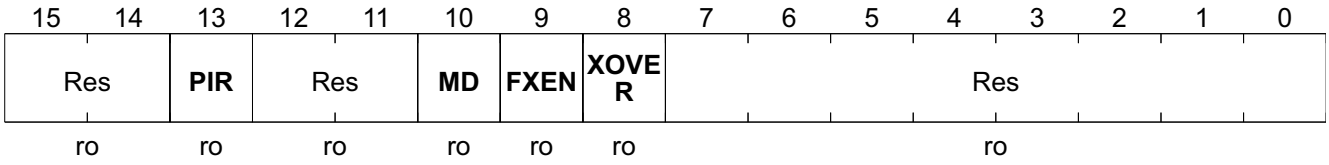


Field	Bits	Type	Description
Res	15:10	ro	**Reserved** Not Applicable
XCHG	9	rw	**Cross Over mode Changed Interrupt Enable** 0_B **XCHG_0**, Interrupt Disable 1_B **XCHG_1**, Interrupt Enable
SCIE	8	rw	**Speed Changed Interrupt Enable** 0_B **SCIE_0**, Interrupt Disable 1_B **SCIE_1**, Interrupt Enable
DCIE	7	rw	**Duplex Changed Interrupt Enable** 0_B **DCIE_0**, Interrupt Disable 1_B **DCIE_1**, Interrupt Enable
PRIE	6	rw	**Page Received Interrupt Enable** 0_B **PRIE_0**, Interrupt Disable 1_B **PRIE_1**, Interrupt Enable
LSCE	5	rw	**Link Status Changed Interrupt Enable** 0_B **LSCE_0**, Interrupt Disable 1_B **LSCE_1**, Interrupt Enable
SEIE	4	rw	**Symbol Error Interrupt Enable** 0_B **SEIE_0**, Interrupt Disable 1_B **SEIE_1**, Interrupt Enable
FCAR	3	rw	**False Carrier Interrupt Enable** 0_B **FCAR_0**, Interrupt Disable 1_B **FCAR_1**, Interrupt Enable
TJIE	2	rw	**Transmit Jabber Interrupt Enable** 0_B **TJIE_0**, Interrupt Disable 1_B **TJIE_1**, Interrupt Enable
RJIE	1	rw	**Receive Jabber Interrupt Enable** 0_B **RJIE_0**, Interrupt Disable 1_B **RJIE_1**, Interrupt Enable
EESE	0	rw	**Error End of Stream Enable** 0_B **EESE_0**, Interrupt Disable 1_B **EESE_1**, Interrupt Enable

PHY Generic Status Register

Note: PHY Status Registers start from 22 to 28 (29 to 30 reserves for further use)

PGSR	Offset	Reset Value
PHY Generic Status Register	16_H	0000_H



Field	Bits	Type	Description
Res	15:14	ro	**Reserved** Not Applicable
PIR	13	ro	**PHY Identifier Register** 0_B **PIR0**, Connection properly 1_B **PIR1**, Broken
Res	12:11	ro	**Reserved** Not Applicable
MD	10	ro	**Medium Detect** Real Time Status for Medium Detect Signal. 0_B **MD_0**, Medium_Detect Fail 1_B **MD_1**, Medium_Detect Pass
FXEN	9	ro	**Fiber Enable** Only Changed when PHY Reset. OR'ed result of PI_SELFX and 17.9 (SELFX) 0_B **FXEN_0**, TX 1_B **FXEN_1**, FX mode
XOVER	8	ro	**Cross Over Status** 0_B **XOVS_0**, MDI mode 1_B **XOVS_1**, MDIX mode
Res	7:0	ro	**Reserved** Not Applicable

PHY Specific Status Register

PSSR	Offset	Reset Value
PHY Specific Status Register	17_H	0060_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				JRX	JTX	POL	POUT	PIN	DUP	SPD	LINK	RPAU	RDUP	RSPD	RANV
ro				ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro

Field	Bits	Type	Description
Res	15:12	ro	**Reserved** Not Applicable
JRX	11	ro	**Real Time 10M Receive Jabber Status** 0_B **JRX_0**, No jabber 1_B **JRX_1**, Jabber
JTX	10	ro	**Real Time 10M Transmit Jabber Status** 0_B **JTX_0**, No Jabber 1_B **JTX_1**, Jabber
POL	9	ro	**Polarity** Only available in 10M. 0_B **POL_0**, Polarity Reversed 1_B **POL_1**, Normal Polarity
POUT	8	ro	**Pause Out Capability** Disabled when Half Duplex. 0_B **POUT_0**, Has Pause Out capability 1_B **POUT_1**, Lack of Pause Out capability
PIN	7	ro	**Pause In Capability** Disabled when Half Duplex. 0_B **PIN_0**, Has Pause In capability 1_B **PIN_1**, Lack of Pause In capability
DUP	6	ro	**Operating Duplex** 0_B **DUP_0**, Half Duplex 1_B **DUP_1**, Full Duplex
SPD	5	ro	**Operating Speed** 0_B **SPD_0**, 10Mb/s 1_B **SPD_1**, 100Mb/s
LINK	4	ro	**Real Time Link Status** 0_B **LINK_0**, Link Down 1_B **LINK_1**, Link Up
RPAU	3	ro	**Pause Recommend Value** Only Changed when PHY Reset. This bit is disabled automatically when RDUP is 0. 0_B **RPAU_0**, Pause Disable 1_B **RPAU_1**, Pause Enable

Field	Bits	Type	Description
RDUP	2	ro	**Duplex Recommended Value** Only Changed when PHY Reset. 0_B **RDUP_0**, Half Duplex 1_B **RDUP_1**, Full Duplex
RSPD	1	ro	**Speed Recommend Value** Only Changed when PHY Reset. 0_B **RSPD_0**, 10M 1_B **RSPD_1**, 100M
RANV	0	ro	**Recommended Auto Negotiation Value** Only Changed when PHY Reset.

PHY Recommend Value Status Register

PRVSR	Offset	Reset Value
PHY Recommend Value Status Register	**18_H**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWDN	**RANV**	**FSEL**	**RSPD**	**RDUP**	**PREC**	Res	**XOVR**	**XOVS**	**RSII**	Res	**PHYA**				
ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro				

Field	Bits	Type	Description
PWDN	15	ro	**Power Down Status**
RANV	14	ro	**Auto Negotiation Recommend Value**
FSEL	13	ro	**Fiber Select Recommend Value**
RSPD	12	ro	**Speed Recommend Value** 0_B **RSPD_1**, 10M 1_B **RSPD_0**, 100M
RDUP	11	ro	**Duplex Recommend Value** 0_B **RDUP_0**, Half Duplex 1_B **RDUP_1**, Full Duplex
PREC	10	ro	**Pause Capability Recommend Value** 0_B **PREC_0**, Pause Disable 1_B **PREC_1**, Pause Enable
Res	9	ro	**Reserved** Not Applicable
XOVR	8	ro	**Cross Over Capability Recommend Value** 0_B **XOVR_0**, Disable 1_B **XOVR_1**, Enable
XOVS	7	ro	**Cross Over Status** 0_B **XOVS_0**, Non-Cross Over 1_B **XOVS_1**, Cross Over

Field	Bits	Type	Description
RSII	6	ro	**RMII_SMII Interface** 0_B **RSII_0**, Non RMII_SMII Interface 1_B **RSII_1**, RMII or SMII Interface used
Res	5	ro	**Reserved** Not Applicable
PHYA	4:0	ro	**PHY Address**

Interrupt Status Register

ISR **Offset** **Reset Value**

Interrupt Status Register **19_H** **0000_H**

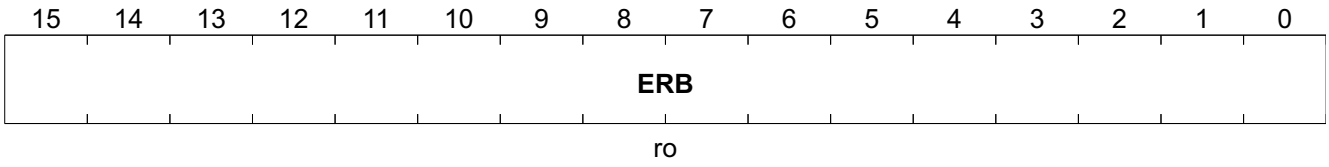
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res						XOVC	SPDC	DUPC	PREC	LNKC	SERR	FCAR	TJAB	RJAB	STRE
cor						cor	cor	cor	cor	cor	cor	cor	cor	cor	cor

Field	Bits	Type	Description
Res	15:10	cor	**Reserved** Not Applicable
XOVC	9	cor	**Cross Over mode Changed** 0_B **XOVC_0**, Cross Over mode Not Changed 1_B **XOVC_1**, Cross Over mode Changed
SPDC	8	cor	**Speed Changed** 0_B **SPDC_0**, Speed Not Changed 1_B **SPDC_1**, Speed Changed
DUPC	7	cor	**Duplex Changed** 0_B **DUPC_0**, Duplex not changed 1_B **DUPC_1**, Duplex Changed
PREC	6	cor	**Page Received** 0_B **PREC_0**, Page not received 1_B **PREC_1**, Page Received
LNKC	5	cor	**Link Status Changed** 0_B **LNKC_0**, Link Status not Changed 1_B **LNKC_1**, Link Status Changed
SERR	4	cor	**Symbol Error** 0_B **SERR_0**, No symbol Error 1_B **SERR_1**, Symbol Error
FCAR	3	cor	**False Carrier** *Note: High whenever Link is Failed* 0_B **FCAR_0**, No false carrier 1_B **FCAR_1**, False Carrier

Field	Bits	Type	Description
TJAB	2	cor	**Transmit Jabber** 0_B **TJAB_0**, No Jabber 1_B **TJAB_1**, Jabber
RJAB	1	cor	**Receive Jabber** 0_B **RJAB_0**, No Jabber 1_B **RJAB_1**, Jabber
STRE	0	cor	**Error End of Stream** 0_B **STRE_0**, No ESD Error 1_B **STRE_1**, ESD Error

Receive Error Counter Register

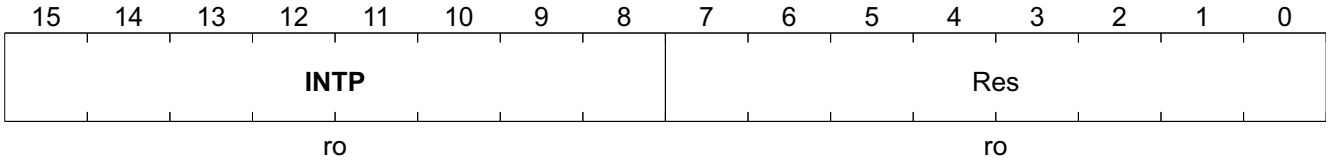
RECR	Offset	Reset Value
Receive Error Counter Register	$1D_H$	0000_H



Field	Bits	Type	Description
ERB	15:0	ro	**Error Counter** Includes. 1_H **100MFC**, 100M False Carrier 2_H **100MSE**, 100M Symbol Error 3_H **10MTJ**, 10M Transmit Jabber 4_H **10MRJ**, 10M Receive Jabber 5_H **ESS**, Error Start of Stream 6_H **EES**, Error End of Stream

Per Port Interrupt and Revision ID Register

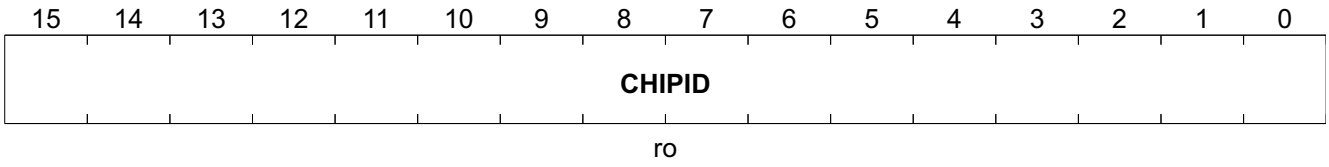
PPIARIR	Offset	Reset Value
Per Port Interrupt and Revision ID Register	$1E_H$	8818_H



Field	Bits	Type	Description
INTP	15:8	ro	**Per Port Interrupt Status 7:0** Only available in Port 0. 0_B **INACP**, Interrupt not asserted in corresponding port 1_B **IACP**, Interrupt asserted in corresponding port
Res	7:0	ro	**Reserved** Not Applicable.

Chip ID Register

CIR	Offset	Reset Value
Chip ID Register	$1F_H$	0000_H



Field	Bits	Type	Description
CHIPID	15:0	ro	**CHIPID 15:0**

5 Electrical Characteristics

5.1 Absolute Maximum Rating

Table 27 Absolute Maximum Rating

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
3.3 V Power Supply	V_{CC33}	3.0	–	3.6	V	–
1.8 V Power Supply	V_{CC18}	1.62	–	1.98	V	–
Input Voltage	V_{IN}	-0.3	–	V_{CC33} + 0.3	V	–
Output Voltage	V_{OUT}	-0.3	–	V_{CC33} + 0.3	V	–
Storage Temperature	T_{STG}	-55	–	155	°C	–
Power Dissipation	PD	–	–	1.85	W	–
ESD Rating	V_{ESD}	–	–	2000	V	–

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

5.1.1 DC Characteristics

Table 28 Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Supply	V_{CC33}	3.135	3.3	3.465	V	–
Input Voltage	V_{IN}	0	–	V_{CC}	V	–
Junction Operating Temperature	T_j	0	25	115	°C	–

5.1.2 DC Characteristics for 3.3 V Operation

Under V_{CC} = 3.0 V~3.6 V, T_j = 0 °C ~ 115 °C

Table 29 DC Characteristics for 3.3 V Operation

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Low Voltage	V_{IL}	–	–	0.3 * V_{CC}	V	CMOS
Input High Voltage	V_{IH}	0.7 * V_{CC}	v	–	V	CMOS
Output Low Voltage	V_{OL}	–	–	0.4	V	CMOS
Output High Voltage	V_{OH}	2.3	–	–	V	CMOS
Input Pull-up/down Resistance	R_I	–	75	v	KΩ	V_{IL} = 0 V or V_{IH} = V_{CC}

5.2 AC Characteristics

5.2.1 XI/OSCI (Crystal/Oscillator) Timing

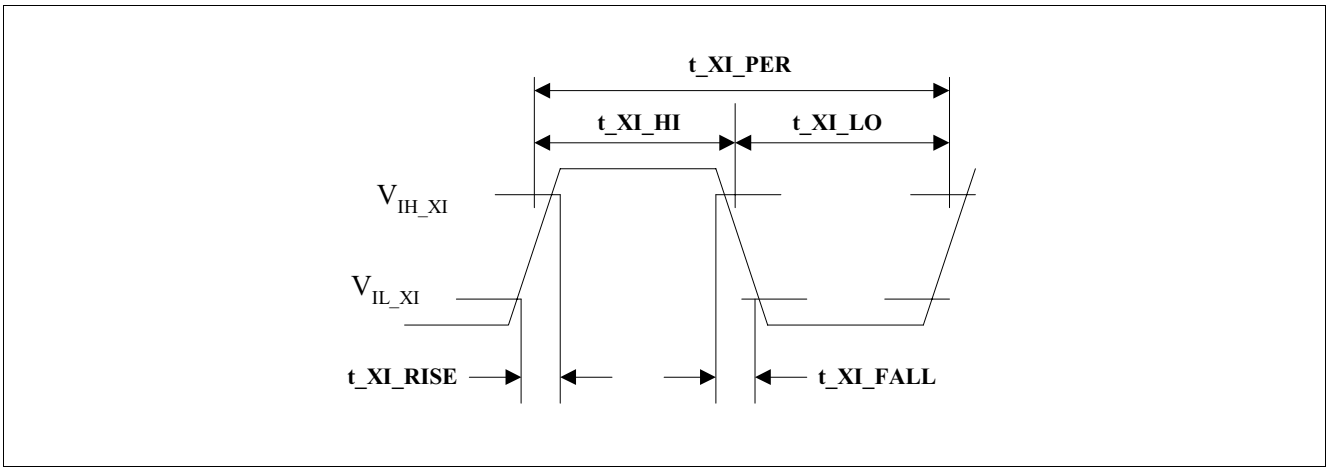


Figure 27 Crystal/Oscillator Timing

Table 30 Crystal/Oscillator Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
XI/OSCI Clock Period	t_{XI_PER}	40.0 - 50 ppm	40.0	40.0 + 50 ppm	ns	–
XI/OSCI Clock High	t_{XI_HI}	14	20.0	–	ns	–
XI/OSCI Clock Low	TX_ILO	14	20.0	–	ns	–
XI/OSCI Clock Rise Time, V_{IL} (max) to V_{IH} (min.)	t_{XI_RISE}	–	–	4	ns	–
XI/OSCI Clock Fall Time, V_{IH} (min.) to V_{IL} (max)	t_{XI_FALL}	–	–	4	ns	–

5.3 RMII Timing

5.3.1 REFCLK Input Timing (When REFCLK_SEL is set to 1)

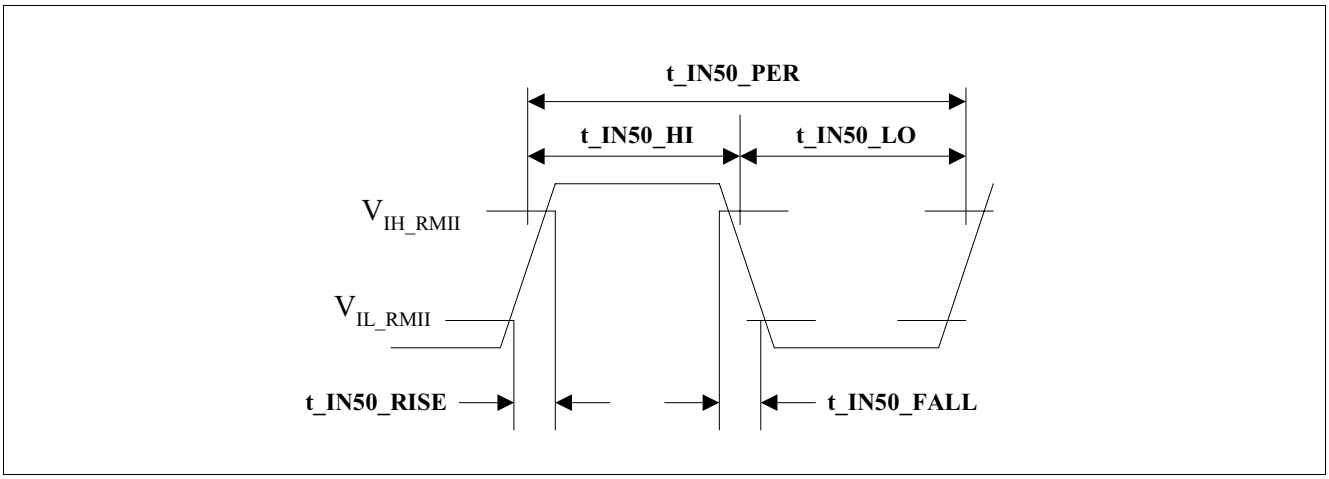


Figure 28 REFCLK Input Timing

Table 31 REFCLK Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
REFCLK Clock Period	t_{IN50_PER}	40.0 - 50 ppm	40.0	40.0 + 50 ppm	ns	–
REFCLK Clock High	t_{IN50_HI}	14	20.0	–	ns	–
REFCLK Clock Low	t_{IN50_LO}	14	20.0	–	ns	–
REFCLK Clock Rise Time, V_{IL} (max) to V_{IH} (min.)	t_{IN50_RISE}	–	–	2	ns	–
REFCLK Clock Fall Time, V_{IH} (min.) to V_{IL} (max)	t_{IN50_FALL}	–	–	2	ns	–

5.3.2 REFCLK Output Timing (When REFCLK_SEL is set to 0)

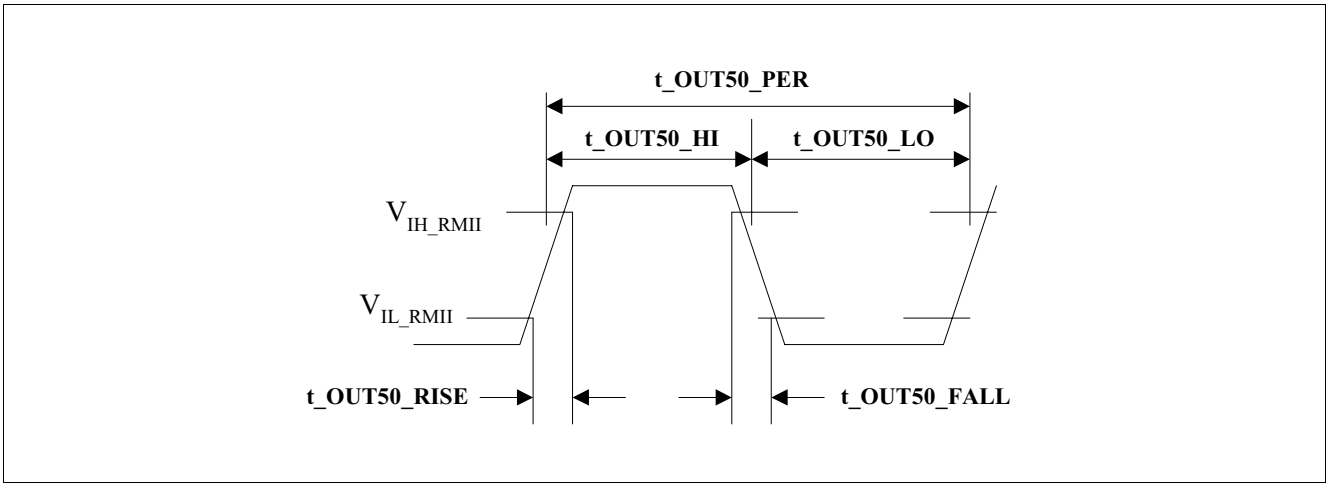


Figure 29 REFCLK Output Timing

Table 32 REFCLK Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
REFCLK Clock Period	t_{OUT50_PER}	40.0 - 50 ppm	40.0	40.0 + 50 ppm	ns	–
REFCLK Clock High	t_{OUT50_HI}	14	20.0	26	ns	–
REFCLK Clock Low	t_{OUT50_LO}	14	20.0	26	ns	–
REFCLK Clock Rise Time, V_{IL} (max) to V_{IH} (min.)	t_{OUT50_RISE}	–	–	2	ns	–
REFCLK Clock Fall Time, V_{IH} (min.) to V_{IL} (max)	t_{OUT50_FALL}	–	–	2	ns	–
REFCLK Clock Jittering (p-p)	t_{OUT50_JIT}	–	0.15	–	ns	v

5.3.3 RMII Transmit Timing

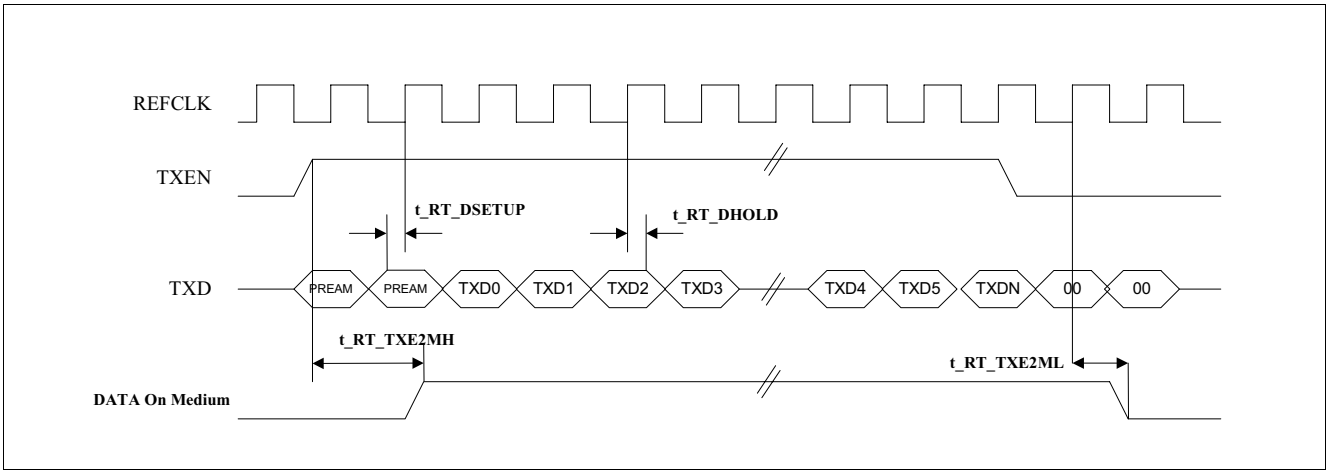


Figure 30 RMII Transmit Timing

Table 33 RMII Transmit Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TXD to REFCLK Rising Setup Time	t_{RT_DSETUP}	2	–	–	ns	–
TXD to REFCLK Rising Hold Time	t_{RT_DHOLD}	2	–	–	ns	–
TXEN asserts to data transmit to medium	$t_{RT\_TXE2MH100}$	–	–	235	ns	–
TXEN asserts to data transmit to medium	$t_{RT\_TXE2MH10}$	–	–	1550	ns	–
TXEN de-asserts to finish transmitting	$t_{RT\_TXE2ML100}$	–	–	260	ns	–
TXEN de-asserts to finish transmitting	$t_{RT\_TXE2ML10}$	–	–	1250	ns	–

5.3.4 RMII Receive Timing

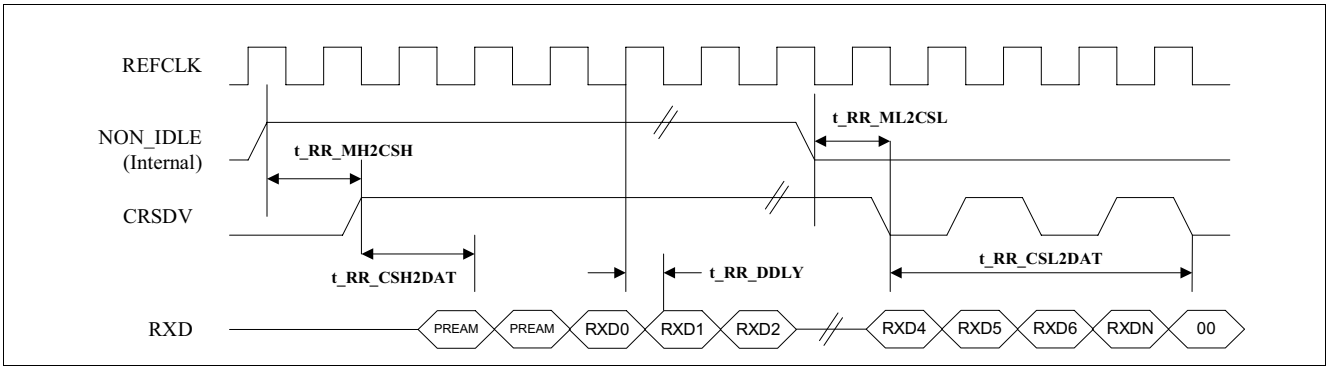


Figure 31 RMII Receive Timing

Table 34 RMII Receive Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Signal Detected on Medium to CRSDV High	$t_{RR\_MH2CSH100}$	–	–	265	ns	–
Signal Detected on Medium to CRSDV High	$t_{RR\_MH2CSH10}$	–	–	1000	ns	–
IDLE Detected on Medium to CRSDV low	$t_{RR\_ML2CSL100}$	–	–	260	ns	–
IDLE Detected on Medium to CRSDV low	$t_{RR\_ML2CSL10}$	–	–	570	ns	–
CRSDV High to Receive Data on RXD	$t_{RR\_CSH2DAT100}$	–	–	160	ns	–
CRSDV High to Receive Data on RXD	$t_{RR\_CSH2DAT10}$	–	–	1600	ns	–
CRSDV Toggle to End of Data Receiving	$t_{RR\_CSL2DAT100}$	–	160	–	ns	–
CRSDV Toggle to End of Data Receiving	$t_{RR\_CSL2DAT10}$	–	1600	–	ns	–
REFCLK Rising to RXD/CRSDV Delay Time	t_{RR_DDLY}	–	v	5	ns	–

5.4 SMII Clock Timing

5.4.1 REFCLK Input Timing (When REFCLK_SEL is set to 1)

Also apply to TX_CLK

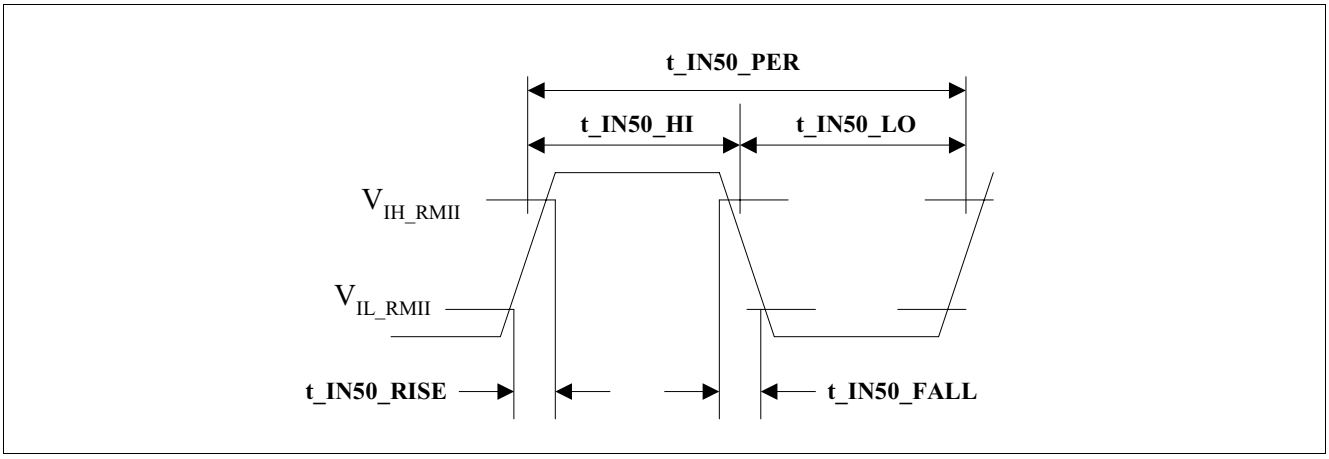


Figure 32 REFCLK Input Timing

Table 35 REFCLK Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
REFCLK/TXCLK Clock Period	t_{IN125_PER}	8.0 - 50 ppm	8.0	8.0 + 50 ppm	ns	–
REFCLK/TXCLK Clock High	t_{IN125_HI}	2.8	4.0	–	ns	–
REFCLK/TXCLK Clock Low	t_{IN125_LO}	2.8	4.0	–	ns	–
REFCLK/TXCLK Clock Rise Time, V_{IL} (max) to V_{IH} (min.)	t_{IN125_RISE}	–	–	2	ns	–
REFCLK/TXCLK Clock Fall Time, V_{IH} (min.) to V_{IL} (max)	t_{IN125_FALL}	–	–	2	ns	–

5.4.2 REFCLK Output Timing (When REFCLK_SEL is set to 1)

Also apply to RXCLK in SS_SMII Mode

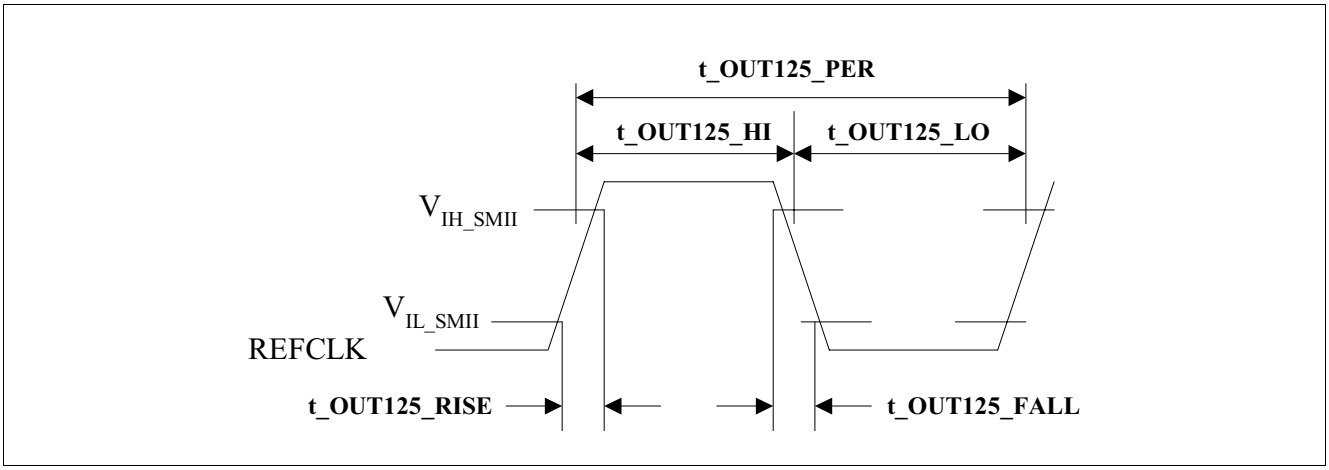


Figure 33 SMII/SS_SMII REFCLK Output Timing

Table 36 SMII/SS_SMII REFCLK Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
REFCLK Clock Period	t_{OUT125_PER}	8.0 - 50 ppm	8.0	8.0 + 50 ppm	ns	–
REFCLK Clock High	t_{OUT125_HI}	2.4	4.0		ns	–
REFCLK Clock Low	t_{OUT125_LO}	2.4	4.0	26	ns	–
REFCLK Clock Rise Time, V_{IL} (max) to V_{IH} (min.)	t_{OUT125_RISE}	–	–	2	ns	–
REFCLK Clock Fall Time, V_{IH} (min.) to V_{IL} (max)	t_{OUT125_FALL}	–	–	2	ns	–
REFCLK Clock Jittering (p-p)	t_{OUT125_JIT}	–	0.15	–	ns	–

5.4.3 SMII/SS_SMII Transmit Timing

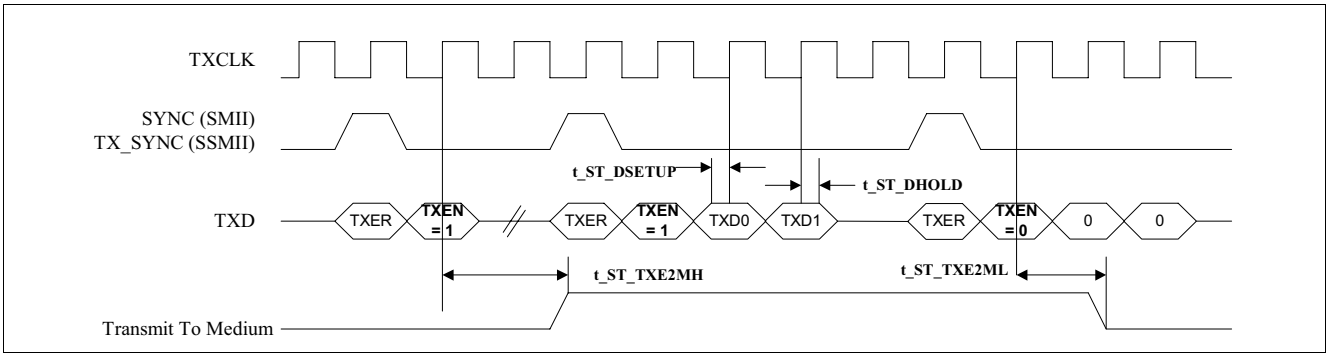


Figure 34 SMII/SS_SMII Transmit Timing

Table 37 SMII/SS_SMII Transmit Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TXD to REFCLK Rising Setup Time	t_{ST_DSETUP}	2	–	–	ns	–
TXD to REFCLK Rising Hold Time	t_{ST_DHOLD}	2	–	–	ns	–
TXEN asserts to data transmit to medium (100M)	$t_{ST\_TXE2MH100}$	–	–	390	ns	–
TXEN asserts to data transmit to medium (10M)	$t_{ST\_TXE2MH10}$	–	–	2340	ns	–
TXEN de-asserts to finish transmitting (100M)	$t_{ST\_TXE2ML100}$	–	–	430	ns	–
TXEN de-asserts to finish transmitting (10M)	$t_{ST\_TXE2ML10}$	–	–	3800	ns	–

5.4.4 SMII/SS_SMII Receive Timing

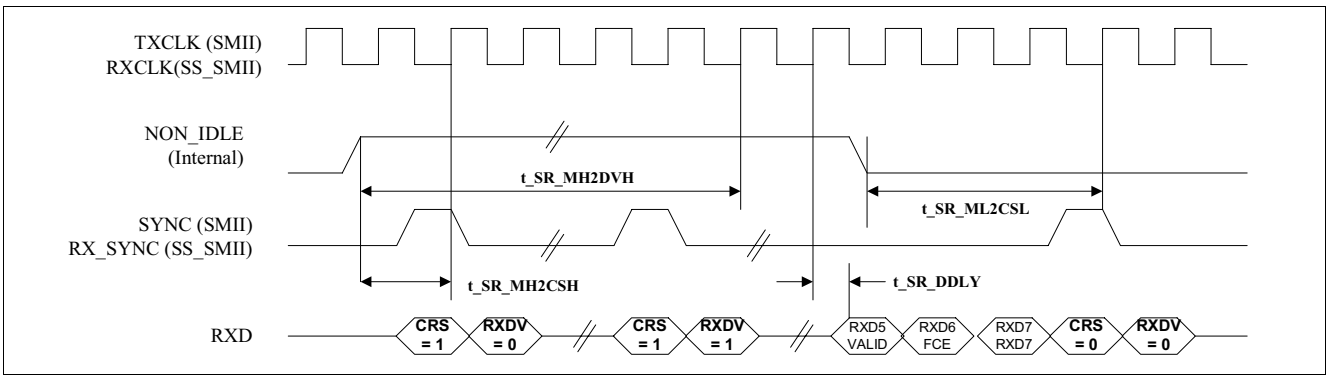


Figure 35 SMII/SS_SMII Receive Timing

Table 38 SMII/SS_SMII Receive Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Signal Detected on Medium to CRS High (100M)	$t_{SR\_MH2CSH100}$	–	–	430	ns	–
Signal Detected on Medium to CRS High (10M)	$t_{SR\_MH2CSH10}$	–	–	680	ns	–
IDLE Detected on Medium to CRS low (100M)	$t_{SR\_ML2CSL100}$	–	–	420	ns	–
IDLE Detected on Medium to CRS low (10M)	$t_{SR\_ML2CSL10}$	–	–	240	ns	–
Signal Detected on Medium to Receive Data Valid (100M)	$t_{SR\_MH2DVH100}$	–	–	470	ns	–
Signal Detected on Medium to Receive Data Valid (10M)	$t_{SR\_MH2DVH10}$	–	–	3840	ns	–
TXCLK Rising to SYNC/RXD Delay Time (SMII)	$t_{SR\_DDLY\_SMII}$	–	–	5	ns	–
RXCLK Rising to RX_SYNC/RXD Delay Time (SS_SMII)	$t_{SR\_DDLY\_SS\_SMII}$	–	–	5	ns	–

5.5 Serial Management Interface (MDC/MDIO) Timing

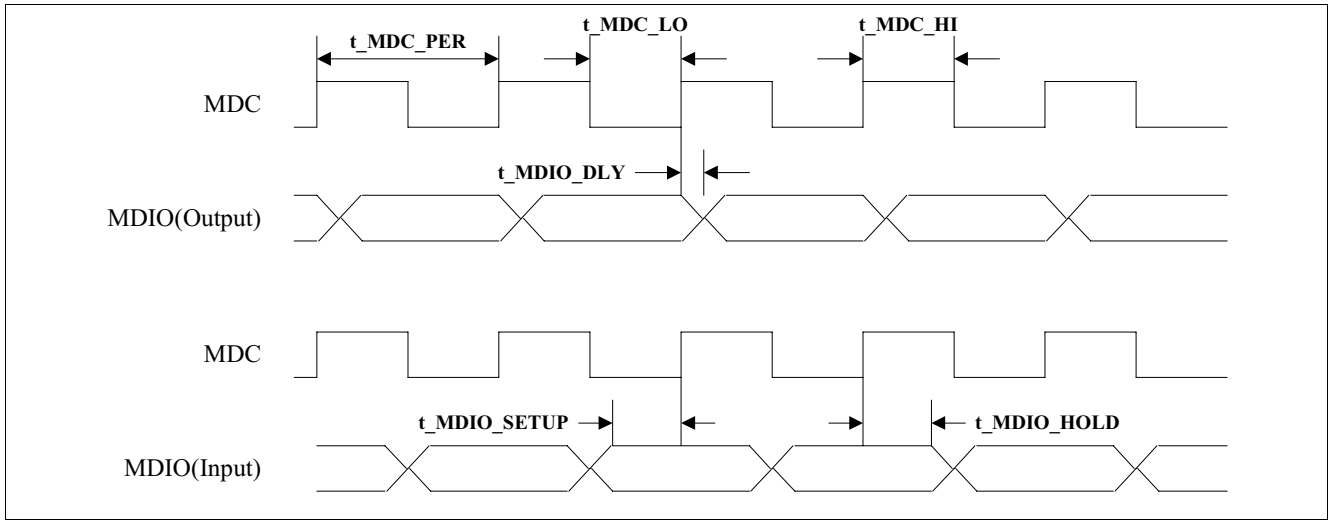


Figure 36 Serial Management Interface (MDC/MDIO) Timing

Table 39 Serial Management Interface (MDC/MDIO) Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MDC Period	t_{MDC_PER}	100	–	–	ns	–
MDC High	t_{MDC_HI}	40	–	–	ns	–
MDC High	t_{MDC_LO}	4zt0	–	–	ns	–

Table 39 Serial Management Interface (MDC/MDIO) Timing (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MDC to MDIO Delay Time	t_{MDIO_DLY}	–	–	20	ns	–
MDIO Input to MDC Setup Time	t_{MDIO_SETUP}	10	–	–	ns	–
MDIO Input to MDC Hold Time	t_{MDIO_HOLD}	10	–	–	ns	v

5.6 Power On Configuration Timing

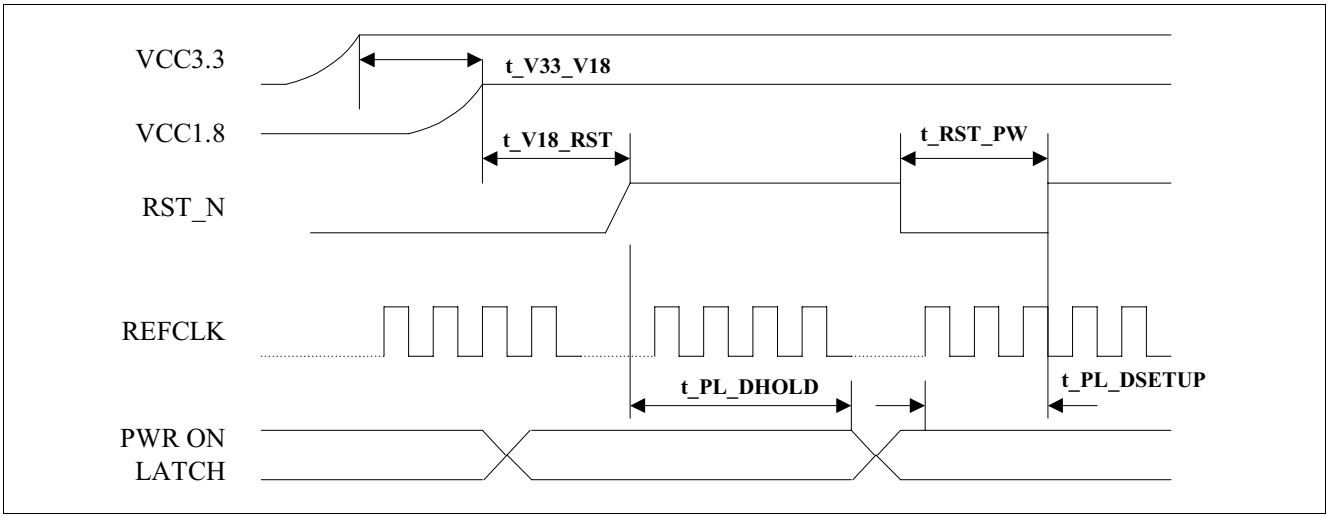


Figure 37 Power On Configuration Timing

Table 40 Power On Configuration Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
3.3 V Power Good to 1.8 V Power Good	t_{V33_V18}	TBD	–	–	ms	–
Hardware Reset With Device Powered up	t_{V18_RST}	200	–	–	ms	–
Hardware Reset With Clock Running	t_{RST_PW}	800	–	–	ns	–
Reset High to Configuration Setup Time	t_{PL_DSETUP}	200	–	–	ns	–
Reset High to Configuration Hold Time	t_{PL_DHOLD}	0	–	–	ns	–

6 Packaging

Package Outline of ADM7008/X, P-QFP-128-1

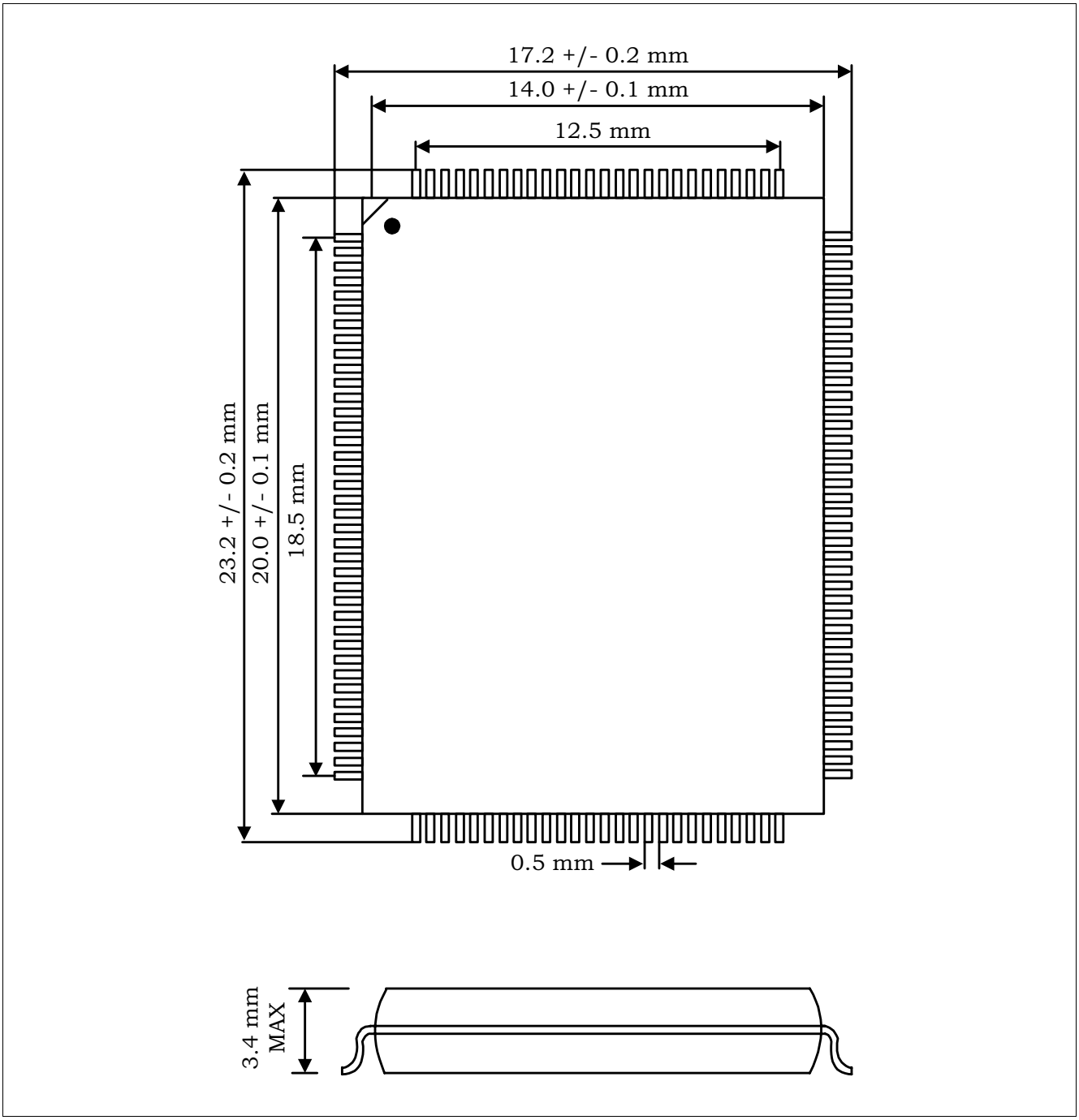


Figure 38 P-QFP-128-1 (Plastic Quad Flat Package)

Note: Dimensions in mm

TerminologyTerminology

A	
ANSI	American National Standards Institute
B	
BER	Bit Error Rate
C	
COL	Collision
CRS	Carrier Sense
CRSDV	Carrier Sense and Data Valid
CTL	Crystal
D	
DSP	Digital Signal Processor
DUPCOL	Duplex and Collision
E	
ESD	End of Stream Delimiter
F	
FEFI	Far End Fault Indication
FIFO	First In First Out
FLP	Fast Link Pulse
FX	Fiber
I	
IA	Information Application
L	
LFSR	Linear Feedback Shifter Register
LLP	Low-power Link Pulse
LNKACT	Link and Activity
LVTTL	TTL Level
M	
MAC	Media Access Controller
MD	Medium Detect
MDC	Management Data Clock
MDIO	Management Data Input/Output
MII	Media Independent Interface
N	
NRZ	None Return to Zero
NRZI	None Return to Zero Inverter
O	
OP	Operation Code
P	
PCS	Physical Coding Sub-layer
PECL	Pseudo Emitter Couple Logic
PHY	Physical Layer

PHYADDR	PHY Address
PMA	Physical Medium Attachment
PMD	Physical Medium Dependent
PNP	A type of Transistor
PQFP	Plastic Quad Flat Pack
R	
REFCLK	Reference Clock
RF	Remote Fault
RMII	Reduced Media Independent Interface
RSMODE	RMII/SMII/SS_SMII Mode Select
RXC	Receive Clock
RXD	Receive Data
RXDV	Receive Data Valid
RXER	Receive Data Error
RXN	Receive Negative (Analog receive differential signal)
RXP	Receive Positive (Analog receive differential signal)
RX_SYNC	Receive Synchronous
S	
SDN	Signal Detect Negative (Fiber signal detect)
SDP	Signal Detect Positive (Fiber signal detect)
SELFX	Select Fiber
SMI	Serial Management Interface
SMII	Serial Media Independent Interface
SOHO	Small Office and Home Office
SQE	Signal Quality Error
SSD	Start of Stream Delimiter
SS_SMII	Source Synchronous Media Independent Interface
SYNC	Synchronous
T	
TA	Turn Around
TDR	Time Domain Reflectometry
TP	Twisted Pair
TP-PMD	Twisted Pair Physical Medium Dependent
TTL	Transistor Logic
TXC	Transmission Clock (MII)
TXCLK	Transmission Clock (SMII/SS_SMII)
TXD	Transmission Data
TXEN	Transmission Enable
TXER	Transmission Error
TXN	Transmission Negative
TXP	Transmission Positive
/J/K	5B signal to detect the start of a frame
/T/R	5B signal to detect the end of a frame

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