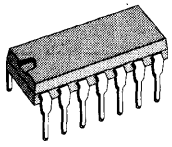
SGS-THOMSON MICROELECTRONICS

TDA9108

MONITOR HORIZONTAL PROCESSOR

- POS/NEG SYNC INPUT
- SYNC POLARITY DETECTION
- 2 PLLs CONCEPT
- 2 COMPLEMENTARY OUTPUTS
- DC ADJUSTABLE FREQUENCY
- DC ADJUSTABLE DUTY CYCLE
- X-RAY PROT INPUT
- BACK PORCH CLAMPING PULSE GENERATOR
- H-DRIVE INHIBITION WHEN $V_S < V_{S\ START}$



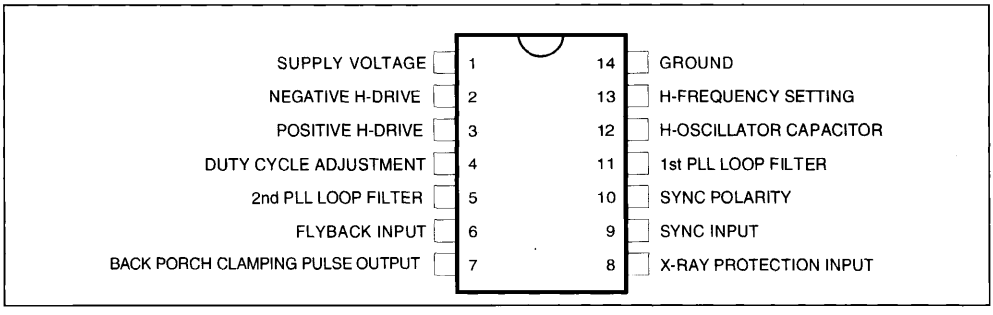
DIP14
(Plastic Package)

ORDER CODE : TDA9108

DESCRIPTION

The TDA9108 is a horizontal deflection processor specially designed for monitor applications. The H-drive output duty cycle, the horizontal frequency and the horizontal position are DC adjustable ; it accepts both POS/NEG polarity on sync input and delivers polarity information on a dedicated pin. All these features make the device a good choice for multifrequency application. In addition to this, X-ray protection, 2 complementary H-drive output , and a back porch clamping pulse generator are also included. It is a monolithic integrated circuit encapsulated in a 14 lead dual line plastic package.

PIN CONNECTIONS



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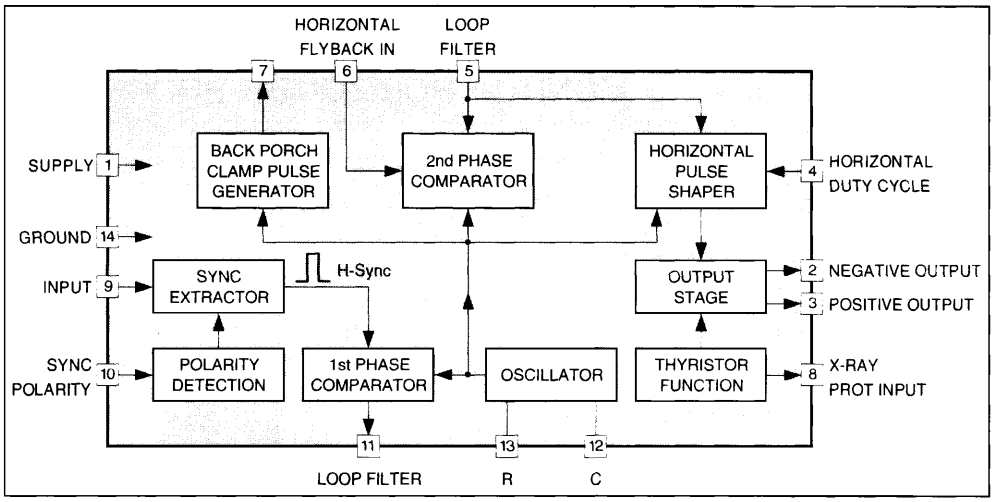
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (Pin 1)	15	V
V_2	Voltage at Pin 2	18	V
V_4	Voltage at Pin 4	0, V_S	V
V_8	Voltage at Pin 8	0 , V_S	V
V_9	Voltage at Pin 9	0 , V_S	V
V_{10}	Voltage at Pin 10	0, V_S	V
I_2	Pin 2 Peak Current	1	A
I_3	Pin 3 Peak Current	0.5	A
I_6	Pin 6 Input Current	30	mA
I_7	Pin 7 Input Current	10	mA
P_{tot}	Total Power Dissipation at $T_{amb} \leq 70^{\circ}C$	0.9	W
T_{stg} , T_j	Storage and Junction Temperature	- 40 , + 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Thermal Resistance Junction-ambient	Max.	90	°C/W

ELECTRICAL CHARACTERISTICS

(refer to the test circuit, V_S = 12V, T_A = 25°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage Range		10	12	13.2	V
I_S	Supply Current (Pin 1)	I_3 = 0		38	55	mA
V_S	Supply voltage at which the output pulses (at Pin 2 and 3) are switched off				4	V

ELECTRICAL CHARACTERISTICS (continued)
(refer to the test circuit, V_S = 12V, T_A = 25°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
HORIZONTAL SYNC. INPUT						
V_{9SW}	Sync Input Threshold	• Sync high • Sync Low	2		V_S 0.8	V V
I_{9SW}	Sync Input Current	• Sync high • Sync Low	 -20	 -7	1	µA µA
SYNC POLARITY SELECTION						
V_{10th}	Polarity Selection Threshold Positive sync on Pin 9 for $V_{10} < V_{10th}$ Negative sync on Pin 9 for $V_{10} > V_{10th}$		2.3	2.5	2.7	V
I_{10}	Input Current	V_{10} = 2V V_{10} = 3V			1 12	µA µA
V_{10ZL}	Low Impedance (2kΩ) Threshold	(see note 1)		6.3		V
X-RAY PROTECTION CIRCUIT						
V_{8th}	X-ray Prot Input Threshold Voltage (when $V_8 > V_{8th}$ Pin 2 and 3 are inhibited until V_S is switched off/on)		2.6	2.9	3.2	V
I_8	Input Current	$V_8 \leq 2.5$ $V_8 \geq 3.3$	-0.5		 0.5	µA µA
FLYBACK INPUT						
V_6	Phase Comparator Input Threshold				10	V
I_6	Input Switching Current		0.1			mA
OUTPUT PULSE						
V_2	Saturation Voltage (Pin 3 grounded)	I_2 = 150mA		2.2	3.2	V
I_2	Output Current (Pin 3 grounded)	V_2 = 5V			150	mA
V_3	Output Voltage (Pin 2 connected to supply)	• High level (I_3 = 150mA) • Low level (I_3 = 100mA)	8.8	9.8 1.5	10.8 2.7	V V
I_3	Output Current Capability	• Source • Sink			150 100	mA mA
R_3	Output Resistance	• At leading edge of output pulse • At falling edge of output pulse		3 20		Ω Ω
DUTY CYCLE ADJUSTMENT						
t_p	Horizontal Output Pulse Duty Cycle on Pin 3 (high level, line transistor off time)	f = 31.5kHz Pin 4 not connected	26	30	34	%
V_4	Voltage on Pin 4 (see note 2)	Pin 4 not connected	0.178 V_S	0.19 V_S	0.202 V_S	V
R_4	Serial Equivalent Resistor on Pin 4 (see note 2)	Pin 4 not connected	1.7	2.3	2.9	kΩ

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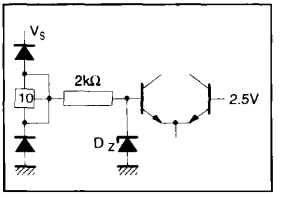
Note 1 : The voltage on the polarity detection comparator is clamped by an internal Zener diode (V_Z).
When voltage on Pin 10 reaches V_Z, then $I_{Pin\ 10} = \frac{V_{Pin\ 10} - V_Z}{2k\Omega}$.



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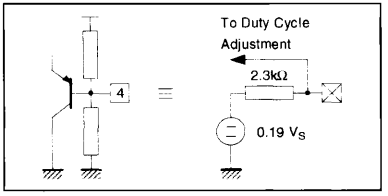
Note 2 : Pin 4 internal schematic



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ELECTRICAL CHARACTERISTICS (continued)

(refer to the test circuit, V_S = 12V, T_A = 25°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
DUTY CYCLE ADJUSTMENT (continued)						
t_{pADJ}	Max. Horizontal Output Duty Cycle Range (function of V_4) $t_p = K4 \cdot \frac{V_4}{V_S}$ (see note 3)	f = 31.5kHz		50		%
K4	Duty Cycle Adjustment Coefficient		1.6	1.8	2	
KEY PULSE OUTPUT						
V_{7K}	Key Pulse Output Peak Voltage (emitter follower)	I_7 = 5mA	4	5		V
V_{7L}	Low Level (outside the key pulse)			0.2	0.5	V
t_{SK}	Phase Relation between Trailing Edge of Key Pulse and Middle of Sync. Input Pulse	f = 31.5kHz Sync width = 2µs	1.1	1.5	1.9	µs
t_K	Key Pulse Duration		1.25	1.7	2.15	µs
OSCILLATOR						
V_{12}	Low Level Threshold Voltage			5.4		V
V_{12}	High Level Threshold Voltage			8.2		V
I_{12}	Charge Current	R_{13} = 10kΩ		0.6		mA
I_{12}	Discharge Current	R_{13} = 10kΩ		0.3		mA
V_{13}	Reference Voltage on Pin 13		2.6	2.9	3.2	V
f_O	Free Running Frequency	R_{13} = 10kΩ C_{12} = 2.2nF	27	30	33	kHz
$f_{Max.}$	Maximum Oscillator Frequency	R_{13} = 47kΩ C_{12} = 2.2nF	66			kHz
Jitt.	Horizontal Jitter	f = 31.5kHz		5		ns
$\frac{\Delta f_O}{\Delta I_{13}}$	Frequency Control Sensitivity	R_{13} = 10kΩ C_{12} = 2.2nF		100		$\frac{Hz}{\mu A}$
Δf_O	Frequency Change when V_S Drops to 7.5V				-6	%
PHASE COMPARATOR						
V_5	Control Voltage Range			9.4 to 8.2		V
I_5	Peak Control Current	During flyback pulse		± 0.85		mA
I_5	Input Current (blocked Phase Detector)	Outside flyback pulse			5	µA
t_D	Permissible Delay between Output Pulse Leading Edge and Flyback Pulse Leading Edge			$t_p - t_f$		µs
$\frac{\Delta t}{\Delta t_D}$	Static Control Error				0.2	%
SYNC PULSE-OSCILLATOR PHASE COMPARATOR						
V_{11}	Control Voltage Range			4.6 to 1.4		V
I_{11}	Control Peak Current	During Sync Pulse		± 2.3		mA
$\frac{\Delta f}{\Delta t}$	Phase Lock Loop Gain	$R_{11\text{-}13}$ = 100kΩ		4		$\frac{kHz}{\mu s}$
f	Catching and Holding Range	See Typical Application		± 700		Hz
OVERALL PHASE RELATIONSHIP						
t_O	Phase Relation between Middle of Flyback Pulse and Middle of Sync. Pulse	R_{13} = 10kΩ C_{12} = 2.2nF		1.1		µs
$\frac{\Delta V_5}{\Delta t_O}$	Adjustment Sensitivity			130		$\frac{mV}{\mu s}$
$\frac{\Delta I_5}{\Delta t_O}$	Adjustment Sensitivity			50		$\frac{\mu A}{\mu s}$

Note 3 : t_d must be ≥ $(H_{period}\left[\frac{t_p}{100} - 0.25\right] - \frac{t_{fly}}{2})$ in order to have ± 5% horizontal phase adjustment range.

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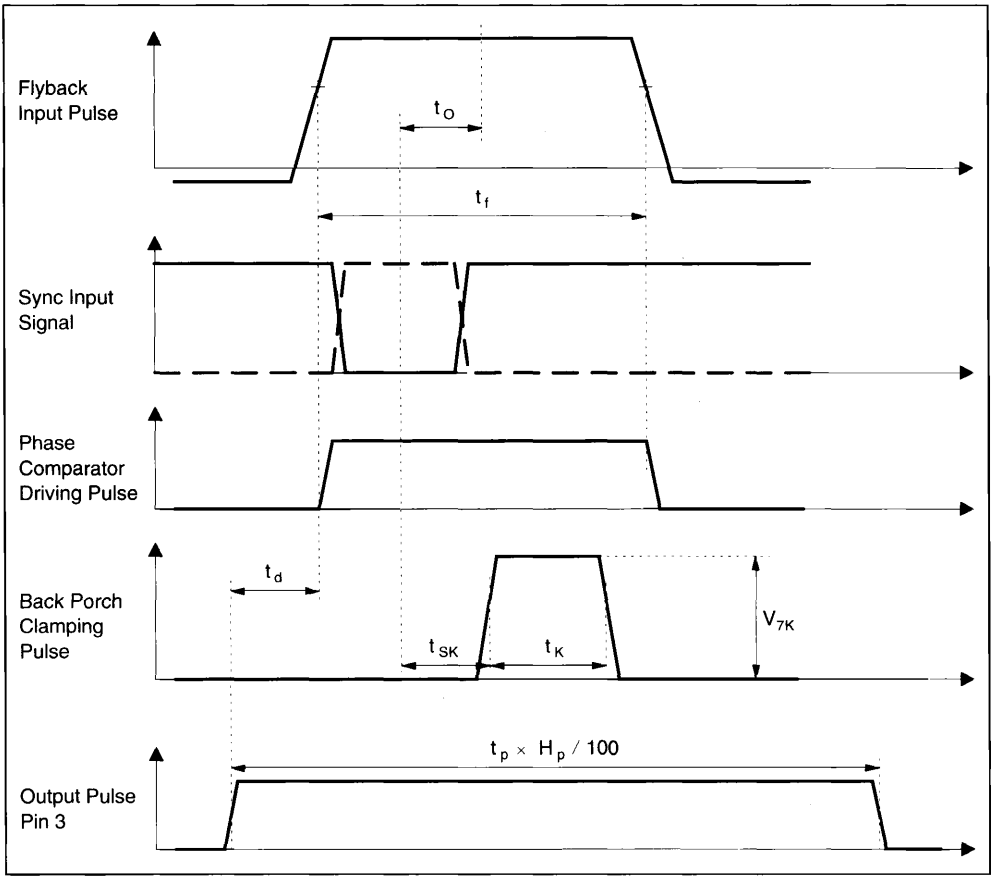
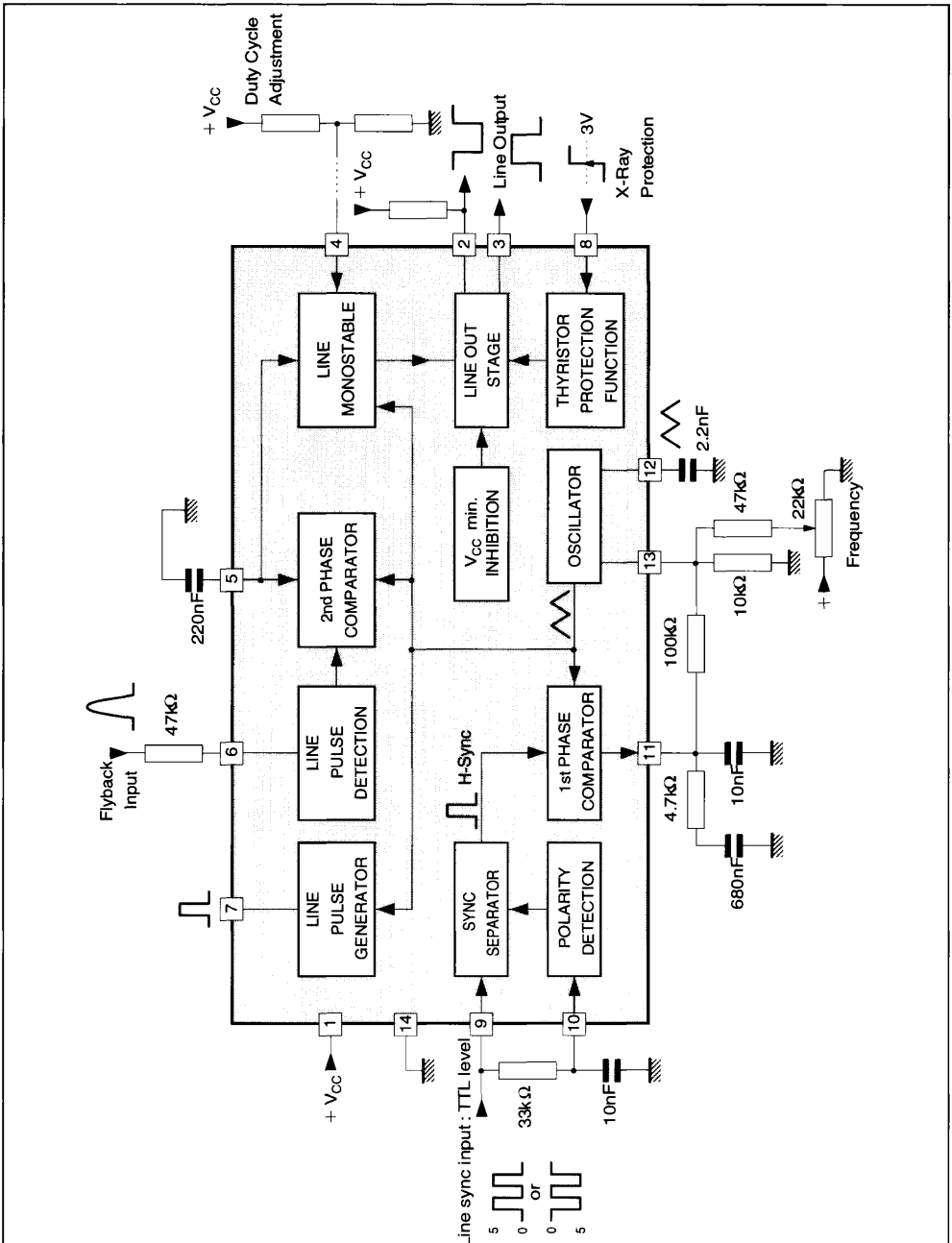
Figure 1 : Relation Ship of Main Waveform Phases



TYPICAL APPLICATION



APPLICATION INFORMATION

Sync Extractor and Polarity Detection

This circuit is able to handle both positive or negative TTL input signal on Pin 9. The voltage on Pin 10 drives an internal inverter providing a constant sync polarity to the 1st phase comparator.

When using a RC network between Pin 9 and 10 (see Typical Application), the IC will adapt itself automatically to positive or negative sync. On an other hand, and in order to simplified the application, the Pin 10 can be connected to ground or supply (through a resistor), in this case the IC will work only with one sync polarity.

1st PLL

It is composed by a phase comparator, the oscillator and an external loop filter (see Figure 2)

- The phase comparator receives the H-sync signal (with positive polarity) and a signal coming from the internal current controlled oscillator. The loop is closed through an external resistor between Pin 11 and 13.
- The oscillator generates a sawtooth waveform on Pin 12 by charging and discharging the external capacitor. The capacitor is discharging by the current flowing Pin 13 and charged by two times this latter (see Figure 3).

The sawtooth is used internally to generate all the required timings.

It is possible to DC control the frequency by adding or substracting a DC current on Pin 13 (see Figure 2).

Figure 2

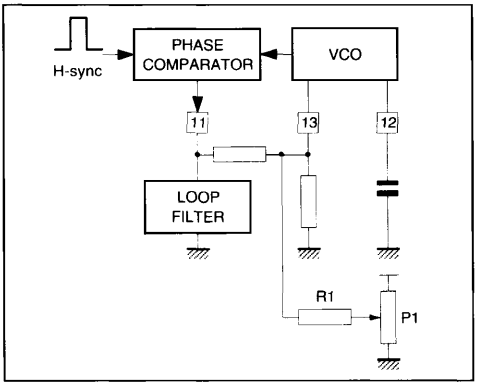
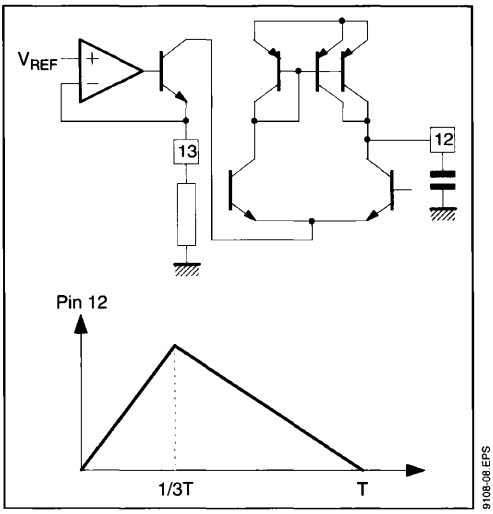


Figure 3



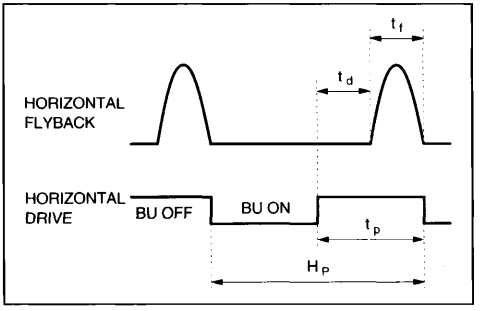
2nd Phase Locked Loop

To compensate the delay introduced by the horizontal final stage, the flyback pulse (Pin 6) and the oscillator waveform (Pin 12) are compared in the 2nd phase comparator. The result of the comparison is a control current which, after it has been filtered by the external capacitor on Pin 5, is sent to a phase shifter which adequately regulates the horizontal output pulses phase.

The maximum phase shift allowed is $t_d = t_p - t_f$ where t_f is the flyback duration (see Figure 4).

If $t_d > t_p - t_f$, then the horizontal output transistor will be tunned on during flyback distroying it.

Figure 4



X-Ray Protection Input (Pin 8)

When the voltage on this pin becomes higher then 2.9V (typ.), the horizontal outputs are inhibited (Pins 2 and 3) and will remains in this condition until a reset is made on supply voltage (power-off/power-on).

H-Duty Cycle (see Figure 5)

The output duty cycle is variable between 0 and 50% by varying the voltage on Pin 4.

In order to maintain ± 5% horizontal phase adjustment possibilities the following equation must be respected.

(1) $H_{period}\left[\frac{t_p}{100} - 0.25\right] - \frac{t_{fly}}{2} \leq t_d \Rightarrow$ If not, t_p will decrease because of H-drive trailing edge wrong position (phase shifter saturation)

(2) $t_d \leq 0.36\ H_p - \frac{t_{fly}}{2} - 2\mu s \Rightarrow$ If not, t_p will decrease because of H-drive leading edge wrong position (phase shifter saturation)

Figure 5