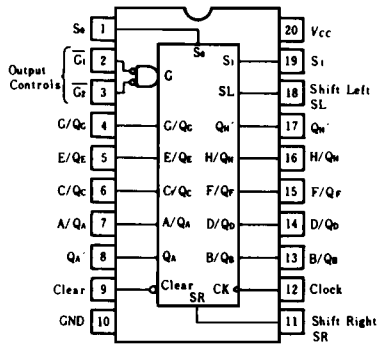
HD74HC323 ● 8-bit Universal Shift/Storage Register (with 3-state Outputs)

This eight-bit universal register features multiplexed I/O ports to achieve full eight bit data handling in a single 20-pin package. HD74HC323 applications are as stacked or push-down registers, buffer storage, and accumulator registers.

Two function-select inputs and two output control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines S_0 and S_1 high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the I/O ports to be clocked into the register. Reading out of this register can be accomplished while the outputs are enabled in any mode. The clear function is synchronous, and a low level at the clear input clears the register on the next low-to-high transition of the clock.

■ PIN ARRANGEMENT

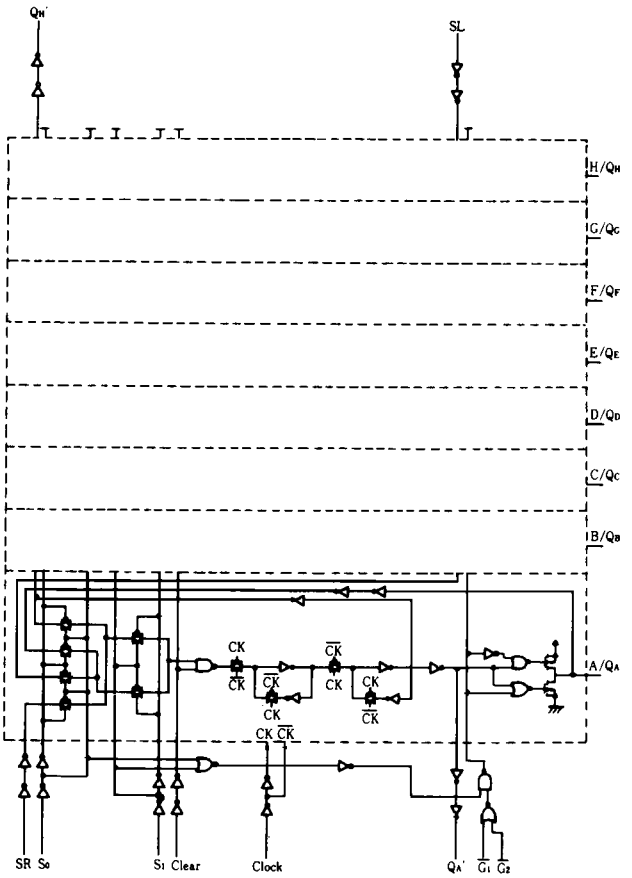


(Top View)

■ FEATURES

- High Speed Operation: t_{pd} (Clock to Q)=20ns typ. (C_L=50pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: V_{CC}=2~6V
- Low Input Current: 1μA max.
- Low Quiescent Supply Current: I_{CC} (static)=4μA max. (Ta=25°C)

■ LOGIC DIAGRAM



■ FUNCTION TABLE

Mode	Inputs								Inputs/Outputs								Outputs	
	Clear	Function Select		Output Control		Clock	Serial		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	Q_A'	Q_H'
		S_1	S_0	$\overline{G}_1+$	$\overline{G}_2+$		S_L	S_R										
Clear	L	×	L	L	L	↑	×	×	L	L	L	L	L	L	L	L	L	L
	L	L	×	L	L	↑	×	×	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	×	×	×	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	×	×	L	L	L	×	×	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	×	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	×	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	×	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	×	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	×	×	↑	×	×	a	b	c	d	e	f	g	h	a	h

a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage Range	V_{CC}	−0.5～+7.0	V
Input Voltage	V_{IN}	−0.5～V_{CC}+0.5	V
Output Voltage	V_{OUT}	−0.5～V_{CC}+0.5	V
Output Current	I_{OUT}	±35	mA
DC Current Drain per V_{CC}, GND	I_{CC}, I_{GND}	±75	mA
DC Input Diode Current	I_{IK}	±20	mA
DC Output Diode Current	I_{OK}	±20	mA
Power Dissipation per Package	P_T	500	mW
Storage Temperature	T_{stg}	−65～+150	°C

■ DC CHARACTERISTICS

Item	Symbol	V_{CC}(V)	Test Conditions			Ta=25°C min	Ta=25°C typ	Ta=25°C max	Ta=−40～+85°C min	Ta=−40～+85°C max	Unit
Input Voltage	V_{IH}	2.0				1.5	—	—	1.5	—	V
		4.5				3.15	—	—	3.15	—	
		6.0				4.2	—	—	4.2	—	
	V_{IL}	2.0				—	—	0.5	—	0.5	V
		4.5				—	—	1.35	—	1.35	
		6.0				—	—	1.8	—	1.8	
Output Voltage	V_{OH}	2.0	V_{in}=V_{IH} or V_{IL}		I_{OH}=−20μA	1.9	2.0	—	1.9	—	
		4.5				4.4	4.5	—	4.4	—	
		6.0				5.9	6.0	—	5.9	—	
		4.5		Q_A～Q_H	I_{OH}=−6mA	4.18	—	—	4.13	—	V
		6.0			I_{OH}=−7.8mA	5.68	—	—	5.63	—	
		4.5		Q'_A, Q'_H	I_{OH}=−4mA	4.18	—	—	4.13	—	
		6.0			I_{OH}=−5.2mA	5.68	—	—	5.63	—	
	V_{OL}	2.0	V_{in}=V_{IH} or V_{IL}		I_{OL}=20μA	—	0.0	0.1	—	0.1	
		4.5				—	0.0	0.1	—	0.1	
		6.0				—	0.0	0.1	—	0.1	
		4.5		Q_A～Q_H	I_{OL}=6mA	—	—	0.26	—	0.33	V
		6.0			I_{OL}=7.8mA	—	—	0.26	—	0.33	
		4.5		Q'_A, Q'_H	I_{OL}=4mA	—	—	0.26	—	0.33	
		6.0			I_{OL}=5.2mA	—	—	0.26	—	0.33	
Off-state output current	I_{OZ}	6.0	V_{in}=V_{IH} or V_{IL}, V_{out}=V_{CC} or GND			—	—	±0.5	—	±5.0	μA
Input Current	I_{in}	6.0	V_{in}=V_{CC} or GND			—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	6.0	V_{in}=V_{CC} or GND, I_{out}=0μA			—	—	4.0	—	40	μA

■AC CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

Item	Symbol	V_{CC}(V)	Test Conditions	Ta=25°C			Ta=−40~+85°C		Unit
				min.	typ.	max.	min.	max.	
Maximum Clock Frequency	f_{max}	2.0		—	—	5	—	4	MHz
		4.5		—	—	27	—	21	
		6.0		—	—	31	—	24	
Propagation Delay Time	t_{PLH} t_{PHL}	2.0	Clock to Q_A' or Q_H'	—	—	150	—	190	ns
		4.5		—	18	30	—	38	
		6.0		—	—	26	—	33	
		2.0	Clock to Q	—	—	175	—	220	ns
		4.5		—	20	35	—	44	
		6.0		—	—	30	—	37	
Output Enable Time	t_{ZH} t_{ZL}	2.0		—	—	150	—	190	ns
		4.5		—	14	30	—	38	
		6.0		—	—	26	—	33	
Output Disable Time	t_{HZ} t_{LZ}	2.0		—	—	150	—	190	ns
		4.5		—	15	30	—	38	
		6.0		—	—	26	—	33	
Output Rise/Fall Time	t_{TLH} t_{THL}	2.0	Q_A', Q_H'	—	—	75	—	95	ns
		4.5		—	5	15	—	19	
		6.0		—	—	13	—	16	
		2.0	Q	—	—	60	—	75	ns
		4.5		—	4	12	—	15	
		6.0		—	—	10	—	13	
Input Capacitance	C_{in}	—		—	5	10	—	10	pF