

# HN624016 Series

1,048,576 × 16-Bit/2,097,152 × 8-Bit CMOS MASK Programmable Read Only Memory

## DESCRIPTION

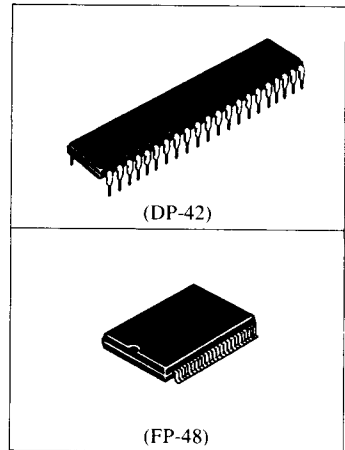
The HN624016 is a 16-Mbit CMOS mask-programmable ROM organized either as 1048576 words by 16 bits or as 2097152 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN624016, which provides large capacity of 16M bits, is ideally suited for kanji character generators.

## FEATURES

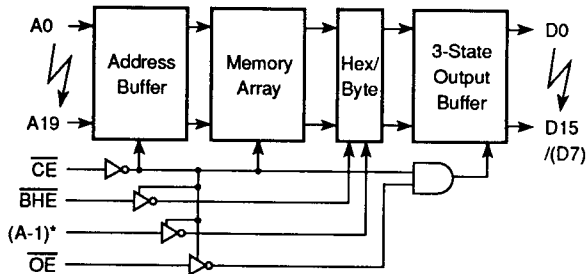
- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access Time .....200ns (max.)
- Low Power Consumption .....100mW (typ.) Active  
5μW (typ.) Standby
- Byte-wide or Word-wide Data Organization with BHE

## ORDERING INFORMATION

Type No.	Access Time	Package
HN624016P	200ns	600 mil 42 pin Plastic DIP
HN624016F	200ns	48 pin Plastic SOP



## BLOCK DIAGRAM



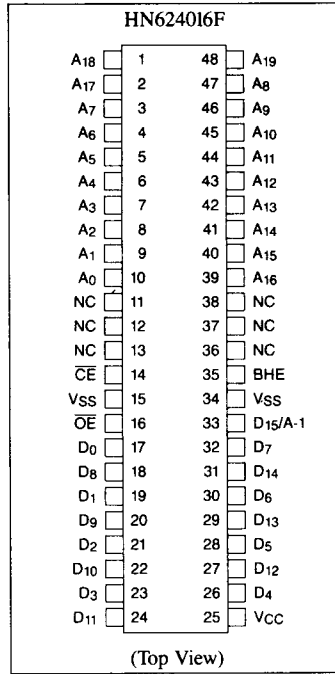
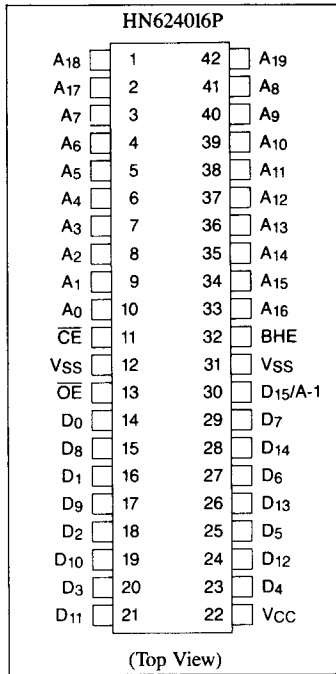
BHE =  $V_{IH}$ ; 16-bit ( $D_{15} \sim D_0$ )

BHE =  $V_{IL}$ ; 8-bit ( $D_7 \sim D_0$ )

\* A-1 is least significant address. When BHE is "low",  $D_{14} \sim D_8$  goes the high impedance state.



■ PIN ARRANGEMENT



**NOTE:** 12-13 pin and 36-37 pin are connected to inner lead frame.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V <sub>CC</sub>	-0.3 ~ +7.0	V	1
All Input and Output Voltage	V <sub>T</sub>	-0.3 ~ V <sub>CC</sub> +0.3	V	1
Operating Temperature Range	T <sub>opr</sub>	0 ~ +70	°C	
Storage Temperature Range	T <sub>stg</sub>	-55 ~ +125	°C	
Temperature Under Bias	T <sub>bias</sub>	-20 ~ +85	°C	

**NOTE:** 1. With respect to V<sub>SS</sub>.

■ RECOMMENDED OPERATING CONDITIONS (V<sub>SS</sub> = 0V, T<sub>a</sub> = 0 ~ 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Input Voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> + 0.3	V
	V <sub>IL</sub>	-0.3	—	0.8	V

■ DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5V ± 10%, V<sub>SS</sub> = 0V, T<sub>a</sub> = 0 ~ 70°C)

Item	Symbol	Test Condition	Min.	Max.	Unit
Supply Current	Active	I <sub>CC</sub> V <sub>CC</sub> = 5.5V, I <sub>DOUT</sub> = 0mA, t <sub>RC</sub> = Min.	—	50	mA
	Standby	I <sub>SB</sub> V <sub>CC</sub> = 5.5V, $\overline{CE} \geq V_{CC} - 0.2V$	—	30	μA
Input Leakage Current	I <sub>IL</sub>	V <sub>IN</sub> = 0 ~ V <sub>CC</sub>	—	10	μA
Output Leakage Current	I <sub>OL</sub>	$\overline{CE} = 2.2V$ , V <sub>OUT</sub> = 0 ~ V <sub>CC</sub>	—	10	μA
Output Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -205μA	2.4	—	V
	V <sub>OL</sub>	I <sub>OL</sub> = 1.6mA	—	0.4	V



■ **CAPACITANCE** ( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 25^\circ C$ ,  $V_{IN} = 0V$ ,  $f = 1MHz$ )

Item	Symbol	Min.	Max.	Unit
Input Capacitance	$C_{IN}$	—	15	pF
Output Capacitance	$C_{OUT}$	—	15	pF

**NOTE:** \* This parameter is sampled and not 100% tested.

■ **AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0 \sim 70^\circ C$ )

Item	Symbol	Min.	Max.	Unit
Read Cycle Time	$t_{RC}$	200	—	ns
Address Access Time	$t_{AA}$	—	200	ns
$\overline{CE}$ Access Time	$t_{ACE}$	—	200	ns
$\overline{OE}$ Access Time	$t_{OE}$	—	100	ns
BHE Access Time	$t_{BHE}$	—	200	ns
Output Hold Time From Address Change	$t_{DHA}$	0	—	ns
Output Hold Time From $\overline{CE}$	$t_{DHC}$	0	—	ns
Output Hold Time From $\overline{OE}$	$t_{DHO}$	0	—	ns
Output Hold Time From BHE	$t_{DHB}$	0	—	ns
$\overline{CE}$ to Output in High Z	$t_{CHZ}^*$	—	70	ns
$\overline{OE}$ to Output in High Z	$t_{OHZ}^*$	—	70	ns
BHE to Output in High Z	$t_{BHZ}^*$	—	70	ns
$\overline{CE}$ to Output in Low Z	$t_{CLZ}$	10	—	ns
$\overline{OE}$ to Output in Low Z	$t_{OLZ}$	10	—	ns
BHE to Output in Low Z	$t_{BLZ}$	10	—	ns

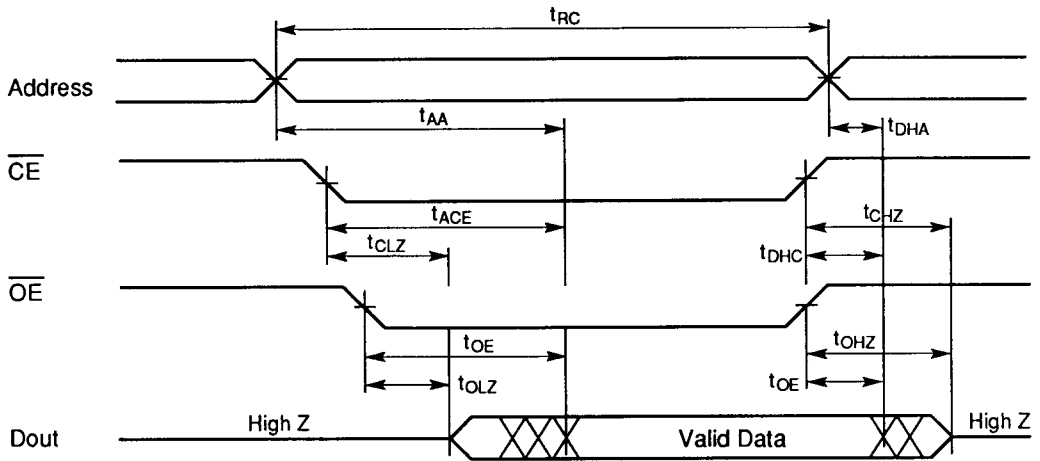
**NOTE:** \*  $t_{CHZ}$ ,  $t_{OHZ}$  and  $t_{BHZ}$  are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

• **Test Conditions**

- Input Pulse Level: 0.8 ~ 2.4V
- Input and Output Timing Reference Level: 1.5V
- Input Rise and Fall Time: 10ns
- Output Load: 1 TTL gate + CL = 100pF  
(including scope and jig capacitance)

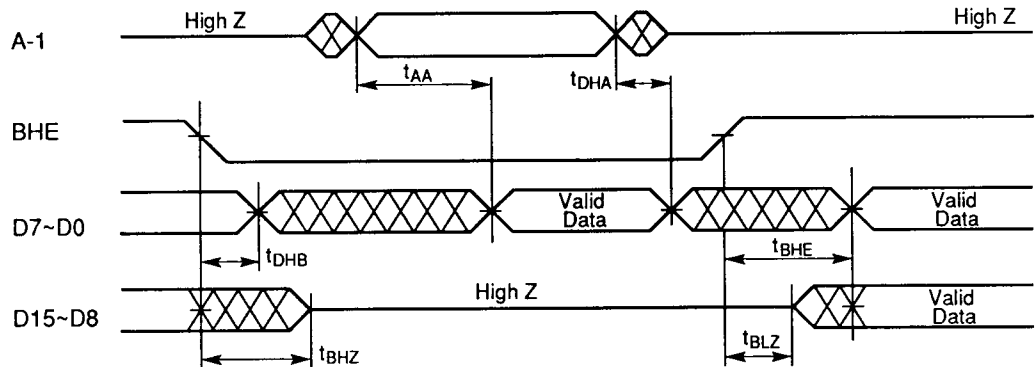
■ TIMING WAVEFORM

• Word Mode (BHE = 'V<sub>IH</sub>') or Byte Mode (BHE = 'V<sub>IL</sub>') (1)



- NOTES:**
1. t<sub>DHA</sub>, t<sub>DHC</sub>, t<sub>DHO</sub>; determined by faster.
  2. t<sub>AA</sub>, t<sub>ACE</sub>, t<sub>OE</sub>; determined by slower.
  3. t<sub>CLZ</sub>, t<sub>OLZ</sub>; determined by slower.

• Word Mode, Byte Mode Switch (2)



- NOTES:**
1.  $\overline{CE}$  and  $\overline{OE}$  are enable A<sub>19</sub> ~ A<sub>0</sub> are valid.
  2. D<sub>15</sub>/A-1 pin is in the output state when BHE is high,  $\overline{CE}$  and  $\overline{OE}$  are enable. Therefore, the input signals of opposite phase to the output must not apply to them.

