MSM6375/74/73/72-xxx

1-Mbit/512-Kbit/256-Kbit/128-Kbit Mask ROM Voice Synthesizer

GENERAL DESCRIPTION

For a new circuit design, it is recommended to use the MSM6650 Family described later.
The MSM6375 series is an ADPCM voice synthesis IC utilizing a CMOS voice processor circuit in conjunction with a built-in MASK ROM for voice data storage. Since it has a built-in 12-bit D/A converter and low pass filter, voice output can easily be accomplished by connecting an external power amplifier and speaker. Two sounds can be synthesized and played back simultaneously making applications with BGM (Background Music) and voice with echo possible. Additionally eight beep tones are available at four selectable durations for use as prompts in a message.
The MSM6376 is an evaluation IC for the MSM6375 series.

f_{OSC} [kHz]	f_S [kHz]	f_{CUT} [kHz]	Beep Tone	LPF Voltage	DAC Voltage
64	4.0	1.5	1 kHz & 2 kHz	2.7 V to 5.5 V	2.4 V to 5.5 V
	6.4	3.0			
	8.0	3.0			
128	8.0	3.0	2 kHz & 4 kHz	4.5 V to 5.5 V	
	12.8	6.0			
	16.0	6.0			

FEATURES

Device	ROM size	Speech period		
		f_S=4.0 kHz	f_S=6.4 kHz	f_S=8.0 kHz
MSM6375-xxx	1 Mbit	64 sec	40 sec	32 sec
MSM6374-xxx	512 Kbit	32 sec	20 sec	16 sec
MSM6373-xxx	256 Kbit	16 sec	10 sec	8 sec
MSM6372-xxx	128 Kbit	8 sec	5 sec	4 sec

Note: f_S=Sampling frequency

- Single-chip CMOS
- ROM Custom
- 4-bit ADPCM system
- Echo or 2-channel mixing functions
- Built-in BEEP Tone
- Maximum number of words: 111
- Built-in 12-bit D/A converter
- Built-in Low-pass filter (LPF)
- Standby function
- Oscillation: RC or crystal
- Package options:
  18-pin DIP (DIP 18-P-300) (Product name: MSM6375-xxxRS/MSM6374-xxxRS/MSM6373-xxxRS/MSM6372-xxxRS)
  24-pin SOP (SOP 24-P-430-K) (Product name: MSM6375-xxxGS-K/MSM6374-xxxGS-K/MSM6373-xxxGS-K/MSM6372-xxxGS-K)

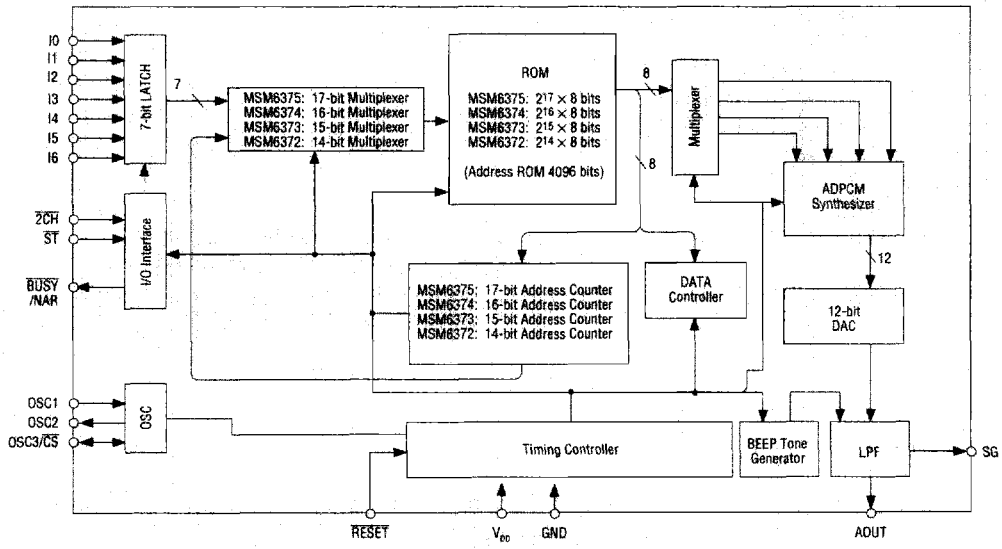
  Chip

Code Option

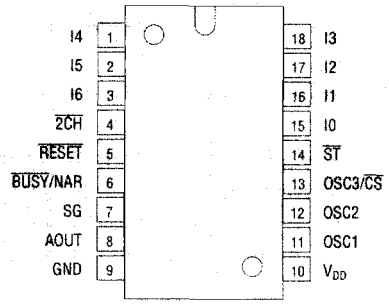
There are 14 types of options for the MSM6375 family as shown below. Select one of them.

MSM6375 Family					
Option name	**RC/XT**	**$\overline{\text{BUSY}}$/NAR**	**DA/LPF**	**Standby**	**CPU/SW**
Option A	RC	NAR	LPF	None	CPU
Option B	RC	$\overline{\text{BUSY}}$	LPF	Available	SW
Option C	XT	NAR	LPF	None	CPU
Option D	RC	$\overline{\text{BUSY}}$	LPF	None	SW
Option E	XT	NAR	LPF	Available	CPU
Option F	XT	NAR	DA	None	CPU
Option G	RC	NAR	LPF	Available	CPU
Option H	RC	$\overline{\text{BUSY}}$	LPF	None	CPU
Option I	RC	$\overline{\text{BUSY}}$	DA	Available	CPU
Option J	RC	NAR	DA	Available	CPU
Option K	XT	$\overline{\text{BUSY}}$	LPF	None	CPU
Option L	RC	$\overline{\text{BUSY}}$	LPF	Available	CPU
Option M	XT	NAR	DA	Available	CPU
Option N	RC	$\overline{\text{BUSY}}$	DA	None	CPU

BLOCK DIAGRAM

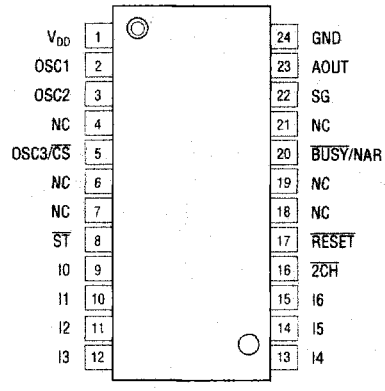


PIN CONFIGURATION (TOP VIEW)



18-Pin Plastic DIP

Note: Applicable to the MSM6375-XXX-RS, MSM6374-XXX-RS, MSM6373-XXX-RS, MSM6372-XXX-RS.



24-Pin Plastic SOP

Note: Applicable to the MSM6375-XXXGS-K, MSM6374-XXXGS-K, MSM6373-XXXGS-K, MSM6372-XXXGS-K.

PIN DESCRIPTIONS

Symbol	Type	Description
I0-I6	I	**Selectable.** *The code when the $\overline{ST}$ pulse is at the "L" level is input and latched at the rising edge of the* $\overline{ST}$ pulse.
$\overline{2CH}$	I	**Echo playback or simultaneous playback of two audible signals.** When only the $\overline{2CH}$ pulse is input in 1-channel operation, echo playback occurs. The echo delay time can be changed by changing the $\overline{2CH}$ pulse input timing. Inputting the $\overline{ST}$ pulse when $\overline{2CH}$=L causes simultaneous playback in 2-channel operation.
SG	O	Connect a capacitor of about 1 µF to this pin when the LPF output is selected as an option. Capacitor connection to this pin improves the SN ratio of the LPF. Leave this pin open when the LPF output is not selected.
AOUT	O	**Analog voice output pin.** Output of the D/A converter or output through the LPF can be selected as an option.
$\overline{BUSY}$/NAR	O	**Busy/Next Address Request.** Output of the $\overline{BUSY}$ signal or NAR signal can be selected as an option. If $\overline{BUSY}$ is selected the level of this pin is "L" while voice synthesis is carried out in the IC. If NAR is selected, the $\overline{ST}$ input for channel 1 is valid when this pin is at the H level.
$\overline{RESET}$	I	**Reset.** The IC is set to the standby state when the input to this pin is at the "L" level. In this state, the oscillation stops and the AOUT is set to the GND level for initialization. This IC has a built-in the power-on reset circuit. For normal functioning of the power-on reset, the power supply must rise within 1 ms. If a 1 ms rise time is unsuitable, apply the $\overline{RESET}$ pulse at the time of power-on.
GND	—	**Ground pin.**
V_{DD}	—	**Power supply pin.** Insert a bypass capacitor of 0.1 µF or more between this pin and the GND pin.
OSC1	I	**Crystal oscillator connecting pin.** This pin becomes the RC connecting pin when RC oscillation is selected. Input from this pin if external clock is used.
OSC2	O	**Cnystal oscillator connecting pin selectable.** This pin becomes the RC connecting pin when RC selected.
OSC3/$\overline{CS}$	I/O	**RC connecting pin.** If crystal oscillation is selected, it becomes the $\overline{CS}$ pin to enable $\overline{ST}$ input when the $\overline{CS}$ is "L". If the $\overline{CS}$ is unnecessary, fix $\overline{CS}$ at the "L" level.
$\overline{ST}$	I	When the $\overline{ST}$ is "L", the signals at I0 to I6 are input to the IC and latched at the rising edge of the $\overline{ST}$. The address input for channel 1 is valid when NAR is "H". For playback in channel 2, the sound volume for channel 2 can be varied by the number of $\overline{ST}$ pulses when the $\overline{2CH}$ is "L". If the SW input interface is selected, repeated synthesis occurs when the $\overline{ST}$ is fixed at the "L" level.

ABSOLUTE MAXIMUM RATINGS

(GND=0V)

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	Ta = 25 °C	−0.3 to +0.7	V
Input Voltage	V_{IN}		−0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	—	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND=0V)

Parameter	Symbol	Condition		Range	Unit
Supply Voltage	V_{DD}	DAC output		+2.4 to +5.5	V
		LPF output	40 kHz ≤ f_{OSC} ≤ 140 kHz	+4.5 to +5.5	
			f_{OSC} ≤ 80 kHz	+2.7 to +5.5	
Operating Temperature	T_{op}	—		−40 to +85	°C
Master Oscillation Frequency (Note 1)	f_{OSC1}	LPF output		40 to 140	kHz
Master Oscillation Frequency (Note 1)	f_{OSC2}	DAC output		40 to 256	kHz

Notes: 1. The precision of the oscillation frequency with the optional RC oscillator depends heavily on the precision of an external capacitor and resistor.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD}=5.0 V, GND=0 V, Ta=−40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	—	4.2	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.8	V
"H" Output Voltage	V_{OH}	I_{OH} = −40 µA	4.6	—	—	V
"L" Output Voltage	V_{OL}	I_{OL} = 40 µA	—	—	0.4	V
"H" Input Current	I_{IH}	V_{IH} = V_{DD}	—	—	10	µA
"L" Input Current	I_{IL}	V_{IH} = 0 V	−10	—	—	µA
Operating Current Consumption	I_{DD}	—	—	4	10	mA
Standby Current Consumption	I_{DS}	—	—	—	10	µA
Relative Precision of D/A	$\|V_{DAE}\|$	No load	—	—	40	mV
D/A Output Impedance	R_{DAO}	—	15	25	35	kΩ
LPF Load Impedance	R_{AOUT}	—	50	—	—	kΩ

DC Characteristics

(V_{DD}=3.1 V, V_{SS}=0 V, Ta=−40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	—	2.6	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.5	V
"H" Output Voltage	V_{OH}	I_{OH} = −10 μA	2.7	—	—	V
"L" Output Voltage	V_{OL}	I_{OL} = 10 μA	—	—	0.4	V
"H" Input Current	I_{IH}	V_{IH} = V_{DD}	—	—	1	μA
"L" Input Current	I_{IL}	V_{IL} = 0 V	−1	—	—	μA
Operating Current Consumption	I_{DD}	—	—	1.5	4	mA
Standby Current Consumption	I_{DS}	—	—	—	1	μA
Relative Precision of D/A Output	$\|V_{DAE}\|$	No load	—	—	20	mV
D/A Output Impedance	R_{DAO}	—	15	25	35	kΩ
LPF Load Impedance	R_{AOUT}	—	50	—	—	kΩ

AC Characteristics

(V_{DD} = 5 V, Ta = −40 to +85°C, f_{OSC} = 64 kHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Master Oscillation Duty Cycle	f_{duty}	—	40	50	60	%
$\overline{RESET}$ Input Pulse Width	$t_{W(\overline{RST})}$	—	10	—	—	µs
$\overline{ST}$ Input Pulse Width (Note 3)	$t_{W(\overline{ST})}$	—	0.35	—	350	µs
$\overline{2CH}$ Input Pulse Width	$t_{W(\overline{2CH})}$	—	0.35	—	—	µs
$\overline{ST}$-$\overline{ST}$ Pulse Interval	t_{SS}	—	0.35	—	—	µs
$\overline{2CH}$ Setup Time	t_{CHS}	—	0.35	—	—	µs
$\overline{2CH}$ Hold Time	t_{SCH}	—	0.35	—	—	µs
Data Set Time	t_{DW}	—	10	—	—	µs
Data Hold Time	t_{WD}	—	10	—	—	µs
CS Setup Time (Note 1)	t_{CS}	—	10	—	—	µs
CS Hold Time (Note 1)	t_{SC}	—	10	—	—	µs
Selectable Sampling Frequency	f_{S1}	f_{OSC}/8	—	8.0	—	kHz
	f_{S2}	f_{OSC}/10	—	6.4	—	kHz
	f_{S3}	f_{OSC}/16	—	4.0	—	kHz
$\overline{BUSY}$ Output Time (1) (Note 5)	t_{SBS}	—	—	—	10	µs
$\overline{BUSY}$ Output Time (2) (Note 2)	t_{BN}	At f_S = 8 kHz	350	375	400	µs
$\overline{BUSY}$ Output Time (3) (Note 2 and 6)	t_{BF}	At master frequency = 64 kHz	—	—	64	ms
$\overline{BUSY}$ Output Time (4) (Note 2)	t_{BA}	At f_S = 8 kHz	350	375	400	µs
NAR Output Time (1) (Note 5)	t_{SNS}	—	—	—	10	µs
NAR output time (2)	t_{NN}	—	—	—	500	ns
NAR Output Time (3) (Note 4)	t_{NAA}	At f_S = 8 kHz	350	375	400	µs
NAR Output Time (4) (Note 4)	t_{NAB}	At f_S = 8 kHz	350	375	400	µs
NAR Output Time (5) (Note 4)	t_{NAC}	At f_S = 8 kHz	350	—	550	µs
D/A Converter Transition Time	t_{DAR}, t_{DAF}	At master frequency = 64 kHz	60	64	68	ms
LPF Stabilizing Time (Note 5)	t_L	At master frequency = 64 kHz	12	16	20	ms
Standby Transition Time (at end of voice output)	t_{STB}	At master frequency = 64 kHz	2.9	3.0	3.1	sec
$\overline{ST}$-$\overline{2CH}$ Pulse Interval	t_{S2CH}	At master frequency = 64 kHz	1.0	—	—	ms
ST Input Wait Time	t_{NS}	—	10	—	—	µs

Notes: 1. When crystal oscillation is selected as an option.
2. When $\overline{BUSY}$ is selected as an option, the duration is proportional to f_S.
3. When the CPU interface is selected as an option, the maximum value is proportional to f_S. The maximum value when playing one word (using the SW interface) is equal to the voice cycle time.
4. When NAR is selected as an option, the duration is proportional to f_S. (When f_S is HIGH, the cycle is shortened.)
5. Applicable at the start of oscillation.
6. When playback occurs during the standby transition period (t_{DAF}).

AC Characteristics

(V_{DD} = 5 V, Ta = –40 to +85°C, f_{OSC1} = 40 to 140 kHz, f_{OSC2} = 40 to 256 kHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Master Oscillation Duty Cycle	f_{duty}	—	40	50	60	%
$\overline{\text{RESET}}$ Input Pulse Width	$t_{W(\overline{RST})}$	—	10	—	—	µs
$\overline{\text{ST}}$ Input Pulse Width (Note 2)	$t_{W(\overline{ST})}$	—	0.35	—	a	µs
$\overline{\text{2CH}}$ Input Pulse Width	$t_{W(\overline{2CH})}$	—	0.35	—	—	µs
$\overline{\text{ST}}$-$\overline{\text{ST}}$ Pulse Interval	t_{SS}	—	0.35	—	—	µs
$\overline{\text{2CH}}$ Setup Time	t_{CHS}	—	0.35	—	—	µs
$\overline{\text{2CH}}$ Hold Time	t_{SCH}	—	0.35	—	—	µs
Data Set Time	t_{DW}	—	10	—	—	µs
Data Hold Time	t_{WD}	—	10	—	—	µs
CS Setup Time (Note 1)	t_{CS}	—	10	—	—	µs
CS Hold Time (Note 1)	t_{SC}	—	10	—	—	µs
Selectable Sampling Frequency	f_{S1}	—	—	$f_{OSC}/8$	—	kHz
	f_{S2}	—	—	$f_{OSC}/10$	—	kHz
	f_{S3}	—	—	$f_{OSC}/16$	—	kHz
$\overline{\text{BUSY}}$ Output Time (1) (Note 3)	t_{SBS}	—	—	—	10	µs
$\overline{\text{BUSY}}$ Output Time (2)	t_{BN}	—	a	b	c	µs
$\overline{\text{BUSY}}$ Output Time (3) (Note 4)	t_{BF}	—	—	—	e	ms
$\overline{\text{BUSY}}$ Output Time (4)	t_{BA}	—	a	b	c	µs
NAR Output Time (1) (Note 3)	t_{SNS}	—	—	—	10	µs
NAR Output Time (2)	t_{NN}	—	—	—	500	ns
NAR Output Time (3)	t_{NAA}	—	a	b	c	µs
NAR Output Time (4)	t_{NAB}	—	a	b	c	µs
NAR Output Time (5)	t_{NAC}	—	a	—	d	µs
D/A Converter Transition Time (Note 3)	t_{DAR}, t_{DAF}	—	e-4	e	e+4	ms
LPF Stabilizing Time	t_L	—	f-4	f	f+4	ms
Standby Transition Time (at end of speech output)	t_{STB}	—	g-0.1	g	g+0.1	sec
$\overline{\text{ST}}$-$\overline{\text{2CH}}$ Pulse Interval	t_{S2CH}	—	h	—	—	ms
ST Input Wait Time	t_{NS}	—	10	—	—	µs

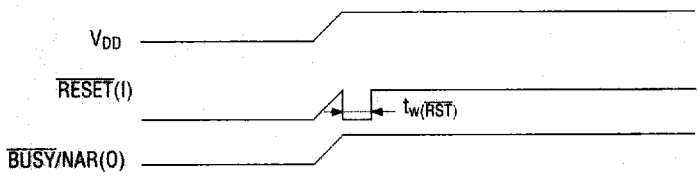
$$a = 350 \times \frac{8\ (kHz)}{f_S\ (kHz)} \qquad b = 375 \times \frac{8\ (kHz)}{f_S\ (kHz)} \qquad c = 400 \times \frac{8\ (kHz)}{f_S\ (kHz)} \qquad d = 550 \times \frac{8\ (kHz)}{f_S\ (kHz)}$$

$$e = 64 \times \frac{64\ (kHz)}{f_{OSC}\ (kHz)} \qquad f = 16 \times \frac{64\ (kHz)}{f_{OSC}\ (kHz)} \qquad g = 3.0 \times \frac{64\ (kHz)}{f_{OSC}\ (kHz)} \qquad h = 1.0 \times \frac{64\ (kHz)}{f_{OSC}\ (kHz)}$$

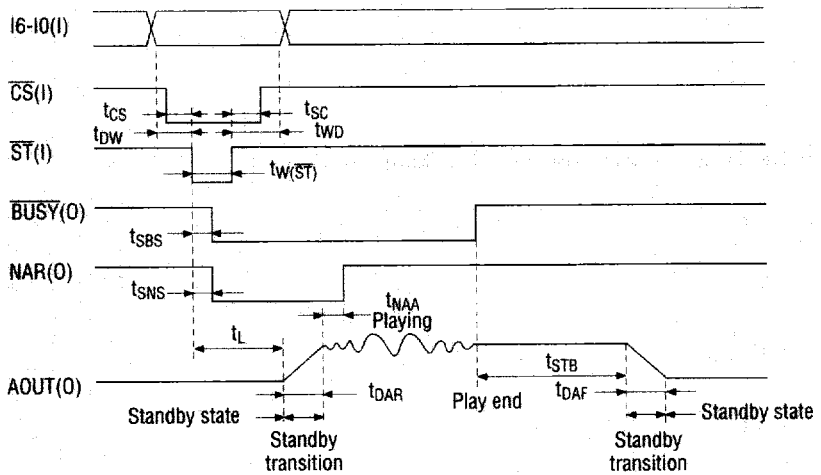
Notes: 1. When crystal oscillation is selected as an option.
2. When the CPU interface is selected as an option, the minimum value when playing one word (using the SW interface) is 0.35 µs and the maximum value is equal to the voice cycle time.
3. Applicable at the start of oscillation.
4. When playback occurs during the standby transition period (t_{DAF}).

TIMING DIAGRAMS

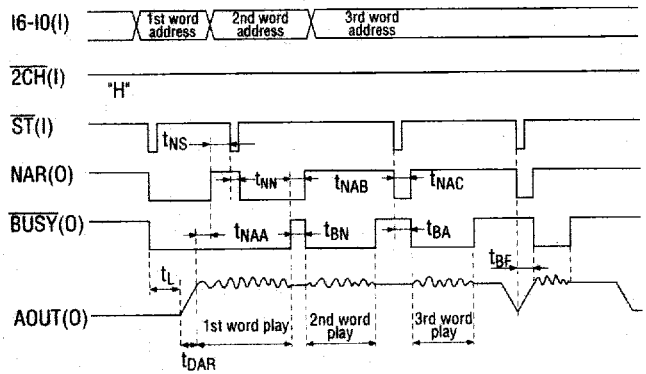
Power-on Timing



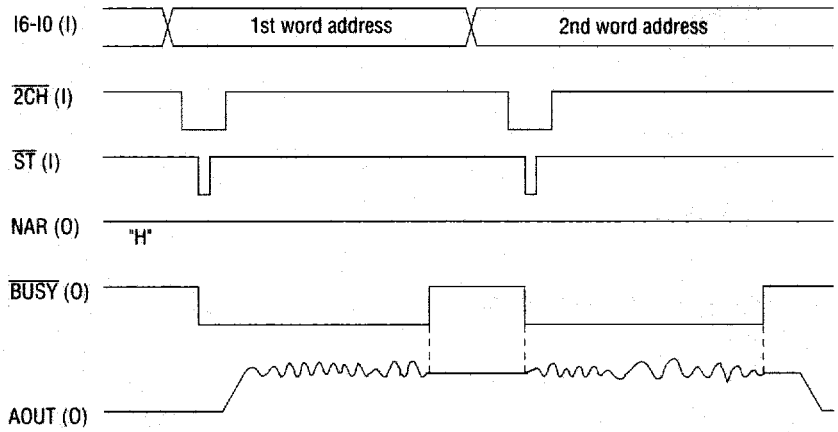
IC Startup and Standby State Timing



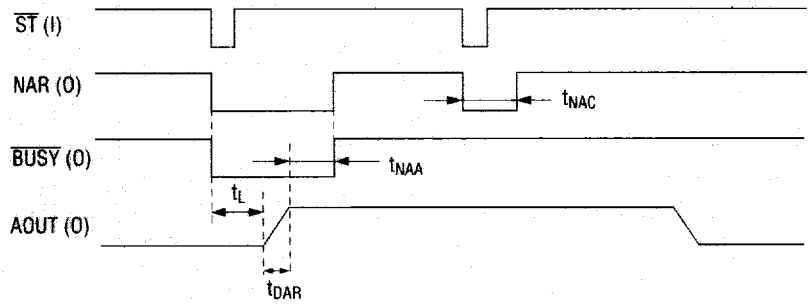
Channel 1 Operation Only (CPU Input Interface) Timing



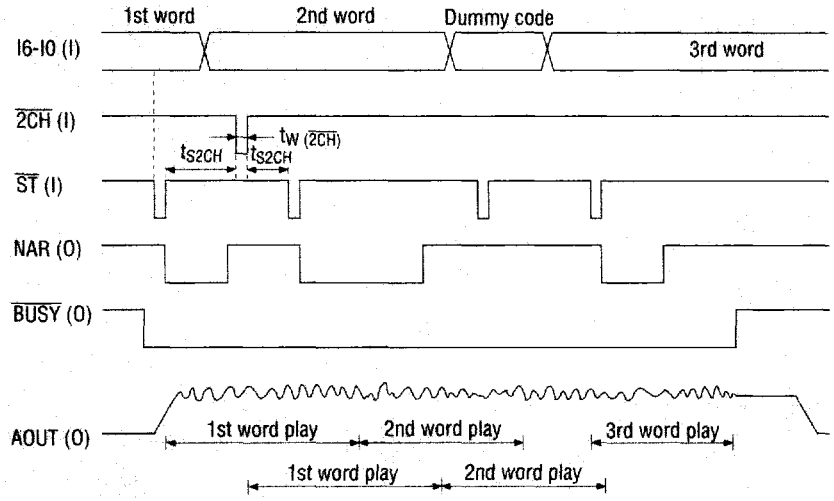
Channel 2 Operation Only (CPU Input Interface) Timing



Address Designation Operation with No Sound Timing

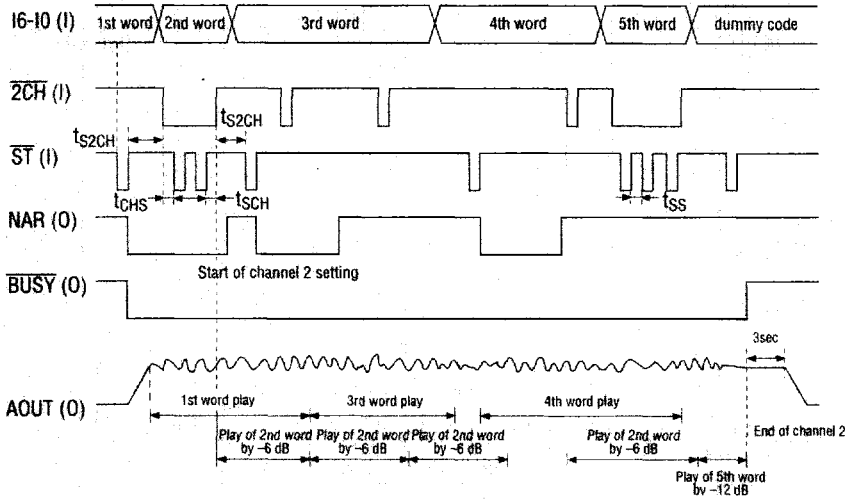


Echo Playback in Channel 1 Timing



Notes: 1. Input of the 2CH pulse without lowering ST starts echo playback. Echo playback is canceled unless play is continuous.
2. During echo playback, the waveform is a combination of the playback of channel 1 by the ST pulse and a –6 dB playback of channel 2 by the 2CH pulse.
3. In continuous play, the echo is applied to the next word (continuous play means playback of another word during a single word play.)
4. Input an unused code as a dummy code from the user selectable code at the end of echo playback. Without this input, the IC may enter the standby mode without waiting for 3 seconds after the end of playback when the standby option is selected.

Simultaneous Playback in Channel 1 and Channel 2 Timing



Notes. 1. Channel 2 starts playing when the $\overline{ST}$ pulse is input and $\overline{2CH}$="L". The sound volume can be changed by the number of the $\overline{ST}$ pulses using the table below.

2. Channel 2 plays a pre-set word each time the $\overline{2CH}$ pulse is input with the same sound volume until the IC goes to the standby state or until channel 2 is reset.

3. Input an unused code as a dummy code from the user selectable codes at the end of playback of channel 2. Without this input, the IC may enter the standby mode without waiting for 3 seconds after the end of play when the standby option is selected.

Number of $\overline{ST}$ pulses	Attenuation
1	No attenuation
2	−6 dB attenuation
3	−12 dB attenuation

FUNCTIONAL DESCRIPTION

Voice Code Selection

User selectable words (phrases) are a maximum of 111-word/phrases. The setting of I0 to I6 shown in Table 1.

Table 1 List of User Selected Words

I0 to I6	Code Explanation
0000000	STOP code
0000001 ↓ 1101111	User selectable codes (111-word)
1110000 ↓ 1110111	BEEP codes
1111000 ↓ 1111111	Test codes (do not use)

Non-Usable Range of Built-in ROM

The last two bytes of the built-in ROM are in the non-usable range. Do not use these bytes when analyzing speech.

Table 2 indicates non-usable addresses for each device type

Table 2 Built-in ROM Configuration and Non-usable Area

ROM configuration

Voice data control area
Voice data control area
Voice data control area

Address list for each area per device

Device	Voice data area	Non-usable area
MSM6372	00220 - 03FFD	03FFE, 03FFF
MSM6373	00220 - 07FFD	07FFE, 07FFF
MSM6374	00220 - 0FFFD	0FFFE, 0FFFF
MSM6375	00220 - 1FFFD	1FFFE, 1FFFF

CPU Interface and SW Input Interface

Select either the CPU interface or the SW (switch) input interface as an option for the input interface.

- **CPU interface**

If the CPU interface is selected, the $\overline{ST}$ pulse becomes valid when the NAR pin is High. User selected words are then fetched internally and vocalized. This interface is effective for playback of several words continuously. Note that when the $\overline{ST}$ pulse is kept at the Low level for longer than 800 µs, one word is played twice (at 8 kHz sampling).

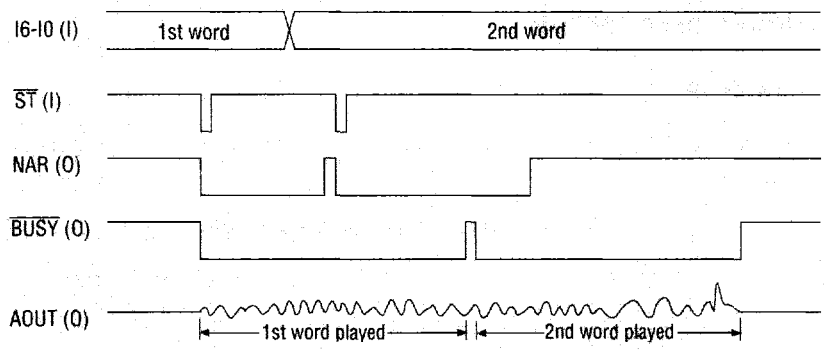


Figure 1 Timing of CPU Interface ($\overline{ST} \leq 350$ µs)

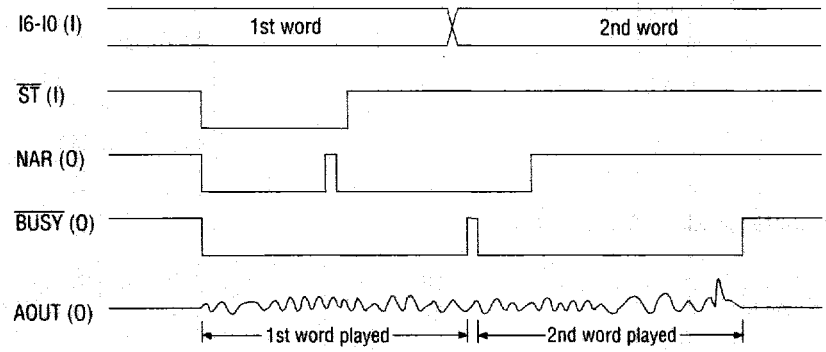


Figure 2 Timing of CPU Interface (800 µs < $\overline{ST}$)

When the $\overline{ST}$ pulse width is between 350 µs and 800 µs, a single word is played once or twice. However, when the $\overline{ST}$ pulse is input from the standby state, a single word is played only once if within 80 µs.

When a $\overline{ST}$ pulse width of longer than 350 µs (master frequency is 64 kHz) is input and the $\overline{BUSY}$ option has been selected, make sure the $\overline{ST}$ pulse is within 800 µs after the rise of $\overline{BUSY}$ pin.

- **SW (switch) input interface**

If the SW input interface is selected, the specified word is played repeatedly when $\overline{ST}$ is set to Low at the end of play of the specified word and is finished when it is set to High.

For example, when this IC is operated using a push switch, the same word is played repeatedly as long as the switch is pressed. If the switch is released, playback stops when the currently playing word is finished.

When playing different words continuously, change the code of I6 to I0 and maintain $\overline{ST}$ at the Low level before the playback is completed.

However, note that playing is interrupted if the input level of I6 to I0 becomes Low instantly when switching the address.

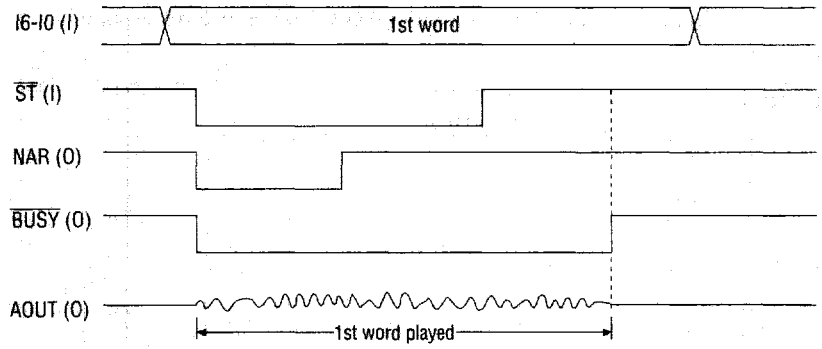


Figure 3 Timing of SW Input Interface (Play One Word)

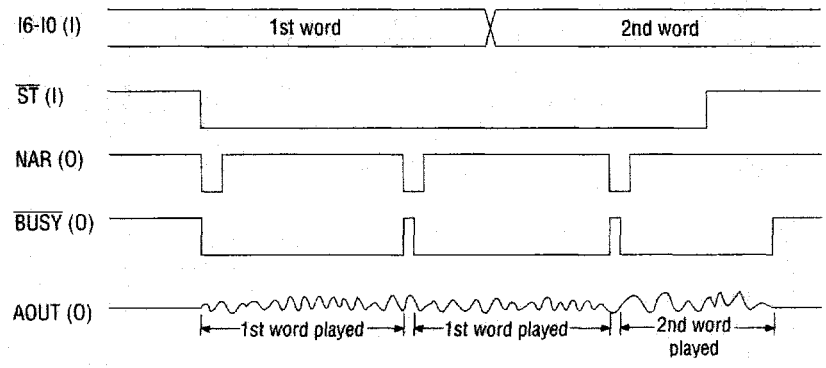


Figure 4 Timing of SW Input Interface (Repeated Play)

In the SW input interface, playback of the 1st and 2nd channels simultaneously is not possible. Neither 2-channel mixing nor echo playback is possible in this interface.

BEEP Tone Generation

Since this IC has an on-chip circuit to generate BEEP tones, the BEEP tones are selected using I6 to I0. Depending on the word code, the frequency and duration can be changed. The amplitude is approximately 1/4 V_{DD}.

The NAR/$\overline{\text{BUSY}}$ pin outputs a Low level during BEEP tone play regardless of whether either NAR or /BUSY is selected as the option. Figure 5 shows an example of such timing.

Neither the STOP code (explained in the next section) nor 2-channel playback is valid during the playback of the BEEP tone. The following table shows the relationship between the BEEP tones and addresses when the oscillation frequency is 64 kHz.

Table 3 Relationship between BEEP Tones and Addresses

I6	I5	I4	I3	I2	I1	I0	BEEP tone frequency	Generating duration (sec)
1	1	1	0	0	0	0	2.0	0.064
					0	1		0.125
					1	0		0.250
					1	1		0.500
				1	0	0	1.0	0.064
					0	1		0.125
					1	0		0.250
					1	1		0.500

When the code for a BEEP tone is input while playing either the 1st channel or the 2nd channel, the BEEP tone is generated after the completion of play. The opposite is also true.

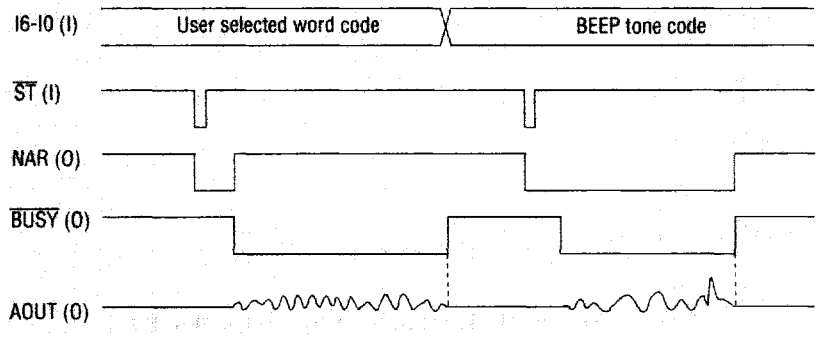


Figure 5 Timing at BEEP Tone Generation

Stop Code

Voice playing is finished when the $\overline{ST}$ pulse is input by setting I6 to I0 to "0000000" during play. The DA converter becomes 1/2 V_{DD}.

The input method of the $\overline{ST}$ pulse is subject to the AC characteristics when the NAR output is "H". When the NAR output is at the "L" level, the STOP code is valid by setting the $\overline{ST}$ pulse to the "L" level longer than 1 msec (f_{OSC}=64 kHz) or by the timing shown in Figure 6.

The STOP code is not valid during the generation of the BEEP tone. When the STOP code is input, only playback is stopped while the oscillation and the analog circuitry are still operating.

When the $\overline{RESET}$ pulse is input, all operations are halted.

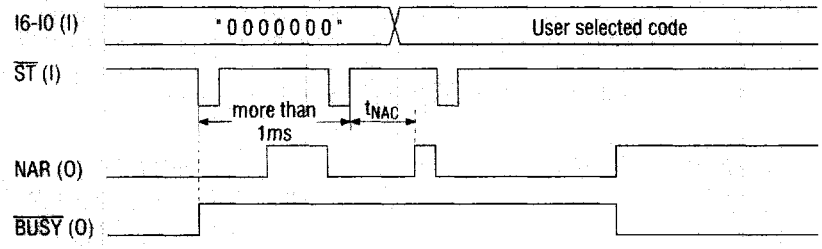


Figure 6 Example of STOP Code Input Timing

Sampling Frequencies

Sampling frequencies can be specified for each word in the voice data of the built-in ROM. When the 1st and the 2nd channels are simultaneously played back, the sampling frequency of the 1st channel has priority.

Three types of sampling frequencies can be selected during voice data analysis. The relationship between the master frequency, f_{OSC}, and the sampling frequency, f_S is as follows:

Selection 1	$f_{S1}=f_{OSC}/8$
Selection 2	$f_{S2}=f_{OSC}/10$
Selection 3	$f_{S3}=f_{OSC}/16$

Echo Playback and Channel 2 Playback

By using the $\overline{2CH}$ input, echo or 2-channel playback is possible. Because both echo and 2-channel playback use the $\overline{2CH}$ pin, switch between modes by returning the IC to the standby state. This function is not available in the SW input interface or during generation of BEEP tones.

- **Echo playback**

Echo playback is performed by combining a voice waveform of the 1st channel with a delayed voice waveform with –6 dB attenuation (half the amplitude of the channel 1 voice waveform).

The echo delay time is the time until the $\overline{2CH}$ pulse is input from the start of play of channel 1.

However, when starting this operation from the standby state, pop noise suppression time is not counted as delay time.

In echo playback, echo is applied to all the words during continuous play of channel 1 (continuous play means playback of the next word during playback.)

• 2-channel mixing playback

Using 2-channel mixing playback, a different word can be played during the play of channel 1. This has a wide range of application such as BGM and combinations of instruments. Voice data on channel 2 can remain the same while the sound volume may be changed to 1, 1/2 and 1/4 according to channel 1. The change in sound volume is determined by the number of $\overline{ST}$ pulses when starting the 2nd channel.

Once 2-channel mixing is set, it is maintained until the standby state or until channel 2 is reset. Because of this, restart can be accomplished by the input of the $\overline{2CH}$ pulse only. (See Table 4.)

Table 4 Number of $\overline{ST}$ Pulses and Attenuation

Number of $\overline{ST}$ pulses	Attenuation
1	No attenuation (100% of voice data)
2	–6 dB attenuation (1/2 of voice data)
3	–12 dB attenuation (1/4 of voice data)

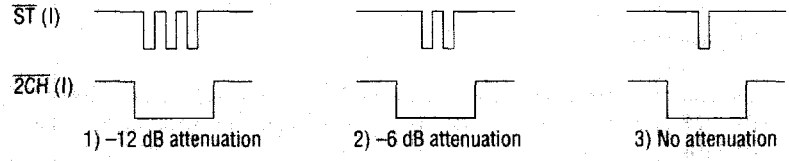


Figure 7 Input Timing of 2-Channel Mixing

Standby Transition

When standby transition is enabled as an option, the IC changes to the standby state and halts all operations unless another word is played within 3 seconds of the completion of playback of a signal word. For this reason, it takes approximately 100 ms before the next playback is started since the IC activates the pop noise suppression circuitry.

When standby transition is disabled as an option, the IC does not go into the standby mode even when playback is completed. At this time, the output from AOUT is approximately $1/2\ V_{DD}$ and the IC still draws current as oscillation is continued. When restarted, the next playback begins after approximately 350 µs.

If disabling standby transition is disabled as an option, the $\overline{RESET}$ pulse must be input to set to the standby state. Pop noise may be generated at the input of the $\overline{RESET}$ pulse since the output level from AOUT becomes GND level instantly.

Voice Output

The voice output pin can be selected by the output of the DA converter either directly or through the built-in low-pass filter.

• Output waveform of DA converter

The output amplitude from the D/A converter is maximum $4095/4096 \times V_{DD}$ of a square wave that synchronizes with a sampling frequency. When selecting the D/A output, addition of an external low-pass filter is highly recommended.

Because the output impedance of D/A output varies between 15 kΩ and 35 kΩ, determine the filter constant so that the resistance variation does not influence the cut-off frequency of the low-pass filter.

Table 4 shows the output level from the AOUT pin when selecting an optional D/A output.

Table 5 Output Level from D/A Converter

Condition	Minimum level	Center level	Maximum level	Unit
1-Channel Playback	$\frac{1}{4} V_{DD}$	$\frac{1}{2} V_{DD}$	$\frac{3}{4} V_{DD}$	V
2-Channel Mixing	0.0	$\frac{1}{2} V_{DD}$	V_{DD}	V
BEEP Tone Playback	$\frac{3}{8} V_{DD}$	$\frac{1}{2} V_{DD}$	$\frac{3}{8} V_{DD}$	V

• Low-pass filter output

Since the low-pass filter is composed of switch capacitors, the cut-off frequency varies proportional to the master clock frequency.

When the sampling frequency (f_S) is 1/8 and 1/10 of the master clock frequency, the cut-off frequency, f_{CUT}, is $f_{CUT}=3/64\ f_{OSC}$ and is $f_{CUT}=3/128$ when f_S is 1/16. Table 6 shows the relationship between the sampling frequencies and the cut-off frequencies.

Table 6 Cut-off Frequency of Low-pass Filter

Sampling frequency (f_S)	Master clock frequency (f_{OSC})	Cut-off frequency (f_{cut})
4.0 kHz	64 kHz	1.5 kHz
6.4 kHz	64 kHz	3.0 kHz
8.0 kHz	64 kHz	3.0 kHz
12.8 kHz	128 kHz	6.0 kHz
16.0 kHz	128 kHz	6.0 kHz

The low-pass filter characteristics when the sampling frequency is 8 kHz are shown in Figure 8. Table 6 shows the output level from AOUT when selecting the low-pass filter option.

Table 7 Output Level of Low-pass Filter

Condition	Minimum level	Center level	Maximum level	Unit
1-Channel Playback	$\frac{1}{4}$ V_{DD}	$\frac{1}{2}$ V_{DD}	$\frac{3}{4}$ V_{DD}	V
2-Channel Mixing	0.7	$\frac{1}{2}$ V_{DD}	V_{DD}–0.7	V
BEEP Tone Playback	$\frac{3}{8}$ V_{DD}	$\frac{1}{2}$ V_{DD}	$\frac{3}{8}$ V_{DD}	V

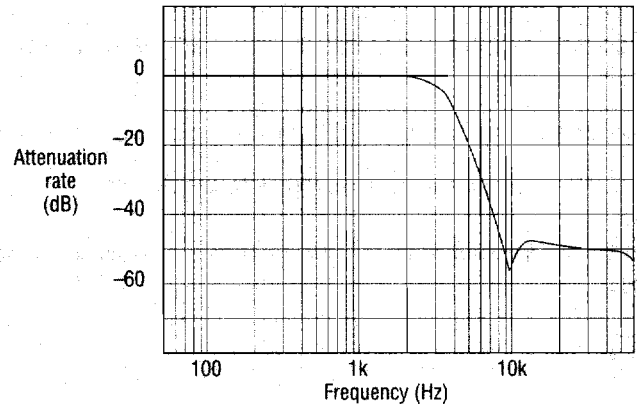


Figure 8 Low-pass Filter Characteristics (f_S=8 kHz)

- **Pop noise low-pass filter output**

Although this IC has a built-in pop noise suppression circuit, the voltage of the circled portion in Figure 9 may be changed abruptly by approximately 0.7 V when selecting the low-pass filter output and may generate a popping sound.

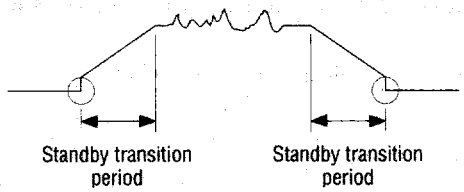
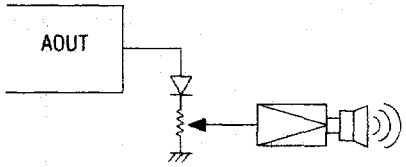


Figure 9 Pop Noise of Low-pass Filter Output

When connecting a diode at the output from AOUT, the popping sound can be reduced as shown in Figure 10.

Figure 10 Pop Noise Suppression Circuit



RC Oscillation

The external circuit diagram for RC oscillation is shown in Figure 11.

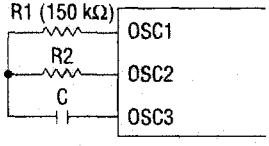


Figure 11 RC Oscillation Frequency

- **Determination of RC constant**

The RC oscillation frequency characteristics are shown in Figure 12. If f_{OSC} is set to 64 kHz, choose the appropriate values for C and R2 using the following as a reference:

C=100 pF, R1=150 kΩ, R2=50 kΩ

- **Fluctuation of RC oscillation frequencies**

When choosing RC oscillation, the RC oscillation frequencies are varied according to the fluctuation of the external C and R2 as well as the process variations of the IC.

When using a 50 kΩ R2, the error due to process variations of the IC is a maximum of ±4%. The fluctuation of the RC oscillation frequency when using a capacitance (C) of ±1% accuracy and a resistance (R2) of ±2% accuracy is a maximum of ±7% approximately.

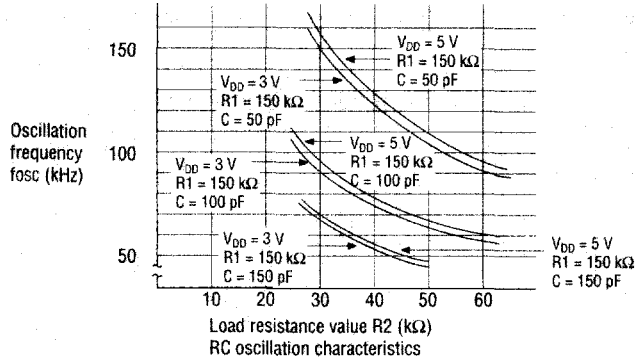


Figure 12 RC Oscillation Frequency

Crystal Oscillation

Figure 13 shows an external circuit using a crystal oscillator, KF-38S4-13PO102 (64 kHz), made by Kyocera Corp.

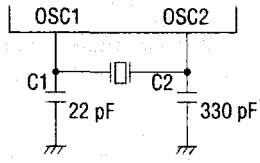


Figure 13 Circuit Diagram of Crystal Oscillator Connection

Connection with MSC1191/1192

When using an MSC1191 and an MSC1192, connect the STBY pin to the OSC3/$\overline{CS}$ pin and the OSC2 pin, respectively. When connecting with an MSC1191/1192, set C and R after mounting the chip to the board as the oscillation characteristics may change.

Option Item List

No.	Item	Center level		Remarks
1	Oscillation circuit	Crystal oscillation	RC oscillation	Crystal oscillation : OSC3/$\overline{CS}$ is a $\overline{CS}$ pin. R_{FB} is built-in. RC oscillation : OSC3/$\overline{CS}$ is a OSC3 pin.
2	Selection of $\overline{BUSY}$ or NAR	$\overline{BUSY}$	NAR	None
3	AOUT output	DA output	LPF output	None
4	Transition to standby	Yes	No	If the next user-specified word is not input within 3 seconds after playback is finished with "Standby" selected, the IC enters the standby state.
5	Input interface	SW input interface	CPU interface	

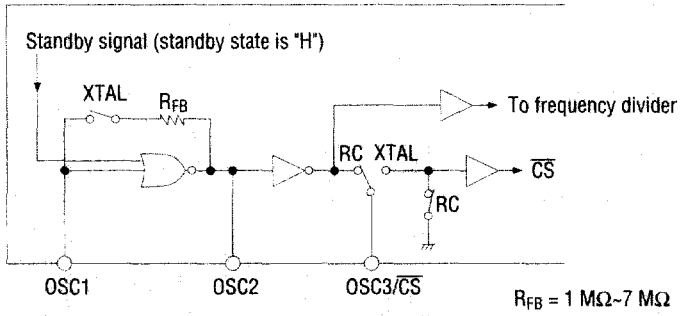


Figure 14 Internal Oscillation Circuit
(The switches in the diagram select RC oscillation)

APPLICATION CIRCUITS

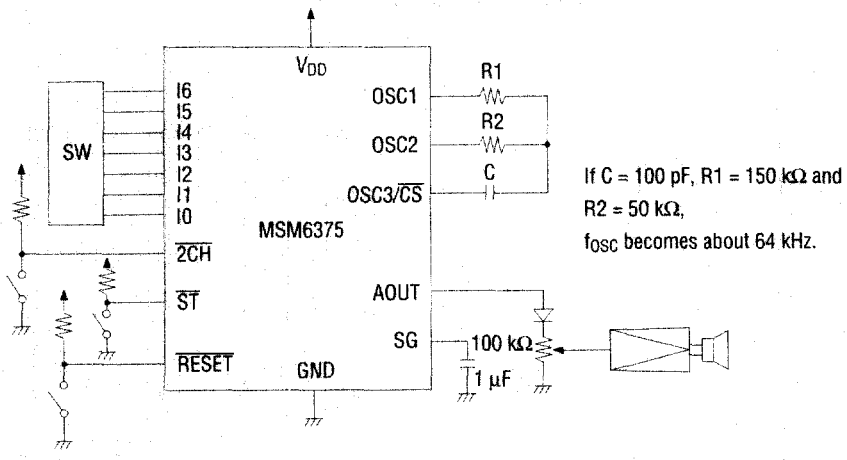


Figure 15 Application Circuit Example when Selecting RC, LPF and SW in Option

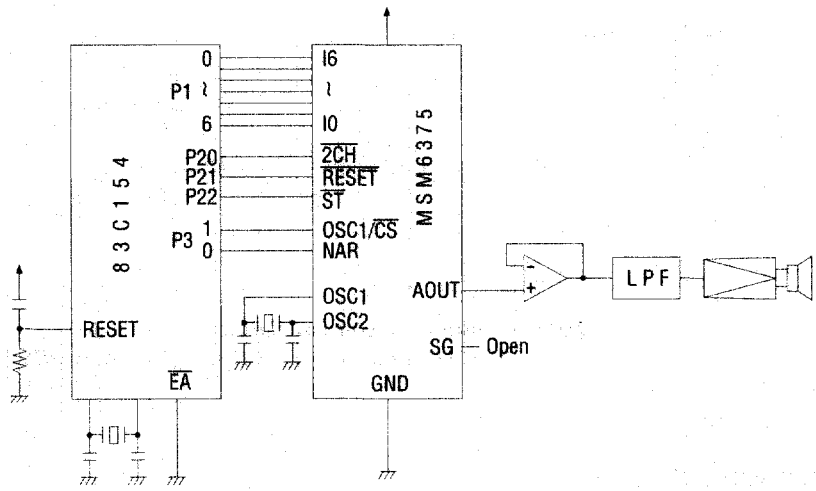


Figure 16 Application Circuit Example when Selecting XT, DAC and CPU in Option

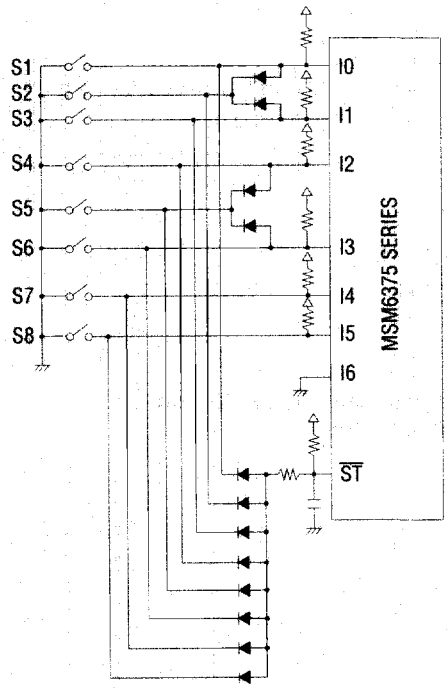


Table for voice address vs. switch address

	I6	I5	I4	I3	I2	I1	I0	ADR
S1	0	1	1	1	1	1	0	3E
S2	0	1	1	1	1	0	0	3C
S3	0	1	1	1	1	0	1	3D
S4	0	1	1	1	0	1	1	3B
S5	0	1	1	0	0	1	1	33
S6	0	1	1	0	1	1	1	37
S7	0	1	0	1	1	1	1	2F
S8	0	1	1	1	1	1	1	1F

Figure 17 Application Circuit Example to Output the Voice of Eight Words by Switch Interface

Figure 18 Application Circuit Example when connecting MSM6374-006 with MSM5055L-108 and MSC1192

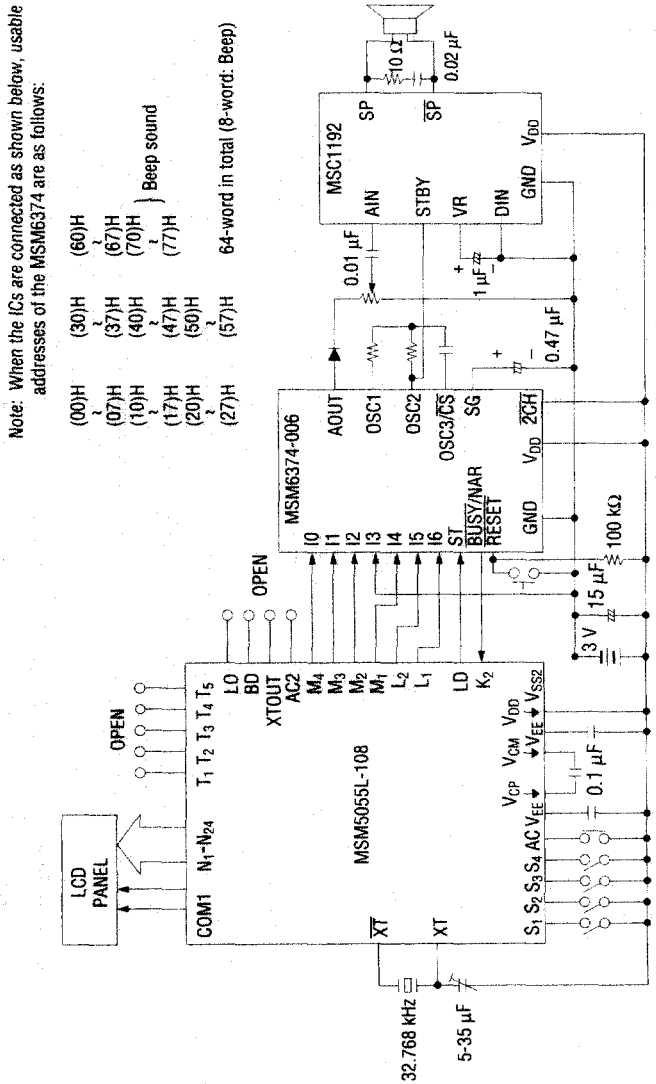
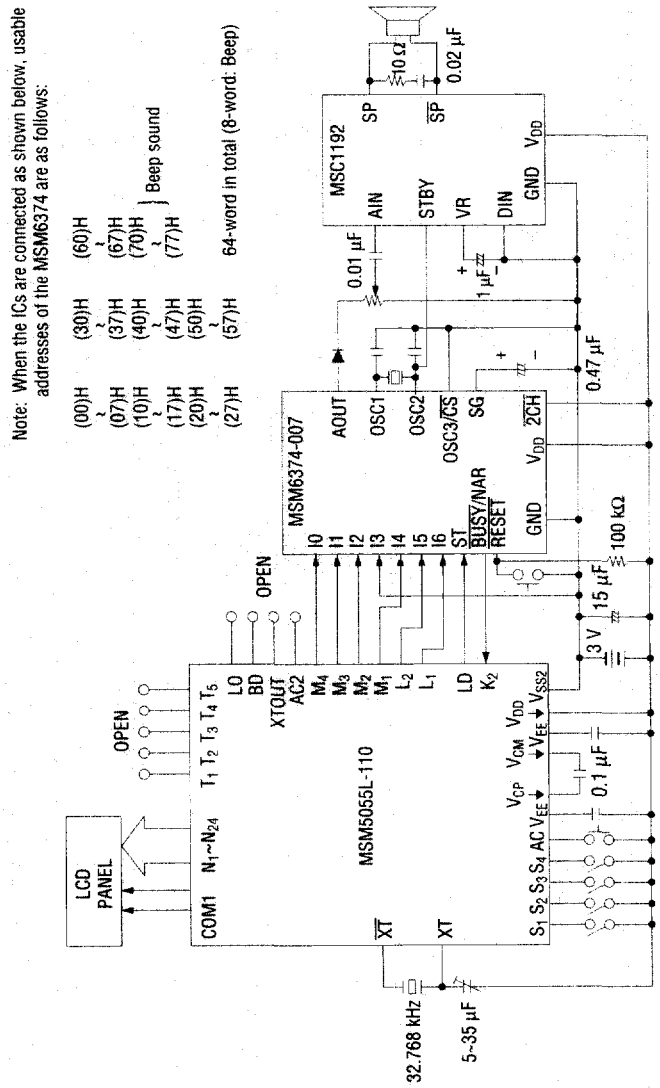


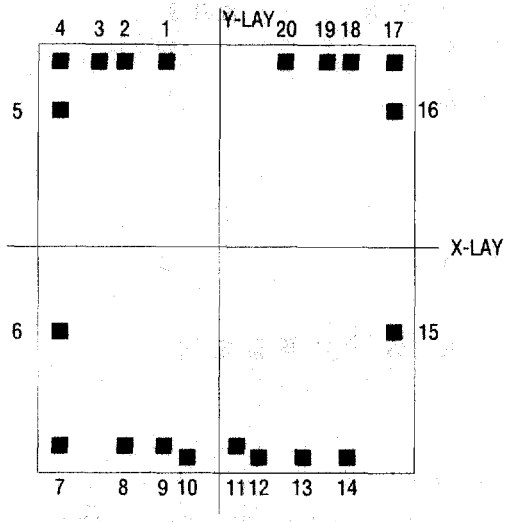
Figure 19 Application Circuit Example when connecting MSM6374-007 with MSM5055L-110 and MSC1192



PAD CONFIGURATION

Pad Layout

Product name	MSM6372-XXX
Function	128 -Kbit ROM built-in voice synthesis IC
Die size	3.49 × 4.00 (mm²)
Die thickness	350 µm±30 µm
Pad size	110 µm²
Substrate voltage	GND



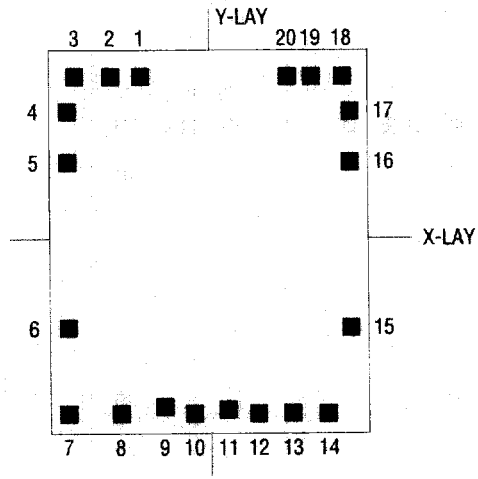
Pad Coordinates

(The die center is located at X=0, Y=0) (Unit: µm)

PAD No.	PAD Name	X-AXIS	Y-AXIS	PAD No.	PAD Name	X-AXIS	Y-AXIS
1	I4	–555	1830	11	AV_{DD}	107	–1754
2	I5	–960	1830	12	DV_{DD}	353	–1830
3	I6	–1140	1830	13	OSC1	766	–1829
4	$\overline{2CH}$	–1545	1830	14	OSC2	1180	–1829
5	$\overline{RESET}$	–1590	1421	15	OSC3/$\overline{CS}$	1590	–644
6	$\overline{BUSY}$/NAR	–1590	–650	16	$\overline{ST}$	1590	1421
7	SG	–1509	–1751	17	I0	1545	1830
8	AOUT	–921	–1752	18	I1	1140	1830
9	AGND	–513	–1720	19	I2	960	1830
10	DGND	–281	–1830	20	I3	555	1830

Pad Layout

Product name	MSM6373-XXX
Function	256 -Kbit ROM built-in voice synthesis IC
Die size	3.49 × 4.70 (mm^2)
Die thickness	350 µm±30 µm
Pad size	110 µm^2
Substrate voltage	GND



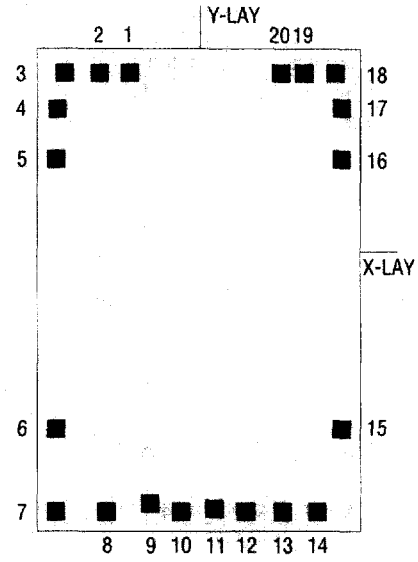
Pad Coordinates

(The die center is located at X=0, Y=0) (Unit: µm)

PAD No.	PAD Name	X-AXIS	Y-AXIS	PAD No.	PAD Name	X-AXIS	Y-AXIS
1	I4	−955	2180	11	AV_{DD}	107	−2104
2	I5	−1135	2180	12	DV_{DD}	353	−2180
3	I6	−1545	2180	13	OSC1	766	−2179
4	$\overline{2CH}$	−1590	1791	14	OSC2	1180	−2179
5	$\overline{RESET}$	−1590	1235	15	OSC3/$\overline{CS}$	1590	−994
6	$\overline{BUSY}$/NAR	−1590	−1024	16	$\overline{ST}$	1590	1225
7	SG	−1509	−2101	17	I0	1590	1791
8	AOUT	−921	−2102	18	I1	1545	2180
9	AGND	−513	−2070	19	I2	1135	2180
10	DGND	−281	−2180	20	I3	955	2180

Pad Layout

Product name	MSM6374-XXX
Function	512 -Kbit ROM built-in voice synthesis IC
Die size	3.52 × 6.17 (mm²)
Die thickness	350 µm±30 µm
Pad size	110 µm²
Substrate voltage	GND



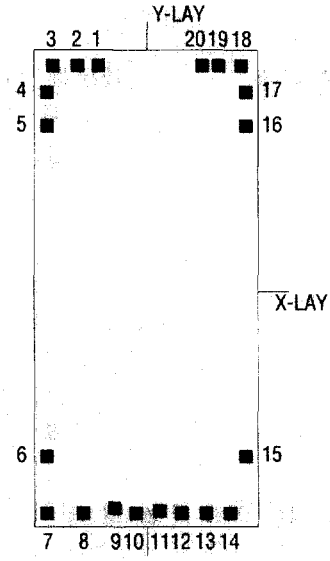
Pad Coordinates

(The die center is located at X=0, Y=0) (Unit: µm)

PAD No.	PAD Name	X-AXIS	Y-AXIS	PAD No.	PAD Name	X-AXIS	Y-AXIS
1	I4	−955	2930	11	AV_{DD}	107	−2854
2	I5	−1135	2930	12	DV_{DD}	353	−2930
3	I6	−1545	2930	13	OSC1	766	−2929
4	$\overline{2CH}$	−1590	2541	14	OSC2	1180	−2929
5	$\overline{RESET}$	−1590	1985	15	OSC3/$\overline{CS}$	1590	−1744
6	$\overline{BUSY}$/NAR	−1590	−1774	16	$\overline{ST}$	1590	1975
7	SG	−1509	−2851	17	I0	1590	2541
8	AOUT	−921	−2852	18	I1	1545	2930
9	AGND	−513	−2820	19	I2	1135	2930
10	DGND	−281	−2930	20	I3	955	2930

Pad Layout

Product name	MSM6375-XXX
Function	1-Mbit ROM built-in voice synthesis IC
Die size	3.52 × 9.16 (mm²)
Die thickness	350 µm±30 µm
Pad size	110 µm²
Substrate voltage	GND



Pad Coordinates

(The die center is located at X=0, Y=0) (Unit: µm)

PAD No.	PAD Name	X-AXIS	Y-AXIS	PAD No.	PAD Name	X-AXIS	Y-AXIS
1	I4	−955	4425	11	AV_{DD}	107	−4349
2	I5	−1135	4425	12	DV_{DD}	353	−4425
3	I6	−1545	4425	13	OSC1	766	−4424
4	$\overline{2CH}$	−1590	4036	14	OSC2	1180	−4424
5	$\overline{RESET}$	−1590	3480	15	OSC3/$\overline{CS}$	1590	−3239
6	$\overline{BUSY}$/NAR	−1590	−3269	16	$\overline{ST}$	1590	3470
7	SG	−1509	−4346	17	I0	1590	4036
8	AOUT	−921	−4347	18	I1	1545	4425
9	AGND	−513	−4315	19	I2	1135	4425
10	DGND	−281	−4425	20	I3	955	4425