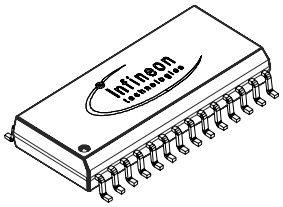
System **B**asis **C**hip **TLE 6260**

Preliminary Data Sheet

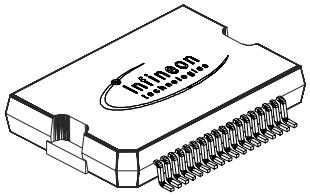
1 Overview

1.1 Features

- Fault tolerant differential CAN-transceiver
- CAN data transmission rate up to 125 kBaud
- Bus failure management
- Fail-safe management and output
- Low power mode management
- Very low power consumption in sleep mode
- Dual low-dropout 5V regulator
- Independent CAN-transceiver supply
- Power on and under-voltage reset generator
- Window watchdog
- Programable time base
- 32/8 bit SPI-Interface
- Three wake-up inputs
- High side switch
- Ground-shift detection
- Wide input voltage and temperature range



P-DSO-28-6
Enhanced Power



P-DSO-36-12
Power Package

Type	Ordering Code	Package
TLE 6260-1 G	Q67007-A9463	P-DSO-28-6
TLE 6260-2 G	on request	P-DSO-28-6
TLE 6260 GP	Q67007-A9464	P-DSO-36-12

2 Description

The TLE 6260 is a monolithic integrated circuit which is available in both, the enhanced power package P-DSO-28-6 and the power package P-DSO-36-12. It incorporates a failure tolerant low speed CAN-transceiver for differential mode data transmission, a triple low dropout voltage regulator as well as a serial peripheral interface (SPI) to control and monitor the IC. Further there are integrated wake-up inputs for monitoring of external contacts, a high side switch to supply e.g. external wake-up contacts, a ground shift detection system, a window watchdog circuit and a bidirectional reset circuit as well as a fail safe output.

The IC is designed to withstand the severe conditions of automotive applications.

3 Pin Configurations

(top view)

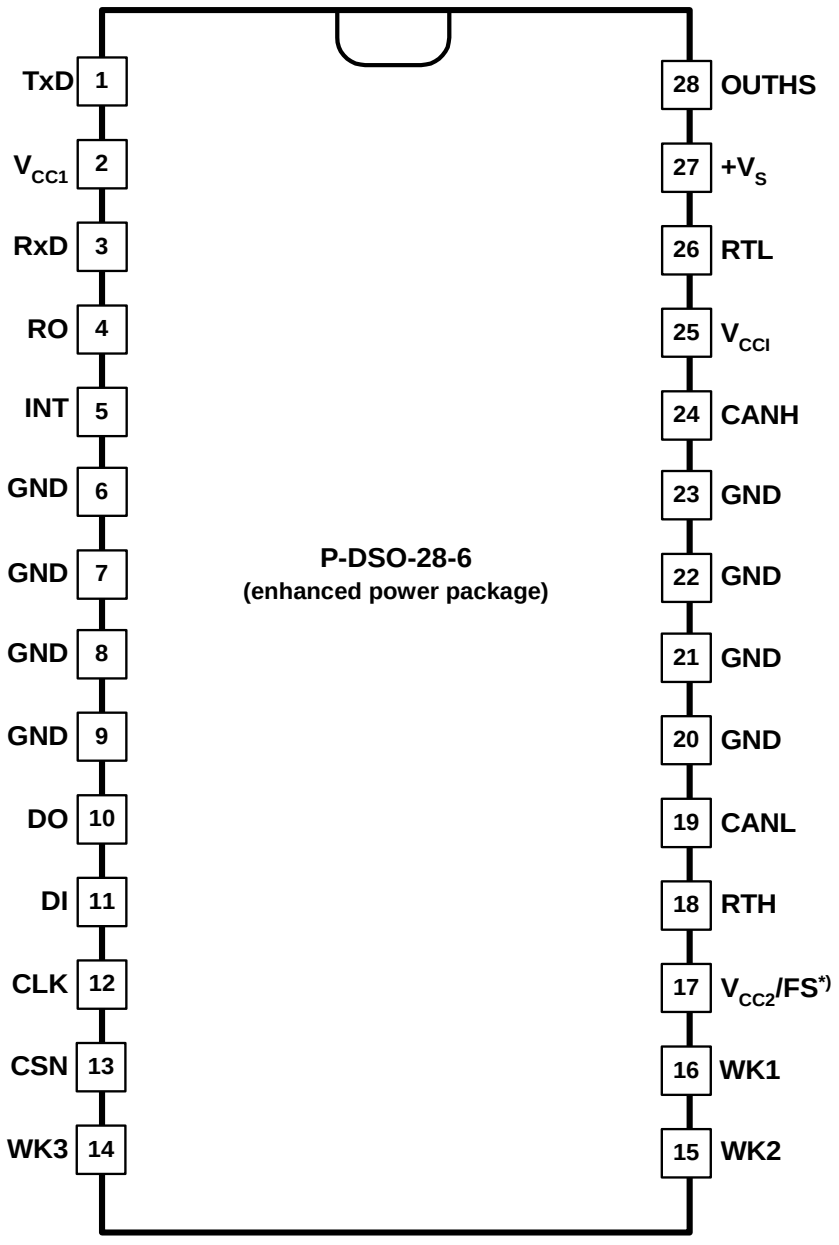


Figure 1

(top view)

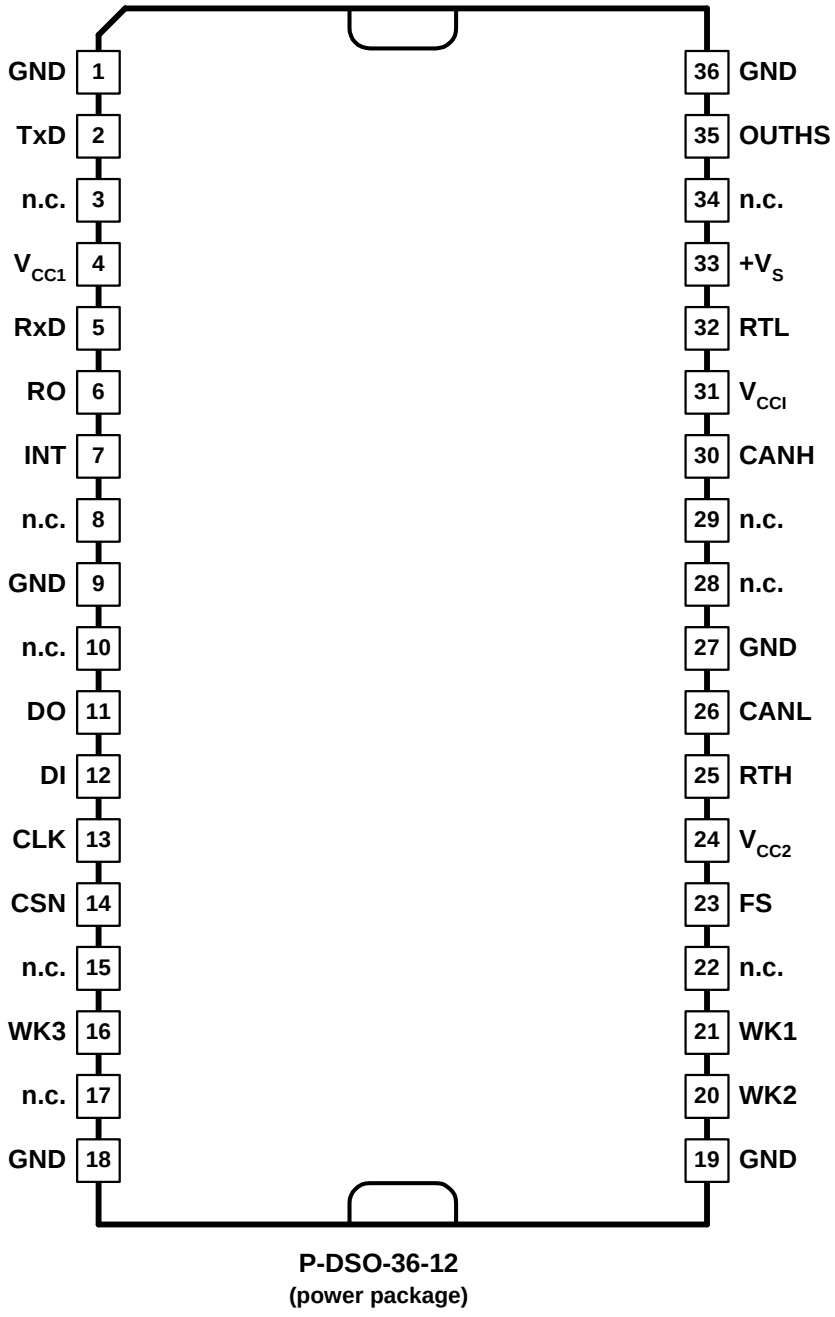


Figure 2

4 Pin Definitions and Functions: P-DSO-28-6

Pin No.	Symbol	Function
1	*TxD*	**CAN Transmit data input;** integrated pull up
2	V_{CC1}	**Output voltage regulator 1**; 5V logic supply, block to GND with an external capacitor $C_Q \geq 6$ µF, ESR < 10 Ω
3	*RxD*	**CAN Receive data output;** integrated pull up
4	*RO*	**Reset output / input**; open drain output, integrated pull up, active low
5	*INT*	**Interrupt output**; monitors failures and events in parallel to the SPI diagnosis word, reseted via SPI
6, 7, 8, 9, 20, 21, 22, 23	*GND*	**Ground**; to reduce thermal resistance place cooling areas on PCB close to these pins.
10	*DO*	**SPI interface data out**; this tristate output transfers diagnosis data to the control device; the output will remain 3-stated unless the device is selected by a low on Chip-Select-Not (CSN); see **table 6** for Diagnosis protocol
11	*DI*	**SPI interface data in**; receives serial data from the control device; serial data transmitted to DI is a 32 / 8 bit control word with the Least Significant Bit (LSB) being transfered first: the input has an active pull down and requires CMOS logic level inputs; DI will accept data on the falling edge of CLK-signal; see **table 5** for input data protocol
12	*CLK*	**SPI interface clock input**; clocks the shiftregister; CLK has an internal active pull down and requires CMOS logic level inputs, works as wake-up input when device is in sleep mode
13	*CSN*	**SPI interface chip select not**; CSN is an active low input; serial communication is enabled by pulling the CSN terminal low; CSN input should only be transitioned when CLK is low; CSN has an internal active pull up and requires CMOS logic level inputs
14	*WK3*	**Wake-Up input 3**; for detection of external wake-up events, wake-up monitored at INT, RxD and SPI, in sleep mode controlled by cyclic sense function when selected
15	*WK2*	**Wake-Up input 2**; for detection of external wake-up events, wake-up monitored at INT, RxD and SPI, in sleep mode controlled by cyclic sense function when selected

Pin No.	Symbol	Function
16	*WK1*	**Wake-Up input 1** or **Battery voltage monitoring input**; for detection of external wake-up events, wake-up monitored at INT, RxD and SPI, in sleep mode controlled by cyclic sense function when selected ; **or** (selectable via SPI) for monitoring the battery voltage
17	V_{CC2} *FS*	**Output voltage regulator 2**; 5V supply, block to GND with an external capacitor $C_Q \geq 10$ µF, ESR < 10 Ω (version TLE 6260-1) **Fail Safe output**; open collector output, internal pull up, to control external safety critical applications (version TLE 6260-2)
18	*RTH*	**Termination input**; for CANH
19	*CANL*	**L bus line**; LOW in dominant state
24	*CANH*	**H bus line**; HIGH in dominant state
25	V_{CCI}	**Internal voltage regulator**; for stabilisation of CAN circuitry supply, block to GND with an external capacitor $C_Q \geq 6$ µF, ESR < 10 Ω
26	*RTL*	**Termination input**; for CANL
27	$+V_S$	**Power supply**; block to GND directly at the IC with ceramic capacitor
28	*OUTHS*	**High side output**; controlled via SPI, in sleep mode controlled by cyclic sense function when selected

5 Pin Definitions and Functions: P-DSO-36-12

Pin No.	Symbol	Function
1,9,18, 19,27,36	*GND*	**Ground**
3,8,10, 15,17, 22,28, 29,34	*n.c.*	**not connected**
2	*TxD*	**CAN Transmit data input;** integrated pull up
4	V_{CC1}	**Output voltage regulator 1**; 5V logic supply, block to GND with an external capacitor $C_Q \geq 6$ µF, ESR < 10 Ω
5	*RxD*	**CAN Receive data output;** integrated pull up
6	*RO*	**Reset output / input**; open drain output, integrated pull up, active low
7	*INT*	**Interrupt output**; monitors failures and events in parallel to the SPI diagnosis word, reseted via SPI
11	*DO*	**SPI interface data out**; this tristate output transfers diagnosis data to the control device; the output will remain 3-stated unless the device is selected by a low on Chip-Select-Not (CSN); see **table 6** for Diagnosis protocol
12	*DI*	**SPI interface data in**; receives serial data from the control device; serial data transmitted to DI is a 32 / 8 bit control word with the Least Significant Bit (LSB) being transfered first: the input has an active pull down and requires CMOS logic level inputs; DI will accept data on the falling edge of CLK-signal; see **table 5** for input data protocol
13	*CLK*	**SPI interface clock input**; clocks the shiftregister; CLK has an internal active pull down and requires CMOS logic level inputs, works as wake-up input when device is in sleep mode
14	*CSN*	**SPI interface chip select not**; CSN is an active low input; serial communication is enabled by pulling the CSN terminal low; CSN input should only be transitioned when CLK is low; CSN has an internal active pull up and requires CMOS logic level inputs
16	*WK3*	**Wake-Up input 3**; for detection of external wake-up events, wake-up monitored at INT, RxD and SPI, in sleep mode controlled by cyclic sense function when seleced

Pin No.	Symbol	Function
20	*WK2*	**Wake-Up input 2**; for detection of external wake-up events, wake-up monitored at INT, RxD and SPI, in sleep mode controlled by cyclic sense function when selected
21	*WK1*	**Wake-Up input 1** or **Battery voltage monitoring input**; for detection of external wake-up events, wake-up monitored at INT, RxD and SPI, in sleep mode controlled by cyclic sense function when selected; **or** (selectable via SPI) for monitoring the battery voltage
23	*FS*	**Fail Safe output**; open collector output, internal pull up, to control external safety critical applications
24	V_{CC2}	**Output voltage regulator 2**; 5V supply, block to GND with an external capacitor $C_Q \geq 10$ µF, ESR < 10 Ω
25	*RTH*	**Termination input**; for CANH
26	*CANL*	**L bus line**; LOW in dominant state
30	*CANH*	**H bus line**; HIGH in dominant state
31	V_{CCI}	**Internal voltage regulator**; for stabilisation of CAN cricuitry supply, block to GND with an external capacitor $C_Q \geq 6$ µF, ESR < 10 Ω
32	*RTL*	**Termination input**; for CANL
33	$+V_S$	**Power supply**; block to GND directly at the IC with ceramic capacitor
35	*OUTHS*	**High side output**; controlled via SPI, in sleep mode controlled by cyclic sense function when selected

6 Functional Block Diagram (P-DSO-36-12 version)

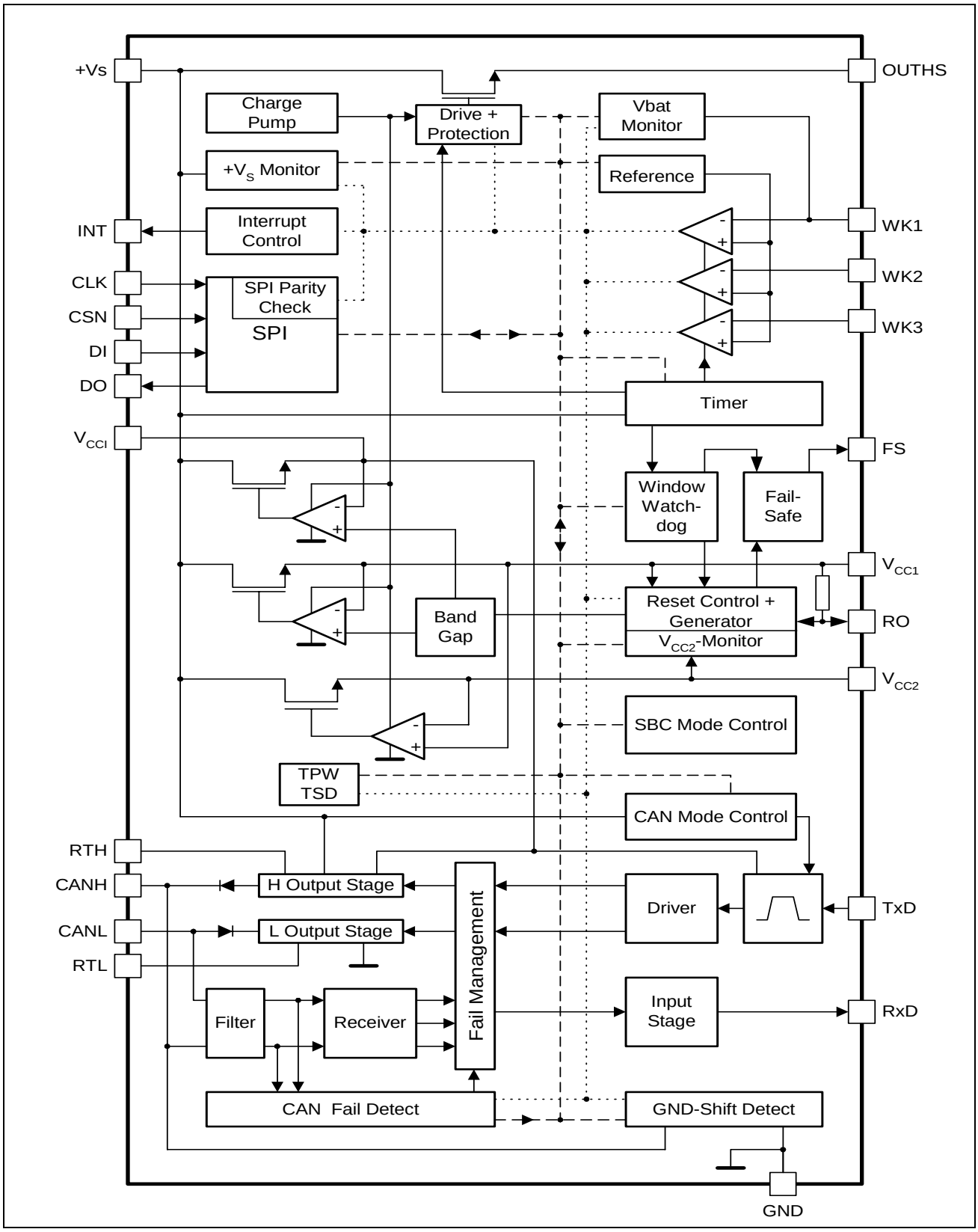


Figure 3

7 Circuit Description

The TLE 6260 which is also called SBC (**S**ystem **B**asis **C**hip) in the following, is a monolithic IC, that incorporates a failure tolerant low speed CAN-transceiver for differential mode data transmission, a triple low dropout voltage regulator for internal and external 5V supply as well as a SPI to control and monitor the IC. Further there are integrated three wake-up monitors, a high side switch, a ground shift detection function, a window watchdog circuit and a reset and fail safe generator.

Figure 3 shows a block schematic diagram of the TLE 6260.

7.1 SBC and CAN Operation Mode

The TLE 6260 offers three different operation modes: SBC-normal mode, SBC-stand-by mode and SBC-sleep mode. Further there is a so called Emergency mode. In SBC-normal mode three additional sub-modes are possible: CAN-normal, CAN-RxD mode, CAN-sleep. These modes are selected via the SPI input bits 4, 5 and 6. Please refer to **table 1**, truth table and **table 8**, SBC modes.

When switching the TLE 6260 from SBC-normal mode in SBC-stand-by mode or SBC-sleep mode the CAN-transceiver is automatically switched to a dynamic mode called RxD-256ms mode. In this mode the transceiver will still transmit messages to the RxD pin and leave the CANL termination at 5V level. If there is no longer any data transmission on the CAN-bus for typ. 256 ms the CAN-transceiver is automatically set to CAN-sleep mode.

Figure 4 shows the mode state diagram of the TLE 6260. It is recommended not to switch directly from SBC-normal to SBC-sleep but to use the SBC-stand-by mode until the CAN-transceiver is set to CAN-sleep. Otherwise a wake-up via the CAN-bus that occurs within typ. 256 ms can not be detected and the TLE 6260 will remain in the SBC-sleep mode.

V_{CC2} can be switched off in the SBC-normal mode whereas it is automatically disabled in the SBC-stand-by and SBC-sleep mode.

When the TLE 6260 is connected to battery voltage the first time (or the $+V_S$ fail condition was met: $+V_S$ fail diagnosis bit 6 = LOW) the TLE 6260 is automatically set to SBC-normal / CAN-sleep. Then it has to be initialised by the microcontroller according to the application specific timing and function requirements. For correct initialisation the SPI input bit 20 (Initialise) has to be set high, otherwise the input bits 21 to 31 are not accepted by the SBC.

Changing of the application specific data is possible at any time in SBC-normal and SBC-stand-by mode. To be sure that the information is not damaged by low input voltage the initialisation has to be repeated after each reset (under-voltage reset, watchdog reset, external reset, power on reset). Also the initialisation has to be refreshed after each wake-up from SBC-sleep mode.

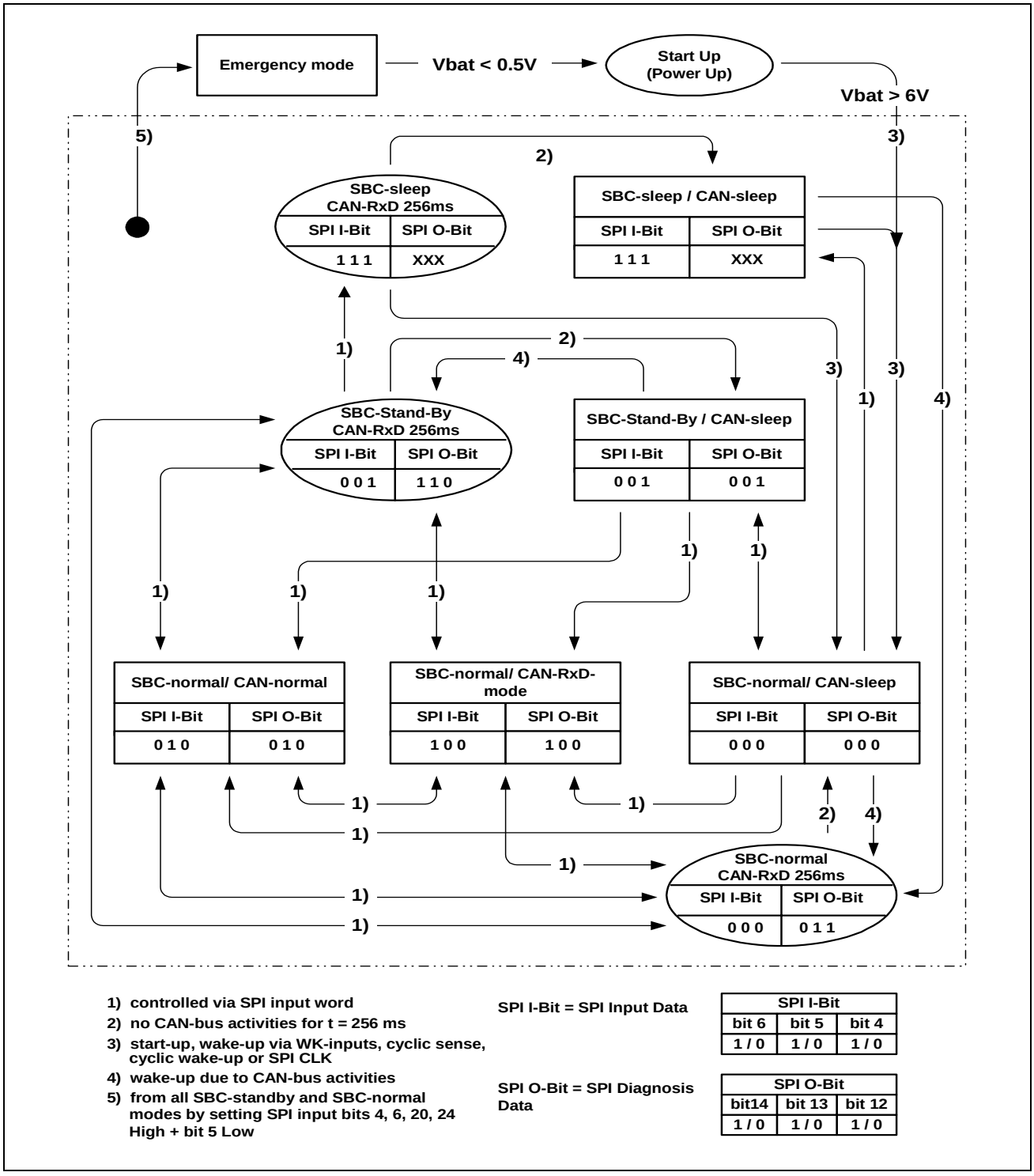


Figure 4: Mode State Diagram

A wake-up due to a message on the CAN bus leads to the SBC-normal / CAN-RxD-256ms mode, where the initialisation has to take place like described before. In this mode the RxD as well as the INT output are set low to signal the wake-up event. Further

the bus termination is automatically set to 5V level immediately. The message can now be received by either changing the mode or releasing the RxD-output by setting bit 12 of the SPI input word high.

The Emergency mode shall only be selected when a fatal error has been recognised that would disturb the whole CAN system. To select this mode, the input bits Initialise (bit 20) and Emergency mode (bit 24) have to be selected in addition to the bits Mode1, Mode2, Mode3 (bit 4 to 6). The Emergency mode can only be left by switching off the power supply.

Table 1 Truth Table for SBC Modes

Feature	SBC-Normal	SBC-Stand-By	SBC-Sleep
V_{CC1}	ON	ON	OFF
Reset Output / Input	ON	ON	OFF
V_{CC2}	OFF / ON	OFF	OFF
CAN-Transceiver / V_{CCI}	normal / RxD 256ms / RxD-mode / sleep	RxD-256ms / sleep	RxD-256ms /sleep
Window Watchdog	ON	ON [1)]	OFF
SPI	ON	ON	OFF
HS-Switch	ON / OFF	ON / OFF	OFF[2)]
Wake-Up Inputs	ON	ON	ON
GND-Shift Monitor	ON [3)]	OFF	OFF
V_{Bat} Monitor	ON[4)]	ON[4)]	OFF
$+V_S$ Monitor	ON	ON	ON
Cyclic Wake-Up	OFF	OFF	ON [5)]
Cyclic Sense	OFF	OFF	ON [5)]
CAN-bus Wake-Up	ON	ON	ON[6)]
SPI Wake-Up	OFF	OFF	ON
Fail Safe Output	ON[7)]	OFF	OFF

[1)] approx. 65 times longer watchdog periode than in SBC-normal mode

[2)] automatically activated when cyclic sense wake-up feature is selected

[3)] only ON when CAN-transceiver is in CAN-normal mode

[4)] only active when selected via SPI by stetting the V_{Bat} Flag

[5)] when both time controlled wake-up features selected, then the cyclic wake-up time is quadrupled

[6)] no bus wake-up capability while RxD-256ms mode is active

[7)] only on when the fail safe requirements are met

7.2 CAN Transceiver

The TLE 6260 is optimised for low speed data transmission up to 125 kbaud in automotive applications. Normally a differential signal is transmitted or received respectively. When a bus wiring failure (see **table7**) is detected the device automatically switches to a dedicated CANH or CANL single-wire mode to maintain the communication if necessary. Therefore it is equipped with one differential receiver and four single ended comparators (two for each bus line). To avoid false triggering by external RF influences the single wire modes are only activated after a certain delay time. As soon as the bus failure disappears the transceiver switches back to differential mode after another time delay. The CAN failures are monitored via SPI diagnosis bits 22 to 31 (see **table 6**). It is possible to distinguish 9 CAN bus failures, the TxD-time-out error as well as thermal shutdown of the CANH / CANL output stage. In addition a bus failure is monitored at pin INT until the next SPI transmission. Bit 6 indicates a common CAN failure. By this a prewarning in parallel to the interrupt at pin INT is possible when the SPI is in 8 bit mode.

The CAN-Failures are stored in the SPI latches until they are reseted by the input bit 12.

To reduce EMI the dynamic slopes of the CANL and CANH signals are both limited and symmetric. This allows the use of an unshielded twisted or parallel pair of wires for the bus. During single-wire transmission (bus-failure) the EMI performance of the system is degraded from the differential mode.

The differential receiver threshold is set to typ. -2.8 V. This ensures correct reception in the normal operation mode as well as in the failure cases 1, 2, 3a and 4 with a noise margin as high as possible. For these failures further failure management is not necessary. Detection of the failure cases 1, 2, 3a and 4 is only possible when the bus is dominant.

When one of the bus failures 3, 5, 6, 6a, and 7 is detected, the defective bus wire is disabled by switching off the affected bus termination and output stage.

Should the TxD input be dominant for a period of typ. 1 ms the TxD time-out feature becomes active and disables the CANH and CANL output driver in order to prevent the bus from being blocked by a permanent TxD signal. A TxD timeout is monitored via the SPI bit 31 and the common CAN-failure bit 6. To check whether the failure condition is still valid, the diagnosis bits have to be frequently reseted via input bit 12. For activation of the output stages when the TxD input becomes recessive again, the SBC has to be set in SBC-normal / CAN-normal via the SPI.

The CAN-transceiver offers three different modes which are controlled via the SPI in SBC-normal mode respectively by the SBC itself in SBC-stand-by and SBC-sleep mode. Further there is the dynamic mode RxD-256ms. Whereas the CAN-normal mode and the CAN-sleep mode correspond to the modes of the stand alone CAN-transceiver TLE6252, the CAN-receive-only mode (RxD-only mode) is similar to the CAN-normal mode but do not allow to transmit any messages to the bus. In SBC-normal mode the

CAN-transceiver mode is selected via the SPI mode control bits 4, 5 and 6. In the SBC-stand-by and SBC-sleep mode the transceiver is automatically set to CAN-RxD-only mode until there is no longer communication on the bus for a period of typ. 256 ms. Then the transceiver is set to CAN-sleep mode.

The transceiver is supplied via $+V_S$ and the internal voltage regulator output V_{CCI}.

In CAN-sleep mode a wake-up via one or both bus lines, CANH or CANL sets the TLE 6260 in SBC-normal mode, CAN-RxD-256ms mode, V_{CC2} OFF. The wake-up is flagged by setting the outputs RxD and INT low. In parallel a CAN-wake-up is monitored via the SPI diagnosis bit 15. The RxD remains low until the CAN-mode is changed or input bit 12 is set high. After or in parallel to the initialisation the CAN-mode has to be changed to SBC-normal / CAN-normal to allow the microcontroller to send a message, or an acknowledgement respectively.

7.3 Low Dropout Voltage Regulator V_{CC1}

The output V_{CC1} is intended for 5V logic supply. It is able to drive external loads up to 100 mA with an output voltage tolerance better than ± 2%.

An external reverse current protection at $+V_S$ is recommended to prevent the output capacitor from being discharged by negative transients or low input voltage.

Stability of the output voltage is guaranteed for output capacitors $C_{Q1} \geq 6$ µF, ESR < 10 Ω. Nevertheless some applications require a much larger output capacitance to buffer the output voltage in case of low input voltage or negative transients.

Bit 0 of the SPI diagnosis word monitors a thermal prewarning of the voltage regulator block. By this the microcontroller is able to reduce the power dissipation of the TLE 6260 by switching off functions of minor priority (e.g. V_{CC2}) before the threshold of the thermal shutdown is reached.

Should a temperature shutdown of V_{CC1} occur, the TLE6260 is automatically set in SBC-sleep mode.

The voltage regulator output V_{CC1} is protected against overload and over-temperature. In case of a V_{CC1} short to GND condition the SBC is automatically switched to SBC-sleep mode after a delay of typ. 128 ms.

7.4 Low Dropout Voltage Regulator V_{CC2}

The V_{CC2} is intended for the internal supply of the CAN power stages and additional external loads (e.g. sensors) up to 150 mA. It's output voltage tracking accuracy is better than $\pm 0.01 * V_{CC1}$.

An external reverse current protection at the supply input Vs is recommended to prevent the output capacitor from being discharged by negative transients or low input voltage.

Stability of the output voltage is guaranteed for output capacitors $C_{Q2} \geq 10$ µF, ESR < 10 Ω. Nevertheless a lot of applications require a much larger output capacitance to buffer the output voltage in case of low input voltage or transients.

The SPI diagnosis bit 0 monitors a thermal prewarning of the voltage regulator block whereas bit 8 flags a thermal shutdown of V_{CC2}. Due to the prewarning function the microcontroller is able to reduce the power dissipation of the TLE 6260 by switching off functions of minor priority (e.g. V_{CC2}) before the threshold of the thermal shutdown is reached. After the thermal shutdown condition disapeares V_{CC2} has to be enabled via the SPI input bit 3.

V_{CC2} can be enabled via the SPI input bit 3 in SBC-normal mode. As soon as V_{CC2} is switched off, the Interrupt output as well as the SPI diagnosis bit 11, V_{CC2} under-voltage are monitoring this. In SBC-stand-by mode, SBC-sleep mode, thermal shut-down condition or any reset condition V_{CC2} is automatically disabled by the SBC itself. When the chip has cooled down after a thermal shutdown condition the SPI input bit 3 has to be set low and then high to activate V_{CC2} again.

The voltage regulator output V_{CC2} is protected against overload and over-temperature as well as shorts to ground or battery voltage.

7.5 Low Dropout Voltage Regulator V_{CCI}

The V_{CCI} is an independent voltage regulator for the internal supply of the CAN-transceiver. It is automatically enabled when its output voltage is higher than typ. 4.5V. Below this threshold it is enabled by the TLE 6260 itself. To stabilise the internal supply an external capacitor $C_{QI} \geq 6$ µF, ESR < 10 Ω is necessary at the pin V_{CCI}. The internal supply is separated from V_{CC2} to ensure save operating of the CAN-transceiver even at a short circuit of V_{CC2} or when the TLE 6260 is set to SBC-stand-by or SBC-sleep mode and the bus has to be terminated to 5V. In addition there is no influence to the V_{CC1} and V_{CC2} output voltage due to load regulation when the CAN-transceiver output stages are in operation.

V_{CCI} is disabled when the CAN transceiver is in CAN-sleep mode. In the CAN RxD-256ms mode V_{CCI} remains activ in order to supply the CAN circuitry.

7.6 Window Watchdog and Reset

When the output voltage V_{CC1} exceeds the reset threshold voltage the reset output RO is switched HIGH after a fixed reset delay time of typ. 2 ms (no delay capacitor at pin RO). A long open window for the initialisation of the TLE 6260 and synchronisation of the watchdog trigger is started. As soon as an under-voltage condition of the output voltage ($V_{CC1} < V_{RT}$) arises, the reset output RO is switched LOW again. This

automatically causes V_{CC2} to be disabled and the CAN-Transceiver to be set to RxD-256ms mode (or sleep mode respectively after typ. 256 ms). The LOW signal of the reset output is guaranteed down to an output voltage $V_{CC1} \geq 1V$. Please refer to **figure 11**, watchdog start-up and reset timing diagram. In order to enhance the reset delay time it is allowed to connect a ceramic capacitor from the RO ouput to ground. Up to the threshold V_{ROCTh} there is only a small pull up current, above that threshold the pull up current is typ. 1mA.

After the above described delayed power on reset (LOW to HIGH transition of RO) the window watchdog circuit is started. Now the microcontroller has to initialise the TLE 6260 (programming of wake-up feature, wake-up timing, watchdog timing, ground-shift threshold) and to service a watchdog trigger signal via the SPI interface (input bit 0) within a fixed long open window of typ. 64 ms.

During the long open window period a change of the SBC mode via the SPI is not accepted.

Within the long open window the watchdog trigger is detected as a “rising edge” of the input bit 0 by sampling a High signal when the CSN becomes HIGH. Default value of bit 0 after each reset is Low. If the trigger signal does not meet the long open window the TLE 6260 is automatically set into SBC-sleep mode.

A correct watchdog service immediately results in starting a closed window followed by an open window. From now on the open window of the watchdog circuit has to be serviced alternating with a Low signal and a High signal. Please refer to **figure 5**, watchdog state diagram and **figure 14**, watchdog timing diagram.

Should a watchdog trigger (in either SBC-normal mode or SBC-stand-by mode) not meet the open window, the reset output RO is set LOW for a fixed period of typ. 2 ms. A watchdog reset automatically results in FS (Fail Safe output) low, OUTHS and V_{CC2} being disabled and the CAN-transceiver being set to CAN-sleep mode or CAN-RxD-256ms mode respectively. In addition, the SPI diagnosis bit 16 is set HIGH to monitor a watchdog reset. Like after any reset condition a long open window is started after the watchdog reset and the TLE 6260 has to be initialised again. A correct watchdog service again results in starting the next closed window and in parallel setting the watchdog reset diagnosis bit 16 LOW. Please refer to **figure 13**, watchdog start-up and reset timing diagram and **figure 14**, watchdog timing. The watchdog timing is selected via the SPI by the input bits 30 and 31 when initialising the SBC (see **table 2**). When changing the SBC mode from normal to stand-by or the other way round, a long open window for synchronisation of the watchdog trigger is started. In SBC-sleep mode the watchdog feature is automatically disabled.

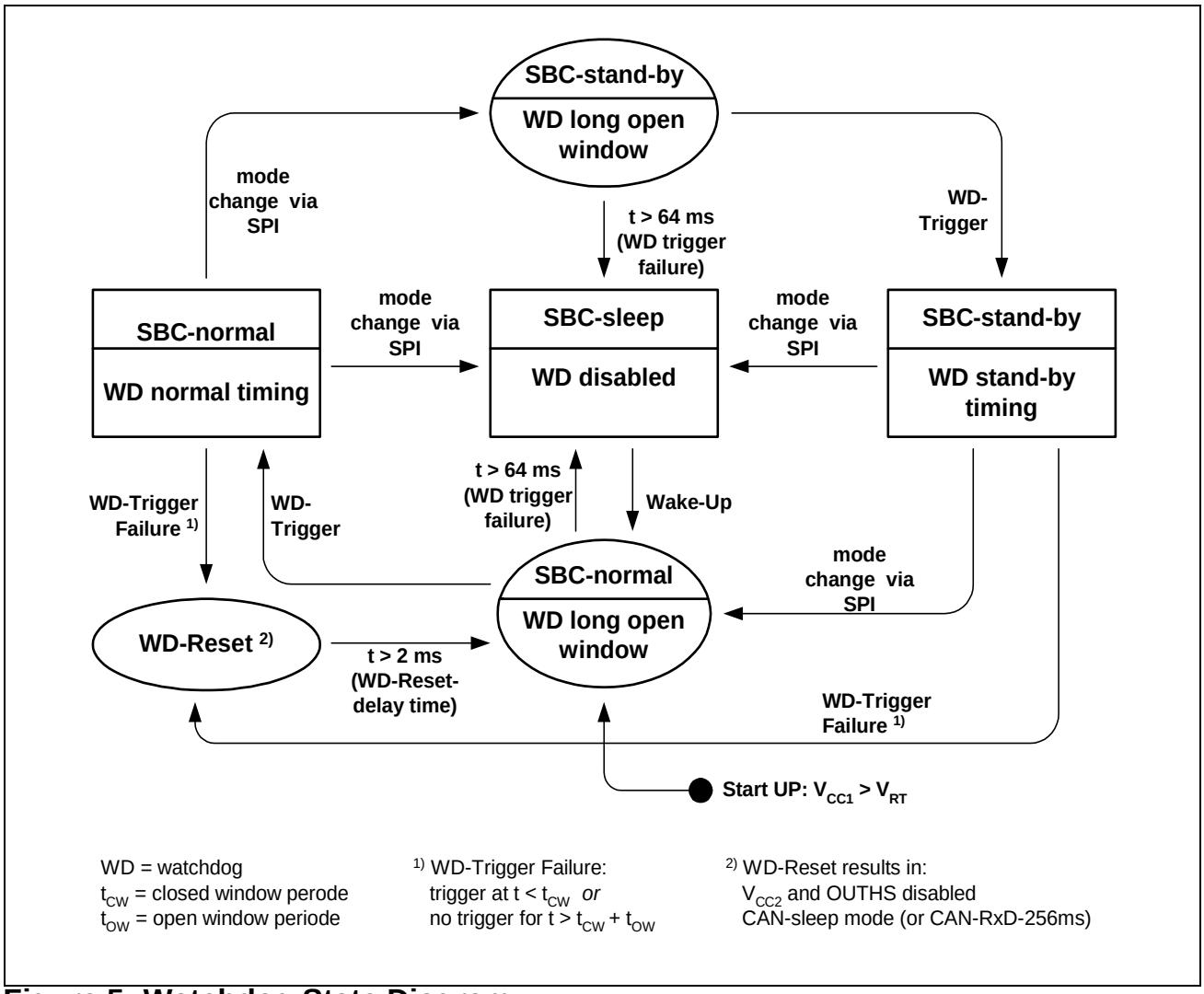


Figure 5: Watchdog State Diagram

Table 2, Watchdog Timing

typ. trigger time t_{WT} SBC-normal	typ. closed window time t_{CW} SBC-normal	typ. trigger time t_{WT} SBC-stand-by	typ. closed window time t_{CW} SBC-stand-by	Input bit 31	Input bit 30
5.3 ms	4 ms	340.5 ms	256 ms	0	0
10.6 ms	8 ms	681.0 ms	512 ms	0	1
20.8 ms	16 ms	1361.9 ms	1024 ms	1	0
42.6 ms	32 ms	2723.8 ms	2048 ms	1	1

7.7 External Reset

The reset output RO can also be used as reset input pin to set the SBC in its default conditions and to restart it. Therefore the voltage at RO has to be set below the threshold V_{RTI}. When the external reset condition is removed the SBC is set to SBC-normal / CAN sleep or CAN-RxD-256ms respectively and expects to initialised during the long open window. The external reset condition is flagged by the SPI diagnosis bit 19 after the start up.

7.8 Fail Safe

The Fail Safe output is high as soon as the watchdog is correctly triggered for the fourth time. Therefore the IC has to be in SBC-normal mode. FS is set low immediately as soon as any reset condition arises or the mode is changed from SBC-normal to either SBC-stand-by or SBC-sleep.

7.9 High Side Switch

The high side output OUTHS is able to switch loads up to 100 mA. Its on-resistance is typ. 2 Ω @ 25°C. This switch is controlled either via the wake-up timing function in SBC-sleep mode (cyclic sense feature selected) or the SPI input bit 2 in SBC-stand-by and SBC-normal mode. The time base of the wake-up timing is programmed via SPI (see **table 3**).

OUTHS is protected against short circuit and overload. This failure is monitored via the interrupt output INT and by the SPI diagnosis bit 9. The interrupt output can be masked for this failure. When the SBC is in sleep mode a short or overload condition at OUTHS causes a wake-up. To enable the high side switch after the overload condition disappeared it has to be disabled via the SPI input bit 2 before it can be switched on again.

As soon as the under-voltage condition of the supply voltage is met ($V_S < V_{UVOFF}$), the switch is automatically disabled by the under-voltage lockout circuitry. Above the V_{UVON} threshold the HS-switch is enabled again. Moreover OUTHS is disabled when a V_{CC1} reset or watchdog reset occurs.

7.10 Wake-Up Mode and V_{BAT}-Monitor

Further to a wake-up via one or both the CAN-bus lines three additional wake-up modes are available. The wake-up mode is selected via the SPI input bits 21 and 22 when initialising the SBC (see **table 5**).

When no wake-up mode is selected (bit 21 = low and bit 22 = low) a change of the voltage level at WK1, WK2 WK3 creates a wake-up from SBC sleep mode. The TLE 6260 is set to SBC normal, CAN sleep.

In cyclic wake-up mode (bit 22 = HIGH) the TLE 6260 is automatically set into SBC-normal mode, CAN-sleep, after a predefined delay time (**figure 4**). The wake-up timing is programmed via the SPI (see **table 3**) when initialising the TLE 6260. In this mode the WK inputs are aktive, too.

In cyclic sense mode (bit 21= HIGH) the high side output OUTHS is periodically activated. As soon as a wake-up request (positive or negative edge of an external contact) is detected for two activation cycles at the wake-up inputs WK1 / WK2 / WK3, the ASIC is set in SBC-normal mode, CAN-sleep, (see **figure 4 and 11**). Application hint: When the cyclic sense feature is used (like shown in **figure 17** for WK2 and WK3) and the high side switch is activated in either SBC-normal mode or SBC stand-by mode a positive edge is created at the wake-up inputs that results in monitoring a “faulty” wake-up request via the SPI diagnosis word and the interrupt output.

It is also possible to select the cyclic sense mode and the cyclic wake-up mode simultaneously. Then the timing for the cyclic wake-up is automatically multiplied by 4.

The wake-up diagnosis bits always show the logic level that has caused a wake-up. In SBC stand-by or SBC-normal mode the WK inputs can be used as digital port expanders. When the CSN becomes high after each SPI transmission the diagnosis bits are set again according to the current voltage level at the inputs WK1 to WK3.

In SBC sleep mode also the SPI input CLK can be used to wake-up the SBC. Therefore a positive edge has to be created at this input.

Each wake-up is monitored via the SPI diagnosis bits 3, 4, 5, 15 and 20 (see **table 6 and 9**) as well as at the interrupt outputs RxD and INT (not SPI wake-up).

The wake-up timing is programmed via the SPI (see **table 3**) when initialising the TLE6260.

Table 3, Wake-Up timing

typ. wake-up periode	Control bit 29	Control bit 28	Control bit 27
64 ms	0	0	0
128 ms	0	0	1
256 ms	0	1	0
512 ms	0	1	1
1024 ms	1	0	0
2048 ms	1	0	1
4096 ms	1	1	0
8192 ms	1	1	1

In case not all wake-up inputs are necessary in the application, the pin WK1 can be used as a battery voltage monitor. As soon as the battery voltage drops below the V_{BAT}-threshold for longer than 20 µs an internal flip-flop is set LOW. Both, the SPI diagnosis bit 1 and the interrupt output INT are monitoring this. In normal operation the flip-flop has to be activated via the SPI control bit 9 by setting it HIGH. This function can be used as an early warning to store data before a V_{CC1} reset occurs.

The wake-up inputs WK1, WK2, WK3 are active also in SBC stand-by and SBC normal mode. If they are not used in combination with the cyclic sense feature each positive or negative edge results in setting the interrupt output LOW as well as monitoring the wake-up source via the SPI diagnosis bits.

7.11 Ground Shift Monitor

In CAN-normal mode this circuit compares the local ground (pin GND) to the recessive state of the CANH line that represents an overall ground level. The ground shift detection threshold has to be programmed via the SPI (see **table 4**) when initialising the TLE6260. As soon as a GND-shift is sampled for two times (see **fig.15**) the interrupt output INT is set low and the SPI diagnosis bit 10 is set. To start the GND-shift detection circuit again, it has to be reseted by the input bit 8.

Table 4, GND-Shift detection threshold

Detection Threshold $V_{GND,th} = V_{CANH,rec.} - V_{GND}$	**Control bit 26**	**Control bit 25**
-2.0 V	0	0
-1.5 V	0	1
-1.0 V	1	0
-0.5 V	1	1

7.12 Interrupt Output INT and Diagnosis

The following failures and events are monitored by a LOW signal at the pin INT. Most of the failures/events can be masked via the SPI input bits 13 to 19 so that unused features do not disturbe the system. Also each failure/event is monitored at INT only until the next SPI transmission (first negative edge at CLK with CSN = low). Then INT becomes high again to monitor new/additional failures/events.

Monitored failures / events:
thermal shutdown V_{CC2}, thermal prewarning V_{CC}, ground shift, short circuit HS-switch, CAN-bus failure, V_{CC2}-undervoltage, wake-up at Wake-Up inputs WK1, WK2, WK3, $+V_S$-Fail, V_{BAT}-Fail and SPI transmission failure.

7.13 SPI (Serial peripheral interface)

The 32-bit wide control word or input word (see **table 5**) is read in via the data input DI, and this is synchronised with the clock input CLK supplied by the µC. The diagnosis word appears synchronously at the data output DO (see **table 6**).

The transmission cycle begins when the chip is selected by the chip select not input CSN (H to L). After the CSN input returns from L to H, the word that has been read in becomes the new control word. The DO output switches to tristate status at this point, thereby releasing the DO bus circuit for other uses.

For details of the SPI timing please refer to **figure 6 to 10**.

For each SPI transmission a parity bit (bit 7) has to be calculated. When the parity bit is correct or rather the SPI transmission is faultless the new control word (input word) is accepted by the SBC. The parity bit has to be set in a way that the number of “1” in the control word is odd. By this one bit error can be detected (hamming distance 2). A transmission failure is monitored by setting the diagnosis bit 7 high. The new control word is not accepted then and the failure is monitored at the INT-output as well as via the SPI diagnosis word (bit 7) of the next SPI transmission.

To reduce the load of the microcontroller the SPI can be switched from 32 bit mode to 8 bit mode by setting bit 1 of the input word high. To get the full diagnosis report or to reset diagnosis bits the input bit 1 has to be set low again. After each reset condition the SPI is automatically switched back to 32 bit to to allow full diagnosis and the required new initialisation. In principal the functionality and behaviour for 8 bit mode is the same as in 32 bit mode. The parity bit in 8 bit mode has to be calculated for the 8 bit SPI input word. The default condition is 32 bit mode.

Table 5

Input Data Protocol

BIT	
31	Watchdog Timing
30	Watchdog Timing
29	Wake-Up Timing
28	Wake-Up Timing
27	Wake-Up Timing
26	GND-Threshold
25	GND-Threshold
24	Emergency Mode
23	not used
22	Cycle Wake-Up
21	Cyclic Sense
20	Initialise
19	Mask WK1/3
18	Mask Thermal Prewarning
17	Mask Ground-Shift
16	Mask CAN-Failure
15	Mask V_{CC2} Undervoltage
14	Mask Thermal Shutdown V_{CC2}
13	Mask Short Circuit OUTHS
12	Reset bits: CAN Failure + Wake-Up CAN + Common CAN-Bus Failure
11	not used
10	$+V_S$ Flag Set
9	V_{BAT} Flag Set
8	GND-Shift-Detection Reset
7	**Parity Bit**
6	**Mode Control 3**
5	**Mode Control 2**
4	**Mode Control 1**
3	**V_{CC2} Enable**
2	**OUTHS Enable**
1	**32 <--> 8 bit SPI (H = 8 bit mode)**
0	**Watchdog Trigger**

H = ON
L = OFF

Table 6

Diagnosis Data Protocol

BIT	
31	Failure 8 (TxD Timeout)
30	CAN Failure 7 (CANL short CANH)
29	CAN Failure 6a (CANH short V_{CC})
28	CAN Failure 6 (CANH short V_{BAT})
27	CAN Failure 5 (CANL short GND)
26	CAN Failure 4 (CANH short GND)
25	CAN Failure 3a (CANL short V_{CC})
24	CAN Failure 3 (CANL short V_{BAT})
23	CAN Failure 2 (CANH open)
22	CAN Failure 1 (CANL open)
21	Thermal Shutdown CAN
20	Wake-Up SPI
19	External Reset
18	V_{CC1} low voltage
17	Thermal Shutdown V_{CC1}
16	Watchdog Reset
15	Wake-Up CAN
14	Mode Status 3
13	Mode Status 2
12	Mode Status 1
11	V_{CC2} Undervoltage
10	Ground-Shift
9	Short Circuit OUTHS
8	Termal Shutdown V_{CC2}
7	**SPI Transmission Error**
6	**Common CAN-Bus Failure**
5	**WK 3 level**
4	**WK 2 level**
3	**WK 1 level**
2	**$+V_S$ Fail Not**
1	**V_{BAT} Fail Not**
0	**Temperature Prewarning V_{CC}**

H = ON
L = OFF

Table 7, CAN bus line failure cases (according to ISO 11519-2)

failure #	failure description
1	CANL line interrupted
2	CANH line interrupted
3	CANL shorted to V_{BAT}, CANL > 7.2 V
3a (no ISO failure)	CANL shorted to V_{CC}; 2.2 V < CANL < 7.2 V
4	CANH shorted to GND
5	CANL shorted to GND
6	CANH shorted to V_{BAT}; CANH > 7.2 V
6a (no ISO failure)	CANH shorted to V_{CC}; 2.2 V < CANH < 7.2 V
7	CANL shorted to CANH
8 (no ISO failure)	TxD permanent LOW time out

Table 8, SBC mode input bits at pin DI

SBC Mode	CAN Mode	V_{CC2} (controled via bit 3)	DI bit 6	DI bit 5	DI bit 4
SBC-normal	CAN-sleep (RxD-256ms)	OFF (ON)	0	0	0
SBC-normal	CAN-RxD-mode	OFF (ON)	1	0	0
SBC-normal	CAN-normal	OFF (ON)	0	1	0
SBC-stand-by	CAN-sleep (RxD-256ms)	OFF	0	0	1
SBC-sleep	CAN-sleep (RxD-256ms)	OFF	1	1	1
Emergency	all functions off		1	0	1

Table 9, SBC and CAN mode diagnosis bits at pin DO

SBC Mode	CAN Mode	DO bit 14	DO bit 13	DO bit 12
SBC-normal	CAN-sleep	0	0	0
SBC-normal	CAN-RxD-only	1	0	0
SBC-normal	CAN-RxD-256ms	0	1	1
SBC-normal	CAN-normal	0	1	0
SBC-stand-by	CAN-RxD-256ms	1	1	0
SBC-stand-by	CAN-sleep	0	0	1

8 Electrical Characteristics

8.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage	V_S	– 0.3	28	V	–
Supply voltage	V_S	– 0.3	40	V	t_p< 0.5s; t_p/T < 0.1
Regulator output voltage	V_{CC1}	– 0.3	6.0	V	
Regulator output voltage	V_{CC2}	– 1.0	28	V	
Regulator output voltage	V_{CC2}	– 1.0	40	V	t_p< 0.5s; t_p/T < 0.1
CAN input voltage (CANH, CANL)	$V_{CANH/L}$	– 10	28	V	
CAN input voltage (CANH, CANL)	$V_{CANH/L}$	– 40	40	V	V_S >0 V t_p< 0.5s; t_p/T < 0.1
Logic input voltages (DI, CLK, CSN, TxD)	V_I	– 0.3	V_{CC1} +0.3	V	0 V < V_S < 24 V 0 V < V_{CC1} < 5.5 V
Logic output voltage (DO, INT, RO, RxD)	$V_{DO/RO/RD}$	– 0.3	V_{CC1} +0.3	V	0 V < V_S < 24 V 0 V < V_{CC1} < 5.5 V
Termination input voltage (RTH, RTL)	$V_{TL/TH}$	– 0.3	V_S +0.3	V	0 V < V_S < 24 V 0 V < V_{CC1} < 5.5 V
Input voltage at Wake Input WK1	V_{WK1}	– 0.3	V_S +1	V	0 V < V_S < 24 V 0 V < V_{CC1} < 5.5 V
Input voltage at Wake Input WK1	V_{WK1}	– 40	0	V	0 V < V_S
Input voltage at Wake Input WK1	V_{WK1}	– 40	40	V	V_S >0 V t_p< 0.5s; t_p/T < 0.1
Input voltage at Wake Inputs WK2, WK3	$V_{WK2/3}$	– 0.3	V_S +1	V	0 V < V_S < 24 V 0 V < V_{CC1} < 5.5 V
Input voltage at Wake Inputs WK2, WK3	$V_{WK2/3}$	– 40	40	V	V_S >0 V t_p< 0.5s; t_p/T < 0.1
Internal regulator output	V_{CCI}	– 0.3	6.0	V	

8.1 Absolute Maximum Ratings (cont'd)

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Currents					
Output current; Vcc	I_{CC}	–	–	A	internally limited
Output current; OUTHS	I_{OUTHS}	*	0.3	A	* internally limited
Temperatures					
Junction temperature	T_j	– 40	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

8.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	5.7	28	V	
Logic input voltage (DI, CLK, CSN, TxD)	V_I	– 0.3	V_{CC1}	V	–
Output capacitor C_{V1}	C_1	6		µF	
Output capacitor C_{V2}	C_2	10		µF	
Output capacitor C_{VI}	C_I	6		µF	
C_1-Series Resistor	R_{ESR1}		10	Ω	f = 10kHz
C_2-Series Resistor	R_{ESR2}		10	Ω	f = 10kHz
C_I-Series Resistor	R_{ESRI}		10	Ω	f = 10kHz
SPI clock frequency	f_{CLK}	–	1	MHz	–
Junction temperature	T_j	– 40	150	°C	–

Thermal Resistances

Junction pin P-DSO-28-6	$R_{thj\text{-}pin}$	–	25	K/W	measured to pin 7
Junction ambient P-DSO-28-6	$R_{thj\text{-}a}$	–	65	K/W	–
Junction case P-DSO-36-10	$R_{thj\text{-}case}$	–	4	K/W	
Junction ambient P-DSO-36-10	$R_{thj\text{-}a}$	–	65	K/W	–

8.3 Electrical Characteristics

V_S = 13.5 V; SBC-normal-mode; – 40 °C < T_j < 140 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Quiescent current Pin $+V_S$						
Current consumption $I_q = I_S - I_{V1/2}$	I_q	–	5	10	mA	TxD recessive
Current consumption $I_q = I_S - I_{V1/2}$	I_q	–	8	15	mA	TxD dominant
Current consumption $I_q = I_S - I_{V1}$	I_q	–	500	800	µA	SBC-stand-by mode
Quiescent current $I_q = I_S$	I_q	–	80	100	µA	SBC-sleep mode; T_j<85°C
Quiescent current $I_q = I_S$	I_q	–		t.b.d	µA	SBC-sleep mode, cycle sense or cycle wake-up; T_j<85°C
Quiescent current $I_q = I_S - I_{OUTHS}$	I_q	–	2		mA	HS-switch + wake-up inputs active; SBC-sleep mode, (cycle sense); T_j<85°C
Thermal Prewarning and Shutdown (junction temperatures)						
Thermal prewarning ON temperature	T_{jPW}	140	155	170	°C	bit 0 of SPI diagnosis word
Thermal prewarning hyst.	ΔT	–	10	–	K	–
Thermal shutdown temp.	T_{jSD}	160	175	190	°C	–
Thermal shutdown hyst.	ΔT	–	30	–	K	–
Ratio of SD to PW temp.	T_{jSD} / T_{jPW}		1.13	–	–	–

8.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; SBC-normal-mode; – 40 °C < T_j < 140 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Voltage Regulator Output V_{CC1}						
Output voltage	V_{CC1}	4.9	5.0	5.1	V	6 V < V_S < 28 V; 0.1mA< I_{CC1}<100mA
Output voltage	V_{CC1}	4.8	5.0	5.2	V	6 V < V_S < 28 V; I_{CC1}< 0.1mA
Output voltage	V_{CC1}	4.8	5.0	5.2	V	6 V < V_S < 28 V; SBC-stand-by mode
Line regulation	ΔV_{CC1}	-20	5	20	mV	6 V < V_S < 16 V; I_{CC} = 1mA
Load regulation	ΔV_{CC1}	-20	-10	20	mV	1mA< I_{CC}<100mA;
Power supply ripple rejection	$PSRR$		40		dB	V_S < 1 Vss; C_Q ≥ 6µF 100Hz< f <100kHz
Output current limt	I_{CC1max}		-120	-100	mA	note 1); V_S = 6.5V
Output current limt	I_{CC1max}	-200	-150		mA	V_{CC1} = 0V; V_S = 6.5V
Dropvoltage $V_{DR} = V_S - V_{CC1}$	V_{DR}		0.10	0.30	V	I_{CC1} = 20 mA; note 1)
Dropvoltage $V_{DR} = V_S - V_{CC1}$	V_{DR}		0.30	0.50	V	I_{CC1} =100 mA; note 1)
Output capacitance	C_{V1}	6			µF	
ESR of output capacitance	R_{ESRV1}			10	Ω	at 10 kHz
Voltage Regulator Output V_{CC2}						
Output voltage tracking accuracy $\Delta V_{CC2} = V_{CC1} - V_{CC2}$	ΔV_{CC2}	-50		50	mV	6 V < V_S < 28 V; 1 mA < I_{CC2} < 100 mA
Output voltage tracking accuracy	ΔV_{CC2}	-100		100	mV	6 V < V_S < 28 V; 1 µA< I_{CC2}< 50µA
Line regulation	ΔV_{CC2}	-20	-5	20	mV	6 V < V_S < 16 V; I_{CC2} = 1mA
Load regulation	ΔV_{CC2}	-20	-10	20	mV	1mA < I_{CC2} < 100mA;

8.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; SBC-normal-mode; – 40 °C < T_j < 140 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Power supply ripple rejection	$PSRR$		40		dB	V_S < 1 Vss; $C_Q \geq 10\mu F$ 100Hz< f <100kHz
Output current limt	I_{CC2max}		-170	-150	mA	note 1); V_S = 6.5V
Output current limt	I_{CC2max}		-100		mA	V_{CC2} = 0V; V_S = 6.5V
Dropvoltage $V_{DR} = V_S - V_{CC2}$	V_{DR}		0.3	0.7	V	I_{CC2} = 100 mA; note 1)
Output capacitance	C_{V2}	10			µF	
ESR of output capacitance	R_{ESRV2}			10	Ω	at 10 kHz

Internal Voltage Regulator V_{CCI}

Output voltage	V_{CCI}	4.8	5.0	5.2	V	6 V < V_S < 28 V; 0.1mA< I_{CCI}<100mA
Line regulation	ΔV_{CCI}	-40	-20	40	mV	6 V < V_S < 16 V; I_{CCI} = 1mA
Load regulation	ΔV_{CCI}	-40	-10	40	mV	1mA < I_{CCI} < 50mA;
Power supply ripple rejection	$PSRR$	tbd	40		dB	V_S < 1 Vss; $C_Q \geq 10\mu F$ 100Hz< f <100kHz
Dropvoltage $V_{DR} = V_S - V_{CCI}$	V_{DR}		0.5	0.7	V	I_{CCI} = 50mA; note 1)

note 1) measured when the output voltage V_{CC} has dropped 100 mV from the nominal value obtained at 13.5 V input voltage V_S

8.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; SBC-normal-mode; – 40 °C < T_j < 140 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
V_{CC1} Reset Generator; Pin RO						
Reset threshold voltage	V_{RT}	4.0	4.2	4.4	V	V_{CC1} decreasing
Reset threshold hysteresis	ΔV_{RT}	200	400	500	mV	
Reset low output voltage	V_{RO}		0.2	0.4	V	I_{RO} = 2mA ($V_{CC1} \geq V_{RT}$) or $V_{CC1} \geq$ 1V: I_{RO} = 200 µA; V_S = 0V
Reset high output voltage	V_{RO}	4.0	4.9	V_{CC1}+ 0.1	V	
External Reset threshold voltage	$V_{RTh,ext}$	0.3* V_{CC1}	2.5	0.7* V_{CC1}	V	V_{RO} decreasing
Reset pull up current	I_{RO}	tbd	-50	tbd	µA	$V_{RO} < V_{ROCTh}$
Reset pull up current	I_{RO}		-1	tbd	mA	$V_{RO} > V_{ROCTh}$
Pull up current switching threshold voltage	V_{ROCTh}		1		V	V_{RO} increasing
Reset reaction time	t_{RR}	1	5	10	µs	$V_{CC1} < V_{RT}$ to RO = L; no C_{RO}
Reset delay time	t_{RD}	1.5		3.5	ms	V_{CC1} = 5V; no C_{RO}
Fail Safe Output; Pin FS						
Fail Safe low output voltage	V_{FS}		0.2	0.4	V	I_{FS} = 2mA ($V_{CC1} \geq V_{RT}$) *or* $V_{CC1} \geq$ 1V: I_{FS}= 200 µA; V_S = 0V
Fail Safe high output voltage	V_{FS}	4.0	4.9	V_{CC1}+ 0.1	V	
Fail Safe pull up current	I_{FS}		-200		µA	V_{FS} = 0V
Watch dog count difference for setting FS High	n_{FS}		4			SBC-normal mode
Fail Safe reaction time	t_{FSR}	1	5	10	µs	$V_{CC1}<V_{RT}$ *or* $V_{RO}<V_{RIT}$ *or* WD-trigger failure to FS = L

8.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; SBC-normal-mode; – 40 °C < T_j < 140 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
V_{CC2} Undervoltage Supervisor; (bit 5 of SPI diagnosis word)						
Tracking error $\Delta V_{CC2} = V_{CC1} - V_{CC2}$	ΔV_{ST}	200	350	500	mV	
Tracking error hysteresis	ΔV_{RT}	80	130	200	mV	
Reaction time	t_{SR}	1	5	10	µs	$V_{CC1} - V_{CC2} > \Delta V_{ST}$ to INT = low
V_{CCI} Undervoltage Supervisor						
Switch ON voltage	$V_{I,on}$	4.35	4.55	4.75	V	
Switch ON/Off hysteresis	$\Delta V_{I,hys}$	1	100		mV	$\Delta V_{I,hys} = V_{I,on} - V_{I,off}$
Interrupt Output; Pin INT						
Interrupt low output voltage	V_{INT}		0.2	0.4	V	I_{INT} = 2mA; V_{CC1} = 5V
Interrupt high output voltage	V_{INT}	4.0	4.8	V_{CC1}+ 0.1	V	
Interrupt pull up current	I_{INT}	-400	-200	-100	µA	V_{INTO} = 0V
+V_S Monitor; (bit 6 of SPI diagnosis word)						
+V_S fail threshold voltage	V_{SFT}	3.5	4.2	5.0	V	
+V_S fail reaction time	t_{SFR}	5	25	50	µs	$+V_S < V_{SFT}$ to bit = L
V_{BAT} Fail Monitor; (bit 4 of SPI diagnosis word)						
V_{bat} fail threshold voltage	V_{BFT}	2.7	3.5	4.3	V	
V_{bat} fail reaction time	t_{BFR}	5	25	50	µs	$V_{bat} < V_{BFT}$ to INT = low

8.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; SBC-normal-mode; – 40 °C < T_j < 140 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Watchdog Generator						
Closed window time	t_{CW}	-15		15	%	timing see table 2
Open window time t_{OW} = t_{CW}	t_{OW}	-15		15	%	timing see table 2
Watchdog reset low time	t_{WR}	1.5	2.5	3.5	ms	
Long open window	t_{LW}		64		ms	
GND-Shift Detection						
Detection threshold accuracy $\Delta V_{GND,th} = V_{CANH,rec} - V_{GND}$	$\Delta V_{GND,th}$	-20		20	%	$V_{GND,th}$ adjustable (see table 4)
Sample periodes to set INT	n_{GND}		2			
Wake-Up Inputs WK1, WK2, WK3						
Wake-up threshold	V_{WAKE}	2.7	3.5	4.3	V	
Sample periodes to set INT	n_{WAKE}		1			
Sample periodes to set INT	n_{WAKE}		2			cyclic sense selected
Auto timing periode accuracy	Δt_{WAKE}	-50%		50%		t_{WAKE} adjustable; (see table 3); cyclic sense mode
Sense time	$t_{WK,ON}$	188	375	562	µs	in cyclic sense mode
Sample point	SP		83%			refering to $t_{WK,ON}$
Interrupt reaction time	t_{WK-INT}			80	ms	Wake-Up = TRUE to INT = LOW; C_{V1} = 10µF
Detection delay time	t_{dWK}	8	20	35	µs	

8.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; SBC-normal-mode; – 40 °C < T_j < 140 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
High Side Output OUTHS; (controlled by cyclic sense feature or bit 2 of SPI input word)						
Static Drain-Source ON-Resistance; I_{OUTHS} = – 0.1 A	$R_{DSON\ HS}$	–	0.8	1.5	Ω	9 V ≤ V_S ≤ 28 V T_j = 25 °C
				2.0	Ω	9 V ≤ V_S ≤ 28 V
			1.0	3.0	Ω	5.2 V ≤ V_S ≤ 9 V T_j = 25 °C
				4.0	Ω	5.2 V ≤ V_S ≤ 9 V
Active zener voltage	V_{OUTHS}	-4.0	-2.5	-1.0	V	I_{OUTHS} = – 0.1 A
Clamp diode forward voltage	V_{OUTHS}		0.7	1.0	V	I_{OUTHS} = 0.1 A
Leakage current	I_{QLHS}	-50			µA	V_{OUTHS} = 0 V
Reverse current	I_{QRHS}		0	3	µA	OUTHS low
Switch ON delay time	t_{dONHS}		2	20	µs	CSN high to OUTHS high, R_L = 100Ω
Switch OFF delay time	t_{dOFFHS}		10	50	µs	CSN low to OUTHS low, R_L = 100Ω
Overcurrent shutdown threshold	I_{SDHS}	-200	-400	-800	mA	
Shutdown delay time	t_{dSDHS}	10	25	40	µs	
UV-Switch-ON voltage	$V_{UV\ ON}$	–	5.35	6.00	V	V_S increasing
UV-Switch-OFF voltage	$V_{UV\ OFF}$	4.50	4.85	5.20	V	V_S decreasing
UV-ON/OFF-Hysteresis	$V_{UV\ HY}$	–	0.5	–	V	$V_{UV\ ON} - V_{UV\ OFF}$
HS on time	t_{HSON}	0.1	0.5	0.8	ms	in cyclic sense mode
Receiver Output R×D						
HIGH level output voltage	$V_{RD,H}$	V_{CCI} - 0.9	4.8	V_{CCI}	V	I_{RD} = -250 mA
LOW level output voltage	$V_{RD,L}$		0.4	0.9	V	I_{xD} = -1.25 mA

8.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; SBC-normal-mode; – 40 °C < T_j < 140 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Transmission Input T×D						
HIGH level input voltage threshold	$V_{TD,H}$	2.0	2.6	3.0	V	V_{TD} rising
LOW level input voltage threshold	$V_{TD,L}$	1.8	2.4	3.0	V	V_{TD} falling
HIGH level input current	I_{TD}	-200	-50	-25	µA	V_{TD} = 4 V
LOW level input current	I_{TD}	-800	-200	-100	µA	V_{TD} = 1 V
TxD threshold hysteresis	V_{TDhys}		0.2		V	$V_{TD,H}$ - $V_{TD,L}$
Bus Lines CANL, CANH						
Differential receiver recessive-to-dominant threshold voltage	$V_{dRD(rd)}$	-2.8	-2.5	-2.2	V	
Differential receiver dominant-to-recessive threshold voltage	$V_{dRD(dr)}$	-3.2	-2.9	-2.6	V	
CANH recessive output voltage	V_{CANHr}	0.1	0.2	0.3	V	TxD = V_{CC}; R_{RTH} < 4 kΩ
CANL recessive output voltage	V_{CANLr}	V_{CCI} -0.2	–	V_{CCI}	V	TxD = V_{CC}; R_{RTL} < 4 kΩ
CANH dominant output voltage	V_{CANHd}	V_{CCI} -1.4	V_{CCI} -1.0	V_{CCI}	V	TxD = 0 V; normal mode; I_{CANH} = – 40 mA
CANL dominant output voltage	V_{CANLd}	–	1.0	1.4	V	TxD = 0 V; normal mode; I_{CANL} = 40 mA
CANH output current	I_{CANH}	-110	-70	-50	mA	V_{CANH} = 0 V; TxD = 0 V
		–	0	–	µA	sleep operation mode; V_{CANH} = 12 V

8.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; SBC-normal-mode; – 40 °C < T_j < 140 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
CANL output current	I_{CANL}	50	70	110	mA	V_{CANL} = 5 V; TxD = 0 V
		–	0	–	µA	sleep operation mode; V_{CANL} = 0 V
Voltage detection threshold for short-circuit to battery voltage on CANH and CANL	$V_{det(th)}$	6.5	7.3	8.0	V	normal operation mode
Voltage detection threshold for short-circuit to battery voltage on CANH	$V_{det(th)}$	V_{BAT} -2.5	V_{BAT} -2.0	V_{BAT} -1.0	V	sleep operation mode
CANH wake-up voltage threshold	V_{WAKEH}	1.2	2.0	2.7	V	–
CANL wake-up voltage threshold	V_{WAKEL}	2.4	3.1	3.8	V	–
Wake-up voltage threshold difference	ΔV_{WAKE}	0.2	–	–	V	DV_{WAKE} = V_{WAKEL} – V_{WAKEH}
CANH single-ended receiver threshold, dom. to rec. edge	V_{CANH}	1.1	1.7	2.0	V	failure cases 3, 5 and 7
CANH single-ended receiver threshold, rec. to dom. edge	V_{CANH}	1.5	2.1	2.5	V	failure cases 3, 5 and 7
CANL single-ended receiver threshold, dom. to rec. edge	V_{CANL}	2.8	3.3	3.8	V	failure case 6 and 6a
CANL single-ended receiver threshold, rec. to dom. edge	V_{CANL}	2.4	2.9	3.4	V	failure case 6 and 6a
CANL leakage current	I_{CANLl}	-5	0	5	µA	V_{CC} = 0 V, V_S = 0 V, V_{CANL} = 13.5 V, T_j < 85 °C
CANH leakage current	I_{CANHl}	-5	0	5	µA	V_{CC} = 0 V, V_S = 0 V, V_{CANH} = 5 V, T_j < 85 °C

8.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; SBC-normal-mode; – 40 °C < T_j < 140 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Termination Outputs RTL, RTH						
RTL to V_{CC} switch-on resistance	R_{RTL}	–	43	95	Ω	I_o = -10 mA; normal operating mode
RTL to BAT switch series resistance	R_{oRTL}	5	16	35	kΩ	sleep operation mode
RTH to ground switch-on resistance	R_{RTH}	–	43	95	Ω	I_o = 10 mA; normal operating mode
RTH output voltage	V_{oRTH}	–	0.7	1.0	V	I_o = 1 mA; sleep operating mode
RTH pull-down current	I_{RTHpd}	40	75	100	µA	normal operating mode, failure cases 6 and 6a
RTL pull-up current	I_{RTLpu}	-100	-75	-40	µA	normal operating mode, failure cases 3, 3a, 5 and 7
RTH leakage current	I_{RTHl}	-5	0	5	µA	V_{CC} = 0 V, V_S = 0 V, V_{RTH} = 5 V, T_j < 85 °C
RTL leakage current	I_{RTLl}	-5	0	5	µA	V_{CC} = 0 V, V_S = 0 V, V_{RTL} = 13.5 V, T_j < 85 °C
Dynamic CAN-Transceiver Characteristics						
CANH and CANL bus output transition time recessive-to-dominant	t_{rd}	0.6	1.2	2.1	µs	10% to 90%; C_1 = 10 nF; C_2 = 0; R_1 = 100 Ω
CANH and CANL bus output transition time dominant-to-recessive	t_{dr}	0.3	0.6	1.3	µs	10% to 90%; C_1 = 1 nF; C_2 = 0; R_1 = 100 Ω
Minimum dominant time for wake-up on CANL or CANH	$t_{wu(min)}$	15	25	40	µs	stand-by mode

8.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; SBC-normal-mode; – 40 °C < T_j < 140 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Failure cases 3 and 6 detection time	t_{fail}	30	45	80	µs	normal operating mode
Failure case 6a detection time		2.0	4.8	8.0	ms	normal operating mode
Failure cases 5, 6, 6a and 7 recovery time		30	45	80	µs	normal operating mode
Failure cases 3 recovery time		250	500	750	µs	normal operating mode
Failure cases 5 and 7 detection time		1.0	2.0	4.0	ms	normal operating mode
Failure cases 5 detection time	t_{fail}	0.4	1.0	4.0	ms	stand-by mode
Failure cases 6, 6a and 7 detection time		0.8	4.0	8.0	ms	stand-by mode
Failure cases 5, 6, 6a and 7 recovery time		0.4	1.0	2.4	µs	stand-by mode
Propagation delay TxD-to-RxD LOW (recessive to dominant)	$t_{PD(L)}$	–	1.5	2.1	µs	C_1 = 100 pF; C_2 = 0; R_1 = 100 Ω; no failures and bus failure cases 1, 2, 3a and 4
		–	1.7	2.4	µs	C_1 = C_2 = 3.3 nF; R_1 = 100 Ω; no bus failure and failure cases 1, 2, 3a and 4
		–	1.8	2.5	µs	C_1 100 pF; C_2 = 0; R_1 = 100 Ω; bus failure cases 3, 5, 6, 6a and 7
		–	2.0	2.6	µs	C_1 = C_2 = 3.3 nF; R_1 =100 Ω; bus failure cases 3, 5, 6, 6a and 7

8.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; SBC-normal-mode; – 40 °C < T_j < 140 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Propagation delay TxD-to-RxD HIGH (dominanat to recessive)	$t_{PD(H)}$	–	1.5	2.0	µs	C_1 = 100 pF; C_2 = 0; R_1 =100 Ω; no failures and bus failure cases 1, 2, 3a and 4
		–	2.5	3.5	µs	C_1 = C_2 = 3.3 nF; R_1 = 100 Ω; no bus failure and failure cases 1, 2, 3a and 4
		–	1.0	2.1	µs	C_1 100 pF; C_2 = 0; R_1 = 100 Ω; bus failure cases 3, 5, 6, 6a and 7
		–	1.5	2.6	µs	C_1 = C_2 = 3.3 nF; R_1 = 100 Ω; bus failure cases 3, 5, 6, 6a and 7
Edge-count difference (falling edge) between CANH and CANL for failure cases 1, 2, 3a and 4 detection	n_e	–	4	–	–	normal operating mode
Edge-count difference (rising edge) between CANH and CANL for failure cases 1, 2, 3a and 4 recovery		–	2	–	–	
Edge-count difference (rising edge) at TxD for differentiation of failure cases 2/4, 1/ 3a and 5/7	n_e	–	2	–	–	normal operating mode (data transmitting)
TxD permanent dominant disable time	t_{TxD}	0.8	1	1.3	ms	normal mode
CAN-RxD-256ms transitition time	t_{RD-256}	130	256	380	ms	

8.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; SBC-normal-mode; – 40 °C < T_j < 140 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
SPI-Interface						
Logic Inputs DI, CLK and CSN						
H-input voltage threshold	V_{IH}	–	–	0.7 * V_{CC1}	V	–
L-input voltage threshold	V_{IL}	0.2 * V_{CC1}	–	–	V	–
Hysteresis of input voltage	V_{IHY}	50	200	500	mV	–
Pull up current at pin CSN	I_{ICSN}	-100	-25	-5	µA	$V_{CSN} = 0.7 \times V_{CC1}$
Pull down current at pin DI and CLK	$I_{ICLK/DI}$	5	25	100	µA	$V_{CLK/DI} = 0.2 \times V_{CC1}$
Input capacitance at pin CSN, DI or CLK	C_I	–	10	15	pF	0 V < V_{CC1} < 5.25 V
Logic Output DO						
H-output voltage level	V_{DOH}	V_{CC1} -1.0	V_{CC1} - 0.3	–	V	I_{DOH} = 1 mA
L-output voltage level	V_{DOL}	–	0.2	0.4	V	I_{DOL} = – 1.6 mA
Tri-state leakage current	I_{DOLK}	-10	–	10	µA	$V_{CSN} = V_{CC1}$ 0 V < V_{DO} < V_{CC1}
Tri-state input capacitance	C_{DO}	–	10	15	pF	$V_{CSN} = V_{CC1}$ 0 V < V_{CC1} < 5.25 V
Data Input Timing						
Clock period	t_{pCLK}	1000	–	–	ns	–
Clock high time	t_{CLKH}	500	–	–	ns	–
Clock low time	t_{CLKL}	500	–	–	ns	–
Clock low before CSN low	t_{bef}	500	–	–	ns	–
CSN setup time	t_{lead}	500	–	–	ns	

8.3 Electrical Characteristics (cont'd)

V_S = 13.5 V; SBC-normal-mode; – 40 °C < T_j < 140 °C; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
CLK setup time	t_{lag}	500	–	–	ns	
Clock low after CSN high	t_{beh}	500	–	–	ns	
DI setup time	t_{DISU}	250	–	–	ns	
DI hold time	t_{DIHO}	250	–	–	ns	
Input signal rise time at pin DI, CLK and CSN	t_{rIN}	–	–	200	ns	
Input signal fall time at pin DI, CLK and CSN	t_{fIN}	–	–	200	ns	
Data Output Timing						
DO rise time	t_{rDO}	–	50	100	ns	C_L = 100 pF
DO fall time	t_{fDO}	–	50	100	ns	C_L = 100 pF
DO enable time	t_{ENDO}	–	–	250	ns	low impedance
DO disable time	t_{DISDO}	–	–	250	ns	high impedance
DO valid time	t_{VADO}	–	100	250	ns	V_{DO} < 0.1 V_{CC1}; V_{DO} > 0.9 V_{CC1}; C_L = 100 pF

9 Timing Diagrams

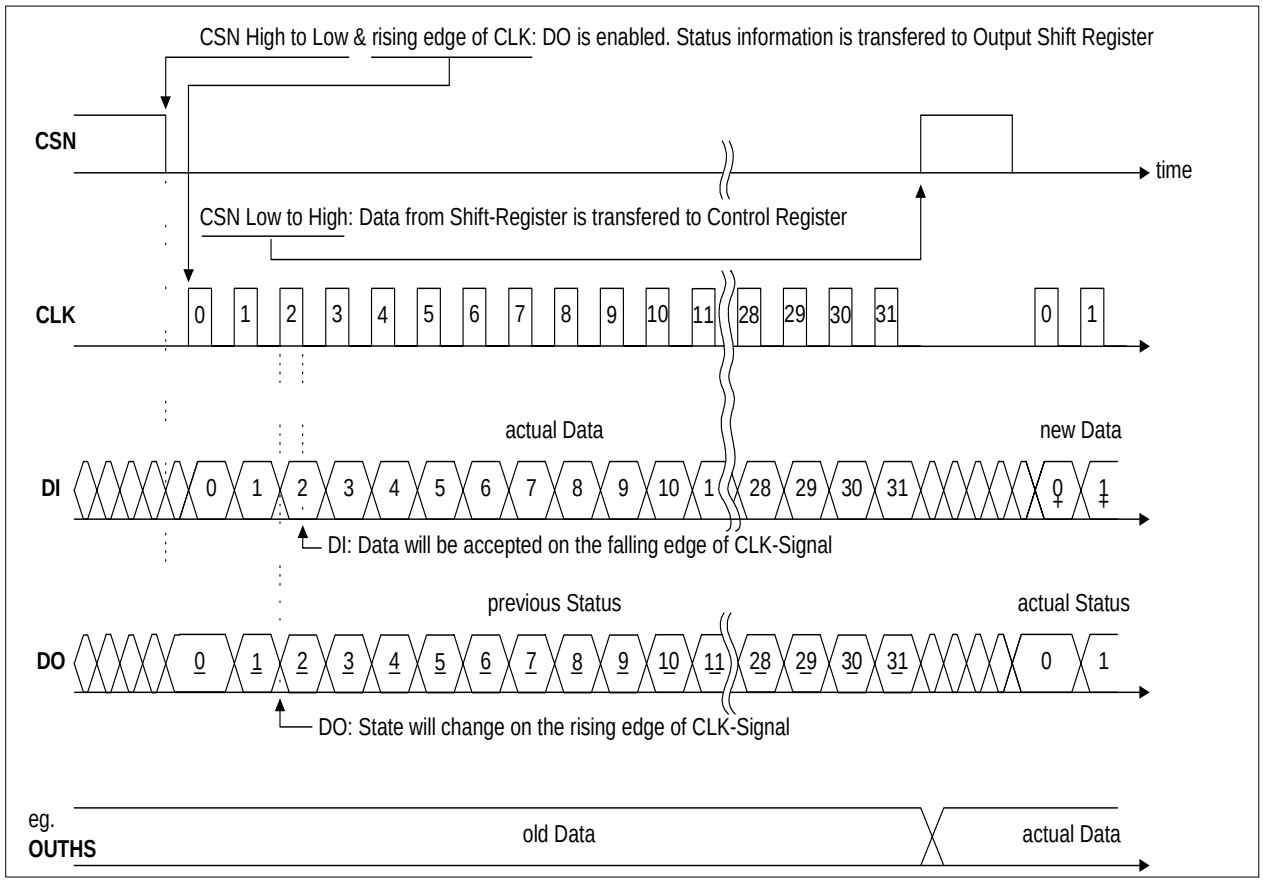


Figure 6
Data Transfer Timing for 32 bit mode (8 bit mode accordingly)

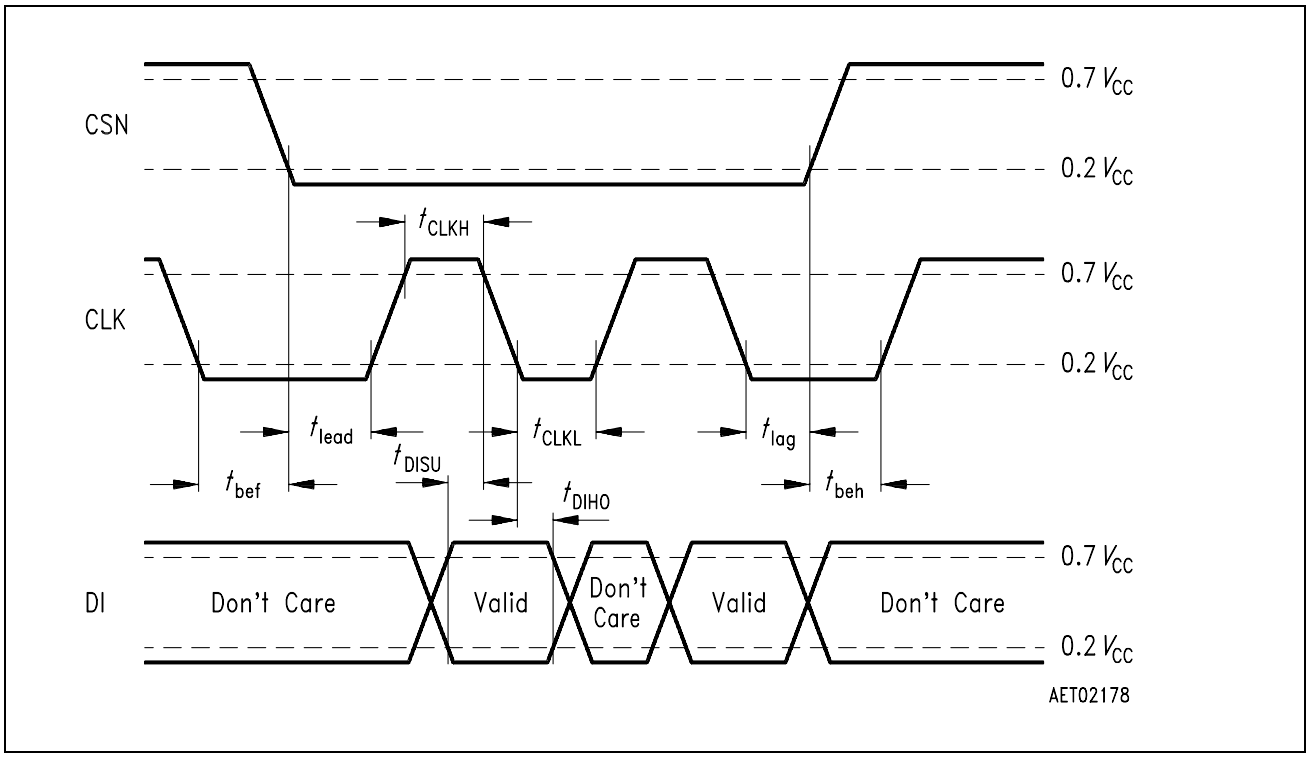


Figure 7
SPI-Input Timing

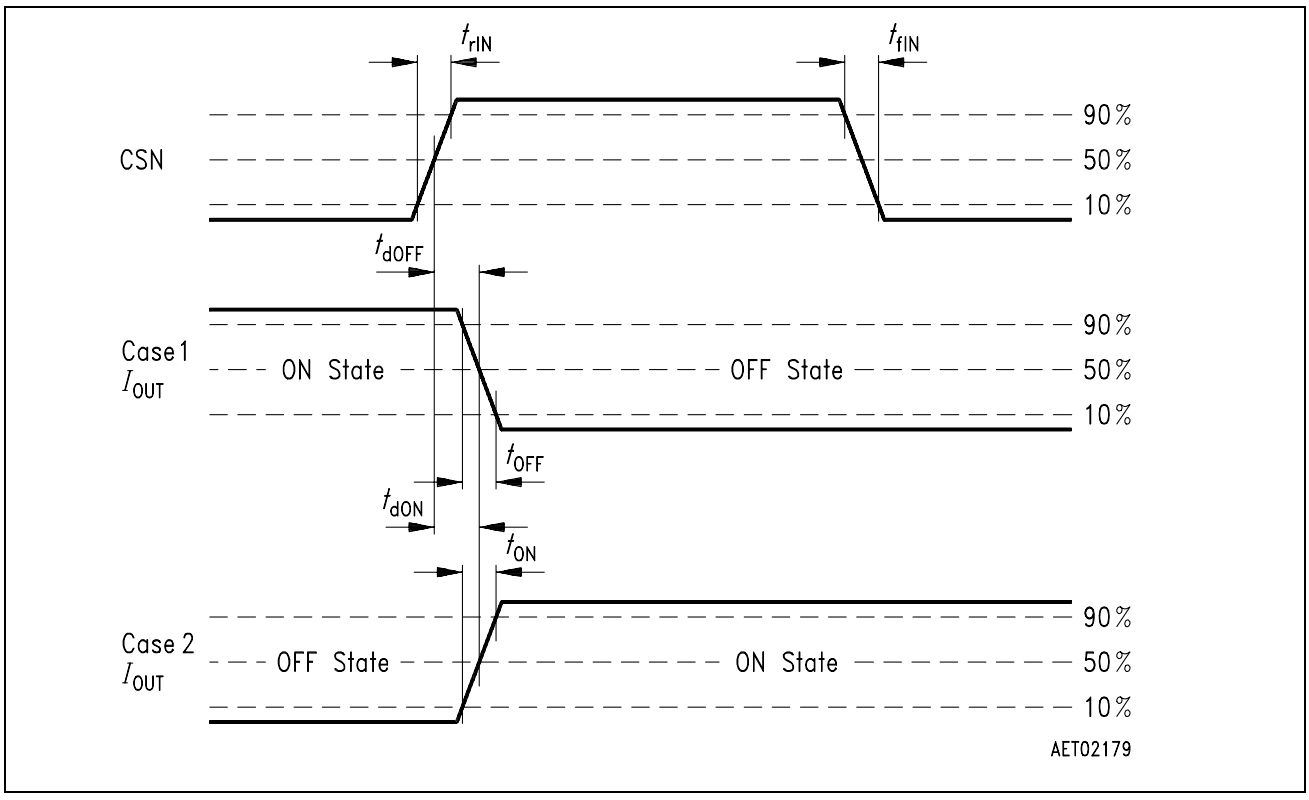


Figure 8
Turn OFF/ON Time

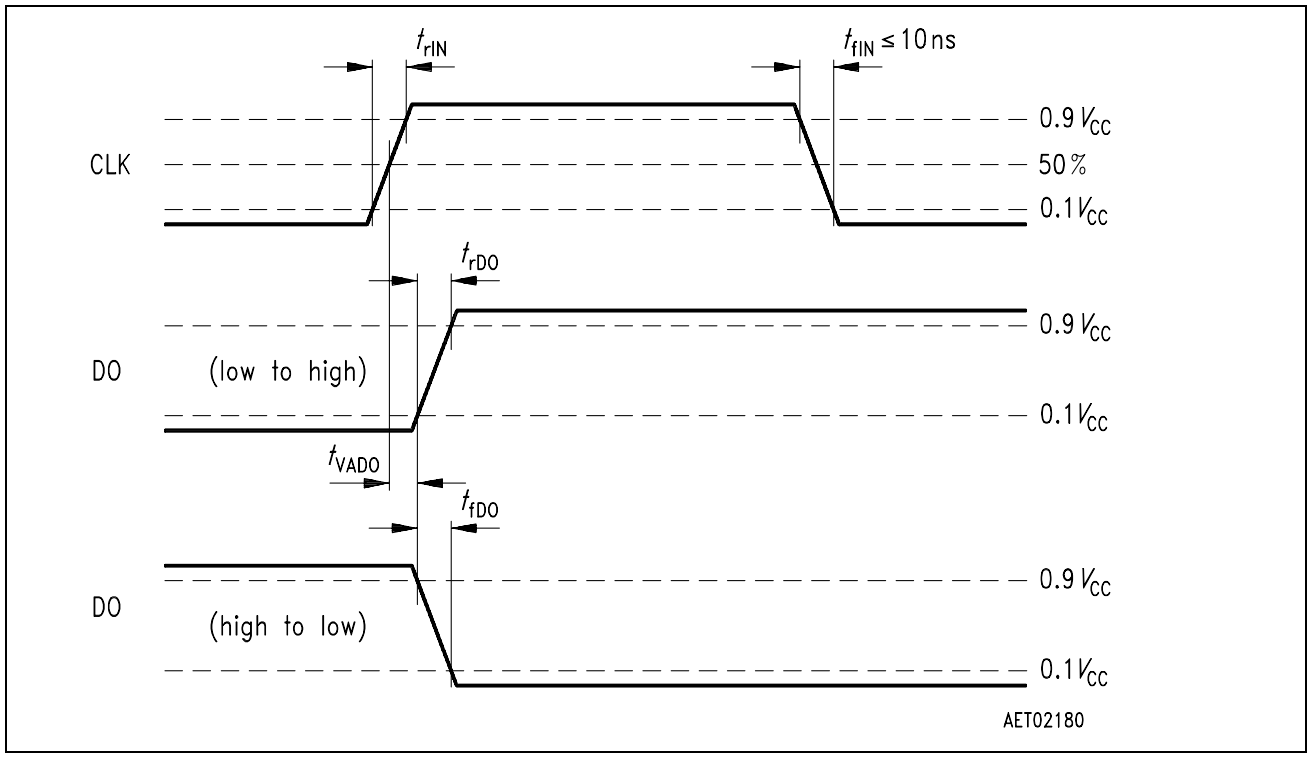


Figure 9
DO Valid Data Delay Time and Valid Time

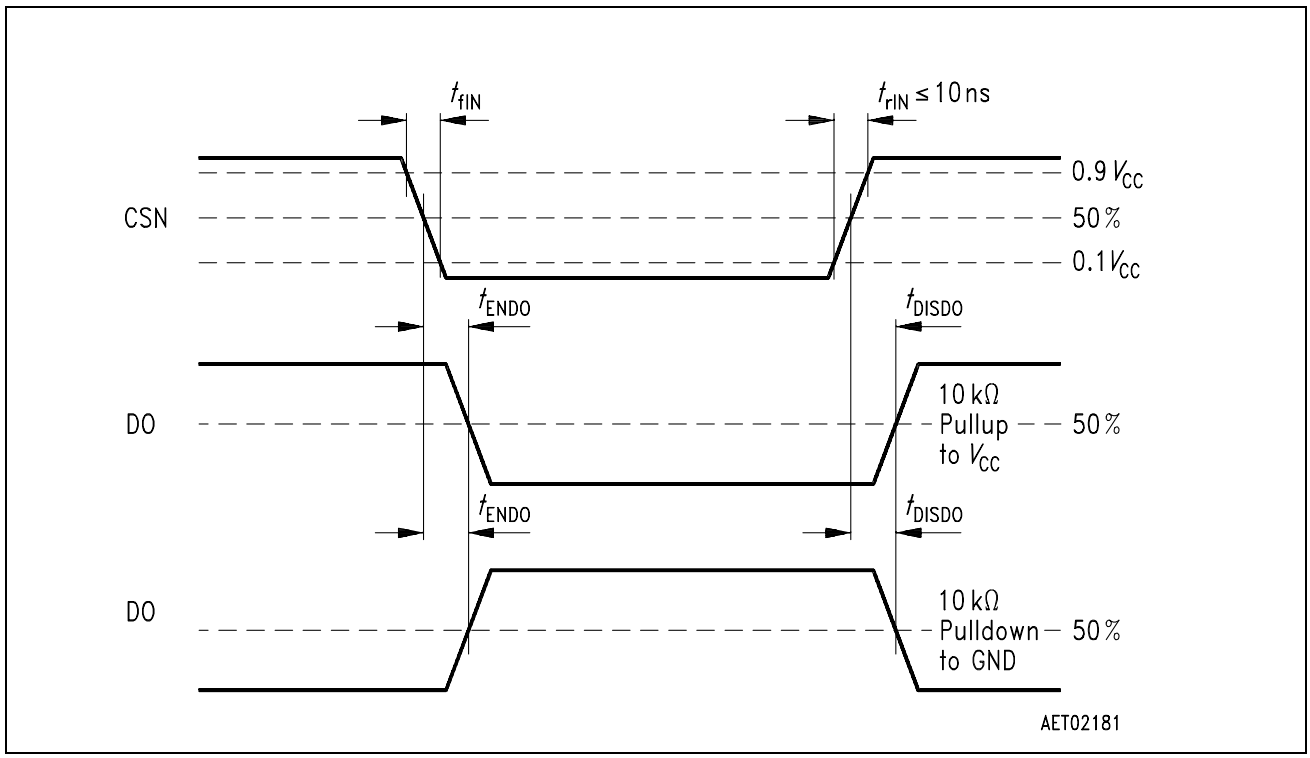


Figure 10
DO Enable and Disable Time

Figure 11: Cyclic sense timing

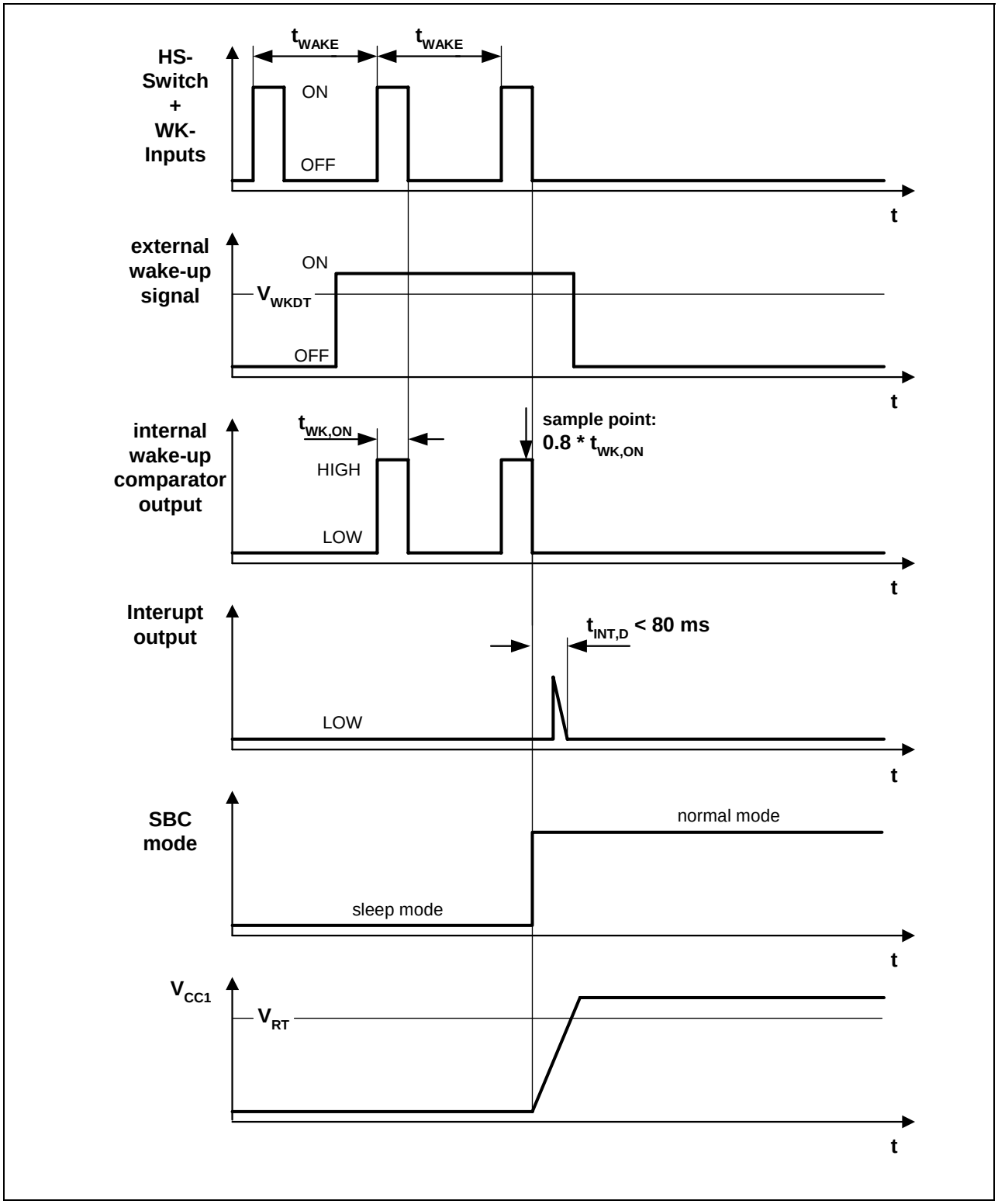


Figure 12: Watchdog Time Definition

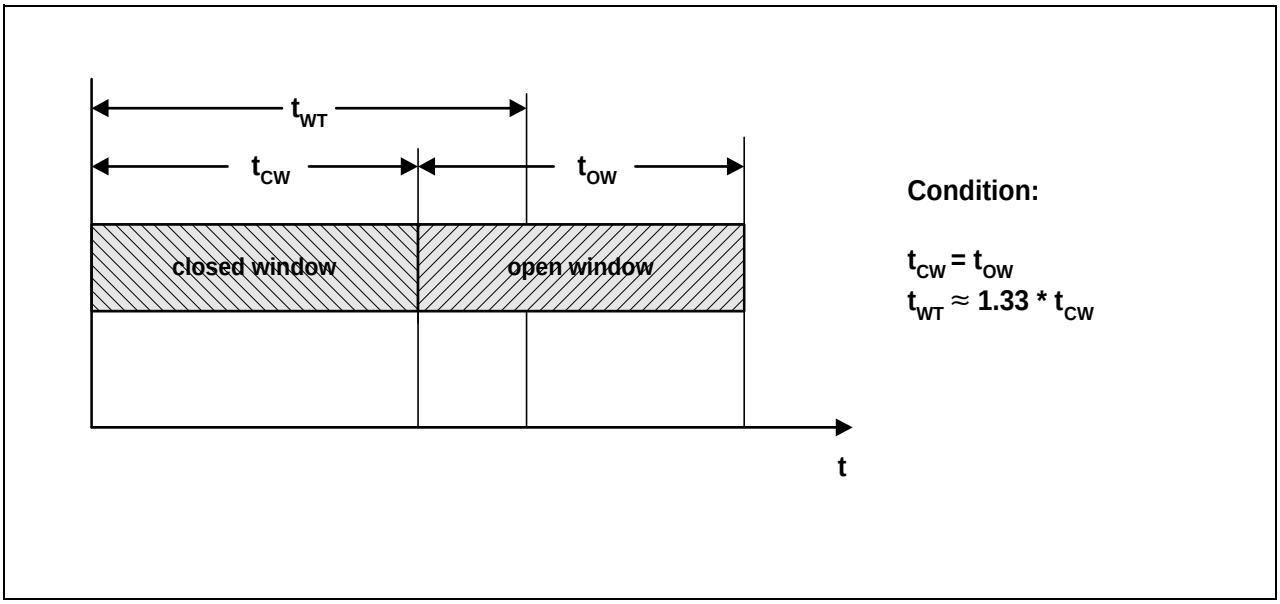


Figure 13: Watchdog Start-Up and Reset Timing Diagram

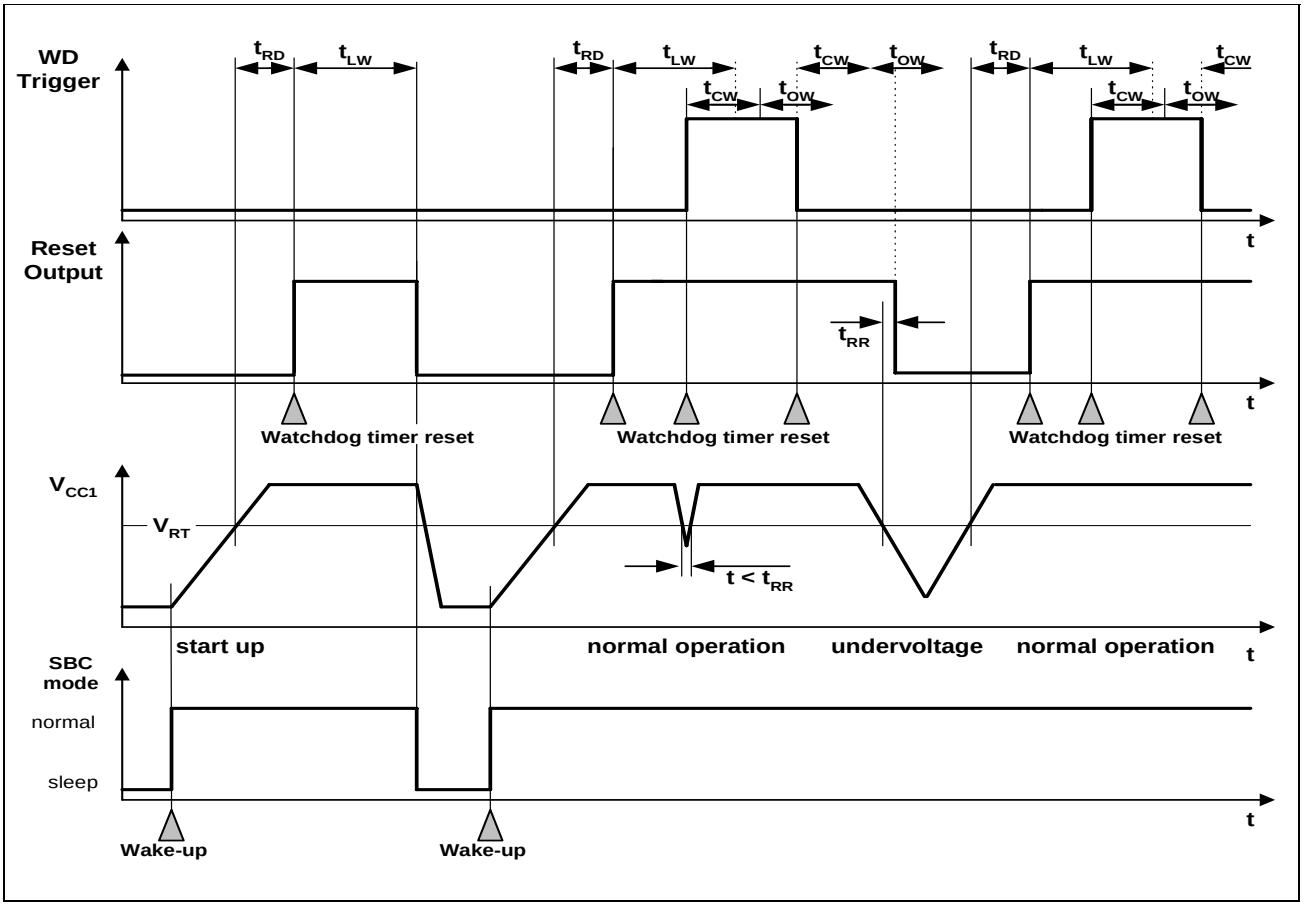


Figure 14: Watchdog Timing Diagram

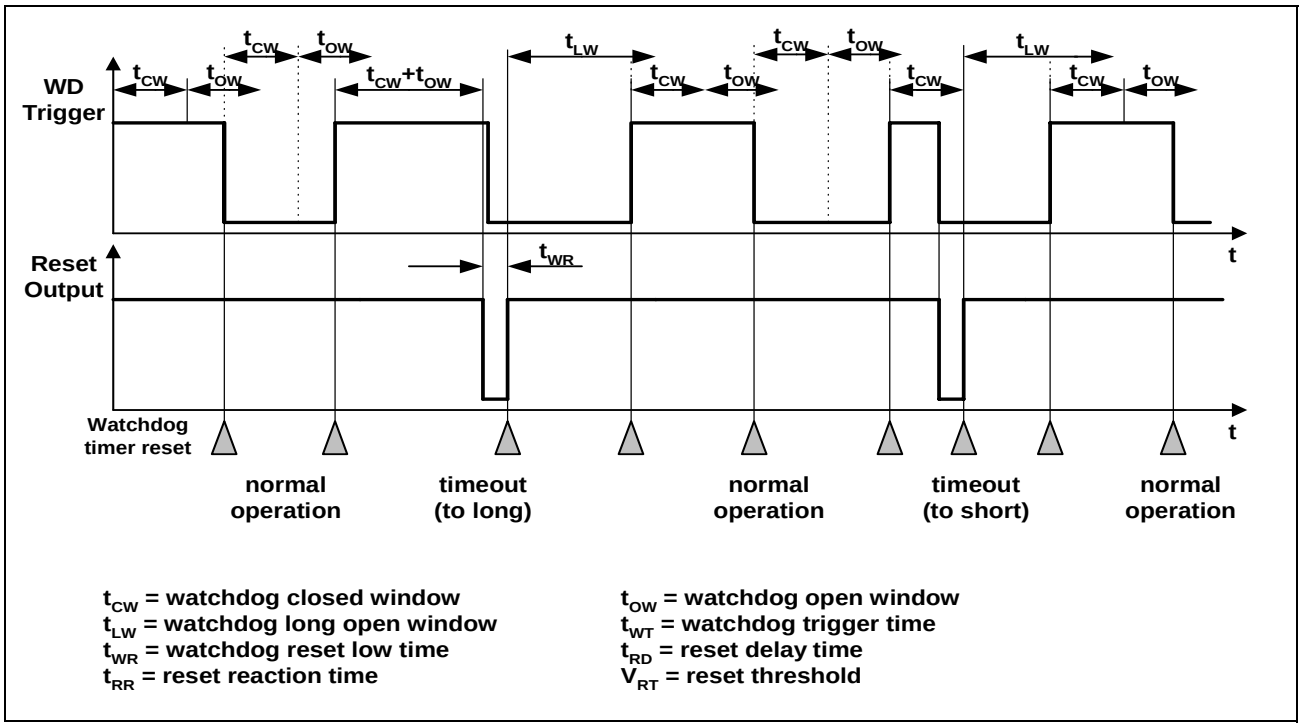


Figure 15: GND-Shift Timing Diagram

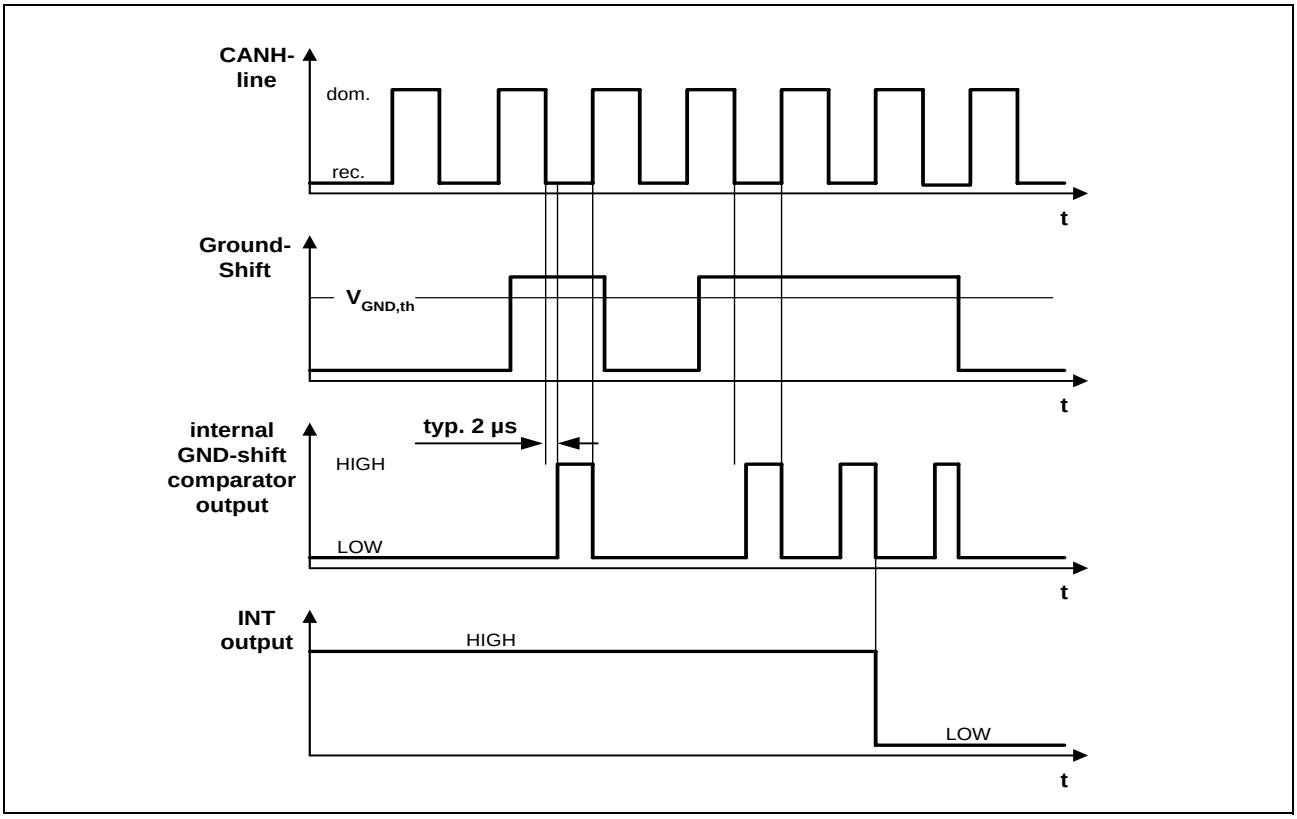


Figure 16: Test circuit

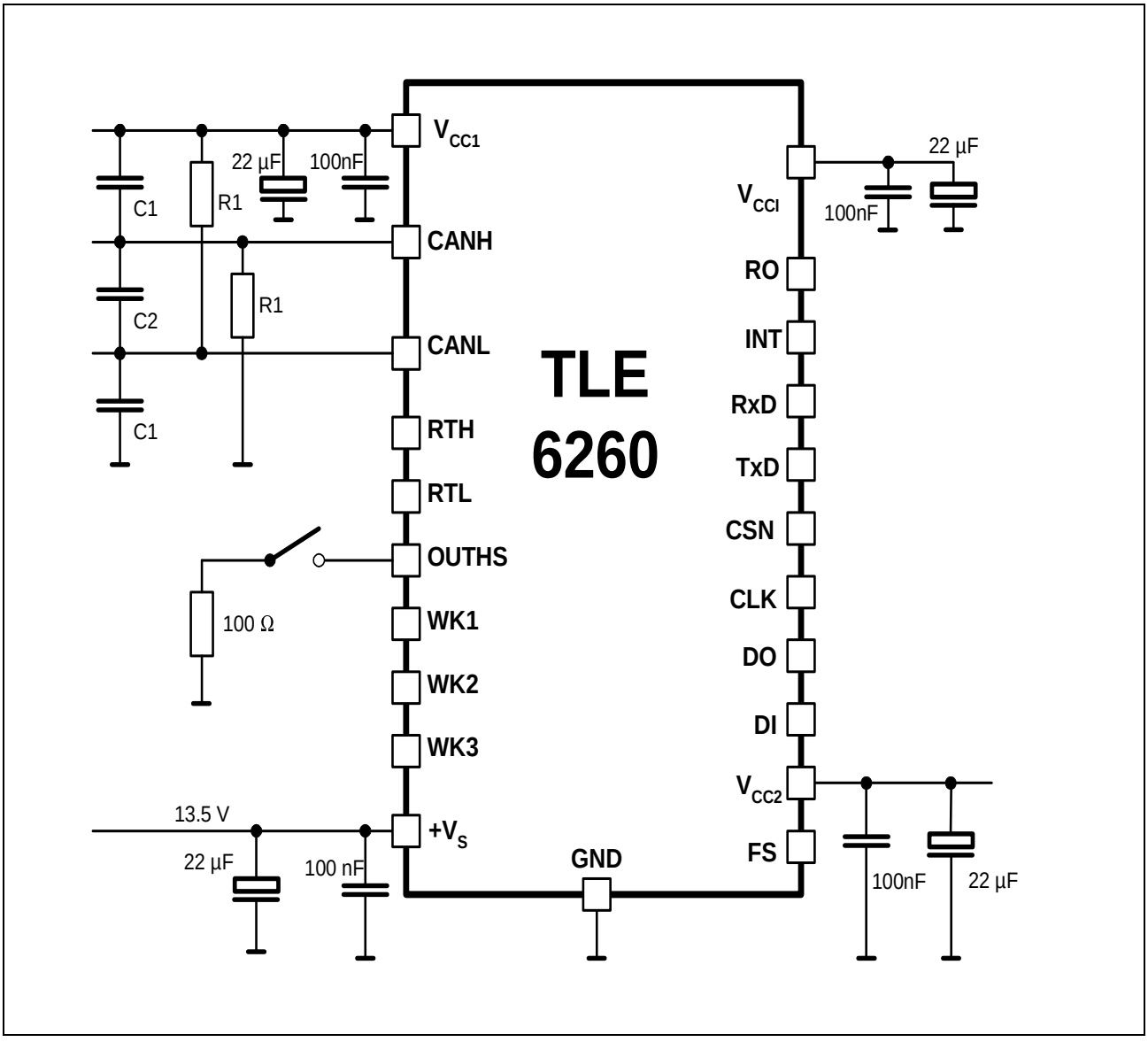
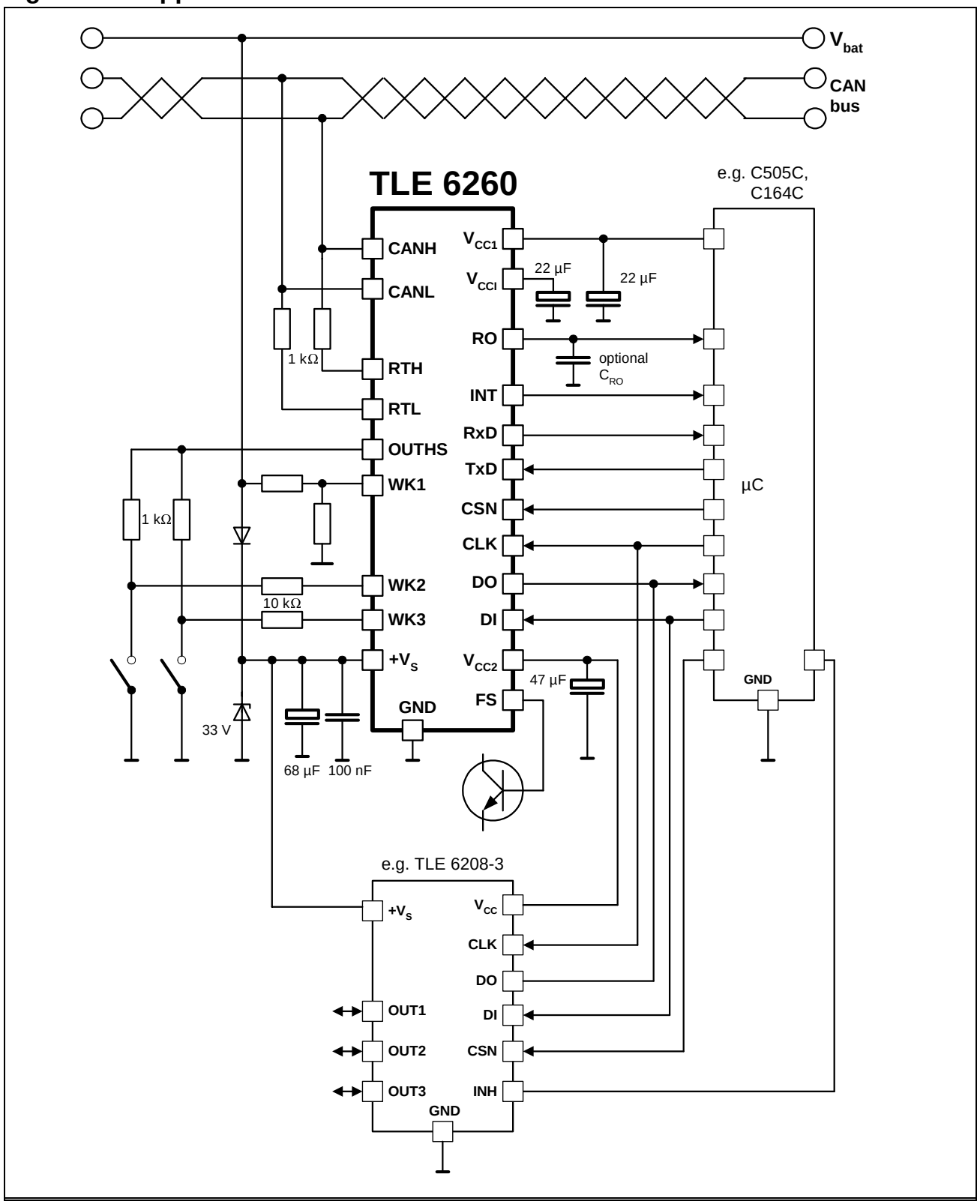
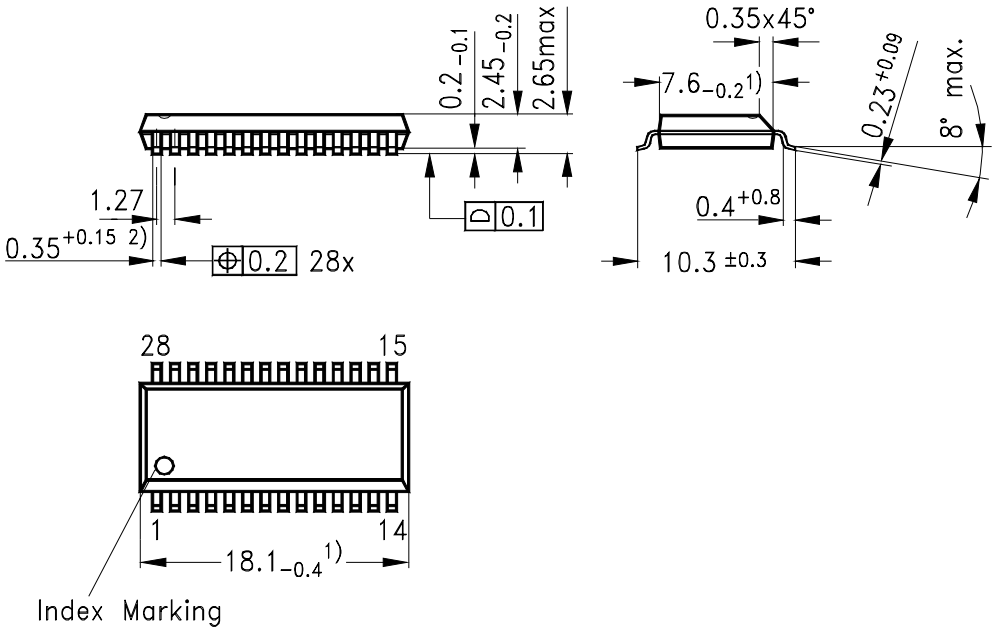


Figure 17: Application Circuit



Package Outlines

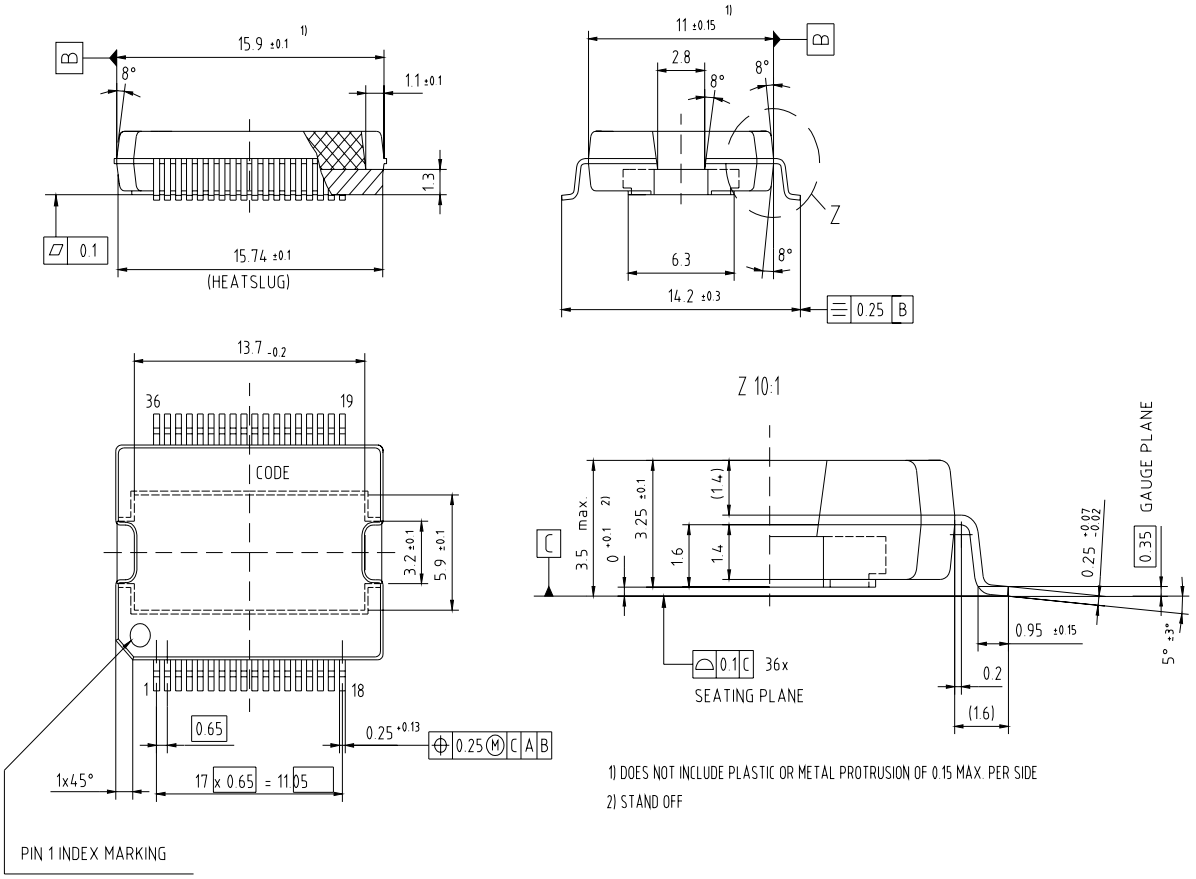
P-DSO-28-6
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.05 max. per side

GPS05123

P-DSO-36-12
(Plastic Dual Small Outline Package)



Edition 1999-10-12

Published by Infineon Technologies AG
St.-Martin-Strasse 53
D-81541 München

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.