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Cache Chipset for 80486 Systems

FEATURES

- Highly integrated VLSI components offer complete solution for secondary cache for 80486 systems
  - MS82C441 Cache Controller
  - MS82C442 Expansion Tag RAM
  - MS82C443 Burst RAM
- Supports true 80486 burst reads with 0 wait states
- Write-back cache update strategy with 16 byte sub-blocks
  - 0 wait-state read hits, write hits and write misses
  - Improves system bus utilization
  - Speeds up DMA operations
  - Maintains cache coherency in multi-processor systems
  - LRU cache line replacement
- Supports burst reads and writes between cache and main memory
  - Allows both sequential and 80486 burst sequence memory requests
  - With Burst RAM allows use of standard cost-effective 32 bit main memory organization (No bank interleaving required). Automatically handles resequencing of data back to 80486
- Tightly coupled 80486 interface
  - Caches full 4GB memory space
  - Cache invalidation cycles supported back to the 80486
- Performance match for 25 and 33 MHz processors.
  - Future migration to 40 and 50 MHz
- Supports 32, 64, 128 , 256 Kbyte and larger caches
  - Controller integrates 64 Kbyte tag directory on-board
  - For larger caches each Expansion Tag RAM offers additional 64 KB true vertical cache expansion for highest hit rates without extending line size
- Direct mapped, 2-way and 4-way set associative cache mapping options supported
- Flexible on-chip support for 4 non-cachable regions. Full support for KEN#.
- On-chip Gate A20 support
- Supports Weitek 4167 co-processor
- Bus snooping ensures cache coherency.
- Direct interface to standard SRAMs or unique Mosel Burst RAMs
  - Burst RAMs offer maximum performance by allowing cache hits and memory accesses to be done in parallel
  - x9 width of Burst RAM allows use of parity functions offered by 80486
  - Burst RAMs allow write-back line replacement cycles to be hidden from processor, providing up to 8x performance improvement over alternative implementations.

The MOSEL MS82C440 Chip Set is the industry's first complete solution for high performance 80486 systems. This solution allows the processor to run at full speed by providing virtually 0 wait state memory accesses at only a small additional cost. The MS82C441 cache controller incorporates enhanced capabilities such as full support for 80486 burst reads, multiple cache associativity options and burst reads and writes between cache and main memory. It uses a write-back cache update strategy, which improves system bus utilization, speeds up DMA operations, and assures cache coherency without performance degradation in high-performance systems. Highly integrated designs incorporate support for non-cachable regions, co-processors and other functions into the chipset, requiring a minimum of external logic and offering significant reductions in system cost, chip count and board space requirements.

Mosel's advanced memory technology and expertise has allowed the development of an innovative high speed data path offering significantly improved performance and higher integration. The proprietary dual-access architecture of the MS82C443 Burst RAM allows for processor accesses and main memory accesses to occur in parallel, offering major improvements in system performance. Addition of the (optional) MS82C442 Expansion Tag RAM allows true vertical cache expansion to 256 KB and beyond for highest performance without increased miss penalty or lengthy line replacement cycle times.

This unique scalable architecture offers the highest performance at every density, while allowing the system designer flexibility to select optimum tradeoffs of cost and performance. It also allows for product families and significant product differentiation. The MOSEL MS82C440 cache chipset offers maximum performance with a minimum of cost and board space.

Cache Benefits

As microprocessor speeds continue to increase, these powerful CPUs are hampered by slow access times of main-memory built from inexpensive DRAMs. The addition of a cache subsystem dramatically improves overall system performance by reducing processor wait states and system bus accesses.

Cache Considerations

The two most important factors which influence system performance are cache hit rate and cache management policies. Hit rate is a function of cache size, cache organization, line size, and sub-block size, as well as external factors relating to software design. Cache management policies include such considerations as memory mapping, memory write mechanism, cache miss handling, line replacement, cache coherency and non-cachable memory.

In a write-thru cache, every write operation from the processor is treated as a miss and written to main memory. This provides a simple mechanism for maintaining cache coherency, but sacrifices performance (since writes to main memory take more cycles) and bus bandwidth (since the system bus is occupied with processor writes). In contrast, a write-back cache reduces system bus traffic by writing to main memory only when a cache line which has been modified by the CPU is about to be replaced by new data from main memory. This drastically reduces the frequency of main memory write accesses, and frees up system bus bandwidth for DMA operations and other system accesses.

The MS82C440 Cache Chipset optimizes the tradeoffs between these factors for an 80486 system. Its' enhanced capabilities and innovative features offer superior performance, design flexibility and integration to the designer while being economical and easy to use

MS82C441 Cache Controller and MS82C442 Expansion Tag RAM

The MS82C441 is a sophisticated second generation write-back cache controller for use with the Intel 80486 microprocessor. It supports direct-mapped, 2-way and 4-way set-associative cache mapping and provides all management logic for a high-performance cache. The MS82C441 integrates 64KB tag directory with 2K entries on-chip. Addition of the MS82C442 Expansion Tag RAM allows true vertical cache expansion up to 256 KB and beyond for highest performance without increased miss penalty or extending cache line length (which can severely impact performance).

Full support for the 80486 is provided by the MS82C441 cache controller, including 0 wait state burst reads and non-cachable regions through KEN#. It also supports burst reads and writes between cache and main memory, and can handle both sequential and 80486 burst sequence memory organizations.

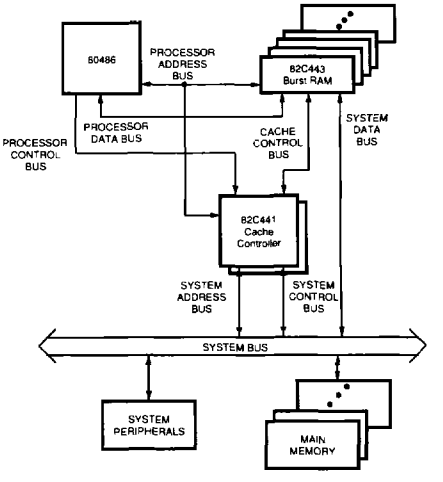
The MS82C441 uses a write-back memory write strategy with an 8 line sub-block size. Bus snooping is included to maintain cache coherency. Non-cachable memory is supported with four general purpose non-cachable regions on-chip. These eliminate the need for fast external logic. Two of these regions may be specified as non-writable to support ROM or BIOS caching. Additional support is included for the Weitek 4167 co-processor.

MS82C443 Burst RAM

While the MS82C441 and MS82C442 provide excellent performance when used with standard SRAMs, the use of the MS82C443 Burst RAM offers an additional dramatic performance improvement. The advanced dual-access architecture of the Burst RAM isolates the processor and system data buses. Since the cache will typically be operating at hit rates >96%, this allows main memory operations to proceed simultaneously with processor cache accesses. Write-back line replacement cycles are hidden from the processor, providing up to an 8X performance improvement in miss processing over other implementations. This innovative approach offers a quantum leap improvement in data path architecture, removing a major bottleneck to increased performance.

The MS82C443 Burst RAM also allows the use of standard, cost-effective 32 bit main memory designs. In conjunction with the MS82C441 cache controller, standard sequential DRAM access modes can be used, and the data will automatically be resequenced into the proper order for the 80486. This unique capability eliminates the need to develop complex and expensive memory architectures such as 64 bit memory buses or bank interleaved memory, while providing maximum performance.

SYSTEM BLOCK DIAGRAM



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