TriQuint SEMICONDUCTOR

AGR21030EF
30 W, 2.110 GHz—2.170 GHz, N-Channel E-Mode, Lateral MOSFET

Introduction

The AGR21030EF is a high-voltage, gold-metalized, laterally diffused metal oxide semiconductor (LDMOS) RF power transistor suitable for wideband code division multiple access (W-CDMA), single and multicarrier class AB wireless base station power amplifier applications.

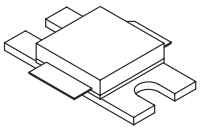


Figure 1. AGR21030EF (flanged) Package

Features

Typical performance for 2 carrier 3GPP W-CDMA systems. F1 = 2135 MHz and F2 = 2145 MHz with 3.84 MHz channel BW, adjacent channel BW = 3.84 MHz at F1 – 5 MHz and F2 + 5 MHz. Third-order distortion is measured over 3.84 MHz BW at F1 – 10 MHz and F2 + 10 MHz. Typical P/A ratio of 8.5 dB at 0.01% (probability) CCDF:
- — Output power: 7 W.
- — Power gain: 14.5 dB.
- — Efficiency: 26%.
- — IM3: –34 dBc.
- — ACPR: –37 dBc.
- — Return loss: –12 dB.

High-reliability, gold-metalization process.

Low hot carrier injection (HCI) induced bias drift over 20 years.

Internally matched.

High gain, efficiency, and linearity.

Integrated ESD protection.

Device can withstand a 10:1 voltage standing wave ratio (VSWR) at 28 Vdc, 2140 MHz, 30 W continuous wave (CW) output power.

Large signal impedance parameters available.

Table 1. Thermal Characteristics

Parameter	Sym	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.0	°C/W

Table 2. Absolute Maximum Ratings*

Parameter	Sym	Value	Unit
Drain-source Voltage	V_{DSS}	65	Vdc
Gate-source Voltage	V_{GS}	–0.5, 15	Vdc
Total Dissipation at T_C = 25 °C	P_D	87.5	W
Derate Above 25 °C	—	0.5	W/°C
CW RF Input Power (V_{DS} = 31 V)	—	10	W
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{STG}	–65, 150	°C

* Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. ESD Rating*

AGR21030EF	Minimum (V)	Class
HBM	500	1B
MM	50	A
CDM	1500	4

* Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. PEAK Devices employs a human-body model (HBM), a machine model (MM), and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114B (HBM), JESD22-A115A (MM), and JESD22-C101A (CDM) standards.

Caution: MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Electrical Characteristics

Recommended operating conditions apply unless otherwise specified: T_C = 30 °C.

Table 4. dc Characteristics

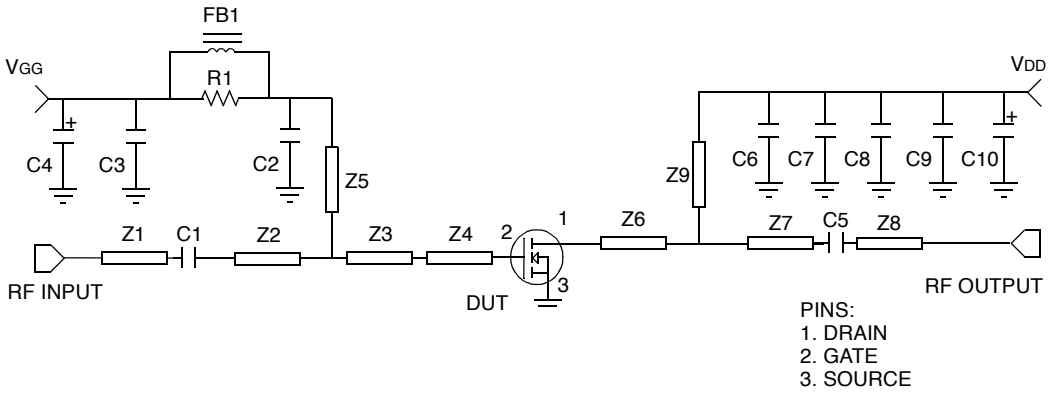
Parameter	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-source Breakdown Voltage (V_{GS} = 0, I_D =150μA)	$V_{(BR)DSS}$	65	—	—	Vdc
Gate-source Leakage Current (V_{GS} = 5 V, V_{DS} = 0 V)	I_{GSS}	—	—	1	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	—	—	50	μAdc
On Characteristics					
Forward Transconductance (V_{DS} = 10 V, I_D = 0.4 A)	G_{FS}	—	2.4	—	S
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 μA)	$V_{GS(TH)}$	2.8	3.4	4.0	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_D = 300 mA)	$V_{GS(Q)}$	3.0	3.8	4.6	Vdc
Drain-source On-voltage (V_{GS} = 10 V, I_D = 0.4 A)	$V_{DS(ON)}$	—	0.30	—	Vdc

Table 5. RF Characteristics

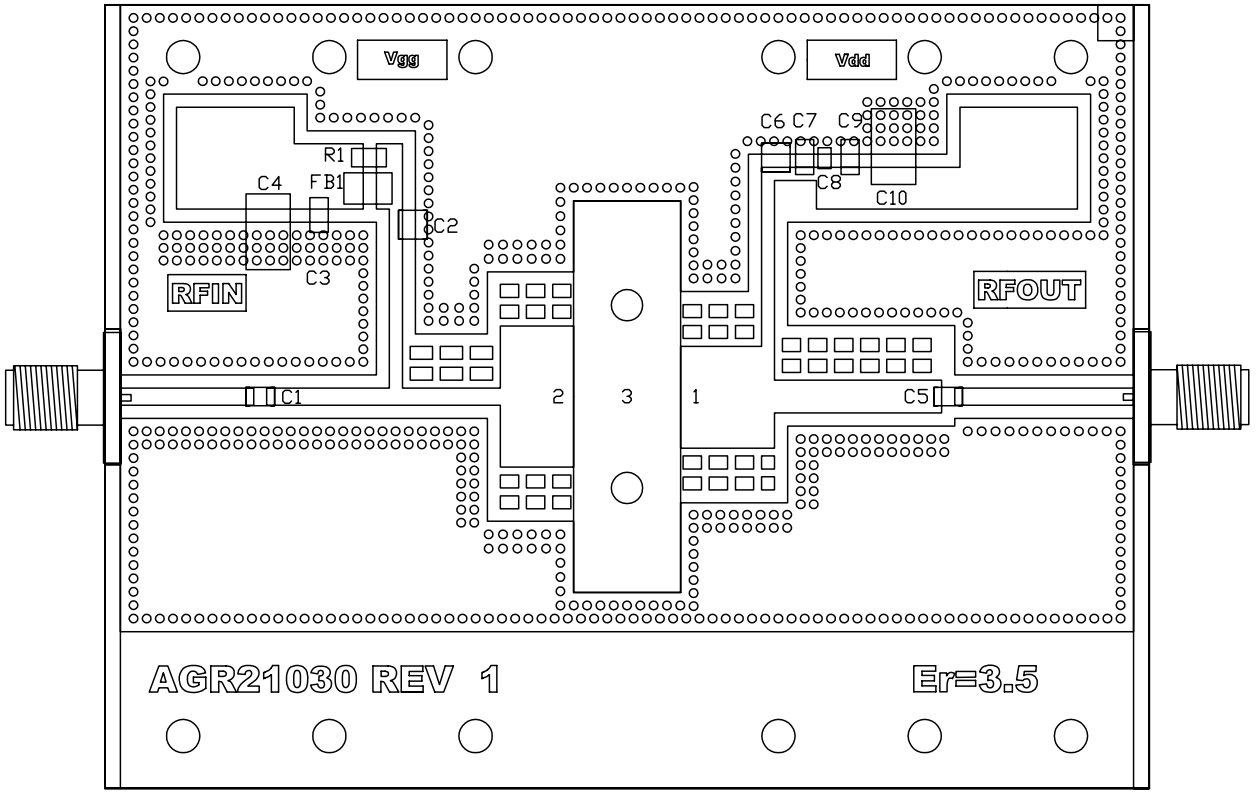
Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Characteristics					
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz) (This part is internally matched on both the input and output.)	C_{RSS}	—	0.8	—	pF
Functional Tests (in Supplied Test Fixture)					
Common-source Amplifier Power Gain*	G_{PS}	13.5	14.5	—	dB
Drain Efficiency*	η	24	26	—	%
Third-order Intermodulation Distortion* (IM3 distortion measured over 3.84 MHz BW @ f1 – 10 MHz and f2 + 10 MHz)	IM3	—	–34	–32	dBc
Adjacent Channel Power Ratio* (ACPR measured over BW of 3.84 MHz @ f1 – 5 MHz and f2 + 5 MHz)	ACPR	—	–37	–36	dBc
Output Power, 1 dB Compression Point (V_{DD} = 28 V, f_C = 2140.0 MHz)	P1dB	27	30	—	W
Input Return Loss*	IRL	—	–12	–10	dB
Output Mismatch Stress (V_{DD} = 28 V, P_{OUT} = 30 W (CW), I_{DQ} = 300 mA, f_C = 2140.0 MHz VSWR = 10:1; [all phase angles])	ψ	No degradation in output power.			

* 3GPP W-CDMA, typical P/A ratio of 8.5 dB at 0.01% CCDF, f1 = 2135 MHz, and f2 = 2145 MHz.
V_{DD} = 28 Vdc, I_{DQ} = 300 mA, and P_{OUT} = 7 W avg.
Nominal operating voltage 28 Vdc. Qualified for a maximum operating voltage of 32 Vdc ±0.5 V.

Test Circuit Illustrations for AGR21030EF



A. Schematic



Parts List:

- Microstrip line: Z1, 0.510 in. x 0.066 in.; Z2, 0.470 in. x 0.066 in.; Z3, 0.375 in. x 0.066 in. Z4, 0.280 in. x 0.540 in.; Z5, 0.570 in. x 0.050 in.; Z6, 0.360 in. x 0.390 in.; Z7, 0.640 in. x 0.125 in.; Z8, 0.685 in. x 0.066 in.; Z9, 0.685 in. x 0.050 in.
- *ATC*® chip capacitor: C1, C5: 8.2 pF 100B8R2JW500X; C2, C6 6.8 pF 100B6R8JW500X.
- *Kemet*® capacitor: C8 0.01 μF C1206104K5RAC7800; C9 0.1 μF GRM40X7R103K100AL.
- *Vitramon*® 1206 capacitor: C3, C7: 22,000 pF.
- *Sprague*® tantalum capacitor: C4, C10: 22 μF, 35 V.
- *Fair-Rite*® ferrite bead: FB1 2743019447.
- 1206 size chip resistor: R1 12 Ω.
- *Taconic*® ORCER RF-35: board material, 1 oz. copper, 30 mil thickness, $\varepsilon r = 3.5$.

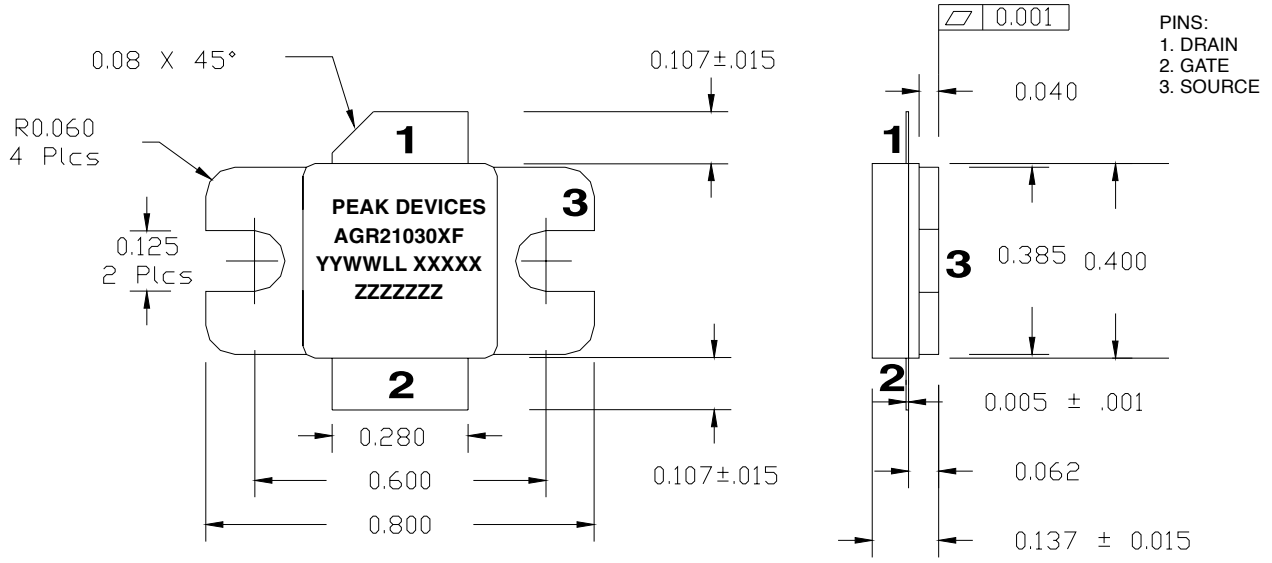
B. Component Layout

Figure 2. AGR21030EF Test Circuit

Package Dimensions

All dimensions are in inches. Tolerances are ±0.005 in. unless specified.

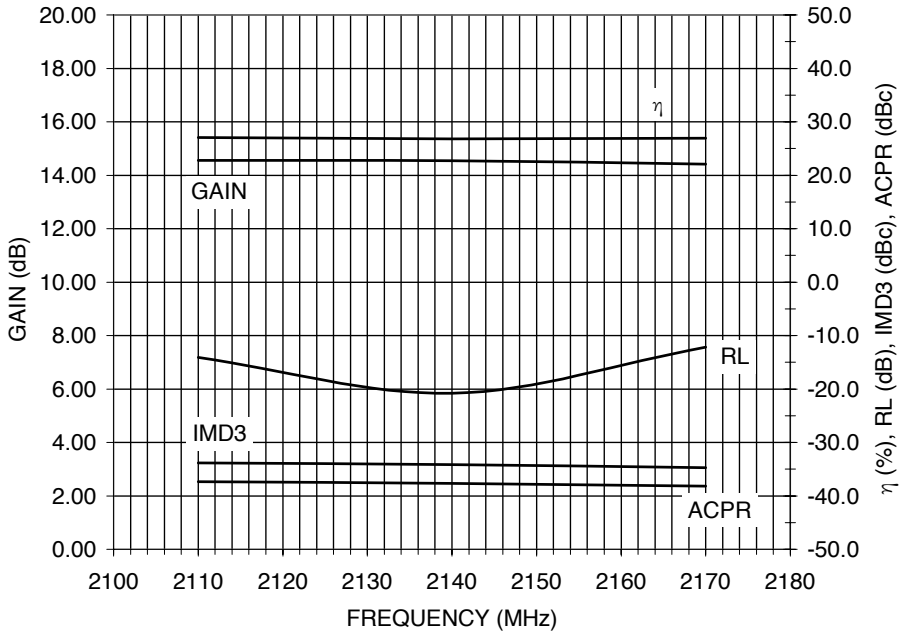
AGR21030EF



Label Notes:

- M before the part number denotes model program. X before the part number denotes engineering prototype.
- The last two letters of the part number denote wafer technology and package type.
- YYWWLL is the date code including place of manufacture: year year work week (YYWW), LL = location (AL = Allentown, PA; T = Thailand). XXXXX = five-digit wafer lot number.
- ZZZZZZZ = seven-digit assembly lot number on production parts.
- ZZZZZZZZZZZZ = 12-digit (five-digit lot, two-digit wafer, and five-digit serial number) on models and engineering prototypes.

Typical Performance Characteristics (continued)



TEST CONDITIONS:
V_{DD} = 28 V, I_{DQ} = 300 mA, P_{OUT} = 7 W.
2-carrier W-CDMA 3GPP, Peak-to-average = 8.5 dB @ 0.01% CCDF, 10 MHz spacing, 3.84 CBW.

Figure 8. Broadband Performance

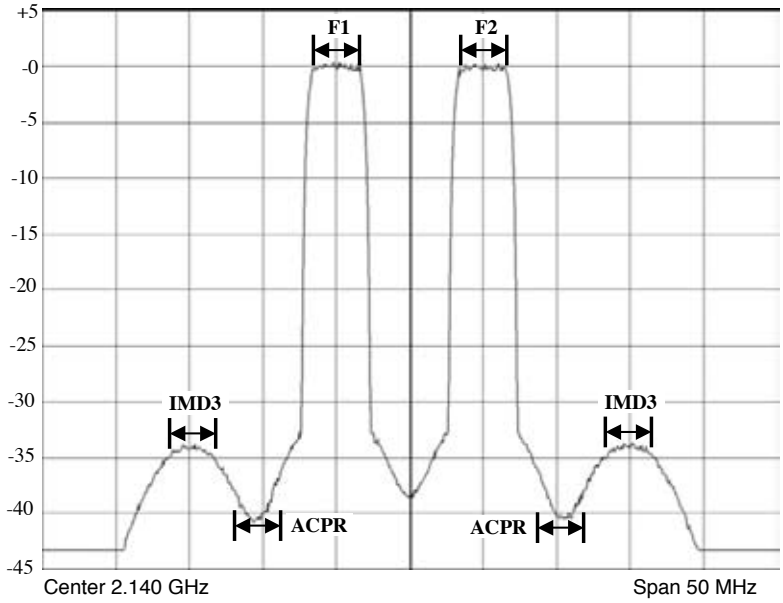


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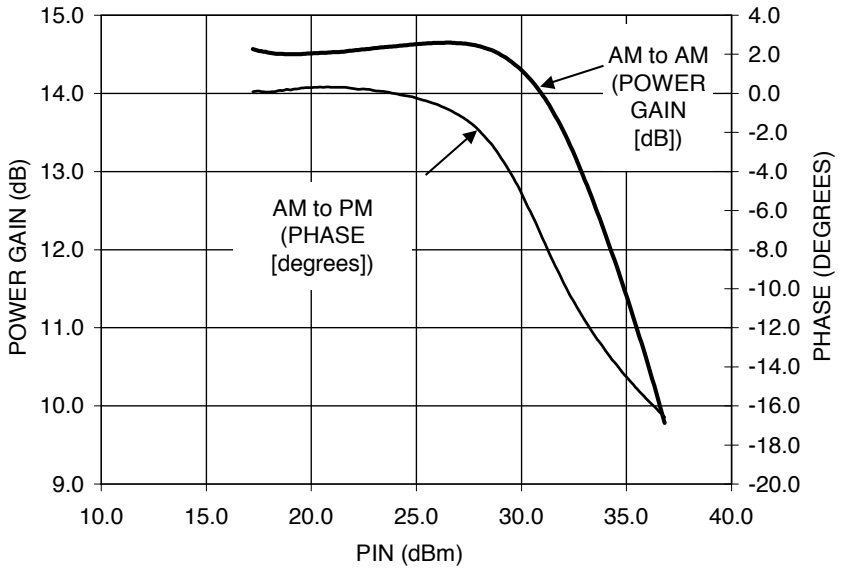
Figure 9. Spectral Plot

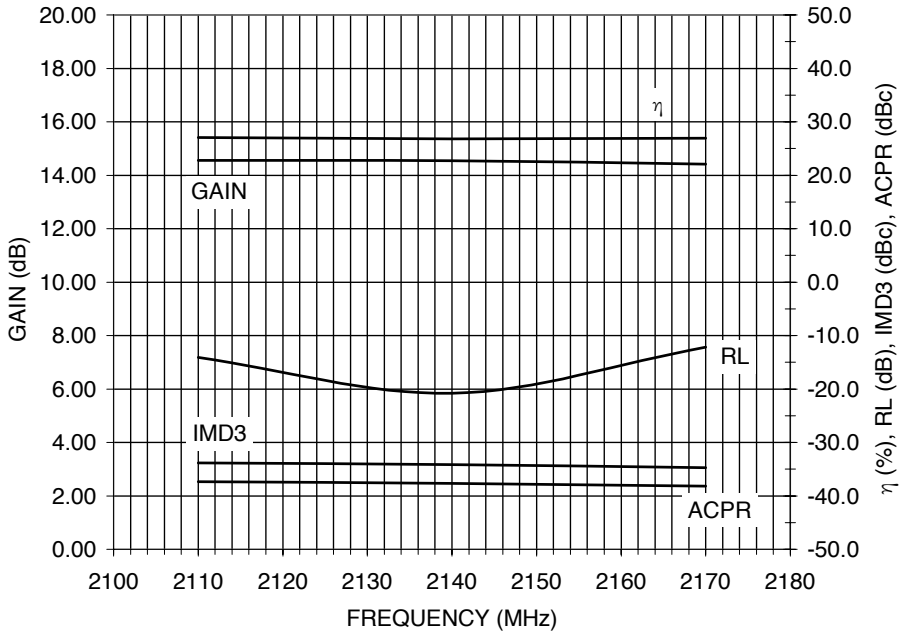
Typical Performance Characteristics (continued)



TEST CONDITIONS:
V_{DD} = 28 Vdc, F = 2140 MHz, I_{DQ} = 300 mA CW input.

Figure 10. AM-AM and AM-PM Characteristics

Typical Performance Characteristics (continued)



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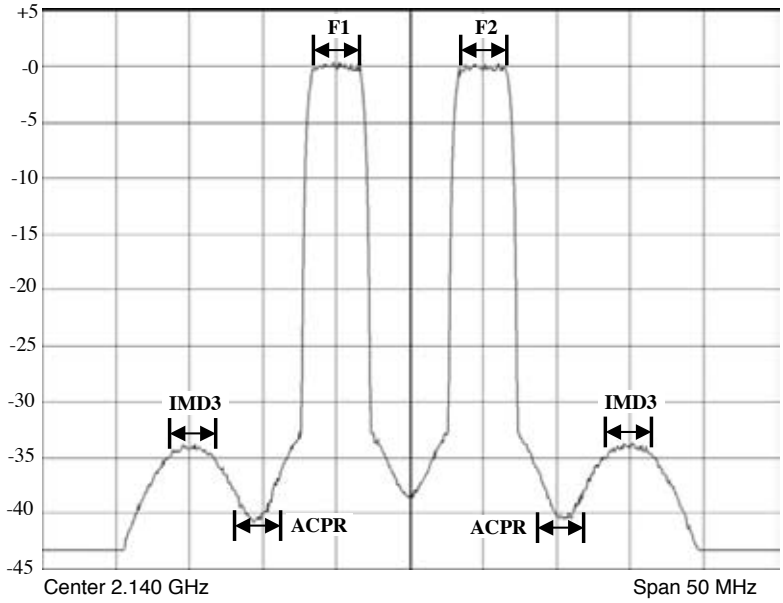

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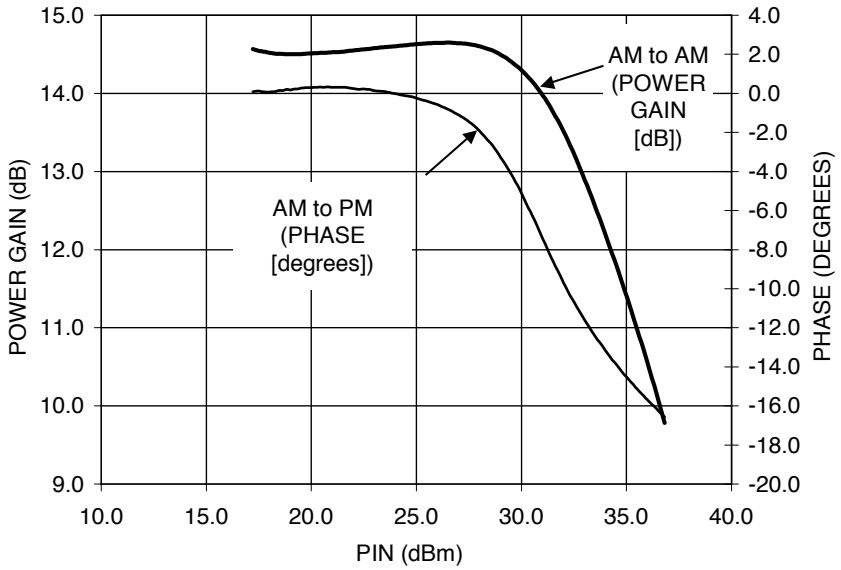
Typical Performance Characteristics (continued)



TEST CONDITIONS:
V_{DD} = 28 Vdc, F = 2140 MHz, I_{DQ} = 300 mA CW input.

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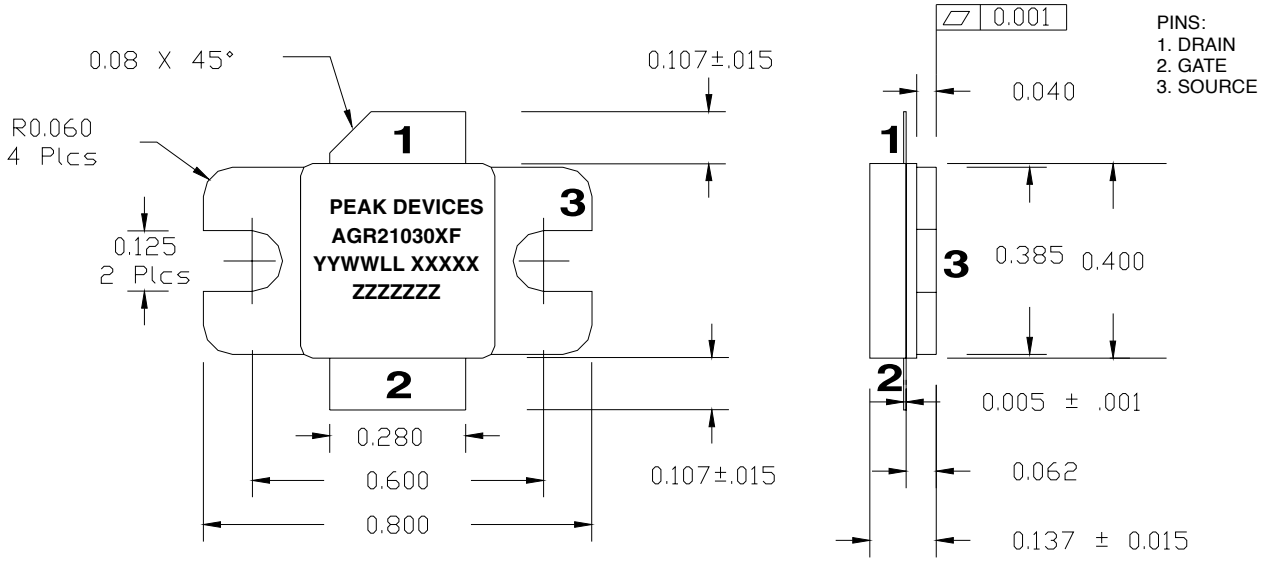

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