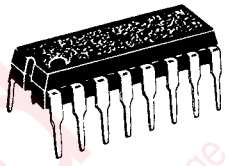
MN4018B/MN4018BS

Presettable divide-by-N Counter

■ Outline

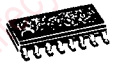
The MN4018B/S is a divide-by-N counter consisting of a 5-bit Johnson counter.
Connection of the outputs $\overline{O}_0 \sim \overline{O}_4$ with the D input enables frequency division respectively into ½, ¼, ⅙, ⅛, and 1/10.
Connection of the output $O_0 \sim O_4$ with the D input through the gate, on the other hand, enables frequency division respectively into ⅓, ⅕, 1/7, and 1/9.
MR and PL are asynchronous, and when MR="H", all the levels of $\overline{O}_n$ becomes NOT $\overline{P}_n$.
The counter advances by one state at the rise of the CP input. The lock preventive gate built-in in the couner assures suitable counter sequence selection.
This divide-by-N counter is equivalent to Motorola's MC14018B and RCA's CD4018B.

P-3



16-pin plastic DIL package

P-4



16-pin PANAFLAT package (SO-16D)

■ Truth Table

CP	MR	PL	$P_0 \sim P_4$	$\overline{O}_n$
↘	L	L	×	$\overline{O}_n$
↗	L	L	×	$\overline{D}_n$
×	L	H	L	H
×	L	H	H	L
×	H	×	×	H

Note) × : don't care

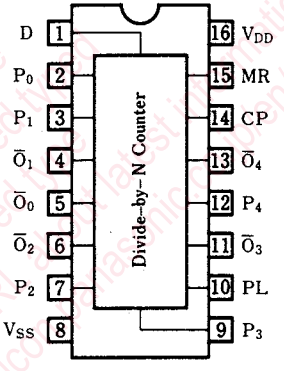
■ Function Selection Table

Number of dividing	Output to D	Notes
10 8 6 4 2	$\overline{O}_4$ $\overline{O}_3$ $\overline{O}_2$ $\overline{O}_1$ $\overline{O}_0$	External connection is not necessary.
9 7 5 3	$\overline{O}_3 \cdot \overline{O}_4$ $\overline{O}_2 \cdot \overline{O}_3$ $\overline{O}_1 \cdot \overline{O}_2$ $\overline{O}_0 \cdot \overline{O}_1$	AND gate is necessary in exterior.

Pin description

PL : Load input
$P_0 \sim P_4$: 4-bit input
D : Data input
CP : Clock input (↗)
MR : Rest input
$\overline{O}_0 \sim \overline{O}_4$: Output (4 bits)

Pin Configuration



■ Absolute Maximum Ratings (Ta=25°C)

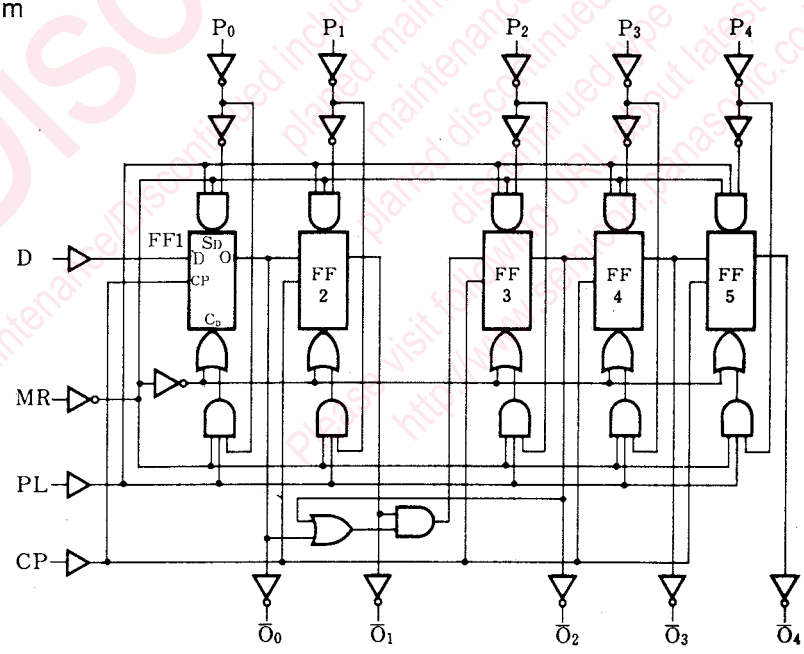
Item		Symbol	Rating	Unit
Supply voltage		V_{DD}	−0.5~+18	V
Input voltage		V_I	$-0.5 \sim V_{DD}+0.5$*	V
Output pin voltage		V_O	$-0.5 \sim V_{DD}+0.5$*	V
Peak input · output pin current		$\pm I_I$	max. 10	mA
Power dissipation (per package)	Ta=−40~+60°C	P_D	max. 400	mW
	Ta=+60~+80°C		Decrease to 200mW at the rate of 8mW/°C	
Power dissipation (per output pin)		P_D	max. 100	mW
Operating ambient temperature		T_{opr}	−40~+85	°C
Storage temperature		T_{stg}	−65~+150	°C

* V_{DD}+0.5V should be lower than 18V.

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Condition	Ta=−40°C min.	Ta=−40°C max.	Ta=25°C min.	Ta=25°C max.	Ta=85°C min.	Ta=85°C max.	Unit
Static supply current	5	I_{DD}	V_I=V_{SS} or V_{DD}	—	20	—	20	—	150	μA
	10			—	40	—	40	—	300	
	15			—	80	—	80	—	600	
Output voltage low level	5	V_{OL}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output voltage high level	5	V_{OH}	V_I=V_{SS} or V_{DD}, $\|I_O\|$<1μA	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input voltage low level	5	V_{IL}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10		V_O=1V or 9V	—	3	—	3	—	3	
	15		V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input voltage high level	5	V_{IH}	$\|I_O\|$<1μA, V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10		V_O=1V or 9V	7	—	7	—	7	—	
	15		V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output current low level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output current high level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V	0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V	1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V	3.6	—	3	—	2.4	—	
Output current high level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V	1.7	—	1.4	—	1.1	—	mA
Input leakage current	15	$\pm I_I$	V_I=0 or 15V	—	0.3	—	0.3	—	1	μA

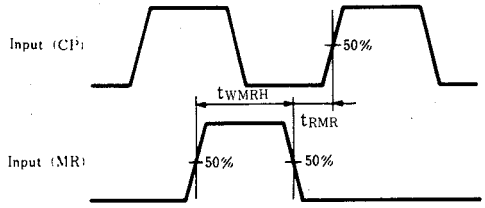
■ Logic Diagram



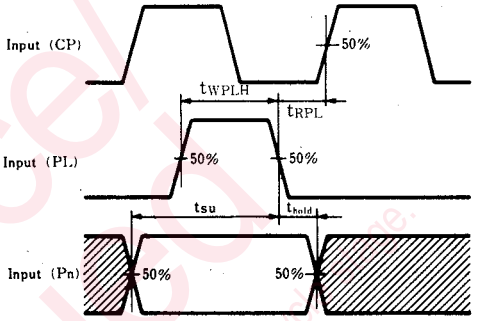
■ Switching Characteristics (Ta=25°C, V_{SS}=0V, C_l=50pF)

Item	V_{DD}(V)	Symbol	min.	typ.	max.	Unit
Output rise time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output fall time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation time CP→$\overline{O}$ (H→L)	5	t_{PHL}	—	185	555	ns
	10		—	65	195	
	15		—	50	150	
Propagation time CP→$\overline{O}$ (L→H)	5	t_{PLH}	—	145	435	ns
	10		—	55	165	
	15		—	40	120	
Propagation time PL→$\overline{O}$ (H→L)	5	t_{PHL}	—	205	615	ns
	10		—	70	210	
	15		—	50	150	
Propagation time PL→$\overline{O}$ (L→H)	5	t_{PLH}	—	175	525	ns
	10		—	65	195	
	15		—	50	150	
Propagation time MR→$\overline{O}$ (L→H)	5	t_{PLH}	—	140	420	ns
	10		—	55	165	
	15		—	40	120	
Set-up time D→CP	5	t_{su}	—	65	195	ns
	10		—	20	60	
	15		—	15	45	
Hold time D→CP	5	t_{hold}	—	−45	30	ns
	10		—	−15	10	
	15		—	−10	10	
Minimum clock pulse width	5	t_{WCPL}	—	70	210	ns
	10		—	25	75	
	15		—	20	60	
Minimum MR pulse width	5	t_{WMRH}	—	50	150	ns
	10		—	20	60	
	15		—	15	45	
Minimum PL pulse width	5	t_{WPLH}	—	75	225	ns
	10		—	25	75	
	15		—	20	60	
MR recovery time	5	t_{RMR}	—	70	210	ns
	10		—	20	60	
	15		—	15	45	
PL recovery time	5	t_{RPL}	—	85	255	ns
	10		—	30	90	
	15		—	20	60	
Maximum clock frequency	5	f_{max}	2	4	—	MHz
	10		6	11	—	
	15		8	16	—	
Input capacitance		C_I	—	—	7.5	pF

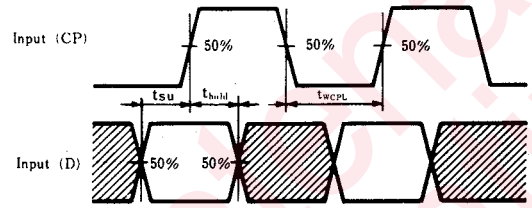
• Switching waveforms



Waveforms showing minimum MR pulse width and MR recovery time.

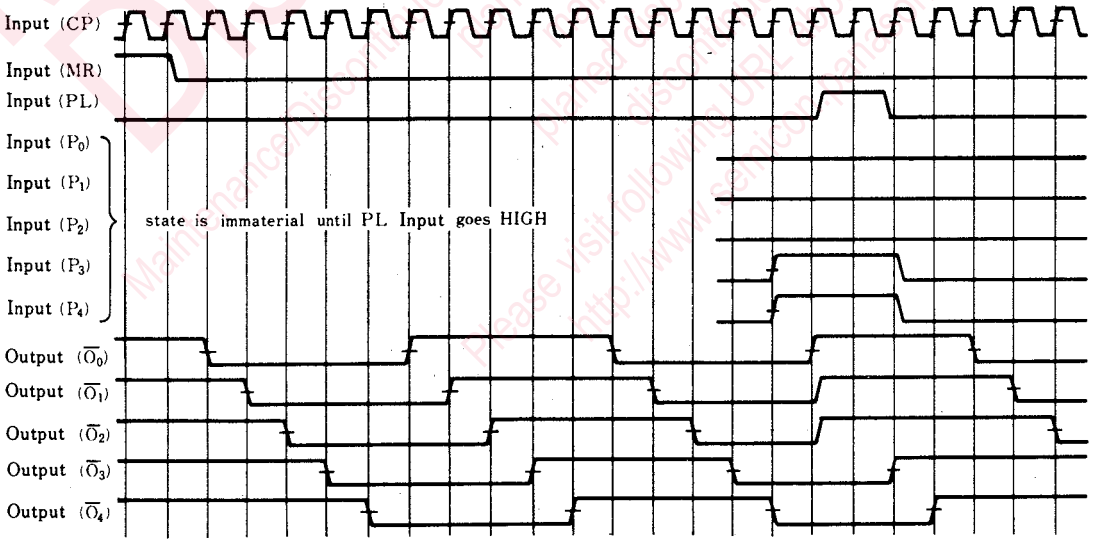


Waveforms showing minimum PL pulse width, recovery time for PL, and set-up and hold times for P_n to PL. Set-up and hold times are shown as positive values but may be specified as negative values.



Waveforms showing minimum clock pulse width, set-up time and hold time for CP and D.

■ Timing Diagram



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