8-Bit μp-compatible D/A converter | NE/SE5018/5019

DESCRIPTION

The NE/SE5018/19 is a complete 8-bit digital-to-analog converter subsystem on one monolithic chip. The data inputs have input latches which are controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal) and high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full-scale while maintaining a low temperature coefficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

FEATURES

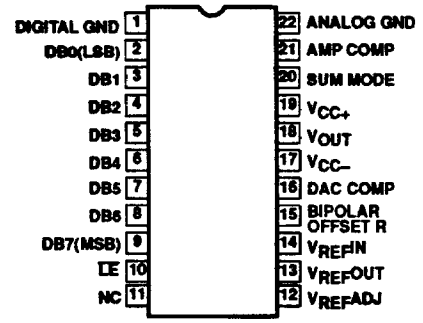
- 8-bit resolution
- Input latches
- Low-loading data inputs
- On-chip voltage reference
- Output buffer amplifier
- Accurate to ± LSB (0.19%)
- Monotonic to 8 bits
- Amplifier and reference both short-circuit protected
- Compatible with 8085, 6800 and many other μPs

APPLICATIONS

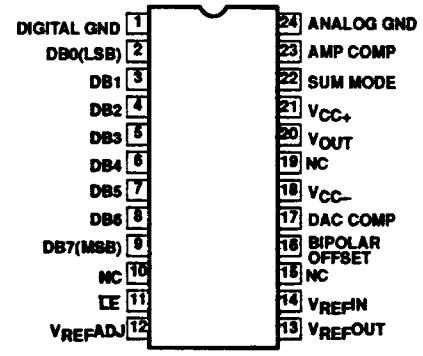
- Precision 8-bit D/A converters
- A/D converters
- Programmable power supplies
- Test equipment
- Measuring instruments
- Analog-digital multiplication

PIN CONFIGURATIONS

F, N Packages

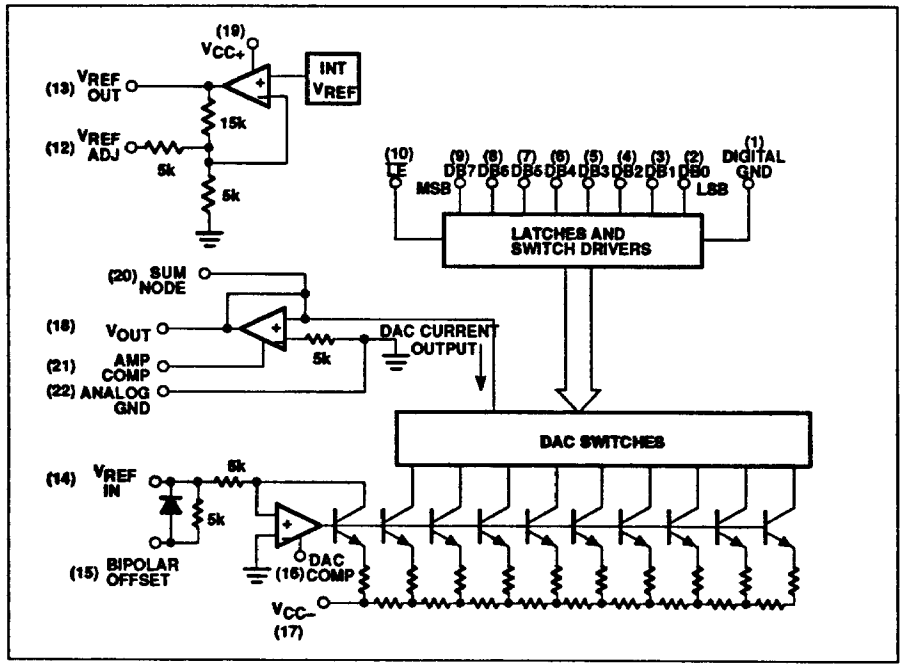


D Package[1]



NOTE:
1. SOL and non-standard pinout

BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
22-Pin Cerdip	0 to +70°C	NE5018/5019F
22-Pin Cerdip	-55°C to +125°C	SE5018/5019F
22-Pin Plastic DIP	0 to +70°C	NE5018/5019N
22-Pin Plastic DIP	-55°C to +125°C	SE5018/5019N
24-Pin SOL Package	0 to +70°C	NE5018/5019D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC+}	Positive supply voltage	18	V
V_{CC-}	Negative supply voltage	-18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF\ IN}$	Voltage at V_{REF} input	12	V
$V_{REF\ ADJ}$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
$I_{REF\ SC}$	Short-circuit current to ground at $V_{REF\ OUT}$	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Maximum power dissipation, T_A=25°C (still-air)[1]		
	F package	1740	mW
	N package	2190	mW
	D package	1600	mW
T_A	Operating temperature range		
	SE5018	-55 to +125	°C
	NE5018	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

NOTES:
1. Derate above 25°C at the following rates:
   F package at 13.9mW/°C
   N package at 17.5mW/°C
   D package at 12.8mW/°C

DC ELECTRICAL CHARACTERISTICS

V_{CC}+=+15V, V_{CC}-=-15V, SE5018. -55°C≤T_A≤125°C, NE5018. 0°C≤T_A≤70°C, unless otherwise specified. [1] Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SE5018			NE/SE5019			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.19			±0.1	%FS
V_{CC}+	Positive supply voltage		11.4	15		11.4	15		V
V_{CC}-	Negative supply voltage		-11.4	-15		-11.4	-15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1=0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1=0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1=0V, 2V<V_{IN}<18V		0.1	10		0.1	10	µA
$I_{IN(0)}$	Logic "0" input current	Pin 1=0V, -5V<V_{IN}<0.8V		-2.0	-10		-2.0	-10	µA
V_{FS}	Full-scale output	Unipolar mode, V_{REF}=5.000V, all bits high, T_A=25°C	9.50		10.5	9.50		10.5	V
+V_{FS}	Full-scale output	Bipolar mode, V_{REF}=5.000V all bits high, T_A=25°C	4.75		5.25	4.75		5.25	V
-V_{FS}	Negative full scale	Bipolar mode, V_{REF}=5.000V, all bits low, T_A=25°C	-5.25		-4.75	-5.25		-4.75	V
V_{ZS}	Zero-scale Output	Unipolar mode, V_{REF}=5.000V all bits low, T_A=25°C	-30		+30	-30		+30	mV
I_{OS}	Output short circuit current	T_A=25°C V_{OUT}=0V		15	40		15	40	mA
$PSR+_{(OUT)}$	Output power supply rejection (+)	V-=-15V, 13.5V≤V+≤16.5V, external $V_{REF\ IN}$=5.000V		0.001	0.01		0.001	0.01	%FS %VS
$PSR-_{(OUT)}$	Output power supply rejection (-)	V+=-15V, -13.5V≤V-≤-16.5V, external $V_{REF\ IN}$=5.000V		0.001	0.01		0.001	0.01	%FS %VS
TC_{FS}	Full-scale temperature coefficient	$V_{REF\ IN}$=5.000V		20			20		ppm/°C
TC_{ZS}	Zero-scale temperature coefficient			5			5		ppm/°C
I_{REF}	Reference output current				3			3	mA
I_{REFSC}	Reference short circuit current	T_A=25°C $V_{REF\ OUT}$=0V		15	30		15	30	mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	V-=-15V, 13.5V≤V+≤16.5V, I_{REF}=1.0mA		0.003	0.01		0.003	0.01	%VR/%VS
$PSR-_{(REF)}$	Reference power supply rejection (-)	V+=-15V, -13.5V≤V-≤16.5V,		0.003	0.01		0.003	0.01	%VR/%VS
V_{REF}	Reference voltage	I_{REF}=1.0mA T_A=25°C	4.9	5.0	5.25	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	I_{REF}=1.0mA		60			60		ppm/°C
Z_{IN}	DAC $V_{REF\ IN}$ input impedance	I_{REF}=1.0mA, T_A=25°C	4.15	5.0	5.85	4.15	5.0	5.85	kΩ
I_{CC}+	Positive supply current	V_{CC}+=15V		7	14		7	14	mA
I_{CC}-	Negative supply current	V_{CC}-=-15V		-10	-15		-10	-15	mA
P_D	Power dissipation	I_{REF}=1.0mA, V_{CC}=±15V		255	435		255	435	mW

NOTES:
1. Refer to Figure 1.

AC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = ±15V, T_A = 25°C

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	NE/SE5018/19			UNIT
					Min	Typ	Max	
t_{SLH}	Settling time	±1/2LSB	Input	All bits low-to-high[2]		1.8		µs
t_{SHL}	Settling time	±1/2LSB	Input	All bits high-to-low[3]		2.3		µs
t_{PLH}	Propagation delay	Output	Input	All bits switched low-to-high[2]		300		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched high-to-low[3]		150		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change[2, 3]		150		ns
t_{PLH}	Propagation delay	Output	$\overline{CE}$	Low-to-high transition[4]		300		ns
t_{PHL}	Propagation delay	Output	$\overline{CE}$	High-to-low transition[5]		150		ns
t_S	Setup time	$\overline{CE}$	Input	[1, 6]	100			ns
t_H	Hold time	Input	$\overline{CE}$	[1, 6]	50			ns
t_{PW}	Latch enable pulse width			[1, 6]	150			ns

NOTES:
1. Refer to Figure 2.
2. See Figure 5.
3. See Figure 6.
4. See Figure 7.
5. See Figure 8.
6. See Figure 9.
7. For reference currents>3mA, use of an external buffer is required.

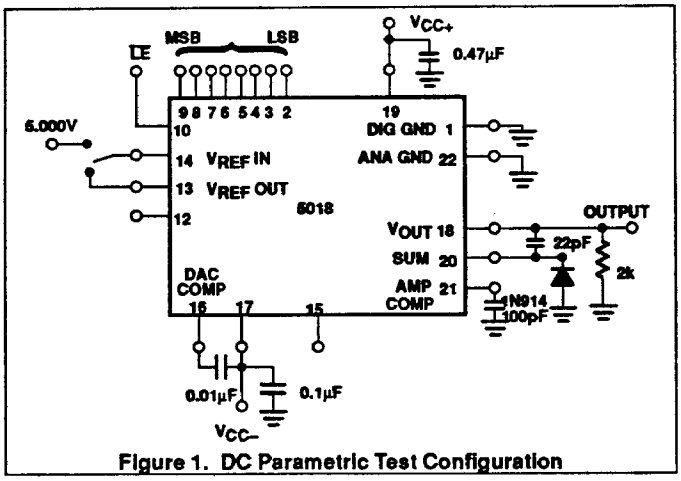


Figure 1. DC Parametric Test Configuration

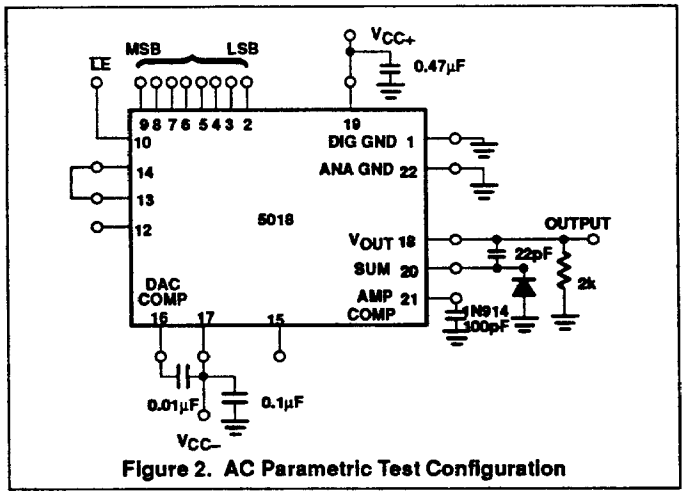


Figure 2. AC Parametric Test Configuration

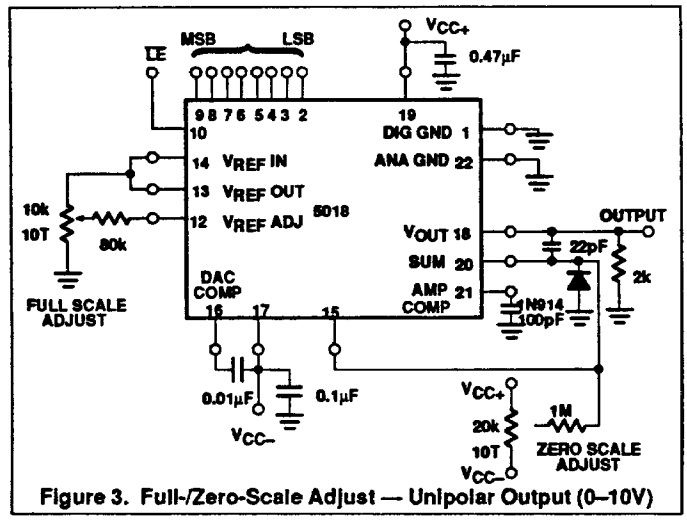


Figure 3. Full-/Zero-Scale Adjust — Unipolar Output (0–10V)

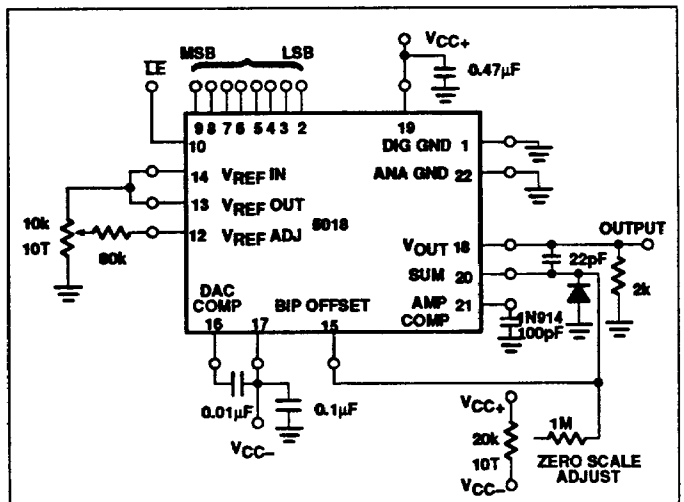


Figure 4. Bipolar Output Operation (–5 to +5V)

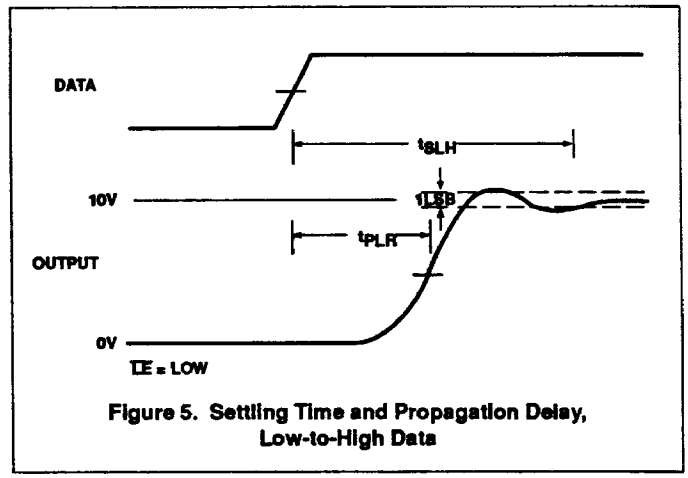


Figure 5. Settling Time and Propagation Delay, Low-to-High Data

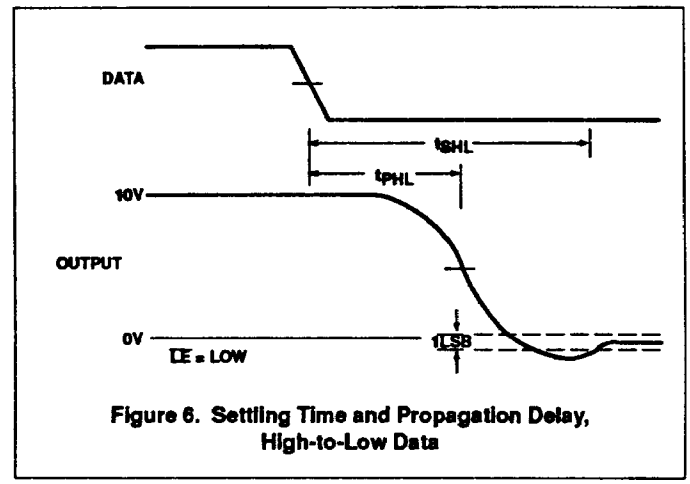


Figure 6. Settling Time and Propagation Delay, High-to-Low Data

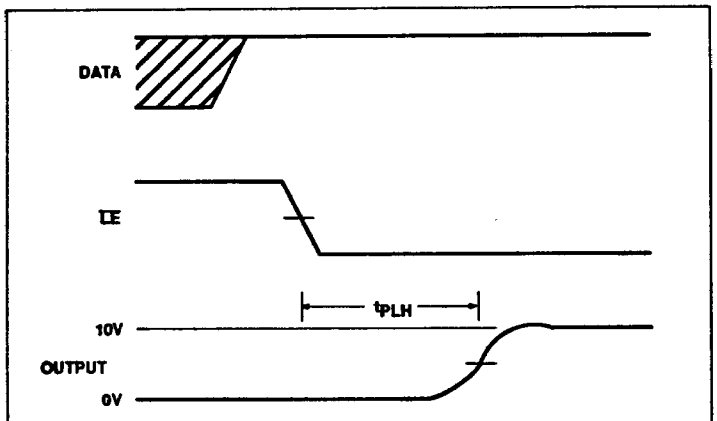


Figure 7. Propagation Delay, Latch Enable to Output

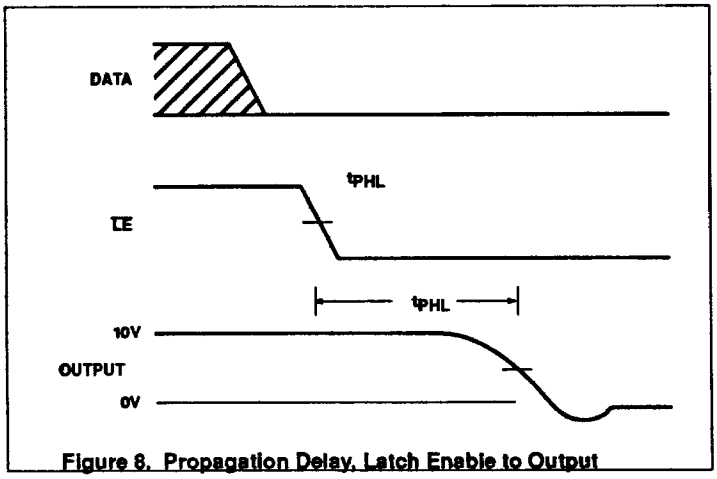


Figure 8. Propagation Delay, Latch Enable to Output

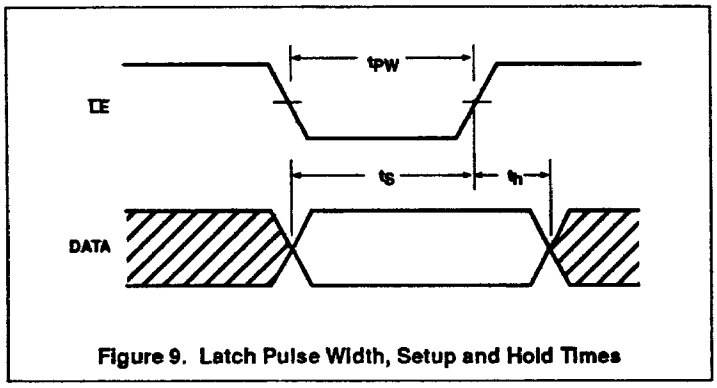


Figure 9. Latch Pulse Width, Setup and Hold Times

Signetics

Packaging Information

T-90-20

Military Products

SIGNETICS STANDARD PACKAGE DESCRIPTIONS

All Military package case outlines and physical dimensions conform with the current revision MIL-M-38510, Appendix C, except for package types which are not included in that specification.

The physical dimensions for standard package types which are not included in Appendix C are included herein in Appendix C format. Case outline letters are assigned to these packages according to JEDEC Publication 101 as follows:

- U: Leadless chip carriers
- X: Dual-in-line packages
- Y: Flat packages
- Z: All other configurations

A case outline suffix number is assigned herein for identification purposes only, and is not marked on the product.

Signetics Military products are offered in a wide range of package configurations to optimally fit our customer needs.

- Dual-in-line Packages; Frit glass sealed CERDIP (F package family) with 8-40 leads, and side-brazed ceramic (I package family) with 48-64 leads.
- Flat Packages; Frit glass sealed alumina CERPAC (W package family) with 14-28 leads, and brazed leaded ceramic (Q package family) with 52 leads.
- Ceramic Chip Carriers; triple laminated, metal-lidded LCC (G package family) with 20-68 terminals.
- Pin Grid Array; metal-lidded ceramic pin grid (P package family) with 68-100 leads.
- Shown in Table 1 are the case outline letters assigned according to Appendix C of MIL-M-38510 and JEDEC publication 101. Unless otherwise noted, all package types are Configuration 1 and all lead finishes are hot solder dip Finish "A".

Table 1.

Package Description	Type Designation	Case Outline	Theta-JC °C/Watt[4]
8DIP3	D-4	P	28
14DIP3	D-1	C	28
16DIP3	D-2	E	28
18DIP3	D-6	V	28
20DIP3	D-8	R	28
22DIP4	D-7	W	28
24DIP3	D-9	L	28
24DIP4	D-11	X[2]	28
24DIP6	D-3	J	28
28DIP6	D-10	X[2]	28
40DIP6	D-5	Q	28
48DIP6	D-14[1]	X[2]	28
50DIP9	D-12[1]	X[2]	28
64DIP9	D-13[1]	X[2]	28
14FLAT	F-2	D	22
16FLAT	F-5	F	22
18FLAT	F-10	Y[2]	22
20FLAT	F-9	S	22
24FLAT	F-6	K	22
28FLAT	F-11	Y[2]	22
52FLAT	Y-1[1]	Y[2]	22
18LLCC	C-9	U[2]	20
20LLCC	C-2[3]	2	20
28LLCC	C-4[3]	3	20
32LLCC	C-12	U[2]	20
44LLCC	C-5	U[2]	20
68LLCC	C-7	U[2]	20
68PGA	P-AB	Z[2]	20
84PGA	P-AB	Z[2]	20

NOTES:
1. Configuration 2.
2. Per JEDEC publication 101.
3. Dimension A (LLCC thickness) is 75mils maximum.
4. See RADC test report RADC-TR-86-97 for thermal resistance confidence and derating.

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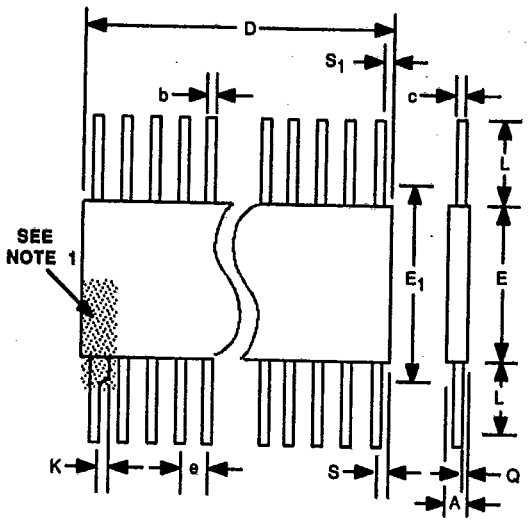
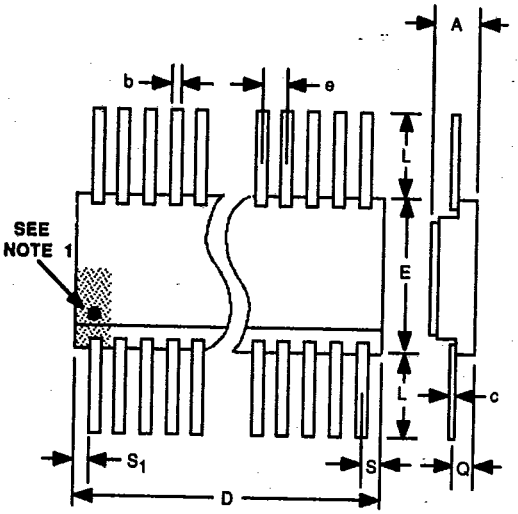
Packaging Information

CASE OUTLINES Y (FLAT PACKAGES)



Configuration 1



Configuration 2

NOTES:

1. A lead tab (enlargement) or index dot is located within the shaded area shown at Pin 1. Other pin numbers proceed sequentially from Pin 1 counterclockwise (as viewed from the top of the device).
2. This dimension allows for off-center lid, meniscus, and glass overrun.
3. The reference pin spacing is 0.050 between centerlines. Each pin centerline is located within ± 0.005 of its logitudinal position relative to the first and last pin numbers.
4. This dimension is measured at the point of exit of the lead body.
5. This dimension applied to all four corner pins.
6. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

OUTLINE	Y1		NOTES
CONFIGURATION	2		
NO. LEADS	52		
SIG. PKG.	QP		
SYMBOL	INCHES		
	Min	Max	
A	0.045	0.100	
b	0.015	0.026	6
c	0.008	0.015	6
D	- -	1.330	2
E	0.620	0.660	
e	0.050 BSC		3
L	0.250	0.370	
Q	0.054	0.0666	4
S	-	0.045	5
S1	0.005	-	5

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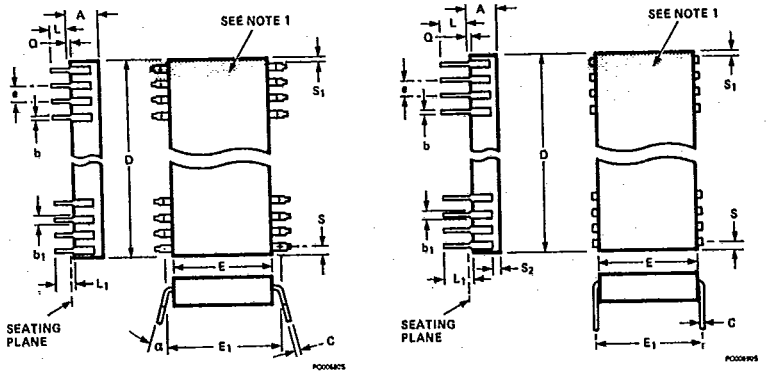
Packaging Information

CASE OUTLINES X (DUAL IN-LINE PACKAGES)



Configuration 1 Configuration 2

1. An index notch is located within the shaded area shown. Pin 1 is adjacent to the notch to the immediate left (as viewed from the top of the device) and other pin numbers proceed sequentially from Pin 1 counterclockwise.
2. The minimum limit for Dimension b1 is 0.023 inches for all four corner pins.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. This dimension is measured at the centerline of the leads for Configuration 2.
5. The reference pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its longitudinal position relative to the first and last pin numbers.
6. This dimension is measured from the seating plane to the base plane.
7. This dimension applies to all four corner pins.
8. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

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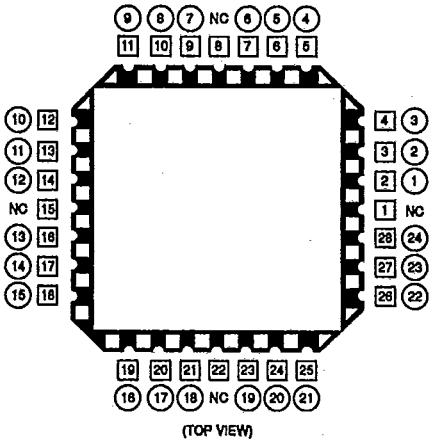
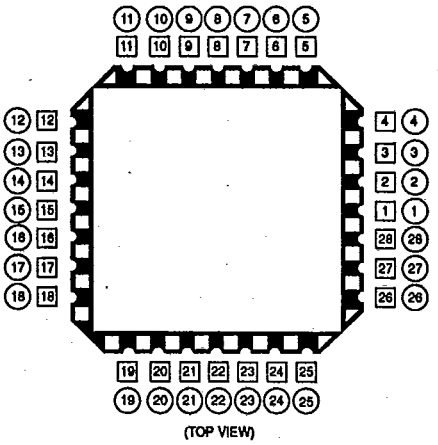
Packaging Information

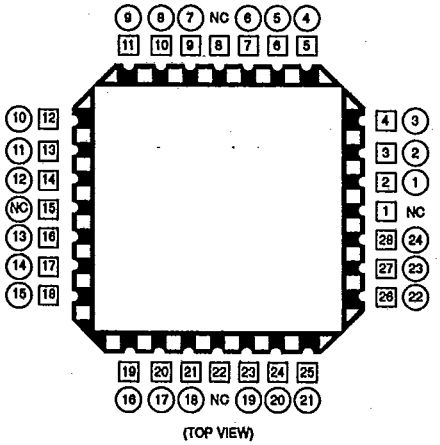
LEADLESS CHIP CARRIER (LLCC) PINOUTS



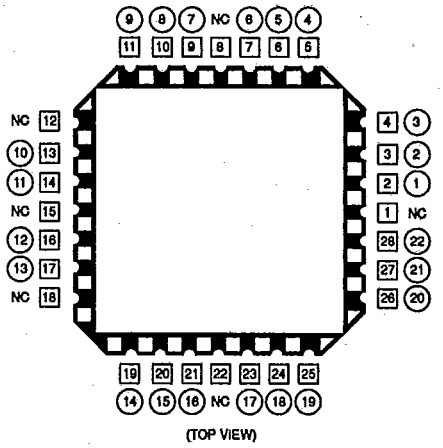
24–Lead Logic Pinout for 28 Terminal Chip Carrier



26–Lead Pinout for 28 Terminal Chip Carrier for all Device Types



24–Lead Memory Pinout for 28 Terminal Chip Carrier



22–Lead Memory Pinout for 28 Terminal Chip Carrier

□ = Chip Carrier Terminal Number
○ = Dual In-Line Lead Number
NC = No Connect