PRELIMINARY

Am53C974A

PCscsi™ II
Bus Mastering Fast SCSI Controller for PCI Systems

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

PCI Features

- Compatible with PCI Specification Revision 2.0
- Direct glueless interface to 33 MHz, 32-bit PCI bus
- Bus Mastering DMA engine (32-bit address/data)
- 132 Mbyte/s burst DMA transfer rate
- Support for Scatter-Gather DMA data transfers
- 96-byte DMA FIFO for low bus latency

SCSI Features

- Fast 8-bit SCSI-2 10 Mbyte/s synchronous or 7 Mbyte/s asynchronous data transfer rate
- Boot ROM support
- Level 1 SCAM support
- On-chip state machine to control the SCSI sequences in hardware
- Patented programmable GLITCH EATER™ Circuitry on $\overline{REQ}$ and $\overline{ACK}$ inputs
- Programmable Active Negation on $\overline{REQ}$, $\overline{ACK}$ and data outputs
- Target Command Set support
- Single-Ended 48 mA outputs to drive the SCSI bus directly

General Features

- Complete software driver support for all major PC operating systems
- Plug-in and software compatible with AMD's PCI product family of SCSI and Ethernet controllers
- Hooks in silicon and software to enable disk drive spin down for power savings
- Fully static design for low frequency and low power operation
- 132-pin PQFP package
- State of the art submicron CMOS process technology

GENERAL DESCRIPTION

The Am53C974A, PCscsi II, is AMD's second generation high-performance Fast SCSI controller with a glueless interface to the PCI local bus. As such, the Am53C974A is a functional superset of the original PCscsi II (Am53C974) device and offers several new features and enhancements for a more complete system solution. The Am53C974A integrates a 32-bit bus mastering DMA engine with an industry standard Fast SCSI-2 block. The DMA engine and accompanying 96 byte DMA FIFO allow 32-bit burst data transfers across the high bandwidth PCI bus at speeds of up to 132 Mbyte/s. Full support for scatter-gather DMA transfers optimize performance in multi-tasking system applications.

The Am53C974A's on-chip state machine controls SCSI bus sequences in hardware and is coupled with the bus mastering DMA engine to eliminate the need for an on-chip RISC processor. For more detailed information refer to the technical manual, PID #18264B.

AMD supports the Am53C974A with a total system solution which includes:

- A full suite of licensable SCSI drivers and utilities fully tested under the following operating system environments:

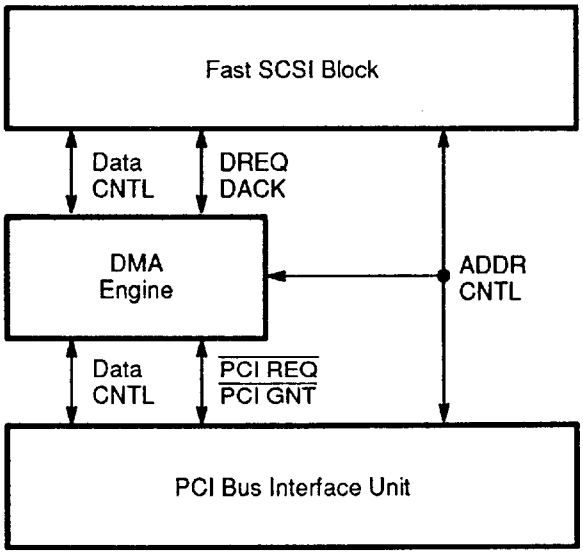
  DOS 5.0 – 6.x
  Windows 3.1x
  Windows NT
  OS/2 2.x
  Netware 3.x, 4.x
  SCO Unix 3.2.4, ODT 3.0

- An INT13h Compatible SCSI ROM BIOS
- ASPI Compatibility
- Complete hardware reference design kit

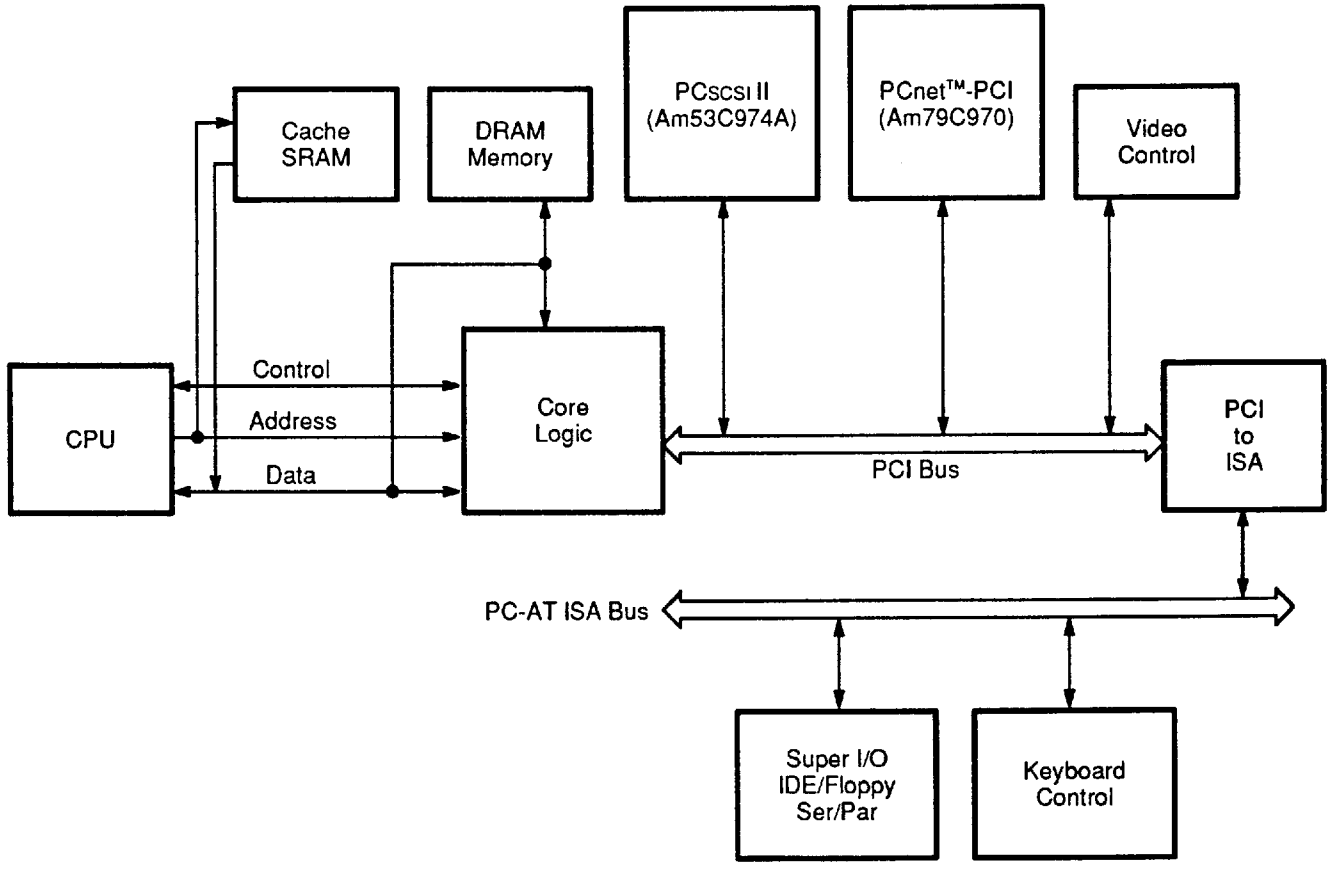
The Am53C974A is part of AMD's PCI product family of plug-in and software compatible SCSI and Ethernet controllers. This product compatibility ensures a low cost system upgrade path and lower motherboard manufacturing costs.

Publication# 19084 Rev. A Amendment/0
Issue Date: June 1994

BLOCK DIAGRAM



19084A-1



19084A-2

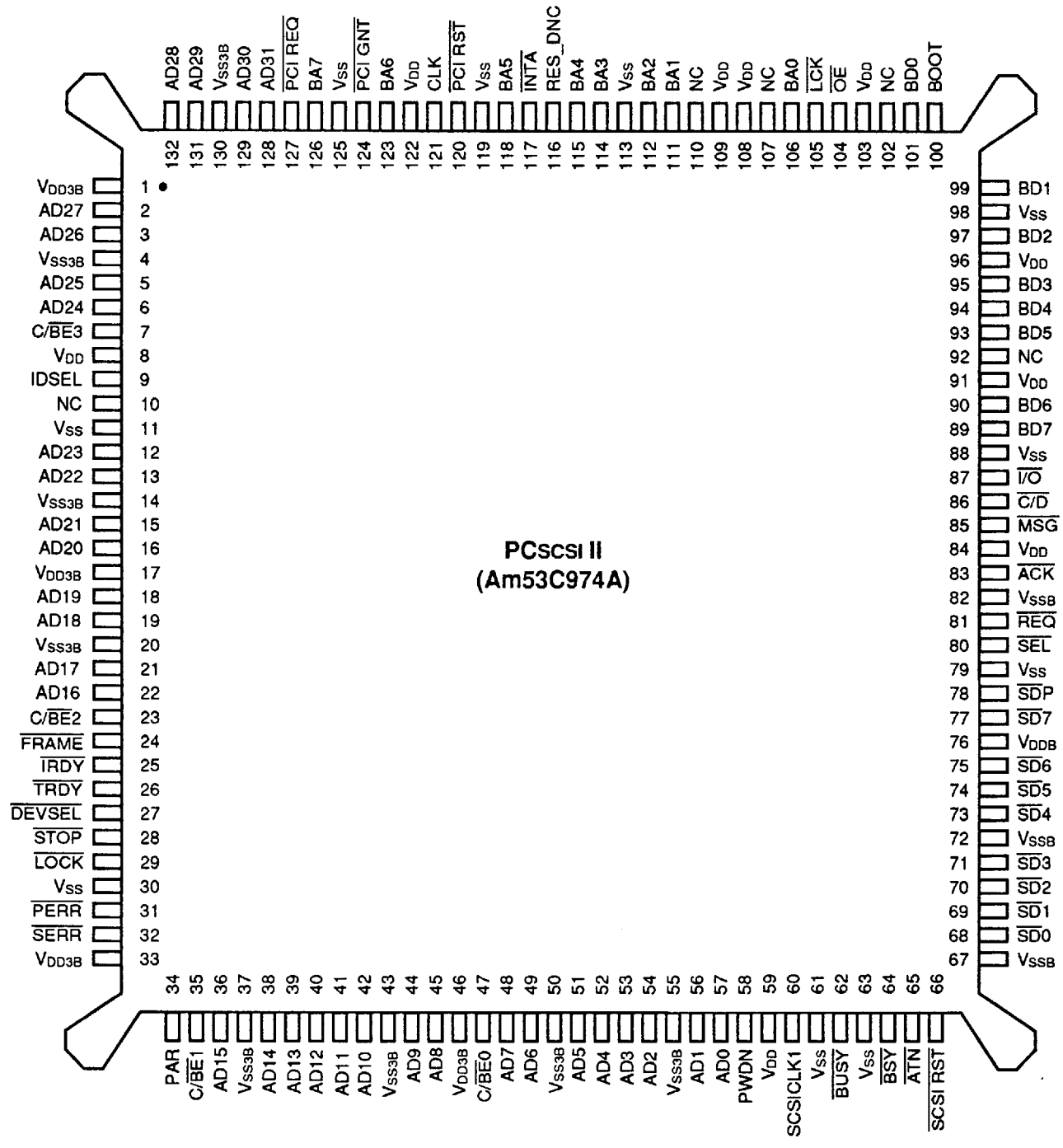
Am53C974A in a PCI System

RELATED AMD PRODUCTS

Part No.	Description
Am33C93A	Synchronous SCSI Controller
Am386®	High-Performance 32-Bit Microprocessor
Am486™	High-Performance 32-Bit Microprocessor
Am53C94/96	High-Performance SCSI Controller
Am53CF94/96	Enhanced Fast SCSI-2 Controller
Am53C974	PCscsi Bus Mastering Fast SCSI Controller for PCI Systems
Am79C960	PCnet-ISA Single-Chip Ethernet Controller
Am79C961	PCnet-ISA+ Single-Chip Ethernet Controller
Am79C965	PCnet-32 Single-Chip 32-Bit Ethernet Controller
Am79C970	PCnet-PCI Single-Chip Ethernet Controller for PCI Local Bus
Am79C974	PCnet-SCSI Combination Ethernet and SCSI Controller for PCI Systems
Am85C30	Enhanced Serial Communication Controller

CONNECTION DIAGRAM

Top View



19084A-3

Notes:

Pin 1 is marked for orientation.

NC = Not connected; connection of an NC pin may cause a malfunction or incompatibility with other products.

RES_DNC = Reserved_DO NOT CONNECT.

QUICK REFERENCE PIN DESCRIPTIONS

Pin Name	Pin Type	Description
PCI		
AD [31:00]	IN/OUT	Address/Data Bus
C/$\overline{BE}$ [3:0]	IN/OUT	Command/Byte Enable signals
PAR	IN/OUT	Parity Signal
$\overline{FRAME}$	IN/OUT	Cycle Frame
$\overline{TRDY}$	IN/OUT	Target Ready
$\overline{IRDY}$	IN/OUT	Initiator Ready
$\overline{STOP}$	IN/OUT	Stop
$\overline{LOCK}$	IN/OUT	Lock
IDSEL	IN	Initialization Device Select
$\overline{DEVSEL}$	IN/OUT	Device Select
$\overline{PCI\ REQ}$	OUT	PCI Request
$\overline{PCI\ GNT}$	IN	PCI Grant
CLK	IN	PCI Clock
$\overline{PCI\ RST}$	IN	PCI Reset
$\overline{PERR}$	IN/OUT	Parity Error
$\overline{SERR}$	OUT	System Error
$\overline{INTA}$	OUT	Interrupt
SCSI Interface		
$\overline{SD}$ [7:0]	IN/OUT	SCSI Data
$\overline{SDP}$	IN/OUT	SCSI Data Parity
$\overline{MSG}$	IN/OUT	Message
$\overline{C/D}$	IN/OUT	Command/Data
$\overline{I/O}$	IN/OUT	Input/Output
$\overline{ATN}$	IN/OUT	Attention
$\overline{BSY}$	IN/OUT	Busy
$\overline{SEL}$	IN/OUT	Select
$\overline{SCSI\ RST}$	IN/OUT	SCSI Bus Reset
$\overline{REQ}$	IN/OUT	Request
$\overline{ACK}$	IN/OUT	Acknowledge
Boot ROM Interface		
BOOT	IN	Boot ROM Enable
BA [7:0]	OUT	Boot ROM Address
BD [7:0]	IN	Boot ROM Data
$\overline{OE}$	OUT	ROM Output Enable
$\overline{LCK}$	OUT	High Address Byte Latch Clock
Miscellaneous		
SCSI CLK1	IN	SCSI Core Clock
RES_DNC	IN	Reserved, DO NOT CONNECT
Power Management		
PWDN	IN	Power Down Indicator
$\overline{BUSY}$	OUT	SCSI Bus Activity Pin
Power Supply		
V_{DD}	+5 V	
V_{SS}	GND	
V_{DDB}	+5 V (Buffer)	
V_{SSB}	GND (Buffer)	
V_{DD3B}	+5 V (PCI)	
V_{SS3B}	GND (5 V PCI)	

PQFP PIN DESIGNATIONS

Listed by Pin Number

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{DD3B}	34	PAR	67	V_{SSB}	100	BOOT
2	AD27	35	C/$\overline{BE1}$	68	$\overline{SD0}$	101	BD0
3	AD26	36	AD15	69	$\overline{SD1}$	102	NC
4	V_{SS3B}	37	V_{SS3B}	70	$\overline{SD2}$	103	V_{DD}
5	AD25	38	AD14	71	$\overline{SD3}$	104	$\overline{OE}$
6	AD24	39	AD13	72	V_{SSB}	105	$\overline{LCK}$
7	C/$\overline{BE3}$	40	AD12	73	$\overline{SD4}$	106	BA0
8	V_{DD}	41	AD11	74	$\overline{SD5}$	107	NC
9	IDSEL	42	AD10	75	$\overline{SD6}$	108	V_{DD}
10	NC	43	V_{SS3B}	76	V_{DDB}	109	V_{DD}
11	V_{SS}	44	AD9	77	$\overline{SD7}$	110	NC
12	AD23	45	AD8	78	$\overline{SDP}$	111	BA1
13	AD22	46	V_{DD3B}	79	V_{SS}	112	BA2
14	V_{SS3B}	47	C/$\overline{BE0}$	80	$\overline{SEL}$	113	V_{SS}
15	AD21	48	AD7	81	$\overline{REQ}$	114	BA3
16	AD20	49	AD6	82	V_{SSB}	115	BA4
17	V_{DD3B}	50	V_{SS3B}	83	$\overline{ACK}$	116	RES_DNC
18	AD19	51	AD5	84	V_{DD}	117	$\overline{INTA}$
19	AD18	52	AD4	85	$\overline{MSG}$	118	BA5
20	V_{SS3B}	53	AD3	86	$\overline{C/D}$	119	V_{SS}
21	AD17	54	AD2	87	$\overline{I/O}$	120	$\overline{PCI\ RST}$
22	AD16	55	V_{SS3B}	88	V_{SS}	121	CLK
23	C/$\overline{BE2}$	56	AD1	89	BD7	122	V_{DD}
24	$\overline{FRAME}$	57	AD0	90	BD6	123	BA6
25	$\overline{IRDY}$	58	PWDN	91	V_{DD}	124	$\overline{PCI\ GNT}$
26	$\overline{TRDY}$	59	V_{DD}	92	NC	125	V_{SS}
27	$\overline{DEVSEL}$	60	SCSICLK1	93	BD5	126	BA7
28	$\overline{STOP}$	61	V_{SS}	94	BD4	127	$\overline{PCI\ REQ}$
29	$\overline{LOCK}$	62	$\overline{BUSY}$	95	BD3	128	AD31
30	V_{SS}	63	V_{SS}	96	V_{DD}	129	AD30
31	$\overline{PERR}$	64	$\overline{BSY}$	97	BD2	130	V_{SS3B}
32	$\overline{SERR}$	65	$\overline{ATN}$	98	V_{SS}	131	AD29
33	V_{DD3B}	66	$\overline{SCSI\ RST}$	99	BD1	132	AD28

NC = No Connect

RES_DNC = Reserved_DO NOT CONNECT.

PQFP PIN DESIGNATIONS

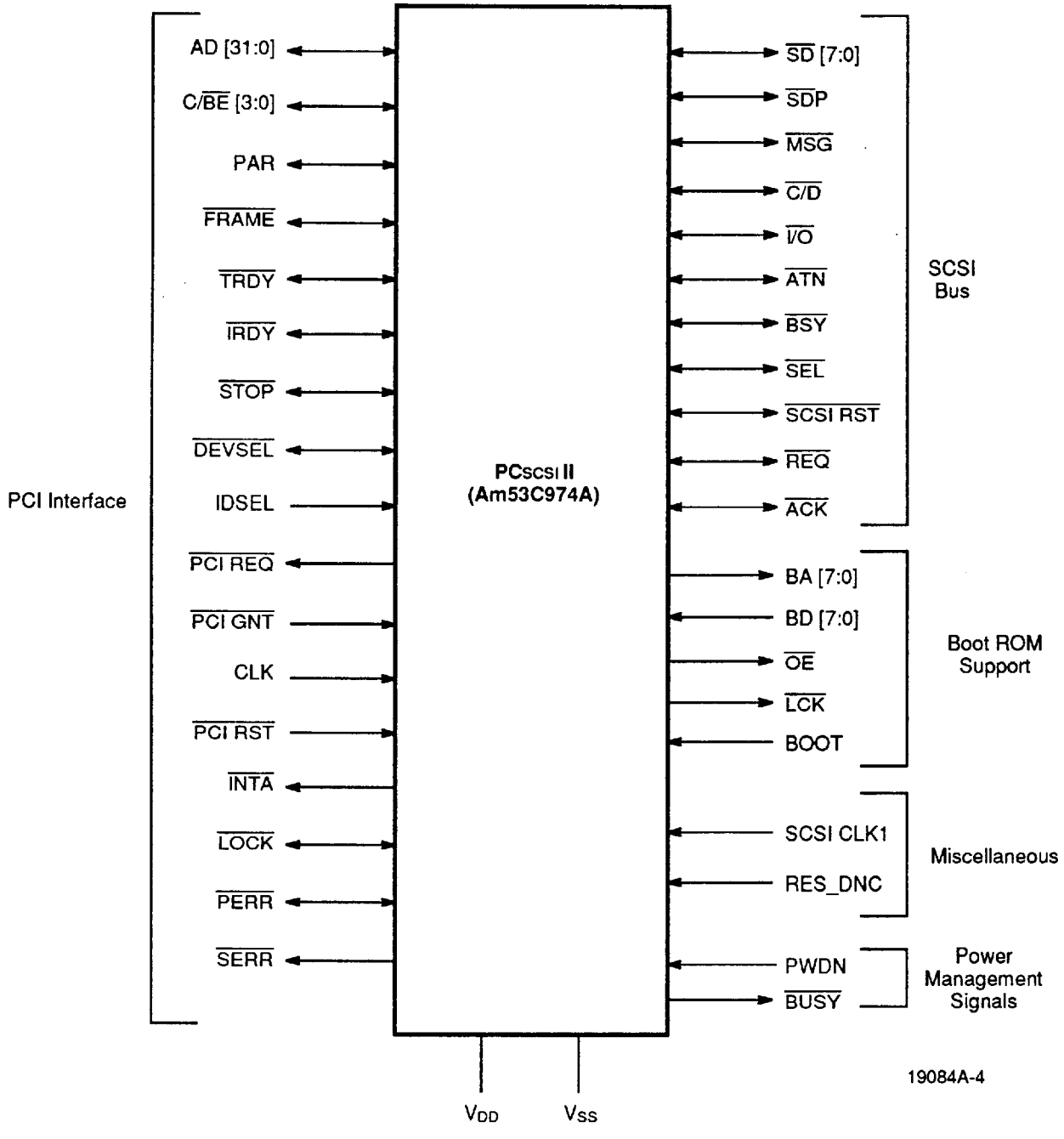
Listed by Pin Name

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
$\overline{ACK}$	83	$\overline{ATN}$	65	$\overline{LOCK}$	29	V_{DD}	84
AD0	57	BA0	106	$\overline{MSG}$	85	V_{DD}	91
AD1	56	BA1	111	NC	10	V_{DD}	96
AD2	54	BA2	112	NC	92	V_{DD}	103
AD3	53	BA3	114	NC	102	V_{DD}	108
AD4	52	BA4	115	NC	107	V_{DD}	109
AD5	51	BA5	118	NC	110	V_{DD}	122
AD6	49	BA6	123	$\overline{OE}$	104	V_{DD3B}	1
AD7	48	BA7	126	PAR	34	V_{DD3B}	17
AD8	45	BD0	101	$\overline{PCI\ GNT}$	124	V_{DD3B}	33
AD9	44	BD1	99	$\overline{PCI\ REQ}$	127	V_{DD3B}	46
AD10	42	BD2	97	$\overline{PCI\ RST}$	120	V_{DDB}	76
AD11	41	BD3	95	$\overline{PERR}$	31	V_{SS}	11
AD12	40	BD4	94	PWDN	58	V_{SS}	30
AD13	39	BD5	93	$\overline{REQ}$	81	V_{SS}	61
AD14	38	BD6	90	RES_DNC	116	V_{SS}	63
AD15	36	BD7	89	$\overline{SCSI\ RST}$	66	V_{SS}	79
AD16	22	BOOT	100	SCSICLK1	60	V_{SS}	88
AD17	21	$\overline{BSY}$	64	$\overline{SD0}$	68	V_{SS}	98
AD18	19	$\overline{BUSY}$	62	$\overline{SD1}$	69	V_{SS}	113
AD19	18	C/$\overline{BE0}$	47	$\overline{SD2}$	70	V_{SS}	119
AD20	16	C/$\overline{BE1}$	35	$\overline{SD3}$	71	V_{SS}	125
AD21	15	C/$\overline{BE2}$	23	$\overline{SD4}$	73	V_{SS3B}	4
AD22	13	C/$\overline{BE3}$	7	$\overline{SD5}$	74	V_{SS3B}	14
AD23	12	$\overline{C/D}$	86	$\overline{SD6}$	75	V_{SS3B}	20
AD24	6	CLK	121	$\overline{SD7}$	77	V_{SS3B}	37
AD25	5	$\overline{DEVSEL}$	27	$\overline{SDP}$	78	V_{SS3B}	43
AD26	3	$\overline{FRAME}$	24	$\overline{SEL}$	80	V_{SS3B}	50
AD27	2	$\overline{I/O}$	87	$\overline{SERR}$	32	V_{SS3B}	55
AD28	132	IDSEL	9	$\overline{STOP}$	28	V_{SS3B}	130
AD29	131	$\overline{INTA}$	117	$\overline{TRDY}$	26	V_{SSB}	67
AD30	129	$\overline{IRDY}$	25	V_{DD}	8	V_{SSB}	72
AD31	128	$\overline{LCK}$	105	V_{DD}	59	V_{SSB}	82

NC = No Connect

RES_DNC = Reserved_DO NOT CONNECT.

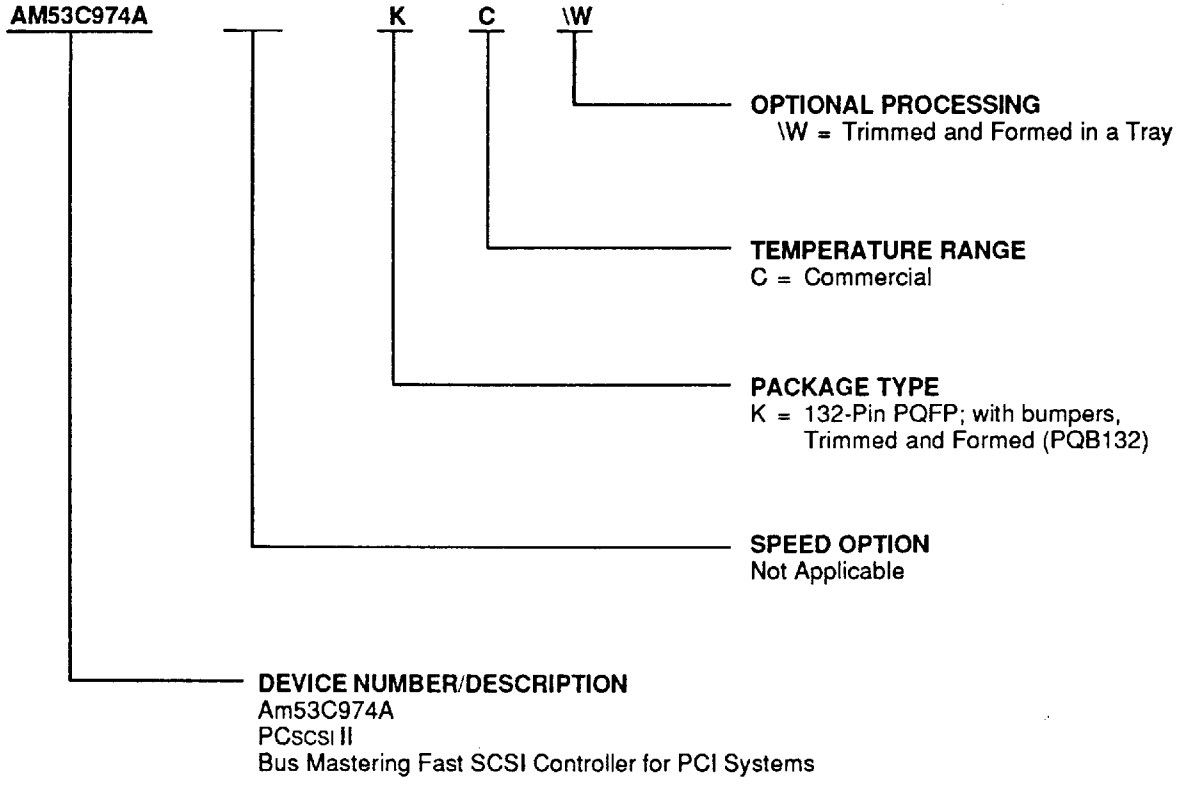
LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
Am53C974A	KC\W

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

DETAILED PIN DESCRIPTION

PCI Bus Interface Signals

The Am53C974A is PCI compliant. The following pin descriptions have been taken from the PCI specification. For more details, refer to the PCI specification Rev. 2.0.

Address and Data Pins

AD [31:00]

Address/Data
(Input/Output, Active High)
Address and Data are multiplexed on the same PCI pins. During the first clock of a transaction the AD [31:00] contains the physical address (32 bits). During the subsequent clocks AD [31:00] may contain valid data. Valid data is transferred during the clocks when $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are both asserted. Little-endian byte ordering is used. AD [07:00] is defined as least significant byte and AD [31:24] is defined as the most significant byte.

When $\overline{\text{PCI RST}}$ is active, AD [31:00] are inputs for NAND tree testing.

C/$\overline{\text{BE}}$ [3:0]

Bus Command/Byte Enable
(Input/Output, Active Low)
Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of the transaction, C/$\overline{\text{BE}}$ [3:0] define the bus command. During the data phase C/$\overline{\text{BE}}$ [3:0] are used as Byte Enables. The Byte Enables define which byte lanes carry meaningful data. C/$\overline{\text{BE}}$ [0] applies to byte 0 (LSB) and C/$\overline{\text{BE}}$ [3] applies to byte 3 (MSB).

When $\overline{\text{PCI RST}}$ is active, C/$\overline{\text{BE}}$ [3:0] are inputs for NAND tree testing.

PAR

Parity
(Input/Output, Active High)
Parity is even across AD[31:00] and C/$\overline{\text{BE}}$[3:0]. Parity is generated and driven during Master Address Cycle, Memory Write, I/O Read, and Configuration Read cycles. Parity is checked during Slave Address Cycle, Memory Read, I/O Write, and Configuration Write cycles.

When $\overline{\text{PCI RST}}$ is active, PAR is an input for NAND tree testing.

Interface Control Pins

$\overline{\text{FRAME}}$

Cycle Frame
(Input/Output, Active Low)
This signal is driven by the Am53C974A when it is the bus master to indicate the beginning and duration of the access. $\overline{\text{FRAME}}$ is asserted to indicate that a bus transaction is beginning. $\overline{\text{FRAME}}$ is asserted while data transfers continue. $\overline{\text{FRAME}}$ is deasserted when the transaction is in the final data phase.

When $\overline{\text{PCI RST}}$ is active, $\overline{\text{FRAME}}$ is an input for NAND tree testing.

$\overline{\text{TRDY}}$

Target Ready
(Input/Output, Active Low)
When the Am53C974A is selected as a slave, it will drive (low) this signal to indicate its ability to complete the current data phase of the transaction. As a master, this signal is an input to the Am53C974A from the selected (slave) device.

$\overline{\text{TRDY}}$ is used in conjunction with $\overline{\text{IRDY}}$ to indicate completion of the data phase. The data phase is complete (on any clock) when both $\overline{\text{TRDY}}$ and $\overline{\text{IRDY}}$ are sampled asserted. During a read transaction, $\overline{\text{TRDY}}$ is asserted when valid data is present on AD [31:00], while during a write transaction, $\overline{\text{TRDY}}$ asserted indicates the target is prepared to accept data. Wait cycles are inserted until both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are asserted together.

When $\overline{\text{PCI RST}}$ is active, $\overline{\text{TRDY}}$ is an input for NAND tree testing.

$\overline{\text{IRDY}}$

Initiator Ready
(Input/Output, Active Low)
When the Am53C974A is the initiator (master), it will drive (low) this signal to indicate its ability to complete the current data phase of the transaction. As a slave, this signal is an input to the Am53C974A from the initiating (master) device.

$\overline{\text{IRDY}}$ is used in conjunction with $\overline{\text{TRDY}}$ to indicate completion of the data phase. The data phase is complete (on any clock) when both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are sampled when asserted. During a read transaction, $\overline{\text{IRDY}}$ asserted indicates the master is prepared to accept data, while during a write transaction, $\overline{\text{IRDY}}$ is asserted to indicate that valid data is present on AD [31:00]. Wait cycles are inserted until both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are asserted together.

When $\overline{\text{PCI RST}}$ is active, $\overline{\text{IRDY}}$ is an input for NAND tree testing.

$\overline{\text{STOP}}$

Stop
(Input/Output, Active Low)
In the slave role the Am53C974A drives the $\overline{\text{STOP}}$ signal to indicate to the bus master to stop the current transaction. In the bus master role the Am53C974A receives the $\overline{\text{STOP}}$ signal and stops the current transaction.

When $\overline{\text{PCI RST}}$ is active, $\overline{\text{STOP}}$ is an input for NAND tree testing.

LOCK

Lock
(Input/Output, Active Low)
In the master role the Am53C974A drives the LOCK signal to indicate to the slave device that multiple transactions may be necessary to complete an operation. When LOCK is asserted, non-exclusive transactions may proceed. Control of LOCK is obtained under its own protocol in conjunction with GNT. In the slave role the Am53C974A receives the LOCK signal from the master.

When PCI RST is active, LOCK is an input for NAND tree testing.

Note: *In the current implementation, the Am53C974A as a master will never generate a LOCK. However, in slave role the chip will respond to a LOCK asserted by a master.*

IDSEL

Initialization Device Select
(Input, Active High)
This signal is used as a chip select for the Am53C974A in lieu of the 24 address lines during configuration read and write transactions.

When PCI RST is active, IDSEL is an input for NAND tree testing.

DEVSEL

Device Select
(Input/Output, Active Low)
This signal when actively driven by the Am53C974A as a slave device signals to the master device that it has decoded its address as the target of the current access. As an input it indicates whether any device on the bus has been selected.

When PCI RST is active, DEVSEL is an input for NAND tree testing.

Arbitration Pins

PCI REQ

PCI Request
(Output, Active Low)
This signal indicates to the arbiter that the Am53C974A desires use of the bus. This is a point to point signal. Every master has its own REQ which will be tri-stated after a power-up or a chip reset.

When PCI RST is active, PCI REQ is an input for NAND tree testing.

PCI GNT

PCI Grant
(Input, Active Low)
This signal indicates that the access to the bus has been granted to the Am53C974A. This is a point to point signal. Every master has its own GNT.

When PCI RST is active, PCI GNT is an input for NAND tree testing.

System Pins

CLK

Clock
(Input)
This signal provides timing for all the transactions on the PCI bus and all PCI devices on the bus including the Am53C974A. All signals are sampled on the rising edge of CLK and all parameters are defined with respect to this edge. The Am53C974A operates at a frequency of up to 33 MHz.

When PCI RST is active, CLK is an input for NAND tree testing.

PCI RST

PCI Reset
(Input, Active Low)
This signal forces the Am53C974A Sequencer to a known state. All Three-State bi-directional signals are forced to a high impedance state and all Sustained Open Drain signals are allowed to float high. The Am53C974A arbiter will tristate PCI REQ if it is a master. This signal completely resets the SCSI core. PCI RST may be asynchronous to the CLK when asserted or deasserted. It is recommended that the deassertion be synchronous to guarantee clean and bounce free edge.

When PCI RST is active, NAND tree testing is enabled. All PCI interface pins are in input mode. The result of the NAND tree testing can be observed on the BUSY output (pin 62).

Error Reporting Pins

PERR

Parity Error
(Input/Output, Active Low)
This signal may be pulsed by the Am53C974A when it detects a parity error during a data phase when its AD[31:00] and C/BE [3:0] lines are inputs.

When PCI RST is active, PERR is an input for NAND tree testing.

SERR

System Error
(Output, Active Low, Open Drain)
This signal may be pulsed by the Am53C974A for reporting address parity errors.

When PCI RST is active, SERR is an input for NAND tree testing.

Interrupt Request Pins

$\overline{\text{INTA}}$
Interrupt Request
(Output, Active Low)
This signal combines the interrupt request from both the DMA engine and the SCSI core. The interrupt source can be determined by reading the DMA Status Register.

When the Write Erase feature is not set in the SBAC register ((B)+70), the $\overline{\text{INTA}}$ signal will be cleared when the Status Register ((B)+54) is read. When the Write Erase feature is set, the $\overline{\text{INTA}}$ signal will only be cleared when a '1' is written to the bit associated with the interrupting condition.

When $\overline{\text{PCI RST}}$ is active, $\overline{\text{INTA}}$ is an input for NAND tree testing.

SCSI Bus Interface Signals

SCSI Bus Pins

$\overline{\text{SD}}$ [7:0]
SCSI Data
(Input/Output, Active Low, Open Drain/Active Negation, Schmitt Trigger)
These pins are defined as bi-directional SCSI data bus.

$\overline{\text{SDP}}$
SCSI Data Parity
(Input/Output, Active Low, Open Drain/Active Negation, Schmitt Trigger)
This pin is defined as bi-directional SCSI data parity.

$\overline{\text{MSG}}$
Message
(Input/Output, Active Low, Open Drain, Schmitt Trigger)
This is a bi-directional signal with a 48 mA output driver. It is an output in the target mode and a Schmitt trigger input in the initiator mode.

$\overline{\text{C/D}}$
Command/Data
(Input/Output, Active Low, Open Drain, Schmitt Trigger)
This is a bi-directional signal with a 48 mA output driver. It is an output in the target mode and a Schmitt trigger input in the initiator mode.

$\overline{\text{I/O}}$
Input/Output
(Input/Output, Active Low, Open Drain, Schmitt Trigger)
This is a bi-directional signal with a 48 mA output driver. It is an output in the target mode and a Schmitt trigger input in the initiator mode.

$\overline{\text{ATN}}$
Attention
(Input/Output, Active Low, Open Drain, Schmitt Trigger)
This signal is a 48 mA output in the initiator mode and a Schmitt trigger input in the target mode. This signal will be asserted when the device detects a parity error or it can be asserted via certain commands.

$\overline{\text{BSY}}$
Busy
(Input/Output, Active Low, Schmitt Trigger, Open Drain)
As a SCSI input signal it has a Schmitt trigger and as an output signal it has a 48 mA drive.

$\overline{\text{SEL}}$
Select
(Input/Output, Active Low, Schmitt Trigger, Open Drain)
As a SCSI input signal it has a Schmitt trigger and as an output signal it has a 48 mA drive.

$\overline{\text{SCSI RST}}$
Reset
(Input/Output, Active Low, Schmitt Trigger, Open Drain)
As a SCSI input signal it has a Schmitt trigger and as an output signal it has a 48 mA drive. The Reset SCSI command will cause the device to drive $\overline{\text{SCSI RST}}$ active for 25 µs – 40 µs depending on the CLK frequency and the conversion factor.

$\overline{\text{REQ}}$
Request
(Input/Output, Active Low, Schmitt Trigger, Open Drain, Active Negation)
This is a SCSI input signal in the initiator mode with a Schmitt trigger. This is a SCSI output signal with a 48 mA drive in the target mode.

$\overline{\text{ACK}}$
Acknowledge
(Input/Output, Active Low, Schmitt Trigger, Open Drain/Active Negation)
This is a SCSI input signal in the target mode with a Schmitt trigger. This is a SCSI output signal with a 48 mA drive in the initiator mode.

Power Management Signals

PWDN

Power Down Indicator
(Input, Active High)
This signal, when asserted, sets the PWDN status bit in the DMA status register and sends an interrupt to the host.

$\overline{\text{BUSY}}$

SCSI Devices Busy
(Output, Active Low)
This signal is logically equivalent to the SCSI bus signal $\overline{\text{BSY}}$. It is duplicated so that external logic can be connected to monitor SCSI bus activity.

The results of the NAND tree testing can be observed on the $\overline{\text{BUSY}}$ pin. $\overline{\text{BUSY}}$ will reflect the state of the SCSI Bus Signal line $\overline{\text{BSY}}$ (pin 64) when $\overline{\text{PCI RST}}$ is deasserted.

Boot ROM Support Pins

BOOT

Boot ROM Present
(Input)

The state of this pin determines whether or not the Boot ROM interface on the Am53C974A is enabled. When this pin is connected to V_{CC}, the interface is enabled to support the Boot ROM feature. When this pin is connected to ground, all input buffers on BD7:0 are disabled, and BA7:0, $\overline{\text{OE}}$, and $\overline{\text{LCK}}$ pins are tri-stated.

BD7:0

Boot ROM Data
(Input)

When the Am53C974A is configured for Boot ROM support (Pin 100 tied to V_{CC}), BD7:0 carries data from the ROM to the Am53C974A. When not configured to support a Boot ROM (Pin 100 tied to ground), the input buffers on these pins are disabled.

BA7:0

ROM Address
(Output)

When the Am53C974A is configured for Boot ROM support (Pin 100 tied to V_{CC}), BA7:0 carries the Boot ROM address from the Am53C974A. When Boot ROM support is disabled (Pin 100 tied to ground), these pins are tri-stated.

$\overline{\text{OE}}$

ROM Output Enable
(Output, Active Low)

When the Am53C974A is configured for Boot ROM support (Pin 100 tied to V_{CC}), this pin is used as the output enable for the ROM. When Boot ROM support is disabled (Pin 100 tied to ground), this pin is tri-stated.

$\overline{\text{LCK}}$

Latch Clock
(Output, Active Low)

When the Am53C974A is configured for Boot ROM support (Pin 100 tied to V_{CC}), this pin is used as a clock to latch the high byte of the ROM address. When Boot ROM support is disabled (Pin 100 tied to ground), this pin is tri-stated.

Miscellaneous Signals

SCSI CLK1

SCSI Clock
(Input)
The SCSI clock signal is used to generate all internal device timings. The maximum frequency of this input is 40 MHz and a minimum of 10 MHz is required to maintain the SCSI bus timings. This pin may be permanently connected to V_{SS}. In this case, the SCSI logic will be driven by the PCI CLK.

Note: *A 40 MHz clock must be supplied at this input to achieve 10 Mbyte/s Synchronous Fast SCSI transfers.*

RES_DNC

Reserved_DO NOT CONNECT
(Input)
This pin (#116) is reserved for internal test logic. It **MUST NOT BE CONNECTED** to anything for proper chip operation.

Power Supply Pins

V_{DD}

+5 V Power
(Input)
These inputs provide power necessary to operate the Am53C974A. All V_{DD} pins must be connected.

V_{DDB}

+5 V Power
(Input)
These inputs are for SCSI Buffers. These pins can be connected to the V_{DD} pins.

V_{DD3B}

+5 V Power
(Input)
All V_{DD3B} pins must be connected to a +5 V supply. These inputs are for PCI interface block.

$V_{SS}/V_{SSB}/V_{SS3B}$

Ground
(Input)
These inputs provide the necessary grounds to operate the Am53C974A. The V_{SSBs}, V_{SS3Bs} and V_{SSs} must be connected together.

FUNCTIONAL DESCRIPTION

This section covers the registers, commands, and operation of each of the three blocks: SCSI, DMA/FIFO, and PCI. The PCI Configuration space and the I/O address space are also covered.

I/O Address Map

The SCSI Core and DMA registers are addressed using the Base address register at offset 10h in the PCI configuration space. The SCSI registers occupy 16 double words and the DMA engine registers occupy 8 double word locations. The I/O address map is as follows:

Start Offset	End Offset	Block Name	Size
0x0000	0x003F	SCSI Core Reg	16 DW/64B
0x0040	0x005F	PCI DMA CCB	8 DW/32B
0x0070	0x0073	PCI DMA CCB	1 DW/4B

The PCI configuration space, DMA and SCSI Core registers are described in the following sections.

PCI Interface

Configuration Registers

PCI configuration registers are used to determine which devices are in the system, and are also used to setup the configuration of those devices. Configuration registers are accessible only by PCI configuration cycles.

The Am53C974A supports the *Vendor ID, Device ID, Command and Status register* in the header, for PCI compliancy. Implementation of the other registers is optional depending on device functionality. Only the registers that are supported by the Am53C974A are described in this section. Please see the *PCI specification* for more detailed information on PCI registers.

Am53C974A supports the 64 byte predefined header portion (00h to 3Fh) of the 256 (100h) byte PCI configuration space. All of the device specific registers are in locations 64–255. All multi-byte numeric fields follow "little-endian" ordering. That is, lower addresses contain the least significant parts of the field. Table 1 shows the PCI configuration space header.

Table 1. The PCI Configuration Space Header

31 16		15 0		Address Offset
Device ID		Vendor ID		00h
Status		Command		04h
Base Class	Sub Class	Prog. If.	Revision ID	08h
BIST*	Header Type*	Latency Timer	Cache Line Size*	0Ch
Base Address				10h
Base Address*				14h
Base Address*				18h
Base Address*				1Ch
Base Address*				20h
Base Address*				24h
Reserved*				28h
Reserved*				2Ch
Expansion ROM Base Address				30h
Reserved*				34h
Reserved*				38h
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch
Reserved	Reserved	Reserved	Reserved	40h**
Reserved	Reserved	Reserved	Reserved	44h**
Reserved	Reserved	Reserved	Reserved	48h**
Reserved	Reserved	Reserved	Reserved	4Ch**

** Not Implemented on Am53C974A. Writes to these locations will have no effect; reads from these locations will return '00h'.*

*** Reserved for SCSI software.*

Vendor ID Register

Address 00h
(Read Only)
This 16-bit register identifies the manufacturer Advanced Micro Devices, Inc. (AMD). The vendor ID is '1022h'.

Device ID Register

Address 02h
(Read Only)
This 16-bit register uniquely identifies this device within AMD's product line. The Am53C974A Device ID is '2020h'.

Command Register

Address 04h
(Read/Write)
The Command Register is used to control the gross functionality of the device. It controls the device's ability to generate and respond to PCI bus cycles. To logically disconnect the Am53C974A device from all PCI bus cycles except Configuration cycles, a value of zero should be written to this register.

Status Register

Address 06h
(Read/Write)
The Status register is used to read status information for the PCI bus. Reads to this register function normally, however writes function differently. On a write, bits may be reset (from 1 to 0), but not set.

Revision ID Register

Address 08h
(Read Only)
This register specifies the device specific revision number. On the Am53C974A, the value of this register is '10h'.

Programming Interface Register

Address 09h
(Read Only)
This register identifies the programming interface of this device. The value in this register is 00h.

Sub-Class Register

Address 0Ah
(Read Only)
This register identifies this device as a SCSI Controller. The value in this register is '00h'.

Base Class Register

Address 0Bh
(Read Only)
This register identifies this device as a Mass Storage controller. The value in this register is '01h'.

Latency Timer Register

Address 0Dh
(Read/Write)
The Latency Timer register is an 8-bit register specifying the maximum time the Am53C974A can continue with bus master transfers after the system arbiter has removed $\overline{GNT}$. The time is measured in CLK cycles. The working copy of the timer will start counting down when the Am53C974A asserts $\overline{FRAME}$ for the first time during a bus mastership period.

The value for the Am53C974A Latency Timer register is programmable.

Base Address Register

Address 10h
(Read/Write)
This register defines base address for I/O operations. The Am53C974A will be selected when AD [31:7] matches the value in the Base Address Register [31:7] during PCI I/O cycles.

Expansion ROM Base Address Register

Address 30h
(Read/Write)

This is a 32-bit read/write register which is used to hold the expansion ROM Base Address. It is used to specify the size and alignment of the expansion ROM for the Am53C974A. It is designed to support expansion ROMs of up to 64K. Bits 31 to 16 are the programmable ROM base address while bits 15 through 11 are hardwired to '0'. Bits 10 to 1 are reserved while bit 0 is the address decode enable bit as defined by the PCI specification Rev. 2.0.

Interrupt Line Register

Address 3Ch
(Read/Write)

The interrupt line register is used to communicate the routing of the interrupt. This register is written by the POST (Power-On Self Test) software as it initializes the PCI devices in the system.

Interrupt Pin Register

Address 3Dh
(Read Only)

This register identifies the interrupt pin used by Am53C974A. This register will contain a value of '1' because the Am53C974A is using $\overline{\text{INTA}}$.

Min_Gnt Register

Address 3Eh
(Read Only)

The Min_Gnt register is an 8-bit read only register. It is hardwired to a value of '04h'. This value equals a burst period of 1 µs calculated at a 33 MHz clock rate. The register value specifies the time in units of 1/4 microseconds. The host should use the value of this register to determine the setting of the Am53C974A's Latency Timer Register.

Max_Lat Register

Address 3Fh
(Read Only)

The Max_Lat register is an 8-bit read only register. It is hardwired to a value of '28h'. This value equals a PCI bus latency of 10 µs calculated at a 33 MHz clock rate. The register value specifies the time in units of 1/4 microseconds. The host should use the value of this register to determine the setting of the Am53C974A's Latency Timer Register.

Reserved Register

Address 40h – 4Ch
(Read/Write)

This register is a 32-bit read/write register which is currently undefined. Writes to this register will store data, and reads from this register reflect the data stored in this register.

Bus Cycle Definition

The following table defines the PCI bus cycles:

Cycle	Bus Cycle Type	Mode Supported
C/$\overline{\text{BE}}$ [3:0]		
0000	Interrupt ACK	*
0001	Special Cycle	*
0010	I/O Read	Slave
0011	I/O Write	Slave
0100	Reserved	*
0101	Reserved	*
0110	Memory Read	Master/Slave
0111	Memory Write	Master
1000	Reserved	*
1001	Reserved	*
1010	Config. Read	Slave
1011	Config. Write	Slave
1100	Memory Read Multiple	**Slave
1101	Dual Address Cycle	*
1110	Memory Read Line	Master/**Slave
1111	Memory Write & Invalidate	*

** These cycles are ignored by the Am53C974A.*

***Both the Slave Memory Read Line and Slave Memory Read Multiple cycles are aliased to the Slave Memory Read Cycle.*

Refer to the technical manual for detailed bus cycle diagrams and explanations.

NAND Tree Testing

The Am53C974A PCscsi II controller provides a NAND tree test mode to allow checking connectivity to the device on a printed circuit board. The NAND tree is built on all PCI bus signals (see Figure 1 and Table 2).

The NAND tree testing is enabled by asserting $\overline{\text{PCI RST}}$. All PCI signals will become inputs when $\overline{\text{PCI RST}}$ is asserted. The result of the NAND tree test can be observed on the $\overline{\text{BUSY}}$ pin.

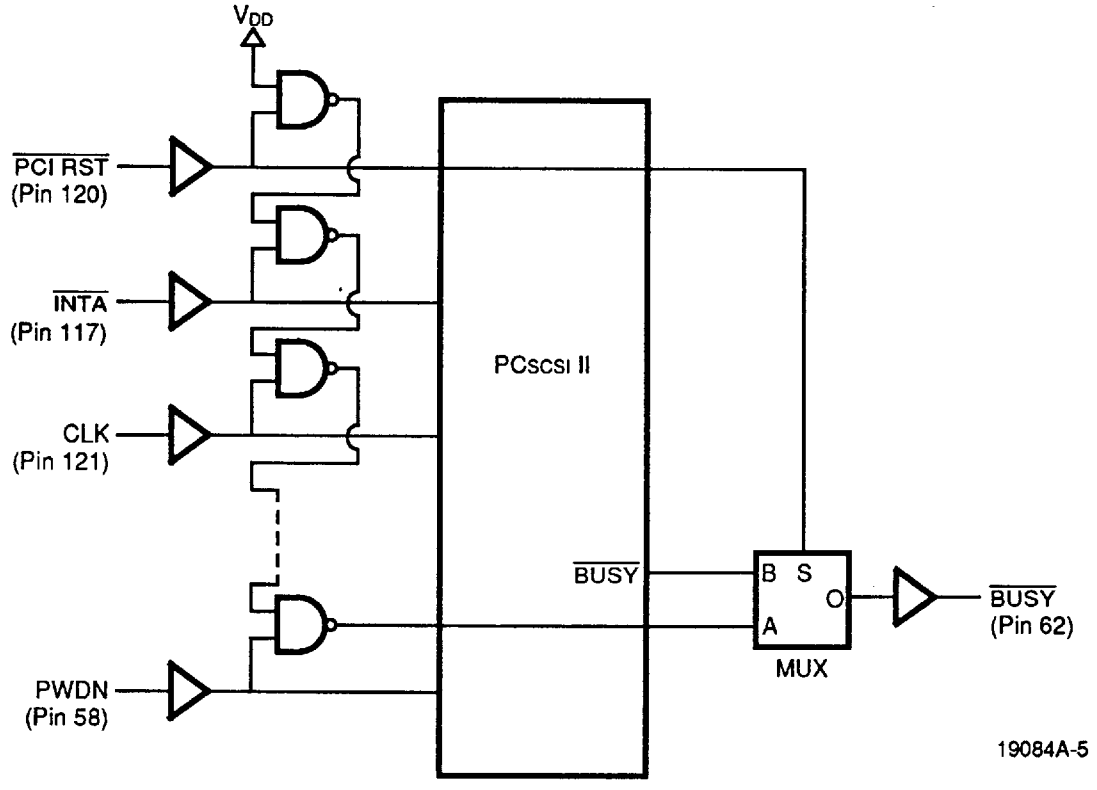


Figure 1. NAND Tree

As shown in Figure 1, Pin 120 (PCI RST) is the first input to the NAND tree. Pin 117 (INTA) is the second input to the NAND tree, followed by pin 121 (CLK). All other PCI bus signals follow, counterclockwise, with pin 58 (PWDN) being the last. Pins labeled NC and all power supply pins are not part of the NAND tree. The complete list of pins connected to the NAND tree is shown in Table 2.

Table 2. The NAND Tree Connection Pins

NAND Tree Input #	Pin #	Name	NAND Tree Input #	Pin #	Name	NAND Tree Input #	Pin #	Name
1	120	PCI RST	19	16	AD20	37	39	AD13
2	117	INTA	20	18	AD19	38	40	AD12
3	121	CLK	21	19	AD18	39	41	AD11
4	124	PCI GNT	22	21	AD17	40	42	AD10
5	127	PCI REQ	23	22	AD16	41	44	AD9
6	128	AD31	24	23	C/BE2	42	45	AD8
7	129	AD30	25	24	FRAME	43	47	C/BE0
8	131	AD29	26	25	IRDY	44	48	AD7
9	132	AD28	27	26	TRDY	45	49	AD6
10	2	AD27	28	27	DEVSEL	46	51	AD5
11	3	AD26	29	28	STOP	47	52	AD4
12	5	AD25	30	29	LOCK	48	53	AD3
13	6	AD24	31	31	PERR	49	54	AD2
14	7	C/BE3	32	32	SERR	50	56	AD1
15	9	IDSEL	33	34	PAR	51	57	AD0
16	12	AD23	34	35	C/BE1	52	58	PWDN
17	13	AD22	35	36	AD15			
18	15	AD21	36	38	AD14			

PCI RST must be asserted low to start a NAND tree test sequence. Initially, all NAND tree inputs except PCI RST should be driven high. This will result in a low output at the BUSY pin. If the NAND tree inputs are driven low in the same order as they are connected to build the NAND tree, BUSY will toggle every time an additional input is low. BUSY will change to a ONE, when INTA is driven low and all other NAND tree inputs stay high. BUSY will toggle back to low, when CLK is additionally driven low. The square wave will continue until all NAND tree inputs are driven low. BUSY will be high, when all NAND tree inputs are low (see Figure 2).

When testing is complete, deassert PCI RST to exit this test mode.

Note: *Some of the pins connected to the NAND tree are outputs in normal mode of operation. They must not be driven from an external source until the Am53C974A controller is configured for NAND tree testing.*

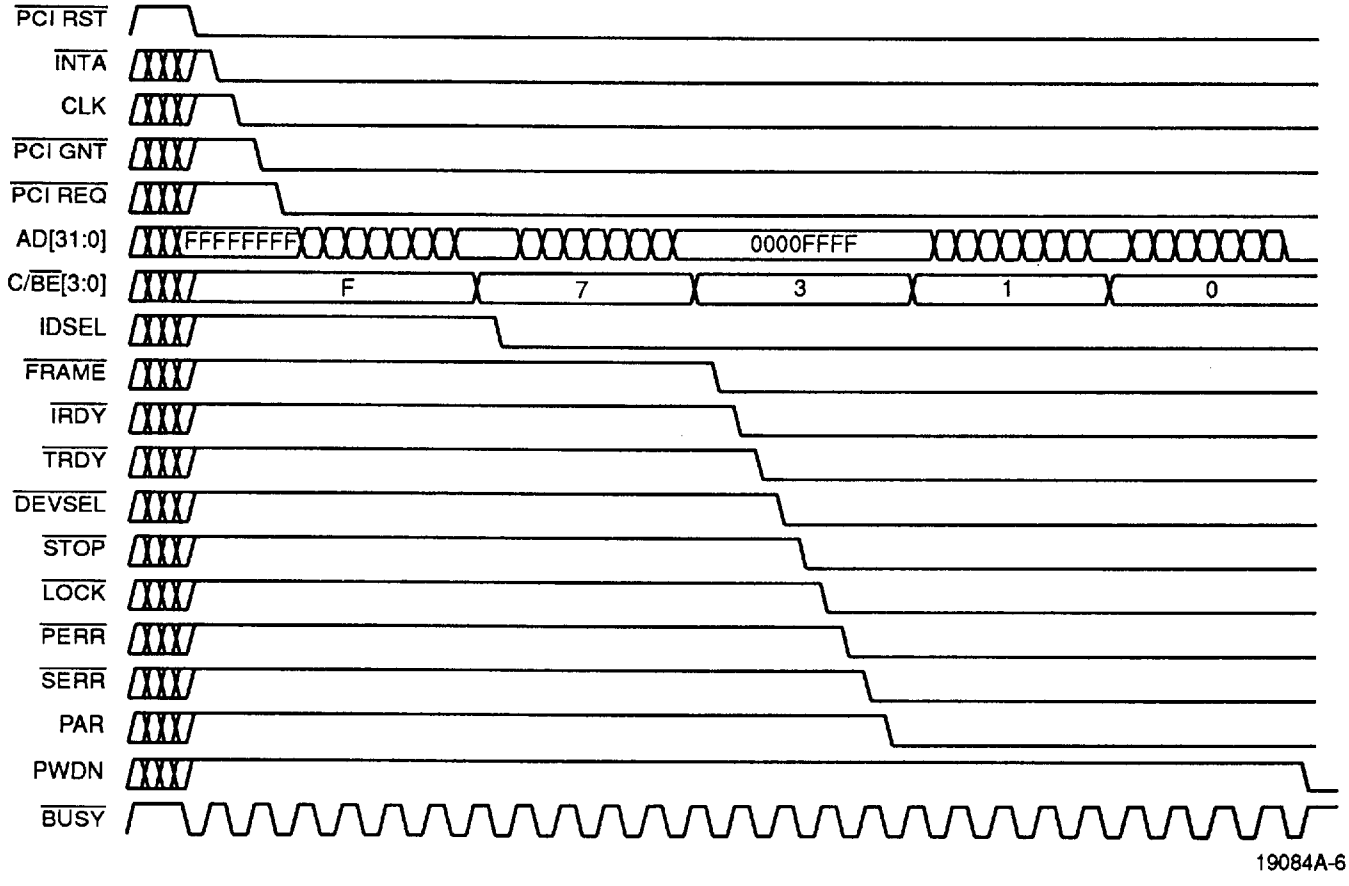


Figure 2. NAND Tree Waveform

DMA Engine and FIFOs

FIFOs

The Am53C974A acts as a bridge between the PCI and SCSI buses. As the maximum data transfer rate on the PCI bus is a very high 132 Mbyte/s compared with the SCSI bus 10 Mbyte/s, buffering is required between the two buses to maximize the PCI bandwidth. The buffering is provided by two FIFOs: 16-byte (16x8 bits) SCSI Core FIFO and an additional 96-byte (24x32 bits) DMA FIFO. These FIFOs provide a temporary storage for all command, data, status and message bytes as they are transferred between the 32-bit PCI bus and the 8-bit SCSI bus.

DMA Registers

The following is a description of the DMA register set or the DMA Channel Context Block (DMA CCB). The register addresses are referenced with the PCI configuration Base Address Register (10h) contents, represented by (B) in the Table 3.

The DMA registers control the DMA operation and transfer length and allow the programmer to specify a scatter-gather list that is stored in main memory. The MDL scatter-gather list will be described later. The three read-only working counter registers allow the system software and other driver layers to monitor the state of the DMA transaction.

Table 3. The DMA Registers

Register Acronym	Addr (Hex)	Register Description	Type
CMD	(B)+40	Command (bits 31:8 reserved, bits 7:0 used)	R/W
STC	(B)+44	Starting Transfer Count (bits 31:24 reserved, bits 23:0 used)	R/W
SPA	(B)+48	Starting Physical Address (bits 31:0 used)	R/W
WBC	(B)+4C	Working Byte Counter	R
WAC	(B)+50	Working Address Counter (bits 31:0 used)	R
STATUS	(B)+54	Status Register (bits 31:8 reserved, bits 7:0 used)	R
SMDLA	(B)+58	Starting Memory Descriptor List (MDL) Address	R/W
WMAC	(B)+5C	Working MDL Counter	R
SBAC	(B)+70	SCSI Bus and Control (bits 31:26 reserved; bits 25:24 used; bits 23:22 reserved; bits 21:0 used)	*

**Certain bits are Read/Write, certain bits are Read only. Refer to the SBAC register's description for more detail.*

Command Register (CMD)

The upper 3 bytes of Command register are reserved, the remaining (LSB) byte is defined as follows:

Address (B)+40h, LSB **READ/WRITE**

7	6	5	4	3	2	1	0
DIR	INTE_D	INTE_P	MDL	Reserved	Reserved	CMD1	CMD0

DIR:

Data transfer direction bit.

INTE_D:

DMA transfer active interrupt bit.

INTE_P:

Page transfer active interrupt bit.

MDL:

Memory Descriptor List (MDL) Starting Physical Address register enable bit.

RESERVED:

Reserved for future expansion. Zero values must be written in these bits.

CMD1-0:

These two bits are encoded to represent four DMA commands: IDLE, BLAST, START, and ABORT.

CMD1	CMD0	Command	Description
0	0	IDLE	Resets the DMA block to the IDLE state. Stops any current transfer. Does not affect status bits or cause an interrupt.
0	1	BLAST	Empties all data bytes in DMA FIFO to memory during a DMA write operation. BCMPLT bit is set in the DMA status register upon completion. This command should not be used during a DMA read operation.
1	0	ABORT	Terminate the current DMA transfer. ***Note:*** *This is only valid after a START command is issued.*
1	1	START	Initiate a new DMA transfer. This bit remains set throughout the entire DMA operation until bit 3 in the DMA status register is set. ***Note:*** *The software should issue a START command only after* ***all*** *other control bits have been initialized.*

Starting Transfer Count (STC)
Address (B)+44h
Read/Write

The STC register is a 24-bit read/write value that contains the number of bytes to be transferred. This register is not modified by the DMA transfer logic, and can be read by the software at any time. The system software can modify this register after the DMA transfer has been started.

Starting Physical Address (SPA)
Address (B)+48h
Read/Write

The SPA register is a 32-bit read/write address that is used as the starting address value for the DMA transfer. This register is not modified by the DMA transfer logic, and can be read by the software at any time. The system software can modify this register after the DMA transfer has been started.

Working Byte Counter (WBC)
Address (B)+4Ch
Read

The WBC register is a 24-bit read-only counter that is initialized to the value in the STC register when the transfer begins. It decrements by 1, 2, or 4 as data is sent to the PCI Bus by the controller. When the DMA transfer stops, a non zero value in this register indicates that the operation aborted earlier than expected (i.e. an error occurred). This register's intermediate values can be read by software in between DMA burst transactions.

Working Address Counter (WAC)
Address (B)+50h
Read

The WAC register is a 32-bit read-only address that is initialized to the value in the SPA register when the transfer begins. It increments as data is processed by the DMA channel, and will contain the address after the last access when the transfer terminates. This register's intermediate values can be read by software in between DMA burst transactions.

Status Register (Status)

The upper 3 bytes of the Status register are reserved, the remaining (LSB) byte is defined as follows:

Address (B)+54h, LSB **READ**

7	6	5	4	3	2	1	0
Reserved	PABORT	BCMPLT	SCSIINT	DONE	ABORT	ERROR	PWDN

The status Flags report the state of the DMA channel, any termination condition and SCSI interrupt.

RESERVED:

Reserved bits.

PABORT:

This bit is used in conjunction with bit 25 in register (B)+70h to indicate that a PCI Master or Target abort condition was detected.

BCMPLT:

This bit indicates the status of the BLAST command. It is only valid when the BLAST command is issued for a SCSI Disconnect and Reselect operation.

SCSIINT:

SCSI core interrupt bit.

DONE:

DMA transfer request termination bit.

ABORT:

DMA transfer request abort bit.

ERROR:

DMA transfer request termination with an error condition bit.

PWDN:

PWDN pin status bit.

Starting Memory Descriptor List Address (SMDLA)
Address (B)+58H
Read/Write

The SMDLA register is a 32-bit read/write address that is used as the starting address of the scatter-gather Memory Descriptor List. This register is not modified by the DMA transfer logic, and can be read by the software at any time. The system software can modify this register after the DMA transfer has been started.

Note: *The MDL start address must be double-word aligned since the hardware ignores non-zero values written to the two low address bits.*

Working MDL Address Counter (WMAC)
Address (B)+5CH
Read

The WMAC register is a 32-bit read-only address that is initialized to the value in the SMDLA register when the transfer begins. It increments by 4 as new MDL entries are fetched by the DMA channel, and will contain the address after the last MDL read when the transfer terminates. This register's intermediate values can be read by software in between DMA burst transactions.

SCSI Bus and Control (SBAC) Address (B)+70

This is a 32-bit register which is used to control the enhancements in the Am53C974A. These enhancements include the Write Erase feature for the DMA Status register, the SCSI Power-down and clock selection feature, and the SCAM support.

Address (B)+73h

31	30	29	28	27	26	25	24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PABTEN	STATUS

Address (B)+72h

23	22	21	20	19	18	17	16
Reserved	Reserved	PWD	SBSY	SCLK	SCAM	REQ	ACK

Address (B)+71h

15	14	13	12	11	10	9	8
RST	BSY	SEL	ATN	MSG	C/D	I/O	SDP

Address (B)+70h

7	6	5	4	3	2	1	0
SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0

RESERVED:

Reserved bits.

PABTEN:

This bit controls the interrupt and status bit for the PCI Abort condition (Master or Target Abort). When this bit is set to '1' and a PCI Abort condition is detected, an interrupt will be generated and bit 6 of the DMA Status register ((B)+54h) will be set to '1'. When this bit is reset to '0', and a PCI Abort condition is detected, an interrupt will not be generated and bit 6 will not be affected by the Abort condition.

STATUS:

This bit controls the Write Erase feature on bits 3:1 of the DMA Status Register ((B)+54h). When this bit is programmed to '1', the state of bits 3:1 are preserved when read. Bits 3:1 are only cleared when a '1' is written to the corresponding bit location. For example, to clear bit 1, the value of '0000_0010b' should be written to the register. When the DMA Status Preserve bit is '0', bits 3:1 are cleared when read.

PWD:

This bit is used to remove the SCSI clock input to the Am53C974A during power-down sequencing. When this bit is '1', the SCSI clock input is disconnected from the SCSI core to save power. When this bit is '0', the clock is connected for SCSI operation.

SBSY:

This is a read only bit which monitors the BUS FREE condition on the SCSI bus. When this bit is '1', the SCSI bus is in use. When this bit is '0', the SCSI bus is free. This bit can be used in conjunction with the PWD bit to initiate power-down sequence.

SCLK:

This read-only bit indicates whether the SCSI core is connected to the PCI clock, or if it is connected to an external SCSI clock. When this bit is '1', the SCSI core is driven by the SCSI clock. When this bit is '0', the SCSI core is driven by the PCI clock.

Note: *For Fast Synchronous (10 Mbytes/sec) operation, the SCSI core must be driven by a 40 MHz source. Normally, this is achieved by an external SCSI clock source since the PCI clock typically operates at 33 MHz.*

SCAM:

When bit 18 is set to '1', bits 17:0 may be programmed to support SCAM protocol. When bit 18 is reset to '0', bits 17:0 are read-only and represent the logical state of the SCSI bus. Reading bits 17:0 always returns the current values of the SCSI bus signals regardless of the value of bit 18.

DMA Scatter-Gather Mechanism

The Am53C974A contains a scatter-gather translation mechanism which facilitates faster I/O data transfers. The mechanism uses a list of page frame addresses stored in system main memory that is called a Memory Descriptor List (MDL). The MDL page frame address allows a single SCSI transfer to read or write to non-contiguous address memory locations. The design eliminates the need for copying either the transfer data or the MDL locations.

SCSI Core

The SCSI core description covers a summary of the register definitions and the commands used by the SCSI core.

Registers

In the Am53C974A, each SCSI register is mapped to a double-word address space, as shown in Table 4. The actual register data occupies the least significant byte (LSB) of that particular double word address. Registers are accessed by specifying the base address (B) and the offset value specified below.

The Am53C974A's base address is stored at offset 10h in the PCI configuration space.

Table 4. SCSI Register Map

Register Acronym	Address (Hex.)	Register Description	Operation
CTCREG	(B)+00	Current Transfer Count Register Low	Read
STCREG	(B)+00	Start Transfer Count Register Low	Write
CTCREG	(B)+04	Current Transfer Count Register Middle	Read
STCREG	(B)+04	Start Transfer Count Register Middle	Write
FFREG	(B)+08	FIFO Register	Read/Write
CMDREG	(B)+0C	Command Register	Read/Write
STATREG	(B)+10	Status Register	Read
SDIDREG	(B)+10	SCSI Destination ID Register	Write
INSTREG	(B)+14	Interrupt Status Register	Read
STIMREG	(B)+14	SCSI Timeout Register	Write
ISREG	(B)+18	Internal State Register	Read
STPREG	(B)+18	Synchronous Transfer Period Register	Write
CFIREG	(B)+1C	Current FIFO/Internal State Register	Read
SOFREG1	(B)+1C	Synchronous Offset Register	Write
CNTLREG1	(B)+20	Control Register One	Read/Write
CLKFREG	(B)+24	Clock Factor Register	Write
RES	(B)+28	Reserved	Write
CNTLREG2	(B)+2C	Control Register Two	Read/Write
CNTLREG3	(B)+30	Control Register Three	Read/Write
CNTLREG4	(B)+34	Control Register Four	Read/Write
CTCREG	(B)+38	Current Transfer Count Register High/Part Unique ID Code	Read
STCREG	(B)+38	Start Transfer Count Register High	Write
RES	(B)+3C	Reserved	Write

Register Descriptions

The SCSI registers are described briefly in the following section. The bit map of the LSB reflects the default state after power-up or chip reset.

Current Transfer Count Register (CTCREG)

Address (B)+38H **READ ONLY**

7	6	5	4	3	2	1	0
CRVL23	CRVL22	CRVL21	CRVL20	CRVL19	CRVL18	CRVL17	CRVL16
X	X	X	X	X	X	X	X

Address (B)+04H **READ ONLY**

7	6	5	4	3	2	1	0
CRVL15	CRVL14	CRVL13	CRVL12	CRVL11	CRVL10	CRVL9	CRVL8
X	X	X	X	X	X	X	X

Address (B)+00H **READ ONLY**

7	6	5	4	3	2	1	0
CRVL7	CRVL6	CRVL5	CRVL4	CRVL3	CRVL2	CRVL1	CRVL0
X	X	X	X	X	X	X	X

CRVL 23:0 – Current Value 23:0

This is a three-byte register which decrements to keep track of the number of bytes transferred during a DMA transfer.

Start Transfer Count Register (STCREG)

Address (B)+38H **WRITE ONLY**

7	6	5	4	3	2	1	0
STVL23	STVL22	STVL21	STVL20	STVL19	STVL18	STVL17	STVL16
X	X	X	X	X	X	X	X

Address (B)+04H **WRITE ONLY**

7	6	5	4	3	2	1	0
STVL15	STVL14	STVL13	STVL12	STVL11	STVL10	STVL9	STVL8
X	X	X	X	X	X	X	X

Address (B)+00H **WRITE ONLY**

7	6	5	4	3	2	1	0
STVL7	STVL6	STVL5	STVL4	STVL3	STVL2	STVL1	STVL0
X	X	X	X	X	X	X	X

STVL 23:0 – Start Value 23:0

This is a three-byte register which contains the number of bytes to be transferred during a DMA operation.

***Note**: The Start Transfer Count register and the STC register of the DMA Engine should be programmed with the same value.*

SCSI FIFO Register (FFREG)

Address (B)+08H **READ/WRITE**

7	6	5	4	3	2	1	0
FF7	FF6	FF5	FF4	FF3	FF2	FF1	FF0
0	0	0	0	0	0	0	0

FF 7:0 – FIFO 7:0

The bottom of the SCSI FIFO is mapped to this register.

SCSI Command Register (CMDREG)

Address (B)+ 0Ch **READ/WRITE**

7	6	5	4	3	2	1	0
DMA	CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0
X	X	X	X	X	X	X	X

Commands to the SCSI core are issued by writing to this register which is two bytes deep.

DMA – Direct Memory Access

This bit notifies the device that the command is a DMA instruction.

CMD 6:0 – Command 6:0

These command bits decode the commands that the device needs to perform.

SCSI Status Register (STATREG)

Address (B)+10H **READ**

7	6	5	4	3	2	1	0
INT	IOE	PE	CTZ	GCV	MSG	C/D	I/O
0	0	0	0	X	X	X	X

This read-only register contains flags to indicate the status and phase of the SCSI transactions.

3/861 2A

INT – Interrupt

The INT bit is set when the device asserts the interrupt output.

IOE – Illegal Operation Error

The IOE bit is set when an illegal operation is attempted.

PE – Parity Error

The PE bit is set if any of the parity checking options are enabled and the device detects a parity error on bytes sent or received on the SCSI Bus.

CTZ – Count To Zero

The CTZ bit is set when the Current Transfer Count Register (CTCREG) has decremented to zero.

GCV – Group Code Valid

The GCV bit is set if the group code field in the Command Descriptor Block (CDB) is one that is defined by the ANSI Committee in their document X3.131 – 1986. This bit is used in conjunction with the SCSI-2 Features Enable (S2FE) bit in the Control Register 2 ((B)+2Ch) to determine if a Group 2 command is a 6-byte or a 10-byte command.

MSG – Message
C/D – Command/Data
I/O – Input/Output

The MSG, C/D and I/O bits indicate the phase of the SCSI bus.

SCSI Destination ID Register (SDIDREG)

Address (B)+10H **WRITE ONLY**

7	6	5	4	3	2	1	0
RES	RES	RES	RES	RES	DID2	DID1	DID0
0	0	0	0	0	X	X	X

RES – Reserved

DID 2:0 – Destination ID 2:0

The DID 2:0 bits are the encoded SCSI ID of the device (0 thru 7) on the SCSI bus which needs to be selected or reselected.

Interrupt Status Register (INSTREG)

Address (B)+14H **READ ONLY**

7	6	5	4	3	2	1	0
SRST	ICMD	DIS	SR	SO	RESEL	SELA	SEL
0	0	0	0	0	0	X	X

The Interrupt Status Register (INSTREG) will indicate the reason for the interrupt.

SRST – SCSI Reset

The SRST bit will be set if a SCSI Reset is detected and SCSI reset reporting is enabled via the DISR (bit 6) of Control Register One (CNTLREG1).

ICMD – Invalid Command

The ICMD bit will be set if the device detects an illegal command code.

DIS – Disconnected

The DIS bit can be set in the Initiator mode or Target mode when the device disconnects from the SCSI bus.

SR – Service Request

The SR bit can be set in the Initiator mode or Target mode when another device on the SCSI bus has a service request.

SO – Successful Operation

The SO bit can be set in the Initiator mode or Target mode when an operation has been successfully completed.

RESEL – Reselected

The RESEL bit is set at the end of the reselection phase indicating that the device has been reselected as an Initiator.

SELA – Selected with Attention

The SELA bit is set at then end of the selection phase indicating that the device has been selected as a Target by the Initiator and that the ATN signal was active during Selection.

SEL – Selected

The SEL bit is set at the end of the selection phase indicating that the device has been selected as a Target by the Initiator and that the ATN signal was inactive during Selection.

SCSI Timeout Register (STIMREG)

Address (B)+14H **WRITE ONLY**

7	6	5	4	3	2	1	0
STIM7	STIM6	STIM5	STIM4	STIM3	STIM2	STIM1	STIM0
X	X	X	X	X	X	X	X

STIM 7:0 – SCSI Timer 7:0

This register determines how long the Initiator will wait for a response to a Selection before timing out.

Internal State Register (ISREG)

Address (B)+18H **READ ONLY**

7	6	5	4	3	2	1	0
RES	RES	RES	RES	$\overline{SOF}$	IS2	IS1	IS0
X	X	X	X	0	0	0	0

The Internal State Register (ISREG) tracks the progress of a sequence-type command.

RES – Reserved

SOF – Synchronous Offset Flag

The SOF is reset when the Synchronous Offset Register (SOFREG) has reached its maximum value.

IS 2:0 – Internal State 2:0

The IS 2:0 bits along with the Interrupt Status Register (INSTREG) indicates the status of the successfully completed intermediate operation.

Synchronous Transfer Period Register (STPREG)

Address (B)+18H **WRITE**

7	6	5	4	3	2	1	0
RES	RES	RES	STP4	STP3	STP2	STP1	STP0
X	X	X	0	0	1	0	1

RES – Reserved

STP 4:0 – Synchronous Transfer Period 4:0

These bits specify the synchronous transfer period or the number of clock cycles for each byte transferred in the synchronous mode.

Current FIFO/Internal State Register (CFISREG)

Address (B)+ 1CH **READ ONLY**

7	6	5	4	3	2	1	0
IS2	IS1	IS0	CF4	CF3	CF2	CF1	CF0
0	0	0	0	0	0	0	0

This register has two fields, the Current FIFO field and the Internal State field.

IS 2:0 – Internal State 2:0

The Internal State Register (ISREG) tracks the progress of a sequence-type command.

CF 4:0 – Current FIFO 4:0

The CF 4:0 bits are the binary coded value of the number of bytes in the SCSI FIFO.

Synchronous Offset Register (SOFREG)

Address (B)+ 1CH **WRITE**

7	6	5	4	3	2	1	0
RAD1	RAD0	RAA1	RAA0	SO3	SO2	SO1	SO0
0	0	0	0	0	0	0	0

RAD 1:0 – REQ/ACK Deassertion Control

These bits may be programmed to control the deassertion delay of the REQ and ACK signals during synchronous transfers.

RAA 1:0 – REQ/ACK Assertion Control 1:0

These bits may be programmed to control the assertion delay of the REQ and ACK signals during synchronous transfers.

SO 3:0 – Synchronous Offset 3:0

The SO 3:0 bits are the binary coded value of the number of bytes that can be sent to (or received from) the SCSI bus without an ACK (or REQ) signal.

Control Register One (CNTLREG1)

Address (B)+20H **READ/WRITE**

7	6	5	4	3	2	1	0
ETM	DISR	RES	PERE	RES	SID2	SID1	SID0
0	0	0	0	0	X	X	X

The Control Register 1 (CNTLREG1) sets up the device with various operating parameters.

ETM – Extended Timing Mode

Enabling this feature will increase the minimum setup time for data being transmitted on the SCSI bus.

DISR – Disable Interrupt on SCSI Reset

The DISR bit masks the reporting of the SCSI reset.

RES – Reserved

This bit is reserved and **must always be set to '0'.**

PERE – Parity Error Reporting Enable

The PERE bit enables the checking and reporting of parity errors on incoming SCSI bytes during the information transfer phase.

RES – Reserved

This bit is reserved and **must always be set to '0'.**

SID 2:0 – SCSI Device ID 2:0

The SID 2:0 bits specify the binary coded value of the device ID on the SCSI bus.

3/86 1 2

Clock Factor Register (CLKFREG)

Address (B)+24H **WRITE**

7	6	5	4	3	2	1	0
RES	RES	RES	RES	RES	CLKF2	CLKF1	CLKF0
X	X	X	X	X	0	1	0

The Clock Factor Register (CLKFREG) must be set to indicate the input frequency range of the device.

RES – Reserved

This bit is reserved and **must always be set to '0'**.

CLKF 2:0 – Clock Factor 2:0

The CLKF 2:0 bits specify the binary coded value of the clock factor.

Reserved

Address (B)+28H **WRITE**

7	6	5	4	3	2	1	0
RES	RES	RES	RES	RES	RES	RES	RES
X	X	X	X	X	X	X	X

RES – Reserved

This register is reserved. Its value must always be set to '00h'.

Control Register Two (CNTLREG2)

Address (B)+2CH **READ/WRITE**

7	6	5	4	3	2	1	0
RES	ENF	RES	RES	S2FE	RES	RES	RES
0	0	0	0	0	0	0	0

The Control Register Two (CNTLREG2) sets up the device with various operating parameters.

RES – Reserved

This bit is reserved and **must always be set to '0'**.

ENF – Enable Features

This bit activates the following product enhancements:

- The Current Transfer Count Register High ((B)+38H) will be enabled, extending the transfer counter from 16 to 24 bits to allow for larger transfers.
- Following a chip or power on reset, up until the point where the Current Transfer Count Register High ((B)+38H) is loaded with a value, it is possible to read the part-unique ID '12h' from this register.
- The SCSI phase will be latched at the completion of each command by bits 2:0 in the Status Register (STATREG). When this bit is '0,' the Status Register (STATREG) will reflect real-time SCSI phases.

S2FE – SCSI-2 Features Enable

The S2FE bit allows the device to recognize two SCSI-2 features: the extended message feature and the Group 2 command recognition. (These features can also be controlled independently by bits 6:5 in CNTLREG3).

Extended Message Feature: When the S2FE bit is set and the device is selected with attention, the device will monitor the ATN signal at the end of the first message byte. If the ATN signal is active, the device will request two more message bytes before switching to the command phase. If the ATN signal is inactive the device will switch to the Command phase. When the S2FE bit is reset as a Target, the device will request a single message byte.

Group 2 Command Recognition: When the S2FE bit is set, Group 2 commands can be recognized as 10-byte commands. When the S2FE bit is reset, the device will interpret Group 2 commands as reserved commands. Thus, the Am53C974A will only request 6-byte commands.

Control Register Three (CNTLREG3)

Address (B)+30H **READ/WRITE**

7	6	5	4	3	2	1	0
ADID CHK	QTAG	G2CB	FAST-SCSI	FASTCLK	RES	RES	RES
0	0	0	0	0	0	0	0

ADID CHK – Additional ID Check

Enables additional check on ID message during bus-initiated Select or Reselect with $\overline{ATN}$.

QTAG – QTAG Control

This bit controls the Queue Tag feature in the Am53C974A. When enabled, the Am53C974A is capable of receiving 3-byte messages during bus-initiated Select/Reselect with ATN.

G2CB – Group 2 Command Block

When this bit is set, the Am53C974A is capable of recognizing 10-byte Group 2 Commands as valid CDBs (Command Descriptor Blocks). (This feature is also controlled by bit 3 of CNTLREG2).

FASTSCSI – Fast SCSI
FASTCLK – Fast Clock

These bits configure the SCSI Core's state machine to support both Fast SCSI timings and SCSI-1 timings.

RES – Reserved

This bit is reserved and **must always be set to '0'.**

RES – Reserved – READ-ONLY (Tied Low)

This reserved bit is internally tied low and is read-only.

RES – Reserved

This bit is reserved and **must always be set to '0'.**

Control Register Four (CNTLREG4)

Address (B)+34H **READ/WRITE**

7	6	5	4	3	2	1	0
GE1	GE0	PWD	RES	RES (R) RAE (W)	RADE	RES	RES
0	0	0	X	0	0	X	X

This register is used to control several AMD proprietary features implemented in the SCSI Core. At power up, this register will show a '0' value on all bits except bit 4.

GE1:0 – GLITCH EATER 1:0

The GLITCH EATER circuitry has been implemented on $\overline{REQ}$, $\overline{ACK}$, and DATA lines and are controlled by bits 7 and 6. The valid signal window may be adjusted by setting the bits in the combinations listed below.

GE1	GE0	Valid Signal Window
0	0	12 ns
1	0	25 ns
0	1	35 ns
1	1	0 ns

PWD – Power-Down Feature

Setting this bit to '1' turns off the input buffers on all the SCSI bus signal lines.

RES – Reserved

This bit is reserved for internal use.

RES – Reserved (Read Only)

This bit is reserved for internal use.

RAE – (Write Only) – Active Negation Control
RADE – Active Negation Control

RAE and RADE Bits 2 and 3 control the Active Negation Drivers which may be enabled on $\overline{REQ}$, $\overline{ACK}$, or DATA lines.

The programming options for this feature are as follows:

RAE	RADE	Function Selected
0	0	Active Negation Disabled
1	0	Active Negation on $\overline{REQ}$ and $\overline{ACK}$ only
X	1	Active Negation on $\overline{REQ}$, $\overline{ACK}$ and DATA

RES – Reserved

This bit is reserved for internal use.

RES – Reserved

This bit is reserved and **must always be set to '0'.**

Reserved

Address (B)+3CH **WRITE**

7	6	5	4	3	2	1	0
RES	RES	RES	RES	RES	RES	RES	RES
0	0	0	0	0	0	0	0

RES – Reserved

This register is reserved. Its value must always be set to '00h'.

Part-Unique ID Register ((B)+38H) Read Only

This register extends the transfer counter from 16 to 24 bits and is only enabled when the ENF bit is set (bit 6, Control Register Two).

This register is also used to store the part-unique ID code for the SCSI. This information may be accessed when all of the following are true:

- A power up or chip reset has taken place
- A value has not been loaded into this register

31861 2D 32PG

SCSI Commands

The following is a summary of the SCSI commands supported by the SCSI Core. For a more detailed description, refer to the *Am53C974A Technical Manual.*

Table 5. Summary of Commands

Command	Code (Hex.)	
	Non-DMA Mode	DMA Mode
Initiator Commands		
Information Transfer	10	90
Initiator Command Complete Steps	11	91
Message Accepted	12	–
Transfer Pad Bytes	–	98
Set ATN*	1A	–
Reset ATN*	1B	–
Target Commands		
Send Message	20	A0
Send Status	21	A1
Send Data	22	A2
Disconnect Steps	23	A3
Terminate Steps	24	A4
Target Command Complete Steps	25	A5
Disconnect	27	–
Receive Message	28	A8
Receive Commands	29	A9
Receive Data	2A	AA
Receive Command Steps	2B	AB
DMA Stop Command	04	–
Access FIFO Command	–	85
Idle State Commands		
Select without ATN Steps	41	C1
Select with ATN Steps	42	C2
Select with ATN and Stop Steps	43	C3
Enable Selection/Reselection*	44	C4
Disable Selection/Reselection	45	–
Select with ATN3 Steps	46	C6
Reselect with ATN3 Steps	47	C7
General Commands		
No Operation*	00	80
Clear FIFO*	01	–
Reset Device*	02	–
Reset SCSI Bus**	03	–

Notes:

** These commands do not generate interrupt.*

***An interrupt is generated when SCSI bus reset interrupt reporting is not disabled (see Control Register1/DISR bit6).*

SCAM Support

The Am53C974A supports Level 1 SCAM as defined in the X3T9.2/93-109r5 (September 30,1993) specification. SCAM (SCSI Configured AutoMagically) is a protocol to assign IDs to SCSI devices after power-on or after a SCSI bus reset. Various types of devices, SCAM master devices, SCAM slave devices, SCAM tolerant devices, and SCAM intolerant devices, can be connected to a SCAM capable SCSI bus. The Am53C974A supports the following requirements for SCAM Master Level 1 implementation:

- Perform SCAM selection.
- Have a hard ID.
- Recognize SCSI bus reset conditions.
- Use selection time-out.
- Shall not assert SCSI RST upon selection time-out.

Additionally, the following must be true to insure that the SCAM procedure is executed properly:

- The Am53C974A will be the only master on the SCSI bus.
- Slaves will power-up concurrently or before the master.

SCAM Implementation:

SCAM operation is controlled by bits 18:0 of register address (B)+70h. Of these 19-bits, bit 18 controls the SCAM enable/disable feature. At power-up, bit 18 will default to '0' and the SCAM logic is disabled. Under this condition, bits 17:0 will reflect the current state of the SCSI bus signals. When bit 18 is '1', the SCAM feature is enabled and bits 17:0 are programmable for SCAM protocol implementation. Note that the SCAM feature should only be enabled when there is no pending or ongoing chip activity. Refer to the SBAC register for a description of each bit.

23	22	21	20	19	18	17	16
RES	RES	PWD	SBSY	SCLK	SCAM	REQ	ACK

15	14	13	12	11	10	9	8
RST	BSY	SEL	ATN	MSG	C/D	I/O	SDP

7	6	5	4	3	2	1	0
SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
Under Bias . . . . . –55°C to +125°C

V_{DD} . . . . . –0.5 V to +7.0 V

DC Voltage Applied
to Any Pin . . . . . –0.5 to (V_{DD} +0.5) V

Input Static Discharge Protection . . . . 2K V pin-to-pin
(Human body model: 100 pF at 1.5K Ω)

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . 0°C to +70°C

Supply Voltage (V_{DD}) . . . . . 4.75 V to 5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

31861 2B

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Parameter Symbol	Parameter Description	Pin Names	Test Conditions	Min	Max	Unit
I_{DDS}	Static Supply Current		V_{DD} MAX		8	mA
I_{DDSM}	Supply Current (Power-Down Mode)		V_{DD} MAX		3	
I_{DDD}	Dynamic Supply Current		V_{DD} MAX		110	mA
I_{LU}	Latch Up Current (Note 1)	All I/O	$V_{LU} \leq 10$ V	−100	+100	mA
SCSI and Power Management Pins						
V_{IH}	Input High Voltage	All SCSI Inputs, PWDN		2.0	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage	All SCSI Inputs, PWDN		V_{SS} − 0.5	0.8	V
V_{IHST}	Input Hysteresis (Note 1)	All SCSI Inputs	4.75 V < V_{DD} < 5.25 V	300		mV
V_{OH}	Output High Voltage (Note 2)		I_{OH} = −2 mA (Note 3)	2.4	V_{DD}	V
V_{SOL1}	SCSI Output Low Voltage	$\overline{SD}$ [7:0], $\overline{SD}$ P	I_{OL} = 4 mA	V_{SS}	0.4	V
V_{SOL2}	SCSI Output Low Voltage	$\overline{ATN}$, $\overline{BSY}$, $\overline{SEL}$, $\overline{SCSI\ RST}$, $\overline{ACK}$	I_{OL} = 48 mA	V_{SS}	0.5	V
I_{IL}	Input Low Leakage	All SCSI Inputs, PWDN	0.0 V < V_{IN} < 2.7 V	−10	+10	µA
I_{IH}	Input High Leakage	All SCSI Inputs, PWDN	2.7 V < V_{IN} < V_{DD}	−10	+10	µA
I_{OZ}	High Impedance Leakage	All I/O Pins	0.4 V < V_{OUT} < V_{DD}	−10	+10	µA
PCI Pins						
V_{IH}	Input High Voltage			2.0	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage			V_{SS} − 0.5	0.8	V
V_{OH}	Output High Voltage (Note 2)		I_{OH} = −2 mA (Note 3)	2.4	V_{DD}	V
V_{OL1}	Output Low Voltage	AD [31:00], C/$\overline{BE}$ [3:0], PAR, $\overline{PCI\ REQ}$	I_{OL} = 3 mA	V_{SS}	0.45	V
V_{OL2}	Output Low Voltage	$\overline{FRAME}$, $\overline{TRDY}$, $\overline{IRDY}$, $\overline{STOP}$, $\overline{DEVSEL}$, $\overline{LOCK}$, $\overline{PERR}$, $\overline{SERR}$, $\overline{INTA}$	I_{OL} = 6 mA	V_{SS}	0.45	V
I_{IL}	Input Low Leakage		0 V ≤ V_{IN} ≤ V_{IL}	−10	+10	µA
I_{IH}	Input High Leakage		V_{IH} ≤ V_{IN} ≤ V_{DD}	−10	+10	µA
I_{OZ}	High Impedance Leakage	All I/O Pins	0.4 V < V_{OUT} < V_{DD}	−10	+10	µA

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*
2. *V_{OH} does not apply to open-drain output pins.*
3. *Outputs are CMOS and will be driven to rail if the load is not resistive.*

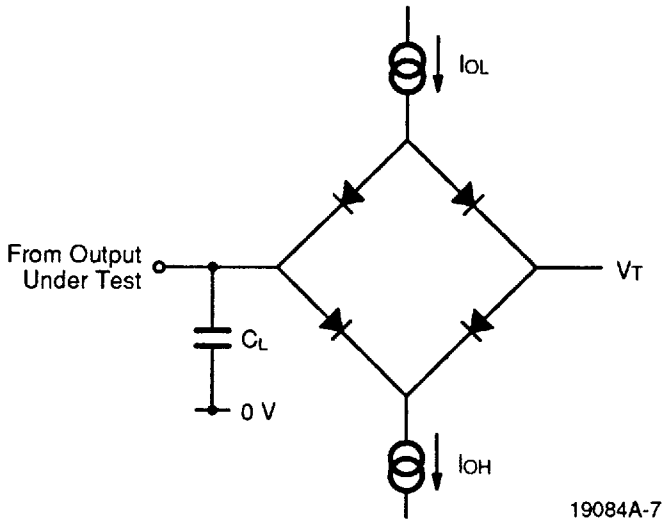
DC CHARACTERISTICS (continued)

Parameter Symbol	Parameter Description	Pin Names	Test Conditions	Min	Max	Unit
Pin Capacitance (V_{CC} = 5.0 V, T_A = 25 C, f = 1.0 MHz)						
C_{IN}	Input Pins	All SCSI Inputs All PCI Inputs except IDSEL, PWDN	V_{IN} = 0 V		10	pF
		IDSEL	V_{IN} = 0 V		8	pF
$C_{I/O}$	I/O or Output Pins	All SCSI, PCI Output and I/O Pins, $\overline{BUSY}$	$V_{I/O}$ = 0 V		12	pF
C_{CLK}	Clock Pins	CLK (PCI) SCSI CLK1 SCSI CLK2	V_{IN} = 0 V		12	pF

Note:

These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING TEST CIRCUIT

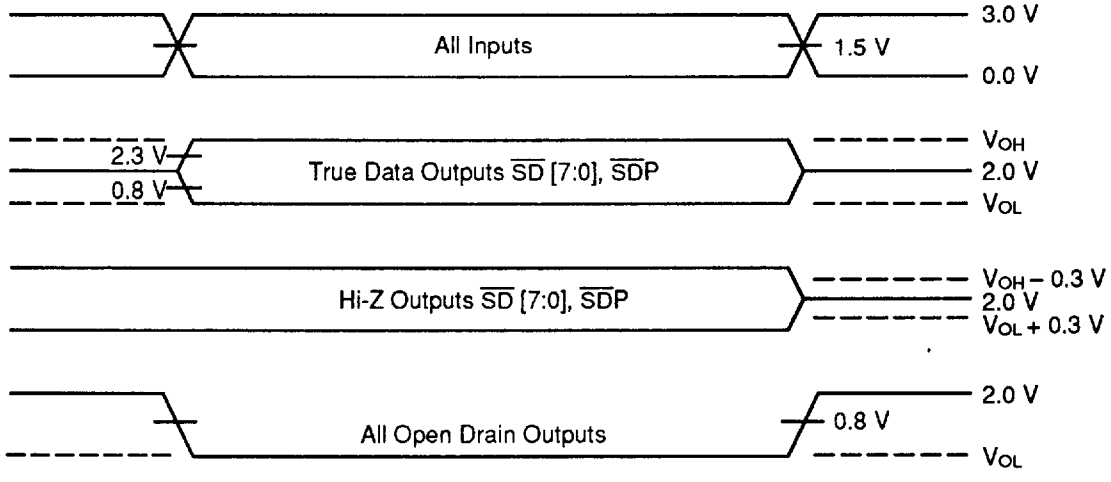


KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

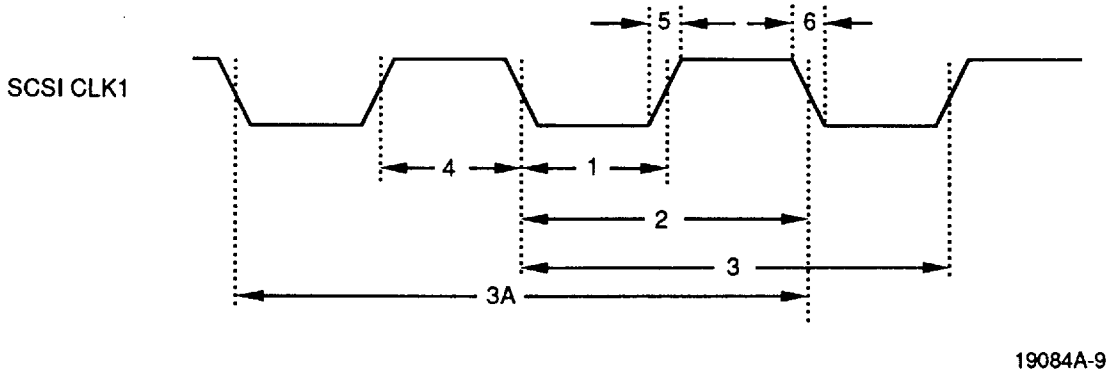
SWITCHING TEST WAVEFORMS



19084A-8

AC SWITCHING CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

SCSI Interface



Clock Input

FastClk Disabled (Control Register Three (0CH) bit 3=0)

No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
1	t_{PWL}[1]	Clock Pulse Width Low		14.58	0.65 • t_{CP}	ns
2	t_{CP}	Clock Period (1 ÷ Clock Frequency)		40	100	ns
3	t_L	Synchronization Latency		54.58	t_{PWL} + t_{CP}	ns
4	t_{PWH}[1]	Clock Pulse Width High		14.58	0.65 • t_{CP}	ns
5	t_{RISE}*	Clock Rise Time	over 2 V p-p	1	4	V/ns
6	t_{FALL}*	Clock Fall Time	over 2 V p-p	1	4	V/ns

Notes:

1. *For Synchronous data transmissions, the following conditions must be true:*

   $2t_{CP} + t_{PWL} \geq 97.92$ ns
   $2t_{CP} + t_{PWH} \geq 97.92$ ns

Clock Frequency Range for Fast Clk disabled.

- *10 MHz to 25 MHz for Asynchronous Transmission*
- *12 MHz to 25 MHz for Synchronous Transmission*

* *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

FastClk Enabled (Control Register Three (0CH) bit 3=1)

No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
1	t_{PWL}	Clock Pulse Width Low		0.4 • t_{CP}	0.6 • t_{CP}	ns
2	t_{CP}	Clock Period (1 ÷ Clock Frequency)		25	50	ns
3A	t_L	Synchronization Latency		54.58	2 • t_{CP}	ns
4	t_{PWH}	Clock Pulse Width High		0.4 • t_{CP}	0.6 • t_{CP}	ns
5	t_{RISE}*	Clock Rise Time	over 2 V p-p	1	4	V/ns
6	t_{FALL}*	Clock Fall Time	over 2 V p-p	1	4	V/ns

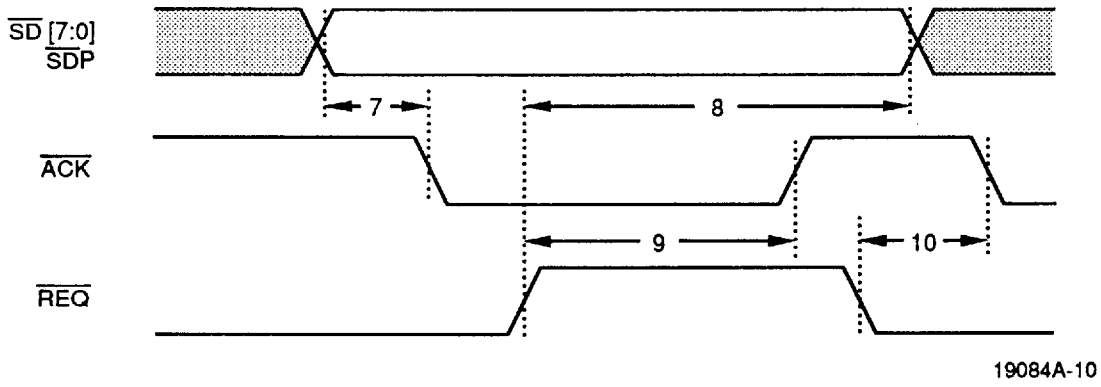
Notes:

Clock Frequency Range for Fast Clk enabled.

- *20 MHz to 40 MHz for Asynchronous Transmission*
- *20 MHz to 40 MHz for Synchronous Transmission*

* *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.*

AC SWITCHING CHARACTERISTICS (continued)

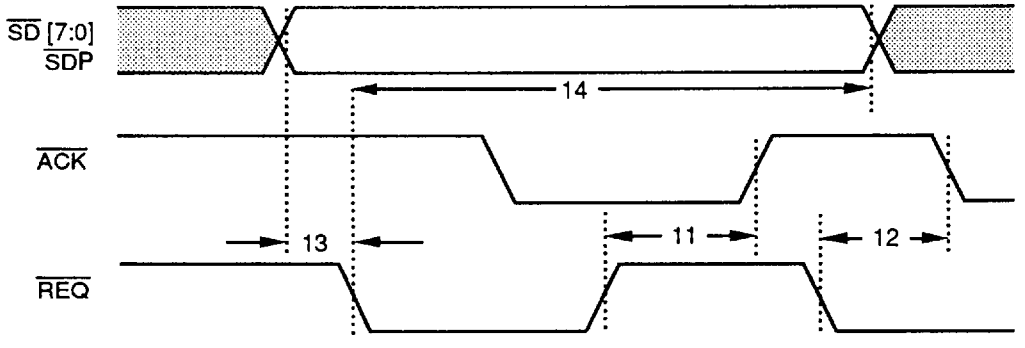


19084A-10

Asynchronous Initiator Send

Single Ended:

No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
7	t_S	Data to ACK ↓ Set Up Time		60		ns
8	t_{PD}	REQ ↓ to Data Delay		5		ns
9	t_{PD}	REQ ↓ to ACK ↓ Delay			50	ns
10	t_{PD}	REQ ↑ to ACK ↑ Delay			50	ns



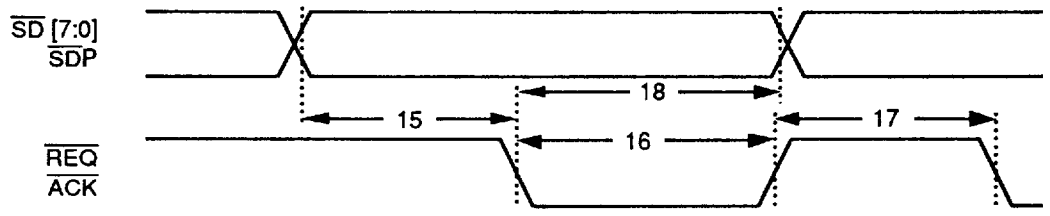
19084A-11

Asynchronous Initiator Receive

Single Ended:

No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
11	t_{PD}	REQ ↓ to ACK ↓ Delay			50	ns
12	t_{PD}	REQ ↑ to ACK ↑ Delay			50	ns
13	t_S	Data to REQ ↑ Set Up Time		10		ns
14	t_H	REQ ↑ to Data Hold Time		18		ns

AC SWITCHING CHARACTERISTICS (continued)



19084A-12

Synchronous Initiator Transmit

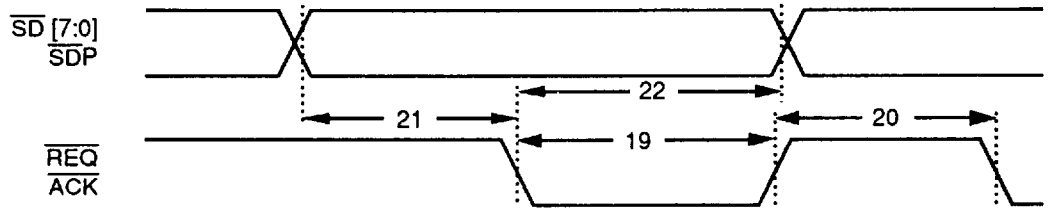
Normal SCSI: (Single Ended)

No.	Parameter Symbol	Parameter Description	Test Conditions	Min*	Max	Unit
15	t_S	Data to REQ or ACK ↓ Set Up Time		55		ns
16	t_{PWL}	REQ or ACK Pulse Width Low		90		ns
17	t_{PWH}	REQ or ACK Pulse Width High		90		ns
18	t_H	ACK or REQ ↓ to Data Hold Time		100		ns

Fast SCSI: (Single Ended)

No.	Parameter Symbol	Parameter Description	Test Conditions	Min*	Max	Unit
15	t_S	Data to REQ or ACK ↓ Set Up Time		25		ns
16	t_{PWL}	REQ or ACK Pulse Width Low		30		ns
17	t_{PWH}	REQ or ACK Pulse Width High		30		ns
18	t_H	ACK or REQ ↓ to Data Hold Time		35		ns

** The minimum values have a wide range since they depend on the Synchronization latency. The synchronization latency, in turn, depends on the operating frequency of the device.*



19084A-13

Synchronous Initiator Receive

No.	Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
19	t_{PWL}	REQ Pulse Width Low		27		ns
19	t_{PWL}	ACK Pulse Width Low		20		ns
20	t_{PWH}	REQ Pulse Width High		20		ns
20	t_{PWH}	ACK Pulse Width High		20		ns
21	t_S	Data to REQ or ACK ↓ Set Up Time		10		ns
22	t_H	REQ or ACK ↓ to Data Hold Time		15		ns

AC SWITCHING CHARACTERISTICS (continued)

SCSI Bus Lines

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
t_{RISE}	Rise Time, 10% to 90%	SCSI Termination + 20 pF	8	20	ns
t_{FALL}	Fall Time, 10% to 90%	SCSI Termination + 20 pF	5	12	ns
dV_H/dt	Slew Rate, Low to High	SCSI Termination + 20 pF	0.15	0.50	V/ns
dV_L/dt	Slew Rate, High to Low	SCSI Termination + 20 pF	0.25	0.80	V/ns

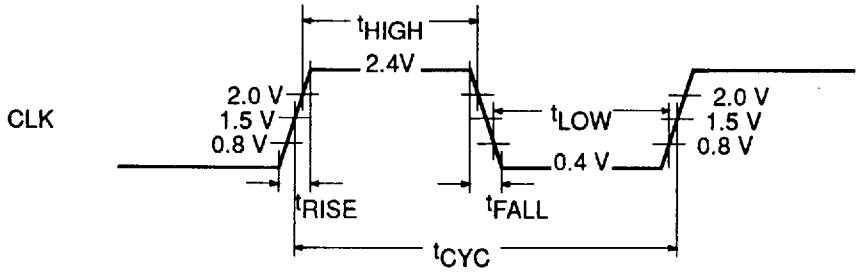
Note:

These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

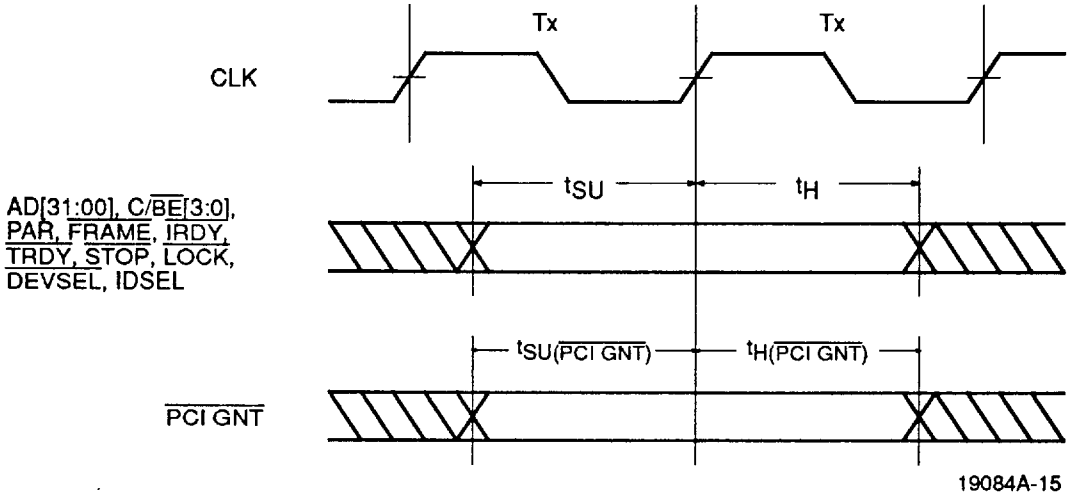
AC SWITCHING CHARACTERISTICS
PCI Bus Interface Unit

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
Clock Timing					
	CLK Frequency		0	33	MHz
t_{CYC}	CLK Period	At 1.5 V	30	∞	ns
t_{HIGH}	CLK High Time	At 2.0 V	12		ns
t_{LOW}	CLK Low Time	At 0.8 V	12		ns
t_{FALL}	CLK Fall Time	over 2 V p-p	1	4	V/ns
t_{RISE}	CLK Rise Time	over 2 V p-p	1	4	V/ns
Output and Float Delay Timing					
t_{VAL}	AD[31:00], C/$\overline{BE}$[3:0], PAR, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{LOCK}$, $\overline{DEVSEL}$, $\overline{PERR}$, $\overline{SERR}$ Valid Delay		2	11	ns
t_{VAL} ($\overline{PCI\ REQ}$)	$\overline{PCI\ REQ}$ Valid Delay		1	12	ns
t_{ON}	AD[31:00], C/$\overline{BE}$[3:0], PAR, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{LOCK}$, $\overline{DEVSEL}$ Active Delay		2	11	ns
t_{OFF}	AD[31:00], C/$\overline{BE}$[3:0], PAR, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{LOCK}$, $\overline{DEVSEL}$ Float Delay			28	ns
Setup and Hold Timing					
t_{SU}	AD[31:00], C/$\overline{BE}$[3:0], PAR, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{LOCK}$, $\overline{DEVSEL}$, IDSEL Setup Time		7		ns
t_H	AD[31:00], C/$\overline{BE}$[3:0], PAR, $\overline{FRAME}$, $\overline{IRDY}$, $\overline{TRDY}$, $\overline{STOP}$, $\overline{LOCK}$, $\overline{DEVSEL}$, IDSEL Hold Time		0		ns
t_{SU} ($\overline{PCI\ GNT}$)	$\overline{PCI\ GNT}$ Setup Time		10		ns
t_H ($\overline{PCI\ GNT}$)	$\overline{PCI\ GNT}$ Hold Time		0		ns

AC SWITCHING WAVEFORMS
PCI Bus Interface Unit (continued)

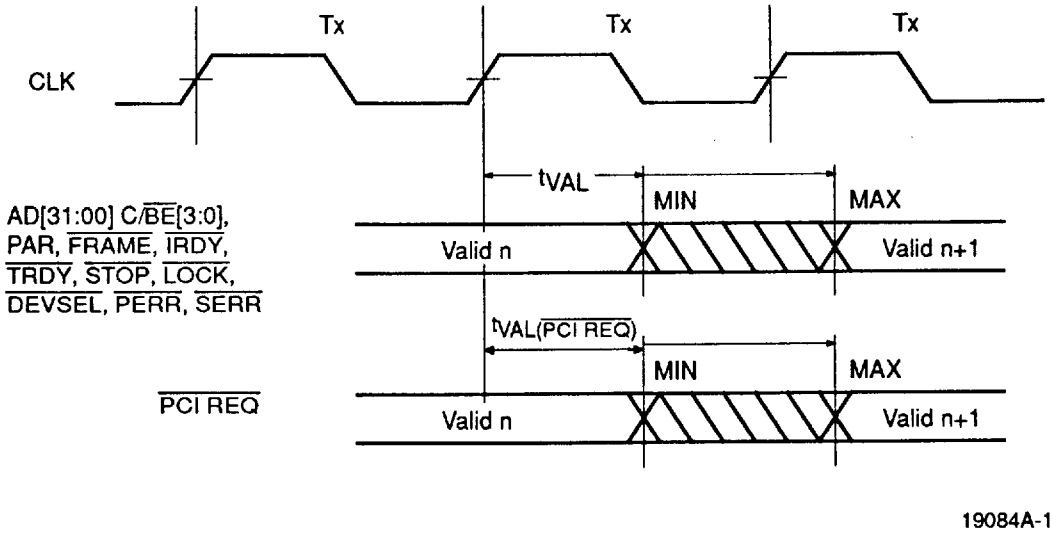


CLK Waveform



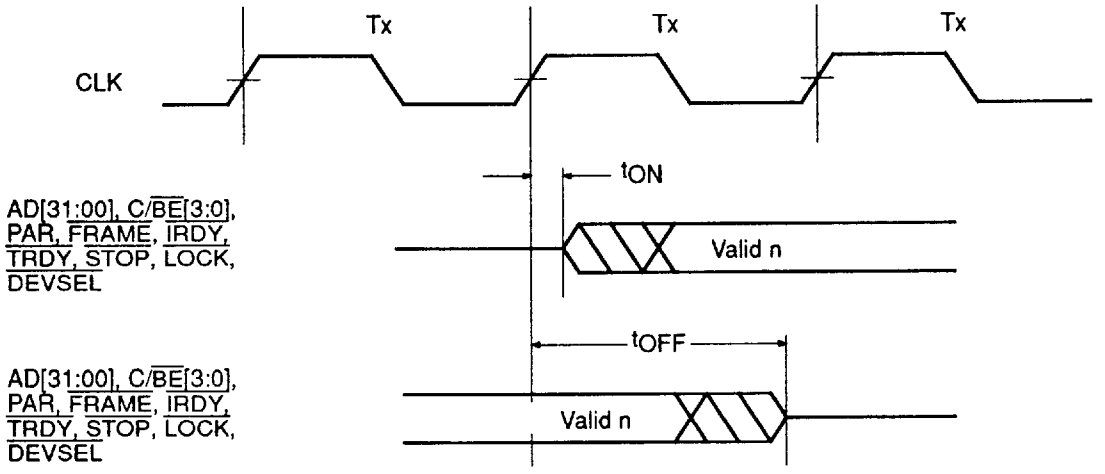
Input Setup and Hold Timing

AC SWITCHING WAVEFORMS
PCI Bus Interface Unit (continued)



19084A-16

Output Valid Delay Timing



19084A-17

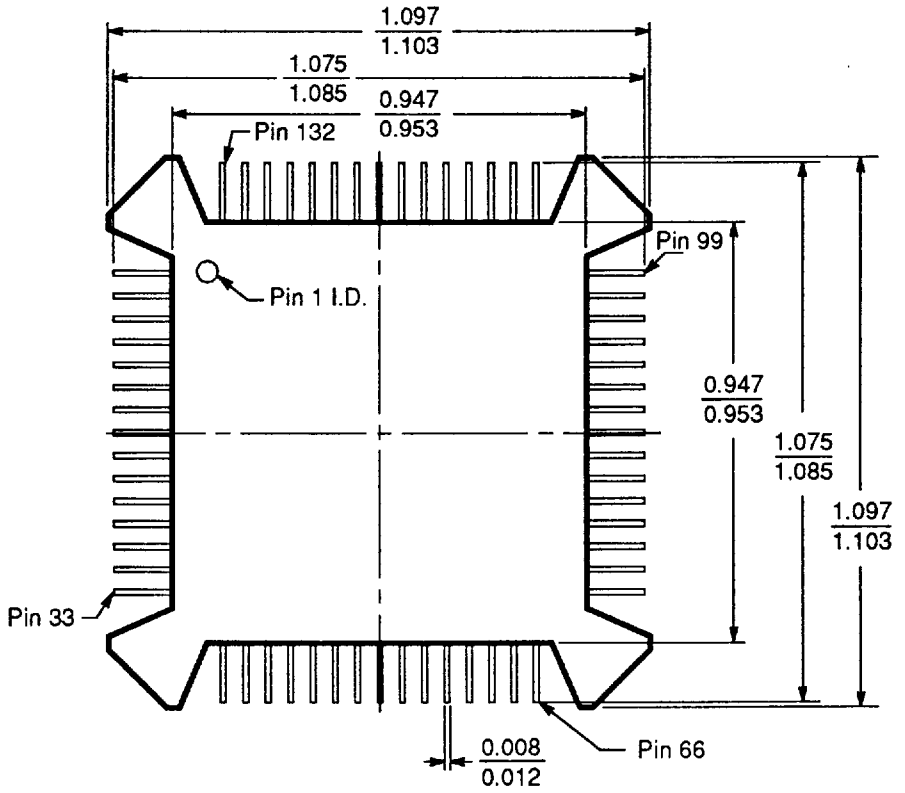
Output Tri-State Delay Timing

31861 1A

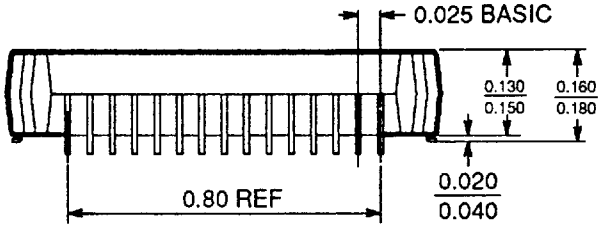
PHYSICAL DIMENSIONS*

PQB132

132-Pin Plastic Quad Flat Pack; Trimmed and Formed (measured in inches)



TOP VIEW



BOTTOM VIEW

16-038-PQB
PQB132
DA87
6-15-94 ae

For reference only, not drawn to scale. BSC is an ANSI standard for Basic Space Centering.