



Integrated Device Technology, Inc.

FAST CMOS OCTAL D FLIP-FLOP WITH MASTER RESET

IDT54/74FCT273T/AT/CT

FEATURES:

- Std., A, and C speed grades
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility
 - $V_{OH} = 3.3\text{V}$ (typ.)
 - $V_{OL} = 0.3\text{V}$ (typ.)
- High drive outputs (-15mA IOH, 48mA IOL)
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, QSOP, CERPACK and LCC packages

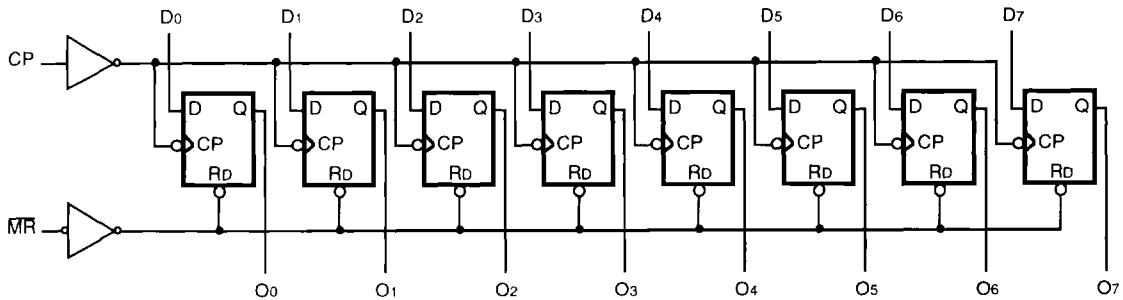
DESCRIPTION:

The IDT54/74FCT273T/AT/CT are octal D flip-flops built using an advanced dual metal CMOS technology. The IDT54/74FCT273T/AT/CT have eight edge-triggered D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) and Master Reset ($\overline{\text{MR}}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{\text{MR}}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

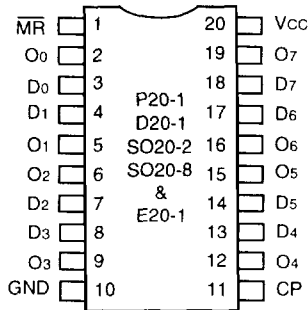
FUNCTIONAL BLOCK DIAGRAM



2568 drw 03

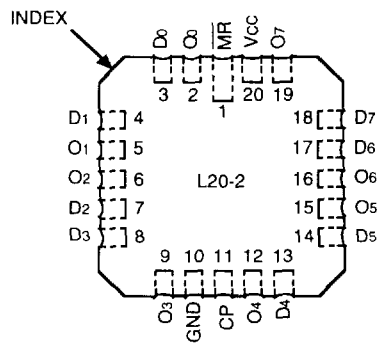
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PIN CONFIGURATIONS



DIP/SOIC/QSOP/CERPACK
TOP VIEW

2568 drw 01



LCC
TOP VIEW

2568 drw 02

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

APRIL 1994

PIN DESCRIPTION

Pin Names	Description
DN	Data Inputs
\overline{MR}	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
ON	Data Outputs

2568 tbl 01

FUNCTION TABLE⁽¹⁾

Operating Mode	Inputs			Outputs
	\overline{MR}	CP	DN	ON
Reset (Clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

2568 tbl 02

NOTE:

- H = HIGH voltage level steady state
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level steady state
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
X = Don't Care
↑ = LOW-to-HIGH Clock Transition

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc +0.5	-0.5 to Vcc +0.5	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	-60 to +120	-60 to +120	mA

2568 lmk 03

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
- Input and Vcc terminals only.
- Outputs and I/O terminals only.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

2568 lmk 04

NOTE:

- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = 0°C to +70°C, VCC = 5.0V ± 5%; Military: TA = -55°C to +125°C, VCC = 5.0V ± 10%

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current ⁽⁴⁾	VCC = Max.	V _I = 2.7V	—	—	±1	μA
I _{IL}	Input LOW Current ⁽⁴⁾	VCC = Max.	V _I = 0.5V	—	—	±1	μA
I _I	Input HIGH Current ⁽⁴⁾	VCC = Max., V _I = VCC (Max.)		—	—	±1	μA
V _{IK}	Clamp Diode Voltage	VCC = Min., I _N = -18mA		—	-0.7	-1.2	V
I _{OS}	Short Circuit Current	VCC = Max. ⁽³⁾ , V _O = GND		-60	-120	-225	mA
V _{OH}	Output HIGH Voltage	VCC = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -6mA MIL. I _{OH} = -8mA COM'L.	2.4	3.3	—	V
			I _{OH} = -12mA MIL. I _{OH} = -15mA COM'L.	2.0	3.0	—	V
V _{OL}	Output LOW Voltage	VCC = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 32mA MIL. I _{OL} = 48mA COM'L.	—	0.3	0.5	V
V _H	Input Hysteresis	—		—	200	—	mV
I _{CC}	Quiescent Power Supply Current	VCC = Max. V _{IN} = GND or VCC		—	0.01	1	mA

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- The test parameter for this parameter is ±5μA at TA = -55°C.

2568 tbi 05

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	VCC = Max. VIN = 3.4V ⁽³⁾		—	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	VCC = Max. Outputs Open MR = VCC One Input Toggling 50% Duty Cycle	VIN = VCC VIN = GND	—	0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	VCC = Max. Outputs Open f _{CP} = 10MHz 50% Duty Cycle MR = VCC One Bit Toggling at fi = 5MHz 50% Duty Cycle	VIN = VCC VIN = GND	—	1.5	3.5	mA
			VIN = 3.4V VIN = GND	—	2.0	5.5	
		VCC = Max. Outputs Open f _{CP} = 10MHz 50% Duty Cycle MR = VCC Eight Bits Toggling at fi = 2.5MHz 50% Duty Cycle	VIN = VCC VIN = GND	—	3.8	7.3 ⁽⁵⁾	
			VIN = 3.4V VIN = GND	—	6.0	16.3 ⁽⁵⁾	

NOTES:

2568 tbl 06

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient.
- Per TTL driven input (VIN = 3.4V); all other inputs at VCC or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} \cdot DH \cdot N_T + I_{CCD} \cdot (f_{CP}/2 + f_i \cdot N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (VIN = 3.4V)
 DH = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at DH
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamperes and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	IDT54/74FCT273T		IDT54/74FCT273AT				IDT54/74FCT273CT				Unit		
			Com'l.		Mil.		Com'l.		Mil.		Com'l.			Mil.	
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.		Min. ⁽²⁾	Max.
tPLH	Propagation Delay CP to ON	CL = 50pF RL = 500Ω	2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	2.0	5.8	2.0	6.5	ns
tPHL	Propagation Delay MR to ON		2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	2.0	6.1	2.0	6.8	ns
tSU	Set-up Time HIGH or LOW DN to CP		3.0	—	3.5	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW DN to CP		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tW	MR Pulse Width LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tREM	Recovery Time MR to CP		4.0	—	5.0	—	2.0	—	2.5	—	2.0	—	2.5	—	ns

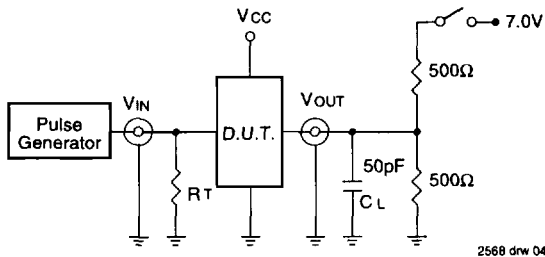
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2568 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2568 drw 04

SWITCH POSITION

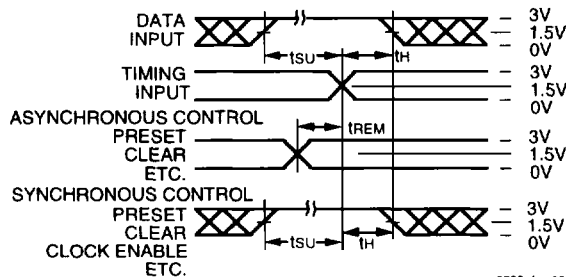
Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

2568 Ink 08

DEFINITIONS:

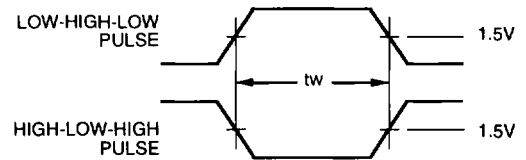
CL= Load capacitance: includes jig and probe capacitance.
 RT = Termination resistance: should be equal to Zout of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



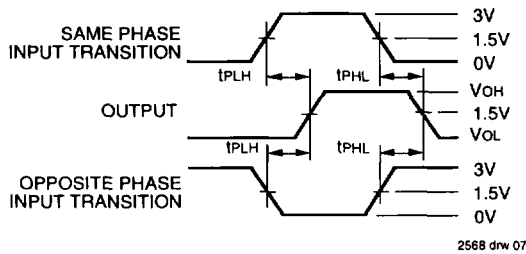
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PULSE WIDTH



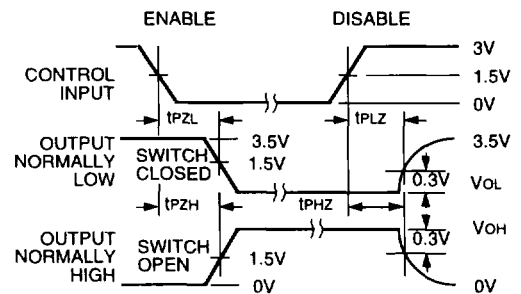
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PROPAGATION DELAY



2568 drw 07

ENABLE AND DISABLE TIMES

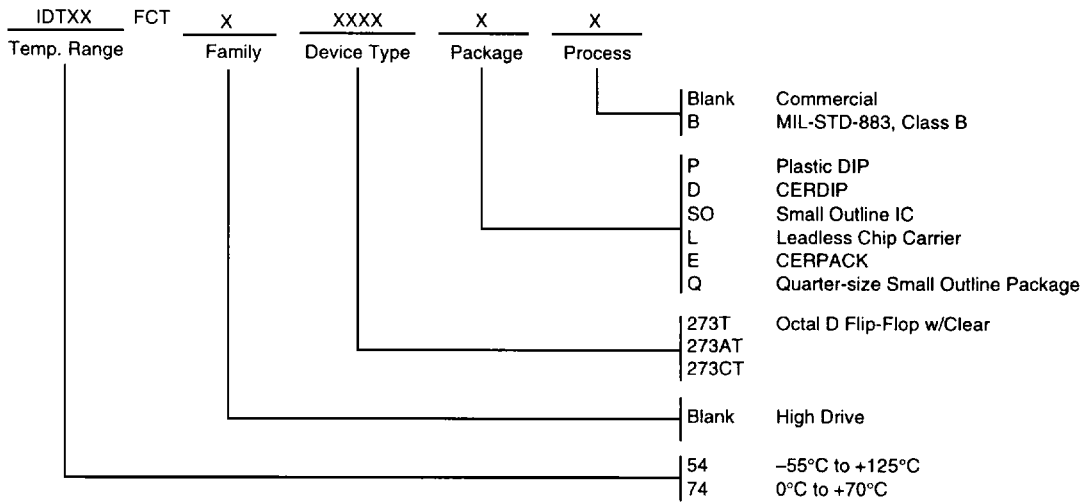


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NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate \leq 1.0MHz; $t_r \leq$ 2.5ns; $t_R \leq$ 2.5ns

ORDERING INFORMATION



256B drw 09