Signetics

74221
Multivibrator

Dual Monostable Multivibrator
Product Specification

Logic Products

FEATURES

- **Pulse width variance is typically less than ±0.5% for 98% of the units**
- **The '221 demonstrates electrical and switching characteristics that are virtually identical to the '121 one-shots**
- **Pin-out is identical to the '123**
- **Overriding Reset terminates output pulse**
- **B input has hysteresis for improved noise immunity**
- **Maximum pulse width:**
  54221: 21 seconds
  74221: 28 seconds

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74221	42ns	36mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74221N
Plastic SO-16	N74221D

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

DESCRIPTION

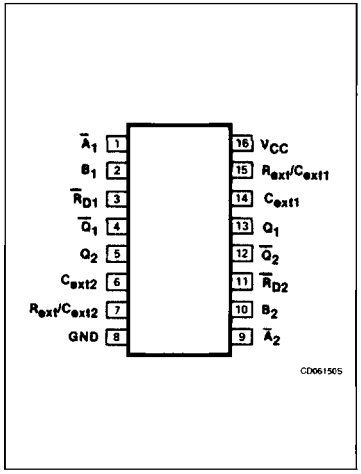
The '221 is a dual monostable multivibrator with performance characteristics virtually identical to those of the '121. Each multivibrator features an active LOW going edge input ($\overline{A}$) and an active HIGH going edge input (B), either of which can be used as an Enable input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

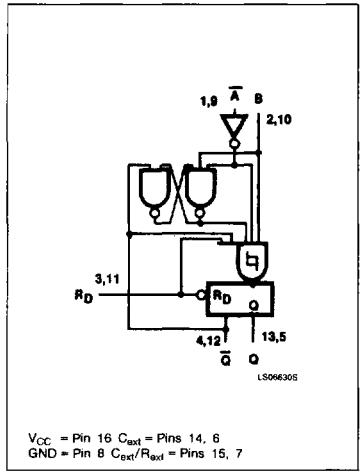
Once fired, the outputs are independent of further transitions of the $\overline{A}$ and B inputs and are a function of the timing components. The output pulses can be terminated by the overriding active LOW Reset ($\overline{R}_D$). Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35 nanoseconds to the maximums shown in the FEATURES by choosing appropriate timing components. With R_{ext} = 2kΩ and C_{ext} = 0, an output pulse of typically 30 nanoseconds is achieved which may be used as a dc triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

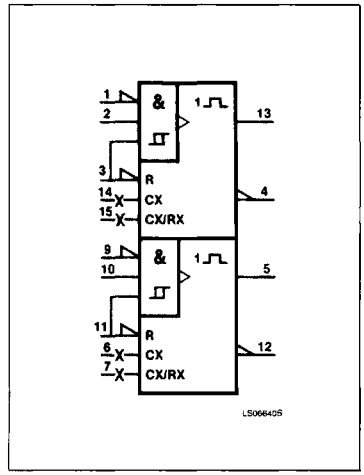
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10pF to 10μF) and more than one decade of timing resistance (2kΩ to 30kΩ for the 54221 and 2kΩ to 40kΩ for the 74221). Throughout these ranges, pulse width is defined by the following relationship: (see Figure A)

$$t_{W(out)} = C_{ext}R_{ext}\ln 2$$
$$t_{W(out)} \cong 0.7C_{ext}R_{ext}$$

In circuits where pulse cutoff is not critical, timing capacitance up to 1000μF and timing resistance as low as 1.4kΩ may be used.

Pin assignments for these devices are identical to those of the '123 so that the '221 can be substituted for those products in systems not using the retrigger by merely changing the value of R_{ext} and/or C_{ext}.

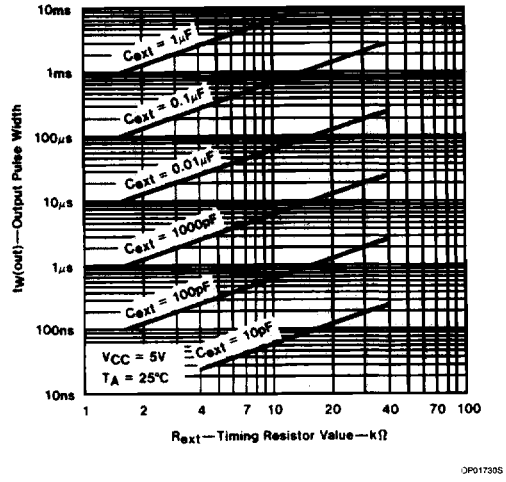


Figure 1. Output Pulse Width vs Timing Resistor Value

FUNCTION TABLE
(Each monostable)

INPUTS			OUTPUTS	
$\overline{R}_D$	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎
In addition, see description and switching characteristics.				

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
⎍ = one HIGH-level pulse
⎎ = one LOW-level pulse

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74
$\overline{A}$	Input	1ul
B, $\overline{R}_D$	Inputs	2ul
All	Outputs	10ul

NOTE:
A 74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
I_{IK}	Input clamp current			−12	mA
I_{OH}	HIGH-level output current			−800	μA
I_{OL}	LOW-level output current			16	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74221			UNIT
				Min	Typ[2]	Max	
V_{T+}	Positive-going threshold at $\overline{A}$ and B	V_{CC} = MIN				2.0	V
V_{T-}	Negative-going threshold at $\overline{A}$ and B	V_{CC} = MIN		0.8			V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, I_{OH} = MAX		2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, I_{OL} = MAX			0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V	$\overline{A}$ input			40	μA
			B, $\overline{R}_D$ inputs			80	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	$\overline{A}$ input			−1.6	mA
			B, $\overline{R}_D$ inputs			−3.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−18		−55	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	Quiescent		26	50	mA
			Triggered		46	80	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

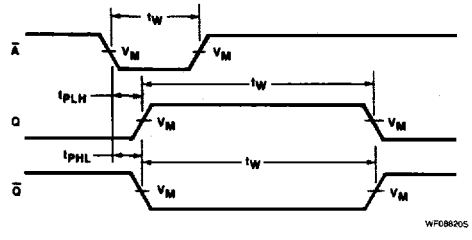
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	74		UNIT
			C_L = 15pF, R_L = 400Ω		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ input to Q & $\overline{Q}$ output	Waveform 1 C_{ext} = 80pF, R_{ext} = 2kΩ		70 80	ns ns
t_{PLH} t_{PHL}	Propagation delay B input to Q & $\overline{Q}$ output	Waveform 2 C_{ext} = 80pF, R_{ext} = 2kΩ		55 65	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{R}_D$ input to Q & $\overline{Q}$ output	Waveform 3 C_{ext} = 80pF, R_{ext} = 2kΩ		40 27	ns ns
t_W	Minimum output pulse width	C_{ext} = 0pF, R_{ext} = 2kΩ	20	50	ns
t_W	Output pulse width	C_{ext} = 80pF, R_{ext} = 2kΩ	70	150	ns
		C_{ext} = 100pF, R_{ext} = 10kΩ	650	750	ns
		C_{ext} = 1μF, R_{ext} = 10kΩ	6.5	7.5	ms

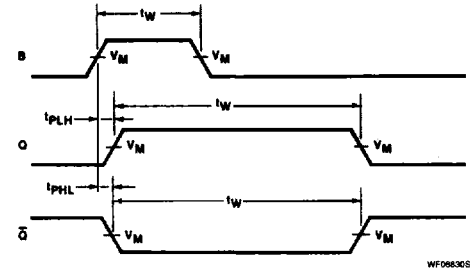
AC SET-UP REQUIREMENTS

PARAMETER		TEST CONDITIONS	74		UNIT
			Min	Max	
t_W	Minimum input pulse width to trigger	Waveforms 1 & 2	50		ns
t_W	Minimum reset pulse width	Waveform 3	20		ns
t_{rec}	Recovery time from reset to trigger input	Waveform 3	15		ns
R_{ext}	External timing resistor range		1.4	40	kΩ
C_{ext}	External timing capacitance range		0	1000	μF
	Output duty cycle	R_{ext} = 2kΩ		67	%
		R_{ext} = R_{ext} (MAX)		90	%

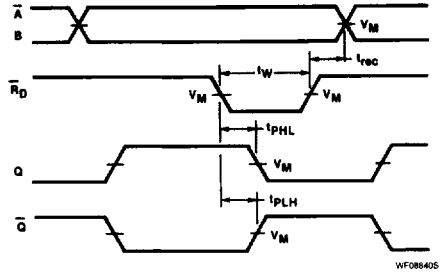
AC WAVEFORMS



Waveform 1. Propagation Delay $\overline{A}$ Input To Q And $\overline{Q}$ Outputs, And Input And Output Pulse Widths



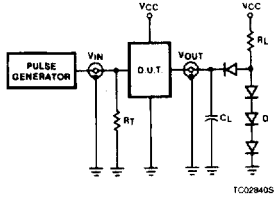
Waveform 2. Propagation Delay B Input To Q And $\overline{Q}$ Outputs, And Input And Output Pulse Widths



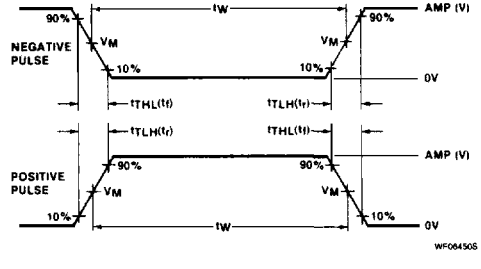
For all waveforms, V_M = 1.5V for 74 and 74S; V_M = 1.3V for 74LS

Waveform 3. Direct Reset Delays And Recovery Time

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Totem-Pole Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

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