

1. GENERAL

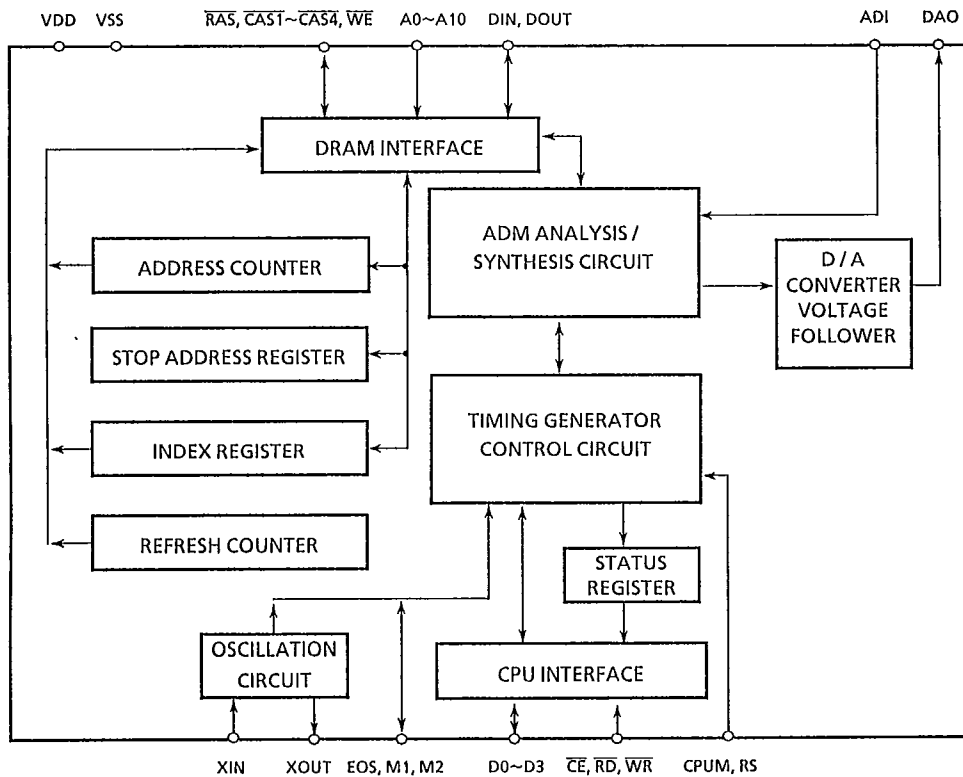
The TC8834 is a single chip CMOS LSI for voice recording / play-back using the ADM (Adaptive Delta Modulation). It composes a voice recording system with a dynamic RAM for voice memory and an audio circuit including a microphone, speaker, filter, amplifier, etc. as an external circuit.

2. FEATURES

- A Single chip LSI for voice recording / play-back.
 - DRAMs (Dynamic RAM) are used as a voice data memory up to 4 pieces of 256 Kbit, or 4 pieces of 1M.
 - It's connectable to microprocessor easily and controlled by 13 kinds of command.
 - Capable of recording / play-back maximum 16 phrases at the manual control.
 - Various switch controls are available for manual control and optimum control method can be selected according to application.
 - 4 kinds of bit rates (32K, 22K, 16K, 11K bps) are provided.
 - Recording / play-back time is up to four minutes and sixteen seconds (with four 1Mbit DRAMs and bit rate to be 16K bps).
 - Voice trigger start function at recording.
 - On-chip ceramic oscillation circuit for recording / play-back.
 - Single 5V power supply.
 - 44-pin mini flat package or 42-pin shrink DIP package.
- The bit rate means the number of bits per second to be used.

3. BLOCK DIAGRAM

3.1 TC8834F Block Diagram



3.2 Block Diagram Description

(1) ADDRESS COUNTER

The 22-bit counter to indicate address of the external DRAMs. Values can be set or read by commands at the CPU control (Note).

(2) STOP ADDRESS REGISTER

The 22-bit register to indicate address to stop recording / play-back. Values can be set by commands at the CPU control, but can not be read.

(3) INDEX REGISTER

The register to indicate address of the index area on DRAMs in the label index mode (Refer to section 5.6).

(4) REFRESH COUNTER

The 10-bit counter to refresh the external DRAMs.

(5) STATUS REGISTER

The 4-bit register which shows the status of TC8834. When \overline{RD} terminal is L label, TC8834 gives this contents to data bus at the CPU control.

(6) CPU INTERFACE

The interface circuit for the external microprocessor. This circuit has also the chattering elimination circuit in the manual control. This chattering elimination circuit has an effect on \overline{RD} , \overline{WR} and \overline{CE} terminals (Start and Stop).

※Note There are two controls available for the TC8834, the CPU control. and the manual control using switches, etc.

3.3 Example of Voice Recording System

3.3.1 CPU Control Type

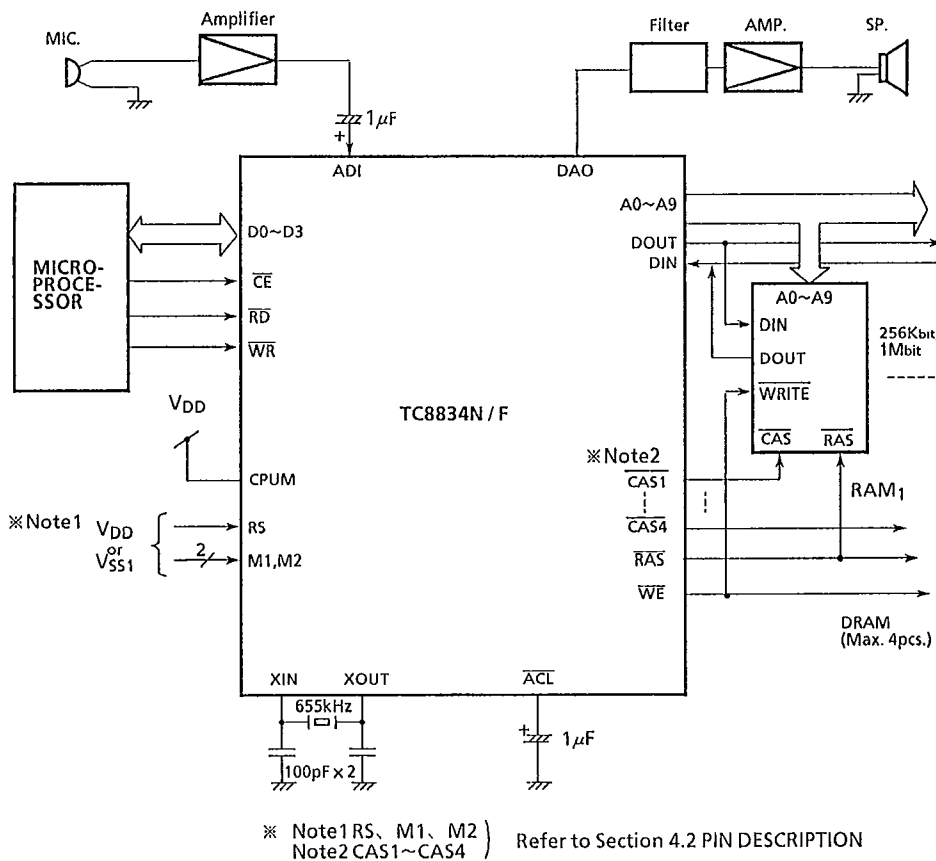


Fig 3.1 CPU control type

3.3.2 Manual Control Type

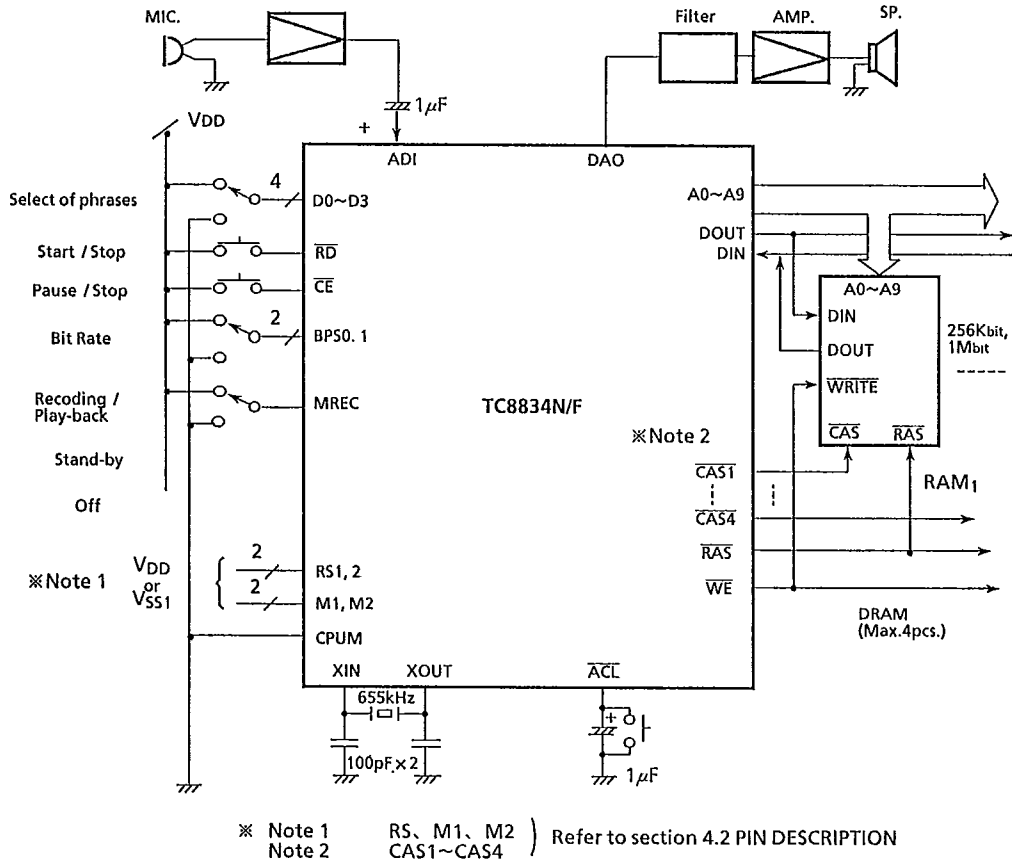
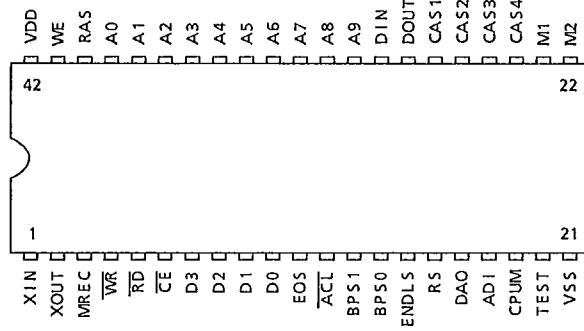


Fig.3.2 Manual control type

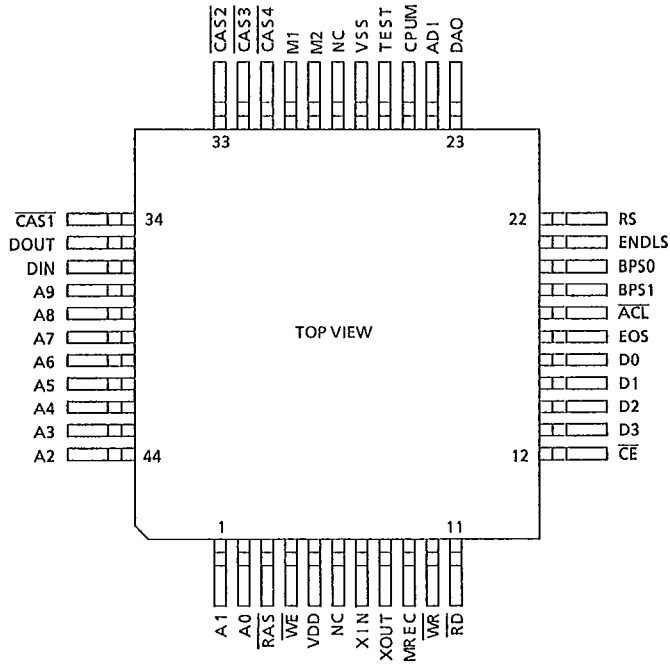
4. PIN ASSIGNMENTS

4.1 Pin Connection

1) SDIP



2) MFP



4.2 Terminal Functions

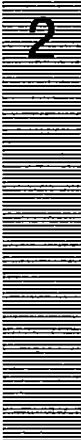
name	no.	Structure.				Functional explanation
		Manual control		CPU control		
		I/O	Pull-up / down	I/O	Pull-up / down	
XIN XOUT	1(7) 2(8)	In Out	-	In Out	-	Input and output terminals of the Ceramic oscillator (Connect a 655kHz Ceramic resonator and capacitors)
MREC	3(9)	In	Pull-down	In	None	Input terminal for recording / play-back select in the manual control.
\overline{WR}	4(10)	In	Pull-down	In	None	In the CPU control mode, input terminal for write strobe (D0 to D3). In the manual control mode, used for START / STOP input of recording / play-back. (voice trigger start at recording).
\overline{RD}	5(11)	In	Pull-down	In	None	In the CPU control mode, input terminal for read strobe (D0 to D3). In the manual control mode, used for START / STOP input of recording / play-back.
\overline{CE}	6(12)	In	Pull-down	In	None	In the CPU control mode, input terminal for chip enable. In the manual control mode, used for STOP input of recording and PAUSE / STOP input of play-back.
D0 D1 D2 D3	7(13) 8(14) 9(15) 10(16)	In	Pull-down	I/O	None	In the CPU control mode, these are bidirectional data bus for commands or status between CPU and TC8832F. In the manual control mode, used as the phrase select input terminals and specify 16 phrases from phrase No. 0 to 15.
EOS	11(27)	Out	-	Out	-	Output terminal for end of speech. Gives high level signal under the recording / play-back waiting and the voice trigger waiting, and low level signal under the recording / play-back.
\overline{ACL}	12(18)	In	Pull-up	In	Pull-up	Input terminal for reset signal.

note 1) When OFF = L, Pull-up resistor is connected.



name	no.	Structure				Functional explanation															
		Manual control		CPU control																	
		I/O	Pull-up / down	I/O	Pull-up / down																
BPS0 BPS1	13(19) 14(20)	In	None	In	None	Input terminal for bit rate select in the manual control. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bit rate</th> <th>BPS1</th> <th>BPS0</th> </tr> </thead> <tbody> <tr> <td>11K bps</td> <td>0</td> <td>0</td> </tr> <tr> <td>16K bps</td> <td>0</td> <td>1</td> </tr> <tr> <td>22K bps</td> <td>1</td> <td>0</td> </tr> <tr> <td>32K bps</td> <td>1</td> <td>1</td> </tr> </tbody> </table> 0 = L level 1 = H level	Bit rate	BPS1	BPS0	11K bps	0	0	16K bps	0	1	22K bps	1	0	32K bps	1	1
Bit rate	BPS1	BPS0																			
11K bps	0	0																			
16K bps	0	1																			
22K bps	1	0																			
32K bps	1	1																			
ENDLS	15(21)	In	None	In	None	Input to designate endless recording.															
RS	16(22)	In	None	In	None	Input terminals for DRAM capacity selector. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Kind</th> <th>RS2</th> <th>RS1</th> </tr> </thead> <tbody> <tr> <td>256k</td> <td>0</td> <td>0</td> </tr> <tr> <td>1M</td> <td>0</td> <td>1</td> </tr> </tbody> </table> 0 = L level 1 = H level	Kind	RS2	RS1	256k	0	0	1M	0	1						
Kind	RS2	RS1																			
256k	0	0																			
1M	0	1																			
DAO	17(23)	Out	-	Out	-	Output terminal of the voice synthesis circuit with voltage follower. Output signal is biased to 1/2 VDD. No voice appears at recording and when the quiet is specified.															
ADI	18(24)	In	-	In	-	Input terminal of the voice analysis circuit. Connected to MICOUT. Otherwise, signal should be input via a coupling capacitor.															
CPUM	19(25)	In	None	In	None	Input terminal for mode change. Fix to low level at the manual control mode, to high level at the CPU control mode.															
TEST	20(26)	In	Pull-down	In	Pull-down	Input terminal for test circuit. (Connect to VSS1.)															
VSS	21(27)	Power Supply	-	Power Supply	-	Power supply terminals to be connected to ground.															

name	no.	Structure				Functional explanation															
		Manual control		CPU control																	
		I/O	Pull-up / down	I/O	Pull-up / down																
M1 M2	22(29) 23(30)	In	None	In	None	Input terminals for programing number of DRAMs. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Number</th> <th>M2</th> <th>M1</th> </tr> </thead> <tbody> <tr> <td>1pc.</td> <td>0</td> <td>0</td> </tr> <tr> <td>2pcs.</td> <td>0</td> <td>1</td> </tr> <tr> <td>3pcs.</td> <td>1</td> <td>0</td> </tr> <tr> <td>4pcs.</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p style="margin-left: 20px;">0 = L level 1 = H level</p>	Number	M2	M1	1pc.	0	0	2pcs.	0	1	3pcs.	1	0	4pcs.	1	1
Number	M2	M1																			
1pc.	0	0																			
2pcs.	0	1																			
3pcs.	1	0																			
4pcs.	1	1																			
$\overline{\text{CAS1}}$ $\overline{\text{CAS2}}$ $\overline{\text{CAS3}}$ $\overline{\text{CAS4}}$	24(31) 25(32) 26(33) 27(34)	Out	-	Out	-	Column address strobe output terminals for DRAMs.															
DOUT	28(35)	Out	-	Out	-	Data output terminal to DRAMs. Connect to DIN terminal of DRAMs.															
DIN	29(36)	In	Pull-up	In	Pull-up	Data input terminal from DRAMs. Connect to DOUT terminal of DRAMs.															
A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	30(37) 31(38) 32(39) 33(40) 34(41) 35(42) 36(43) 37(44) 38(1) 39(2)	Out	-	Out	-	Address output terminals for DRAMs.															
$\overline{\text{RAS}}$	40(3)	Out	-	Out	-	Row address strobe output terminal for DRAMs.															
$\overline{\text{WE}}$	41(4)	Out	-	Out	-	Write strobe output terminal for DRAMs.															
VDD	42(5)	Power Supply	-	Power Supply	-	Power supply terminals to be connected to positive.															



5. SPECIFICATIONS

5.1 Recording / Reproducing Part

System	ADM system
D / A Converter	10-bit voltage type
Bit rate	32K / 22K / 16K / 11K bps
Number of max. phrases	At the manual control 16 phrases Label index mode at the CPU control 64 phrases Direct mode at the CPU control No restriction

5.2 Others

RAM for storing voice data	Up to 4 pcs. of 256K bit, or 4 pcs. of 1M bit.
	Example of usable DRAM
	1M DRAM °TC511000Ax 256K DRAM °TMM41256Ax
Oscillation frequency	655 kHz (ceramic oscillator)

TOSHIBA (UC/UP)

64E D

5.3 Operations and Functions

When composing a voice Recording / play-back system with TC8834, control method is classified into the CPU control and the manual control using switches, etc.

5.4 Manual Control

5.4.1 Selection of Phrase

Using 4 input terminals of D0~D3, The recording / play-back of maximum 16 phrases can be performed. Before starting the recording / play-back, Phrase No. should be specified in 4bit code. Phrase number are as follows, and can be selected at random.

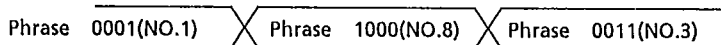
Table 5.1 Phrase No.

Terminal name Phrase No	(MSB) D3	D2	D1	(LSB) D0
No. 0	0	0	0	0
No. 1	0	0	0	1
:	:	:	:	:
:	:	:	:	:
:	:	:	:	:
No. 15	1	1	1	1

1 = H Level
0 = L Level

Recording

Recording is made in order of phrase NO.1、NO.8、NO.3



Play-back

Play-back is made in order of phrase NO.8、NO.1、NO.3

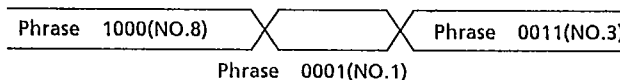


Fig.5.1 Example of phrase selection



5.4.2 Selection of Bit Rate

The TC8834 can use 4 kinds of bit rates as shown in Table 5.2, 11K, 16K, 22K and 32K bps, which are selected by BPS0 and BPS1 terminals. Since a bit rate is independently specified for sound recording and play-back, it is possible to change reproduced voice to slow or fast speaking. However, the recorded phrases are reproduced at low tone as a tape recorder when slowly spoken and at high tone when rapidly spoken.

Table 5.2 Bit rate

Terminal name Bit rate	BPS1	BPS0
11Kbps	0	0
16Kbps	0	1
22Kbps	1	0
32Kbps	1	1

1 = H Level
0 = L Level

Note

Selection of phrase and bit rate is decided when \overline{RD} or \overline{WR} terminals are set at H level (Start input) and when releasing the Pause state.

5.4.3 Recording

The TC8834 has the 22-bit address counter, and voice data is written into DRAMs from the address designated by it's value. When the recording newly, first, it is necessary to reset the address counter by \overline{ACL} signal.

Setting the MREC terminal to H level results in the recording waiting state. When the \overline{RD} terminal goes to H level (Start input), the recording starts and the address counter is added successively. Further, when the \overline{WR} terminal is set to H level, input of a signal over the trigger level (Refer to section 5.7.1) to the ADI terminal leads to starting recording. When the \overline{CE} , \overline{RD} or \overline{WR} is set at H level (Stop input) or when the value on the address counter reaches the maximum address (Refer to section 5.8) of DRAMs. The recording is stopped. Since this maximum address is changed with the RS, M1 and M2 terminals, the full capacity of DRAMs can be effectively used.

However, when the DRAMs capacity is fully used, subsequent recording is not allowed to protect the data stored previously in DRAMs. Therefore, the address counter should be reset by the \overline{ACL} terminal before new recording.

When the recording starts, a value of the address counter at the start (Start address) and when the recording ends, that at the stop (Stop address) are automatically written into a part of DRAM, respectively (Refer to section 5.6).

5.4.4 Play-back

Setting the MREC terminal to L level results in the play-back waiting state. When the \overline{RD} or \overline{WR} terminal is set at H level, the TC8834 starts the play-back after loading the start address and stop address, which have been written at the recording, into the address counter and stop address register, respectively.

The play-back is stopped when the \overline{RD} or \overline{WR} terminal is set at H level or when the value of the address counter agrees with the stop address. Further, when the \overline{CE} terminal is set at H level during the play-back, the play-back is paused. Play-back is continued when the \overline{RD} or \overline{WR} terminal is set at H level under this condition. In addition, when the \overline{CE} terminal is set at H label again under the pause state, the reproducing ends and the system is returned to the play-back waiting state.

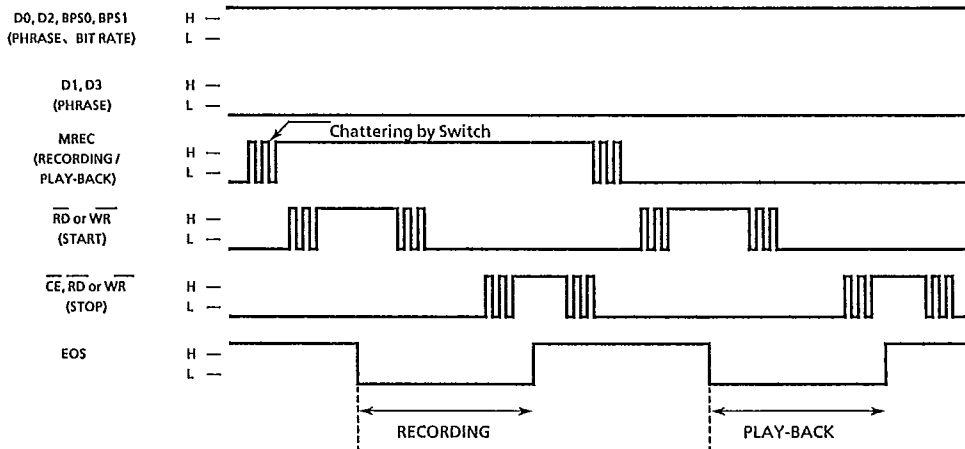


Fig.5.2 Recording / Play-back phrase No.5 , bit rate is 32Kbps

Note

Refer to section 5.6 Label index mode, addition of phrases and change of phrase contents when many phrases are involved.



5.4.5 Details of Start / Stop

At the Manual control, start / stop of the recording / play-back are controlled by \overline{RD} , \overline{WR} and \overline{CE} terminals. These terminals have many functions and various operating methods are selectable according to applications.

Operations when H level signals are applied to the terminals under various state may be summarized as follows.

Table 5.3 Status change table at the manual control

State \ Input	\overline{RD} (START / STOP)	\overline{WR} (START / STOP)	\overline{CE} (PAUSE / STOP)
Recording waiting	Starts recording. (A)	Placed in the voice trigger waiting state. The recording starts when a signal over the trigger level is input to ADI. (B)	Kept in the recording waiting state.
Voice trigger waiting	Returns to the recording waiting state. Address counter advances at max. +400(HEX). (C)	Returns to the recording waiting state. Address counter advances at max. +1(HEX). (D)	Returns to the recording waiting state. Address counter advances at max. +1(HEX). (E)
Recording	Stops recording and returns to the recording waiting state. (F)	Stops recording and returns to the recording waiting state. (G)	Stops recording and returns to the recording waiting state. (H)
Play-back waiting	Starts play-back. (I)	Starts play-back. (J)	Kept in the play-back waiting state.
Play-back	Stops play-back and returns to the play-back waiting state. (K)	Stops play-back and returns to the play-back waiting state. (L)	Placed in the play-back pause state. (M)
Play-back pause	Releasing the play-back pause and returns to the play-back state. (Play-back continuous) (N)	Releasing the play-back pause and returns to the play-back state. (Play-back continuous) (O)	Releasing the play-back pause and returns to the play-back state. (Play-back continuous) (P)

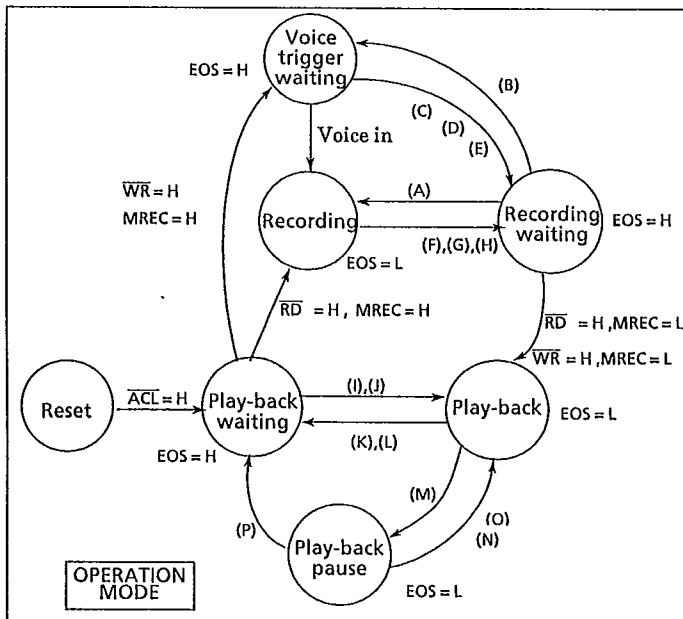


Fig.5.3 Status change at the manual control



Example 1. In case of providing the switches for record / play-back, start and pause operations in recording / play-back over 2 phrases.

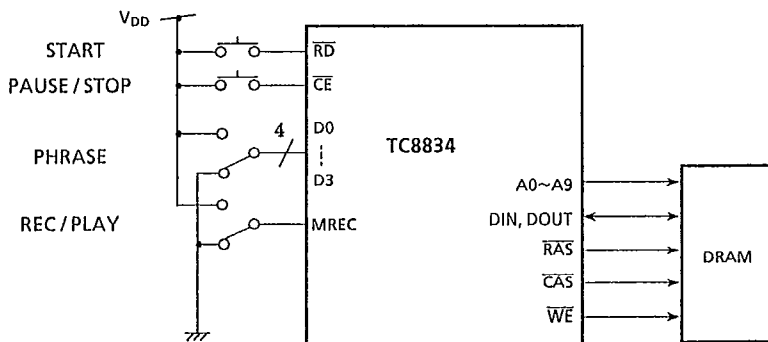


Fig.5.4 Switches connection 1

Example 2. In case of providing the switches for recording / play-back and start operations in recording / play-back over 2 phrases.

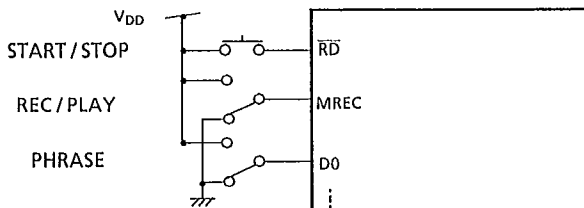


Fig.5.5 Switches connection 2

Example 3. In case of providing the switches for recording / play-back start operations in recording / play-back only 1 phrase.

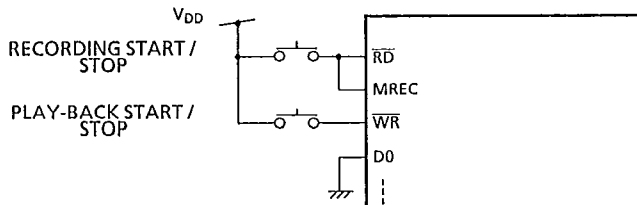


Fig.5.6 Switches connection 3

5.4.6 Chattering Elimination Circuit

At the manual control, the chattering elimination circuit is actuated to prevent from malfunction due to the switches connected to the \overline{RD} , \overline{WR} and \overline{CE} terminals.

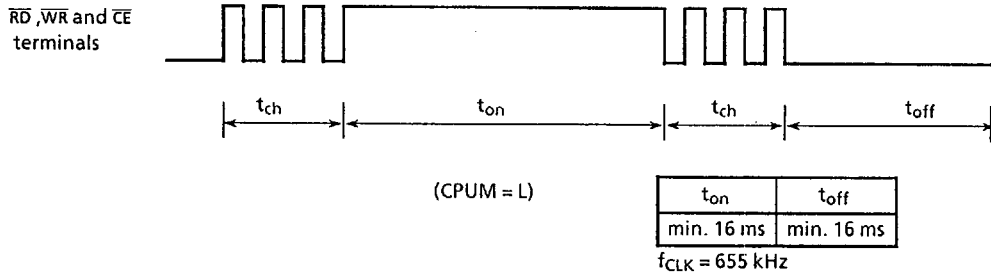


Fig.5.7 Chattering elimination circuit

Start and stop signals should be applied stably for more than t_{ON} and t_{OFF} .

5.4.7 Start / Stop Input and Internal State

Phrase No. , bit rate and recording / play-back status are read at the leading edge of internal start pulse. An internal start pulse has a concern with an external start input as Fig. 5.8

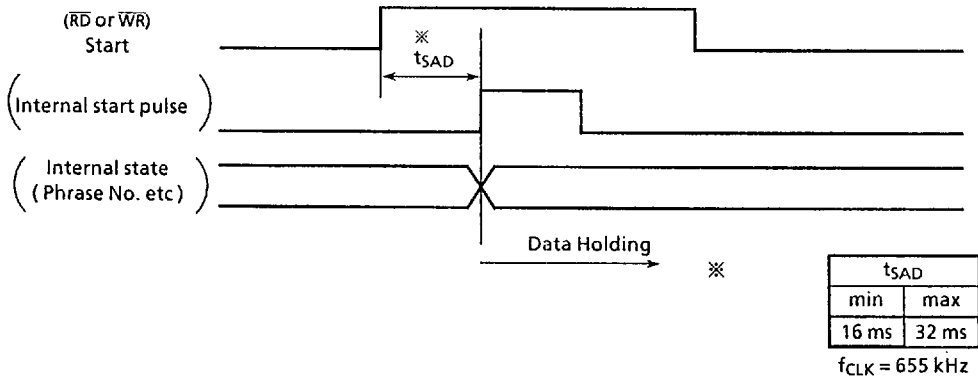


Fig.5.8 Internal pulse



It is possible to input externally D0~D3 (Phrase), BPS0, BPS1 (Bit rate), MREC (Recording / play-back), \overline{RD} or \overline{WR} (Start) as shown in Fig. 5.9.

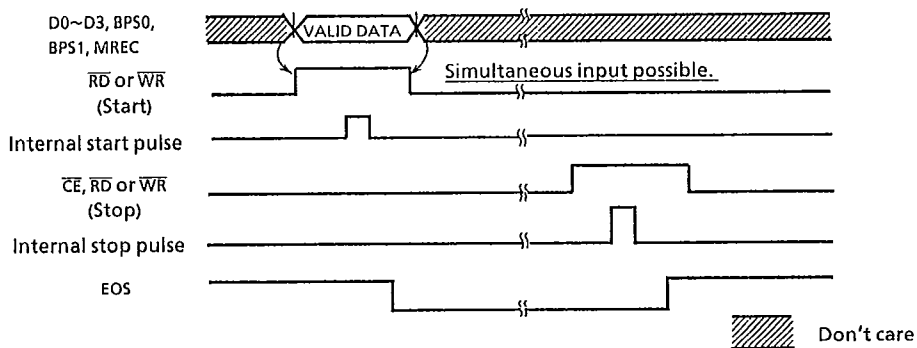


Fig.5.9 How to give start and stop input

5.4.8 EOS Delay Time at Manual Control

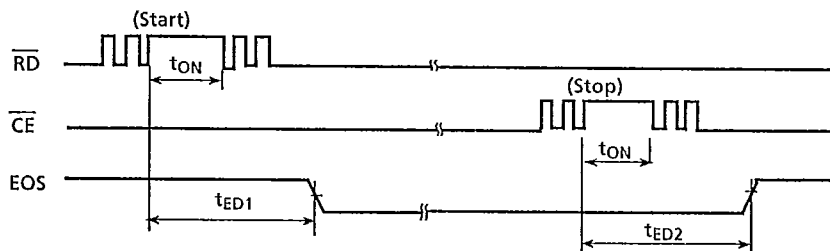


Fig.5.10 Timing of EOS at manual control(1) CHAT = L.

Table 5.4 Delay time of EOS at manual control

SYMBOL	ITEM	CONDITION	MIN	TYP	MAX	UNIT
t _{ED1}	EOS Delay Time 1	\overline{RD} (Start of recording)	-	-	20960 / f _{CLK}	sec
		\overline{RD} (Start of play-back)	-	-	22000 / f _{CLK}	
t _{ED2}	EOS Delay Time 2	$\overline{CE} / \overline{RD} / \overline{WR}$ (Stop)	-	-	20960 / f _{CLK}	
t _{ON}	pulse width	$\overline{CE} / \overline{RD} / \overline{WR}$	10480 / f _{CLK}	-	-	

5.4.9 Pull-down Resistors

In the manual control mode, the internal pull-down resistors are connected to input terminals such as start input, bit rate change-over terminals, etc.

However, the pull-down resistors are connected only when CPUM=L and input terminals that are pulled down as follows D0, D1, D2, D3, \overline{RD} , \overline{WR} , \overline{CE} , MREC, BPS1, BPS0, ENDLS.



5.5 CPU Control

At the CPU control, the operation is controlled by 13 kinds of commands and a CPU can read the status of TC8834 by 4bit status register.

In addition, the TC8834 has the ADDRESS OVERFLOW DETECTOR (Note 1) and ADDRESS COMPARATOR FLIPFLOP (Note 2) which control the recording and play-back operations.

(Note 1) ADDRESS OVERFLOW DETECTOR Refer to section 5.2.5

(Note 2) ADDRESS COMPARATOR FLIPFLOP..... Refer to section 5.2.6

The stop-group commands described hereinafter denote STOP, START and TRIG commands in the recording, START and TRIG commands in the play-back, and STOP command in the play-back pause.

5.5.1 How to Write Commands

As shown in Fig. 5.11, ①using \overline{RD} pulse, read status from TC8834 and check BUSY flag ②If not busy state, after setting up command in D0~D3, write a command using \overline{WR} pulse. In case of such 3 nibble commands as LABEL, ③after rechecking BUSY flag by \overline{RD} pulse, ④write the 2'nd and 3'rd nibbles.

After the 1'st and 2'nd nibbles of a 3 nibble command, other commands can not be written.

This also applies to 7 nibble commands like ADLD1 and ADLD2.

How to write DTRD and ADRD commands, refer to section 5.5.13

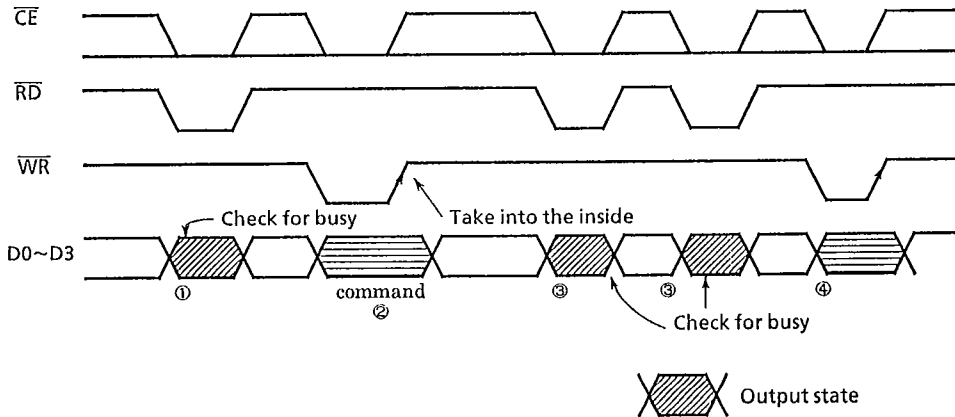


Fig.5.11 How to write command

5.5.2 Commands of TC8834

- (1) NOP (1 nibble) D3
- | | | | |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
|---|---|---|---|
- D0

No operation. But under the recording waiting state, this command sets into the play-back waiting state. In addition, this command is used to reset REC and OVR flag in the status register.

- (2) START (1 nibble) D3
- | | | | |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
|---|---|---|---|
- D0

This command is used to start the recording / play-back in the DIRECT MODE from the address shown by the address counter. When this command is executed under the recording / play-back, the recording / play-back is stop. Further, when executed under the play-back pause state, releases the pause and starts to continue the play-back.

- (3) STOP (1 nibble) D3
- | | | | |
|---|---|---|---|
| 0 | 0 | 1 | 0 |
|---|---|---|---|
- D0

When this command is executed under the recording, the recording is stopped. If during recording by the LABEL command, a value of the address counter is written into the INDEX AREA of DRAM as the stop address. Further, during recording with the ENDLS terminal at H level (ENDLESS MODE), the contents of the address counter are transferred to the stop address register. this command is executed under the play-back, the system to play-back pause. The play-back is stopped if this command is issued again under the play-back pause.

- (4) ADLD1 (7 nibbles) D3
- | | | | |
|---|---|---|---|
| 0 | 0 | 1 | 1 |
|---|---|---|---|
- D0

Sets the successive 6 nibbles data in the address counter. Resets the ADDRESS COMPARATOR FLIPFLOP.

- (5) ADLD2 (7 nibbles) D3
- | | | | |
|---|---|---|---|
| 0 | 1 | 0 | 0 |
|---|---|---|---|
- D0

Sets the successive 6 nibbles data in the stop address register. Sets the ADDRESS COMPARATOR FLIPFLOP.

- (6) CNDT (2 nibbles) D3
- | | | | |
|---|---|---|---|
| 0 | 1 | 0 | 1 |
|---|---|---|---|
- D0

Specifies bit rate and silent output with the successive 1 nibble data. When the quiet output is specified, the DAO terminal is placed at Vref level by force.

- (7) LABEL (3 nibbles) D3
- | | | | |
|---|---|---|---|
| 0 | 1 | 1 | 0 |
|---|---|---|---|
- D0

Specifies Phrase No. by the successive 2 nibbles data and starts the recording / play-back. When this command is issued under the recording waiting state, the contents of the address counter and bit rate are written into the INDEX AREA of DRAM, and then it becomes the voice trigger waiting state. When a signal over the trigger level is applied to the ADI terminal under this state, a recording starts. In the play-back waiting state, starts the play-back after reading start address, stop address and bit rate from INDEX AREA of DRAM.

- (8) ADDR (1 nibble) D3

0	1	1	1
---	---	---	---

 D0

Reads the contents of the address counter. The contents are come out by 4 bits at a time from the high order address side against 6 successive read accesses. During this period, the contents of the status register can not be read. Next command should not be issued without performing 6 read accesses.

- (9) REC (1 nibble) D3

1	0	0	0
---	---	---	---

 D0

Changes the playing-back waiting state to the recording waiting state. Return from the recording waiting state to the play-back waiting state by the NOP or CLEAR command.

- (10) DTWR (2 nibbles) D3

1	0	0	1
---	---	---	---

 D0

Writes 4 bits of the successive 1 nibble data into DRAMs from the address shown by the address counter, the address counter is increased in 4 addresses.

- (11) DTRD (1 nibble) D3

1	0	1	0
---	---	---	---

 D0

Reads out data of DRAMs in 4 bits data from the address shown by the address counter for the successive one read access. During this period, the contents of the status register can not be read, the address counter is increased in 4 addresses. During the recording waiting state, this command should not be issued.

- (12) TRIG (1 nibble) D3

1	0	1	1
---	---	---	---

 D0

Starts the recording / play-back in the DIRECT MODE from the address shown by the address counter. This command issued in the recording waiting state leads to the voice trigger waiting state, and only when a signal over the trigger level is applied to the ADI terminal, recording starts. When this command is issued in the play-back waiting state, the play-back is started immediately. All the other functions are identical to those the START command.

- (13) CLEAR (1 nibble) D3

1	1	0	0
---	---	---	---

 D0

In addition to the functions of the NOP command, this command clears the address counter and bit rate, and inhibits the ADDRESS OVERFLOW DETECTOR.

Note Under the recording / play-back and play-back pause, any command other than START, STOP and TRIG should not be issued.

Table 5.5 Command list

	1'st nibble D3 D2 D1 D0	2'nd nibble D3 D2 D1 D0	3'rd nibble D3--D0	4th nibble D3--D0	5th nibble D3--D0	6th nibble D3--D0	7th nibble D3--D0															
NOP	0 0 0 0	—	—	—	—	—	—															
START	0 0 0 1	—	—	—	—	—	—															
STOP	0 0 1 0	—	—	—	—	—	—															
ADLD1	0 0 1 1	A23 A22 A21 A20	A19—A16	A15—A12	A11—A8	A7—A4	A3—A0															
ADLD2	0 1 0 0	S23 S22 S21 S20	S19—S16	S15—S12	S11—S8	S7—S4	S3—S0															
CNDT	0 1 0 1	* SL BR1 BR0	<table border="1"> <thead> <tr> <th>Bit rate</th> <th>BR1</th> <th>BR0</th> </tr> </thead> <tbody> <tr> <td>11K bps</td> <td>0</td> <td>0</td> </tr> <tr> <td>16K bps</td> <td>0</td> <td>1</td> </tr> <tr> <td>22K bps</td> <td>1</td> <td>0</td> </tr> <tr> <td>32K bps</td> <td>1</td> <td>1</td> </tr> </tbody> </table>					Bit rate	BR1	BR0	11K bps	0	0	16K bps	0	1	22K bps	1	0	32K bps	1	1
	Bit rate	BR1						BR0														
	11K bps	0						0														
	16K bps	0						1														
22K bps	1	0																				
32K bps	1	1																				
		SL																				
	Sound	0																				
	Silent	1																				
LABEL	0 1 1 0	* * LB5 LB4	LB3—LB0	LB = Phrase no.																		
ADRD	0 1 1 1	1'st read A23 A22 A21 A20	2'nd read A19—A16	3'rd read A15—A12	4th read A11—A8	5th read A7—A4	6th read A3—A0															
REC	1 0 0 0	—	—	—	—	—	—															
DTWR	1 0 0 1	Bn Bn + 1 Bn + 2 Bn + 3	n = Contents of the address counter before executing command. Bn = Data to be written into DRAMs. Addressed by n.																			
DTRD	1 0 1 0	1'st read Bn Bn + 1 Bn + 2 Bn + 3	n = Contents of the address counter before executing command. Bn = Data to be read from DRAMs. Addressed by n.																			
TRIG	1 0 1 1	—	—	—	—	—	—															
CLEAR	1 1 0 0	—	—	—	—	—	—															

* = Don't care

Note

A waiting time of 122μs is required between issuing the ADRD / DTRD commands and reading the first nibble data. (f_{clk} = 655k112)



5.5.3 Status Register

The status register consists of 4 bits. When the \overline{RD} terminal is set to L level at the CPU control, data of the status register is came out to D0~D3 terminals and the internal operating status of the TC8834 can be checked. Each flag of the status register is explained in following (Table 5.6).

(1) BUSY flag

When this flag is set, it indicates that the TC8834 is in reset state or processing a command internally. Don't give any command from microprocessor. If the command is given, the internal status may possibly becomes uncertainty.

(2) EOS flag

This flag becomes set under the recording / play-back waiting state, and reset during recording or play-back. The value is the same as a value appeared at the EOS terminal.

(3) REC flag

Becomes set when the REC command is input executed. Reset by the NOP and CLEAR commands.

(4) OVR flag

It is indicated that the recording ends as the address counter exceeded maximum address of DRAMs under the recording by LABEL command. This status is reset by NOP and CLEAR commands.

Table 5.6 Status register

Terminals name	D3	D2	D1	D0
Status register	BUSY	EOS	REC	OVR

5.5.4 BUSY Flag

Conditions for setting BUSY flag set are broadly classified into the following three conditions. Further, busy period is shown in the Fig. 5.12 and Table 5.7

(1) Reset process

When the \overline{ACL} terminal becomes L level, BUSY flag becomes set. When the \overline{ACL} terminal returns to H level again, the internal state of TC8834 is initialized and after all are completed, BUSY flag becomes reset.

(2) Command process

When it is detected that both of the \overline{CE} and \overline{WR} terminals have become L level at the CPU control, BUSY flag becomes set. When the process of command is completed, BUSY flag returns to reset again. The command process is actually started after return of at least either one of the \overline{CE} or \overline{WR} terminal to H level has been detected. (The table 5.7 shows period from the \overline{CE} , \overline{WR} terminal returned H level to BSY flag reset).

(3) Address overflow process

When the address counter is overflow during the recording in the LABEL INDEX MODE, TC8834 automatically stops the recording and executes the same process as that when the STOP command is accepted. During this period, BUSY flag also becomes set.

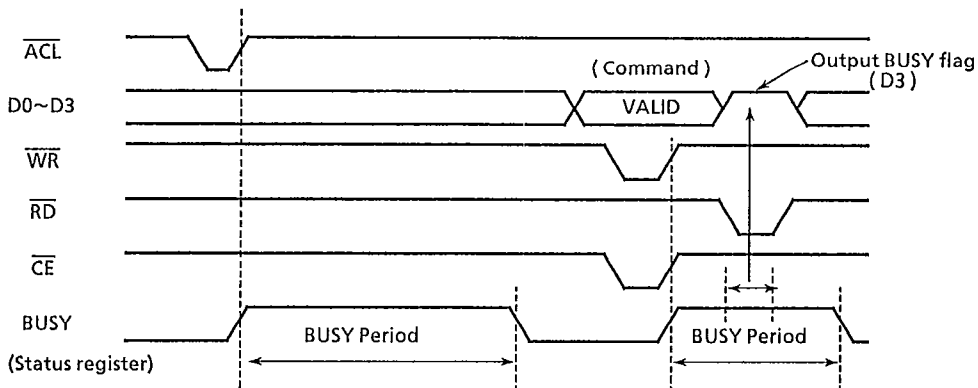


Fig.5.12 BUSY timing

Table 5.7 BUSY Period

BUSY Conditions		Period (max.)	UNIT
Reset process		$20 / f_{CLK}$	(sec)
NOP, START, TRIG, REC, CLEAR Commands		$30 / f_{CLK}$	
ADRD, DTRD Commands		$80 / f_{CLK}$	
CNDT Command	1'st nibble	$30 / f_{CLK}$	
	2'nd nibble	$40 / f_{CLK}$	
ADLD1, ADLD2, DTWR Command	1'st nibble	$30 / f_{CLK}$	
	After 2'nd nibble	$60 / f_{CLK}$	
LABEL Command	1'st nibble	$30 / f_{CLK}$	
	2'nd nibble	$20 / f_{CLK}$	
	3'rd nibble	Recording	
Play-back		$690 / f_{CLK}$	
Stop-group commands	LABEL INDEX MODE Recording	$420 / f_{CLK}$	
	Other (Recording / Play-back)	$30 / f_{CLK}$	
Address overflow process		$340 / f_{CLK}$	

f_{CLK} = Oscillation frequency (Hz)

5.5.5 Address Overflow Detector

When the address counter exceeds maximum address that is determined by the terminals RS, M1, and M2, it is detected by this detector. It becomes valid only when the LABEL command is given under the recording.

When the address overflow is detected, the recording is stopped, a value of the maximum address is written into the index area of DRAM as the stop address, and then the address counter is preset at address 1000 (HEX). In addition, the OVR flag in the status register is set. During this procedure, BUSY flag in the status register also become set.

5.5.6 Address Comparator Flipflop

When this flipflop has been set, the recording / play-back is stopped if the contents of the address counter agree with those of the stop address register. When it has been reset, the recording / play-back is not stopped until the STOP command is given. (Exception : Address overflow in the preceding item).

This flipflop is set when the ADLD2 command is given or when the LABEL command is given under the play-back, and it is reset when the ADLD1 or CLEAR command is given or when the LABEL command is given under the recording.

5.5.7 Modes in CPU Control

There are two modes about both recording and play-back at the CPU control.

- (1) DIRECT MODE Designate start / stop address, and bit rate by each command.
- (2) LABEL INDEX MODE Designate phrase by LABEL command, start / stop address are written into the some part (Index area) of DRAM. Refer to section 5.3 LABEL INDEX MODE.

Be careful that recording by LABEL command is always started by the voice trigger.

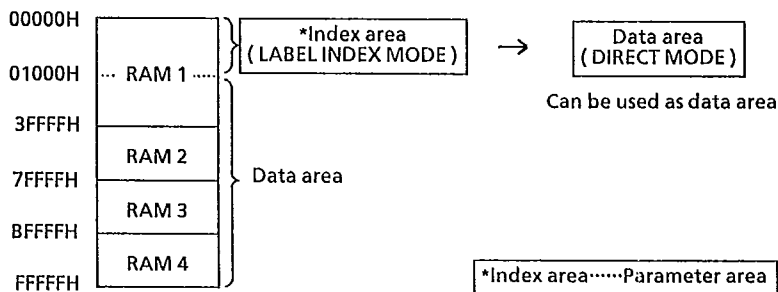


Fig.5.13 Memory map (In case of 256K DRAM)



5.5.8 Status Change at the CPU Control

At the CPU control, the TC8834 is controlled by 13 kinds of command. The relations between the recording and play-back state and commands which are concerned with the recording and play-back operations are as follows.

Table 5.8 Status change table at the CPU control

Command State	START command	TRIG command	LABEL command	STOP command
Recording waiting	Starts recording. (A)	Placed in the voice trigger waiting state. The recording starts when a signal over the trigger level is applied to ADI. (B)	Placed in the voice trigger waiting state. The recording starts when a signal over the trigger level is applied to ADI. (C)	Kept in the recording waiting state.
Voice trigger waiting	Returns to the recording waiting state. Address counter advances at max. + 1(HEX). (D)	Returns to the recording waiting state. Address counter advances at max. + 1(HEX). (E)	Don't give the LABEL command.	Returns to the recording waiting state. Address counter advances at max. + 1(HEX). (F)
Recording	Stops recording and returns to the recording waiting state. (G)	Stops recording and returns to the recording waiting state. (H)	Don't give the LABEL command.	Stops recording and returns to the recording waiting state. (I)
Play-back waiting	Starts play-back. (J)	Starts play-back. (K)	Starts play-back. (L)	Kept in the play-back waiting state.
Play-back	Stops play-back and returns to the play-back waiting state. (M)	Stops play-back and returns to the play-back waiting state. (N)	Don't give the LABEL command.	Placed in the play-back pause state. (O)
Play-back pause	Releasing the play-back pause and returns to the play-back state (Play-back continuous). (P)	Releasing the play-back pause and returns to the play-back state (Play-back continuous). (Q)	Don't give the LABEL command.	Releasing the play-back pause and returns to the play-back waiting state (Play-back stop). (R)

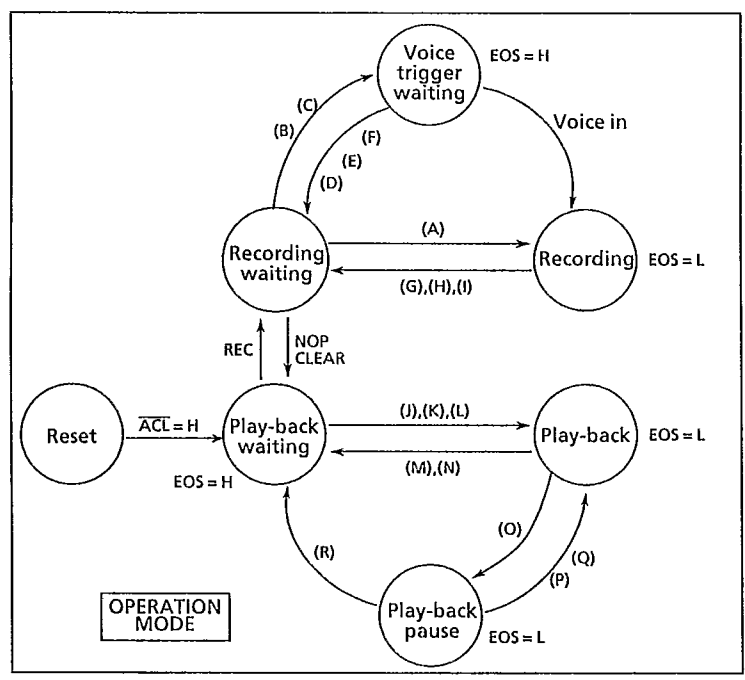


Fig.5.14 Status change at the CPU control



5.5.9 Example for the Flowchart of Recording / Play-back at LABEL INDEX MODE

(1) Recording

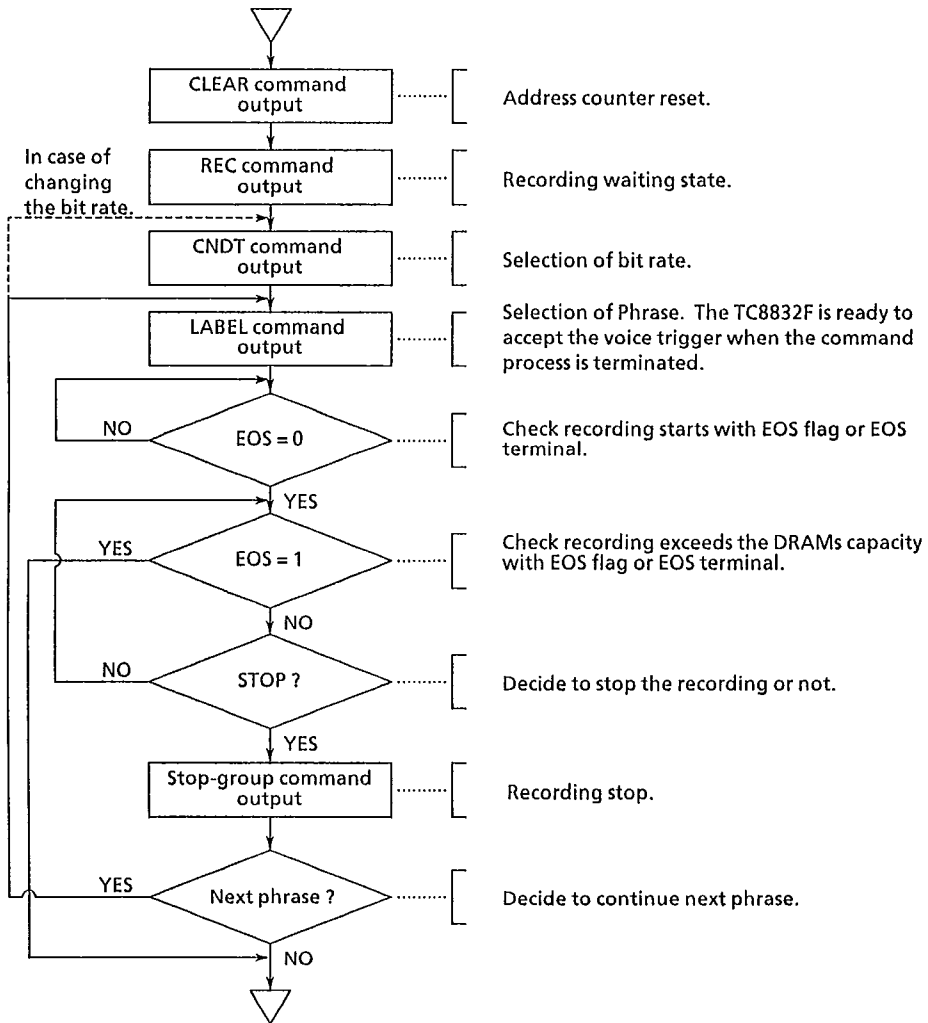
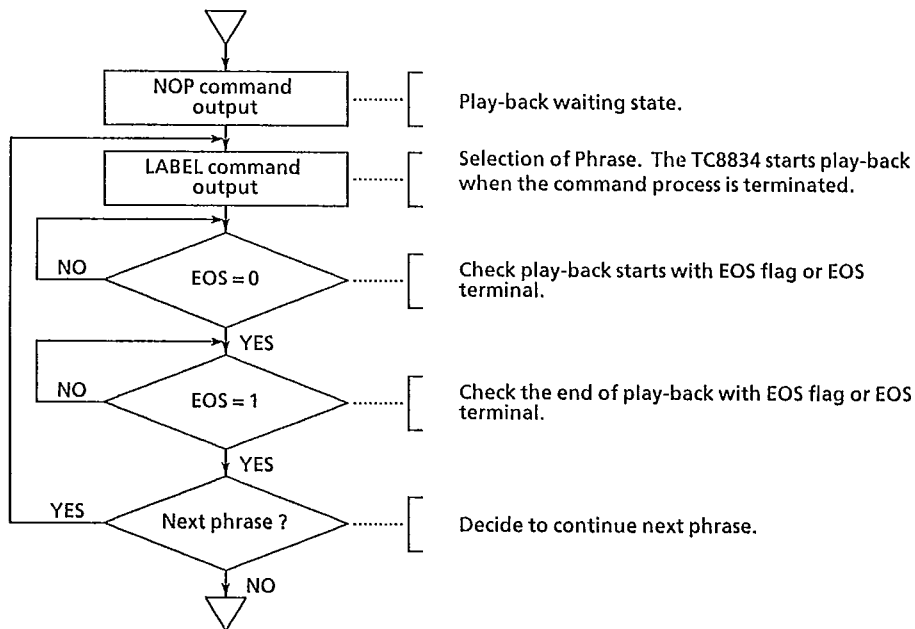


Fig.5.15 Recording procedure at the LABEL INDEX MODE

(2) Play-back



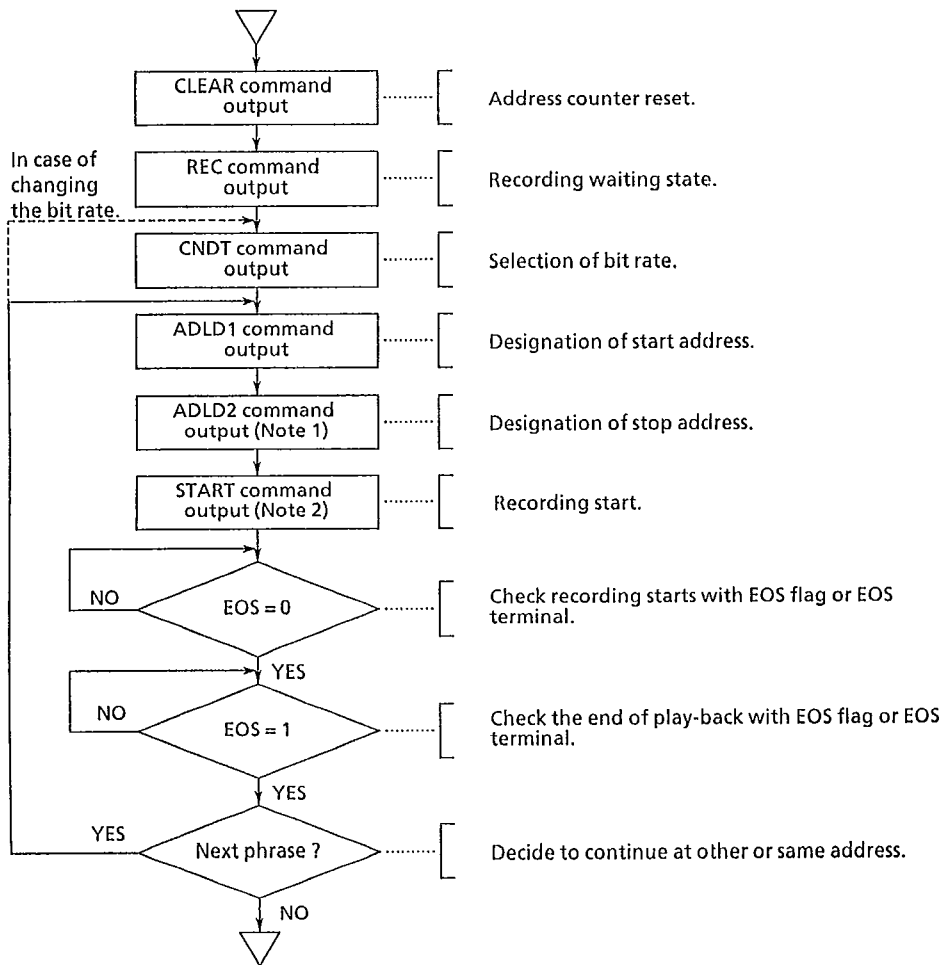
Note At the CPU control, the bit rate of play-back becomes that set previously at the recording. Therefore, fast / slow speaking at the manual control mode cannot be specified.

Fig.5.16 Reproducing procedure at the LABEL INDEX MODE



5.5.10 Example for the Flowchart of Recording / Play-back at DIRECT MODE

(1) Recording

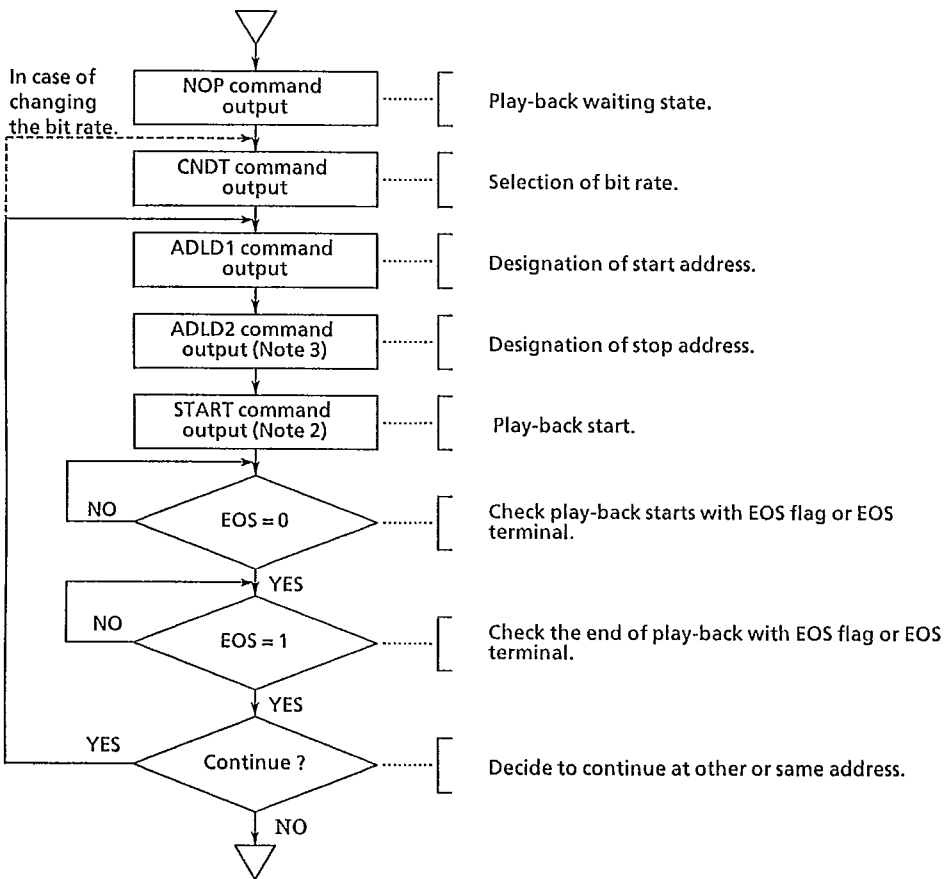


Note 1 If ADLD2 command is not designated, recording becomes endless state. In this case, recording should be terminated by using STOP command.

Note 2 When the TRIG command is given in stead of START command, the voice trigger is activated.

Fig.5.17 Recording procedure at the DIRECT MODE

(2) Reproducing



Note 3 It is possible to produce the endless play-back when ADLD2 is designated for the maximum address of DRAM at the recording and omits it at the play-back. STOP command is used to terminate it.
But, only when four DRAMs are connected.

Fig.5.18 Reproducing procedure at the DIRECT MODE



5.5.11 Write / Read Data of DRAMs

(1) Data write

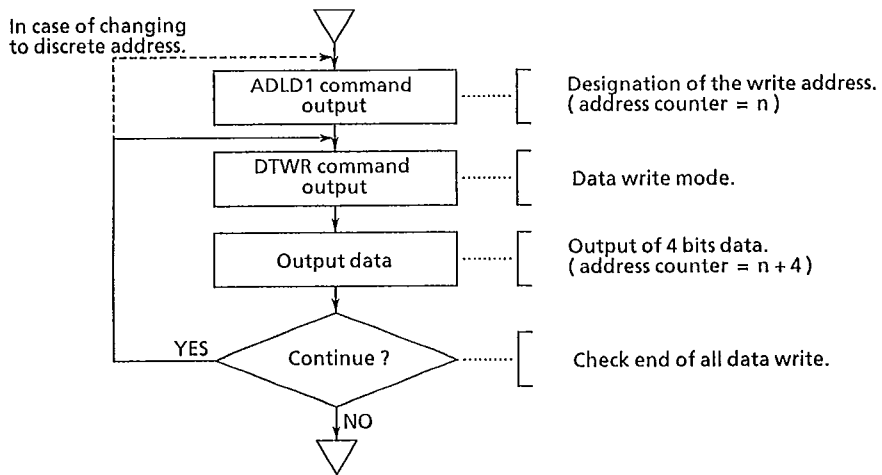


Fig.5.19 Data write procedure

(2) Data read

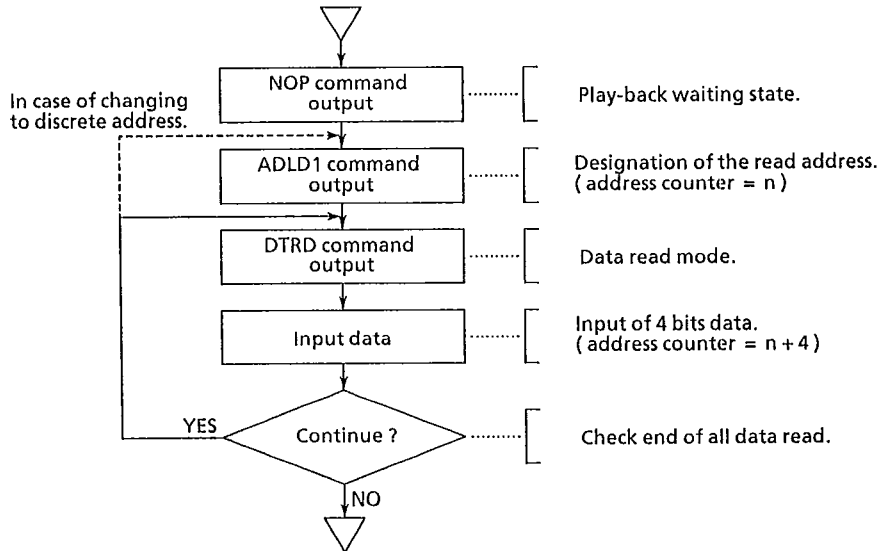


Fig.5.20 Data read procedure

5.5.12 Read Address

ADRD command is used to read a content of address counter at stop of recording and play-back

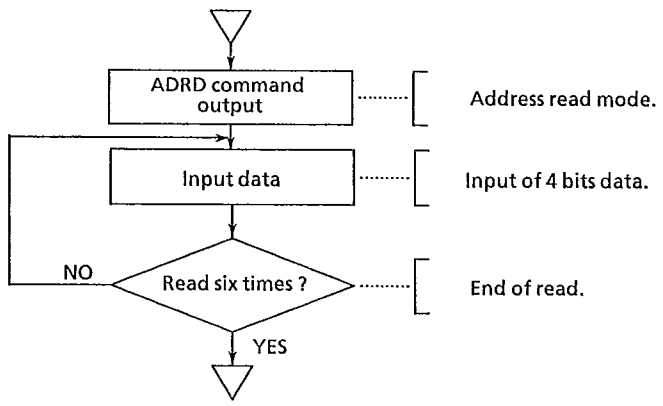
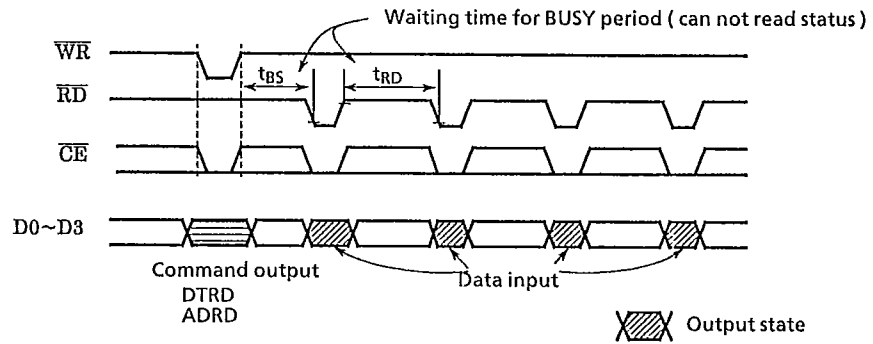


Fig.5.21 Address read procedure

5.5.13 How to DTRD / ADRD Commands



※ $t_{RD} = 60 / f_{CLK}$, ($f_{CLK} = 655kHz$, t_{RD} is about $92\mu s$)
 $t_{BS} = 80 / f_{CLK}$, ($f_{CLK} = 655kHz$, t_{BS} is about $124\mu s$)
 Refer to section 9.4 AC characteristics, other AC parameter.

Fig.5.22 How to DTRD / ADRD command



5.5.14 EOS Delay Time at CPU Control

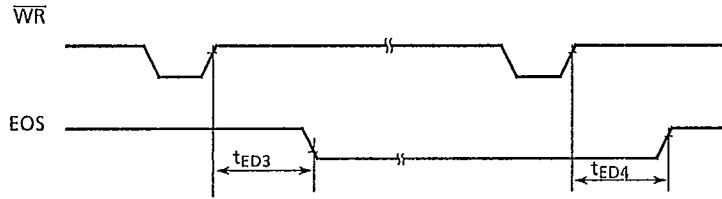


Fig.5.23 Delay timing of EOS at CPU control

Table 5.9 Delay time of EOS at CPU control

SYMBOL	ITEM	CONDITION	MIN	TYP	MAX	UNIT
t_{ED3}	EOS Delay Time 3	START	-	-	$50 / f_{CLK}$	sec
		LABEL (Play-back)	-	-	$700 / f_{CLK}$	
t_{ED4}	EOS Delay Time 4	STOP (LABEL INDEX MODE)	-	-	$460 / f_{CLK}$	
		STOP (DIRECT MODE)	-	-	$140 / f_{CLK}$	

f_{CLK} = Oscillation frequency (Hz)

5.6 Label Index Mode

The recording / play-back methods for manual control and the LABEL INDEX MODE at the CPU control are described here.

At the manual control (LABEL command under CPU control), the address is indirectly specified using phrase number and index area in which TC8834 writes the start addresses, stop address and bit rate of each phrase. The memory maps of DRAMs in the LABEL INDEX MODE are as follow.

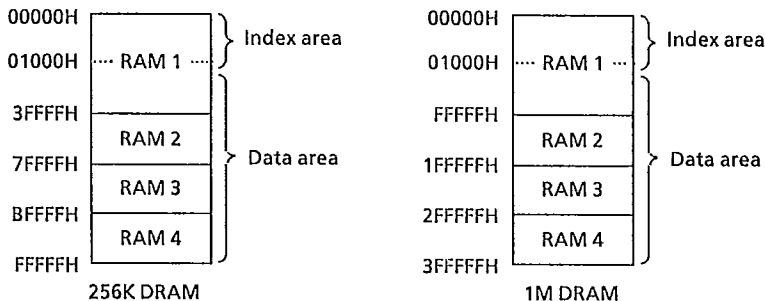


Fig.5.24 Memory map in the LABEL INDEX MODE

Maximum address that can be changed varies depending upon type and quantity of connected DRAMs. In any case, address 0 (HEX) ~ FFF (HEX) are used as the index area, and the succeeding address 1000 (HEX) and up become the voice data area.

Start address, stop address, and bit rate are recorded in the index area by the TC8834 at the recording. And data read out from this area are loaded on the address counter before the play-back.

5.6.1 Recording of Phrase

In performing the recording newly, Reset the TC8834 by the \overline{ACL} signal or CLEAR command then address counter is preset to 1000 (HEX).

A bit rate and a phrase No. are specified and start signal is issued, then the recording starts. The contents of the address counter (Start address) is written into the index area of DRAM before recording. During the recording, the value of the address counter is increased successively.

When the stop signal is issued during the recording, the recording ends and the contents of the address counter (Stop address) and bit rate are written into the index area. Thereafter the value of the address counter are added with one to prepare for next recording.



To perform the recording for other phrase successively, phrase No. , is newly designated and the start signal is issued (Fig. 5.25).

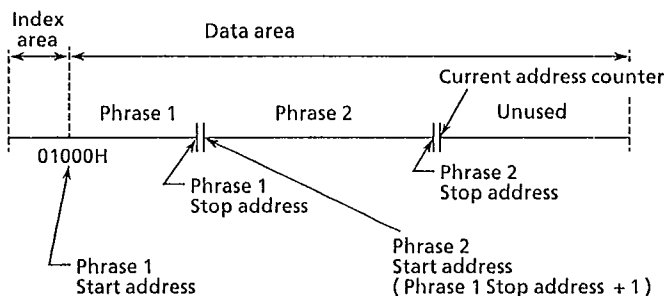


Fig.5.25 In case of recording two phrases

5.6.2 Play-back of Phrase

When any recorded phrase No. is selected and start input is given, voice corresponding to that phrase No. is reproduced. Phrase No. can be designated irrespective of sequence of the recording. Further, it is also possible to stop speaking by giving the stop input during play-back. Thereafter, when the start input is given again using the same phrase No., the play-back is performed from the beginning of that phrase. It is also possible to pause under play-back.

If the play-back is started by designating phrase No. that was not used for the recording, what sound is reproduced is uncertain. However, it is possible to stop the play-back by giving the stop input.

The play-back is started after the start address, stop address and bit rate are set in the TC8834 from the index area of DRAM. When the play-back ends, the value of the address counter are added with (+ 1)

5.6.3 Addition of Phrase

First, reproduce the last phrase at the recording completely so that the address counter can indicate the address next to the stop address of the last phrase. Change the play-back waiting state to the recording waiting state. Don't reset the TC8834 at this time. When the recording is made by designating any unrecorded phrase No. to be added.

5.6.4 Change of Phrase Contents

To change the contents of phrases that have been once recorded, reproduce a phrase preceding the phrase to be changed to make the address counter indicate the start address of the phrase to be changed. (For example, when phrases have been recorded in order of 5-7-3-6 and the contents of phrase No. 3 is necessary to change, reproduce phrase No. 7 completely).

Don't reset the TC8834 at this time. When the recording is made by designating phrase No. to be changed successively, the contents of that phrase are changed to new contents.

If the recording time of the new phrase is longer than that of phrase before change, the first part of next phrase may be changed (Fig. 5.26). When the changed phrase is reproduced under this state, the new contents are spoken properly but when it is tried to reproduce next phrase, the play-back is started at the middle of the changed phrase to the end and then sound is reproduced successively from the middle of next phrase. This is phenomenon that is taken place as the start address of next phrase written in the index area remains unchanged from the previous address.

On the contrary, when the recording time of the new phrase is shorter than before change, the late part data of the phrase before change is left. When new phrase is reproduced, it stops at the end properly. Needless to say, next phrase is also properly reproduced. In this case, the part between the stop address of the changed phrase and the start address of next phrase is not used.

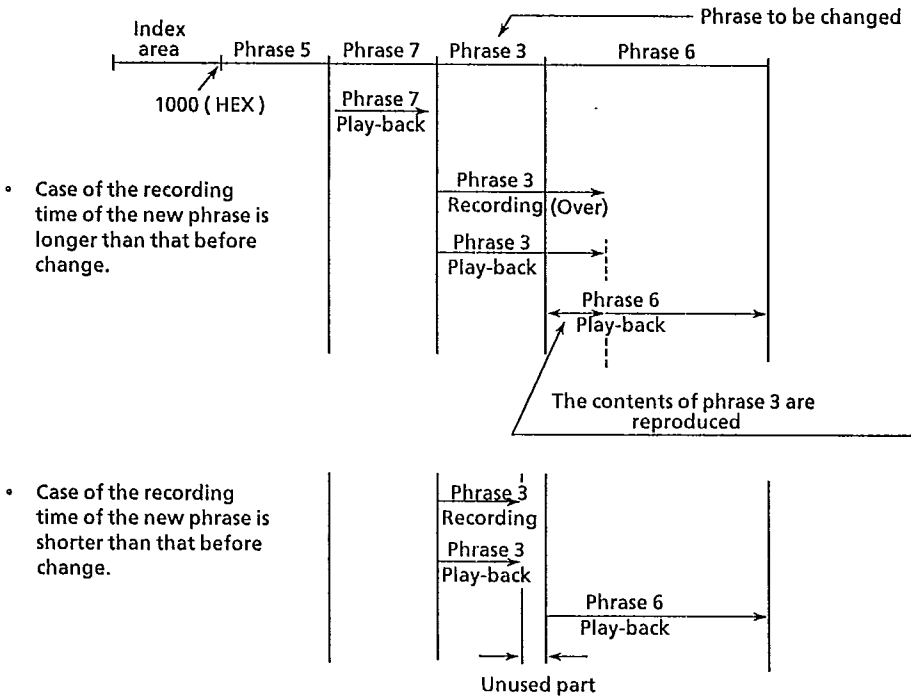


Fig.5.26 Change of phrase contents



5.6.5 LABEL INDEX MODE Operations

The operations of the TC8834 and DRAMs in LABEL INDEX MODE are described in the following.

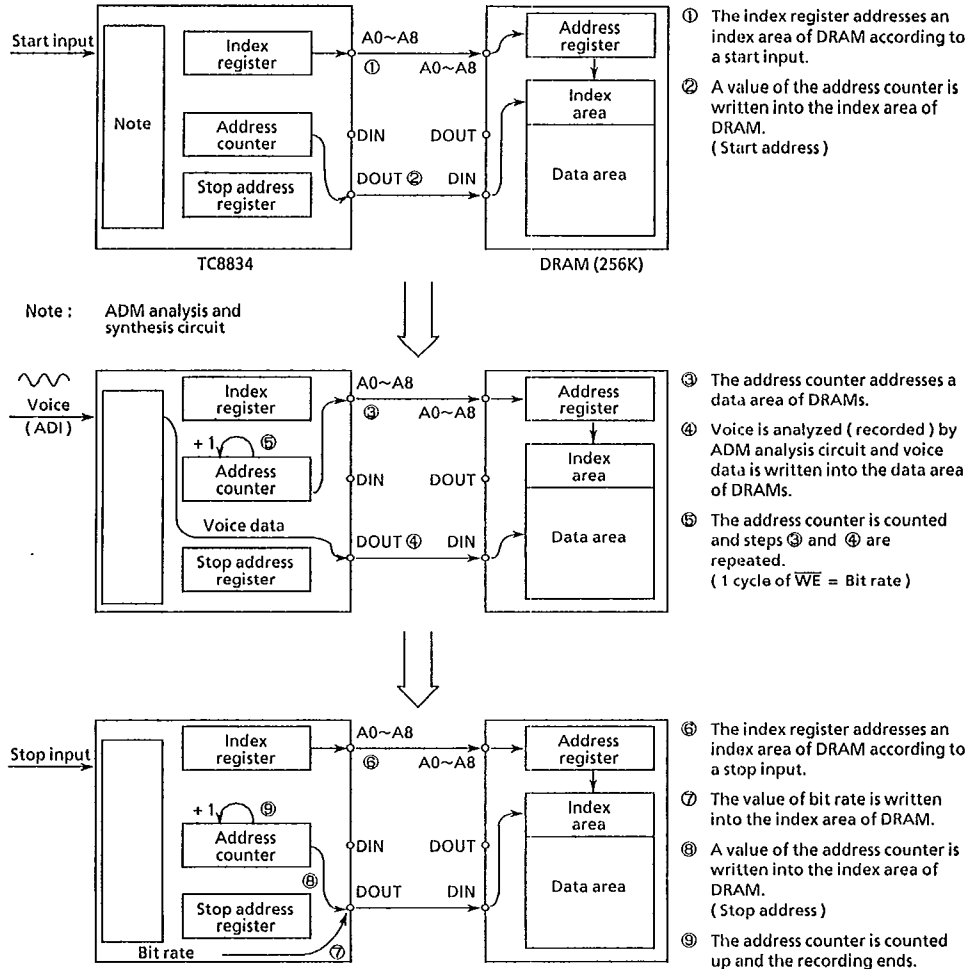


Fig.5.27 Recording

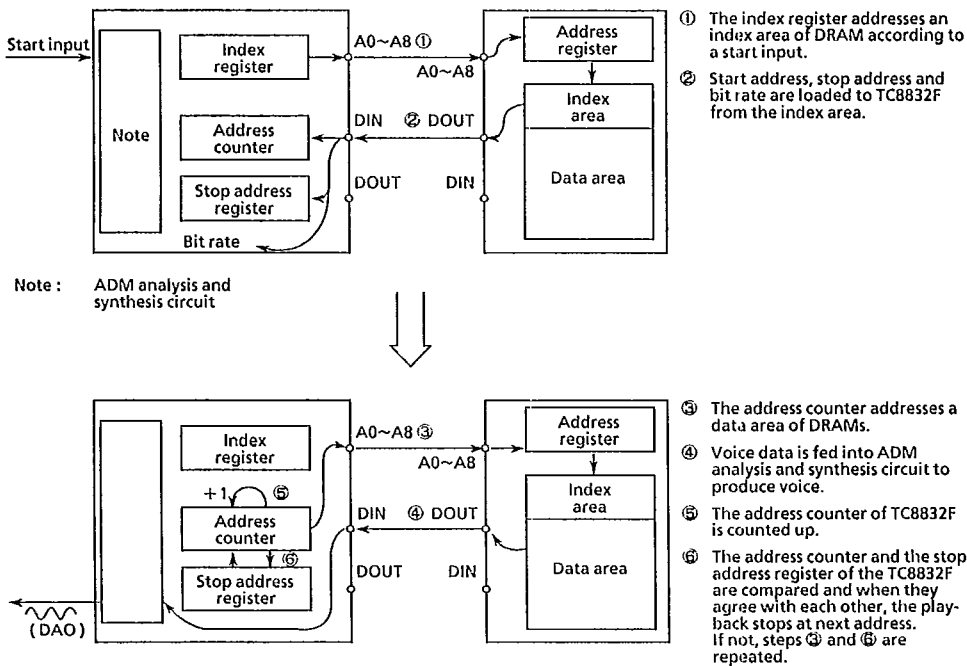


Fig.5.28 Play-back



5.6.6 The Index Area

The index area is used for the recording / play-back at the manual control and LABEL INDEX MODE at the CPU control. This area consists of 4K bits from address 0 (HEX) to FFF (HEX), securing for 64 phrase (64 bits per phrase).

At the recording, start address, stop address and bit rate of each phrase are written into index area. And at the play-back, the contents of this area are read out and set in the address counter, etc. The contents of the index area for each phrase are shown in the table 5.11. A0~A21 denote the start address, S0~S21 the stop address, and A21 and S21 represent the most significant bits of them respectively. Further, BR0 and BR1 denote bit rate which are identical to those to be set by the CNDT command, the same contents as written 3 times.

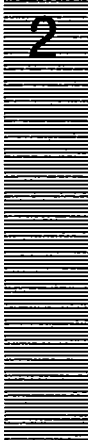
Bit rate is written at both the manual control and CPU control. Read out of bit rate at time of play-back, however, is carried out only at the CPU control. At the CPU control, the same value of bit rate at the recording is automatically set as the bit rate for the play-back. However, at the manual control, the bit rate at the recording and that at the play-back can be set independently by BPS0 and BPS1 terminals.

To read out the contents of the index area, obtain the top address of the index area corresponding to each phrase from phrase No. , and after setting it in the address counter by the ADLD1 command, read it in unit of 4 bits by the DTRD command. On the contrary, to write data into the index area, after setting the top address of the index area in the same manner as above, write data by the DTWR command.

Table 5.10 Memory map of index area

Address of DRAM A11 A0	Data	Address of DRAM A11 A0	Data
PPPPPP000000	-	PPPPPP100000	-
000001	-	100001	-
000010	A21	100010	S21
000011	A20	100011	S20
000100	A19	100100	S19
000101	A18	100101	S18
000110	A17	100110	S17
000111	A16	100111	S16
001000	A15	101000	S15
001001	A14	101001	S14
001010	A13	101010	S13
001011	A12	101011	S12
001100	A11	101100	S11
001101	A10	101101	S10
001110	A 9	101110	S 9
001111	A 8	101111	S 8
010000	A 7	110000	S 7
010001	A 6	110001	S 6
010010	A 5	110010	S 5
010011	A 4	110011	S 4
010100	A 3	110100	S 3
010101	A 2	110101	S 2
010110	A 1	110110	S 1
010111	A 0	110111	S 0
011000	-	111000	-
011001	-	111001	-
011010	BR1	111010	-
011011	BR0	111011	-
011100	BR1	111100	-
011101	BR0	111101	-
011110	BR1	111110	-
011111	BR0	111111	-

PPPPPP = Phrase No.
A0~A21 = Start address
S0~S21 = Stop address
BR0~BR1 = Bit rate
- = Unused



5.7 Other Functions

5.7.1 Voice Trigger Function

The TC8834 has the voice trigger function to start recording only when a voice signal over the trigger level is applied to the ADI terminal. This function eliminates unnecessary silent from the beginning of recording and allows efficient use of DRAMs.

(1) Recording

To perform the recording by the voice trigger, place the system in the trigger waiting state by setting the \overline{WR} terminal at H level at the manual control or by issuing the TRIG command or LABEL command at the CPU control.

When a signal over the specified trigger level is applied to the ADI terminal under this state, the address counter of TC8832F begins to operate and recording starts. The output from the EOS terminal or EOS bit of the status register change at this point of time.

(2) Releasing trigger waiting state

To return to the recording waiting state by releasing the trigger waiting state, give the recording stop input. That is, set one of the \overline{CE} , \overline{RD} and \overline{WR} at H level at the manual control. Further, at the CPU control, issue one of the STOP, START and TRIG commands.

However, be careful at the address counter increase by values shown in the following table. Further, it is intended to perform the recording in the label index mode, start address and stop address are written into the index area in DRAM

Table 5.11 Releasing trigger waiting state and address counter increment

	Stop input	Address counter
Manual control	\overline{CE} , \overline{WR}	+ 1H
	\overline{RD} (CHAT = L)	+ 400H (max.)
	\overline{RD} (CHAT = H)	+ 4H (max.)
CPU control	STOP, START TRIG commands	+ 1H (max.)

(3) Play-back

Play-back starts immediately irrespective of level of signal that is applied to the ADI terminal.

(4) Timing of voice trigger

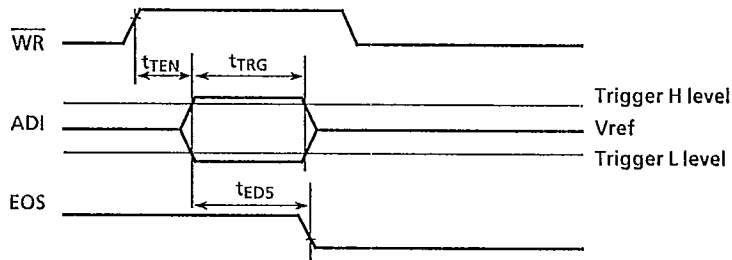


Fig.5.29 Timing of voice trigger

Table 5.12 Delay time of voice trigger

SYMBOL	ITEM	CONDITION	MIN	TYP	MAX	UNIT
t_{TEN}	Trigger enable time	CHAT = L	$20960 / f_{CLK}$	-	-	sec
		CHAT = H	$400 / f_{CLK}$	-	-	
t_{TRG}	Trigger pulse width	11 Kbps	$720 / f_{CLK}$	-	-	
		16 Kbps	$480 / f_{CLK}$	-	-	
		22 Kbps	$360 / f_{CLK}$	-	-	
		32 Kbps	$240 / f_{CLK}$	-	-	
t_{ED5}	EOS Delay Time 5	11 Kbps	-	-	$740 / f_{CLK}$	
		16 Kbps	-	-	$500 / f_{CLK}$	
		22 Kbps	-	-	$380 / f_{CLK}$	
		32 Kbps	-	-	$260 / f_{CLK}$	

※ Trigger level is refer to section 9.5.3 characteristics.

f_{CLK} = Oscillation frequency (Hz)

(5) Precautions

A signal which is applied to ADI terminal should be biased to $1/2V_{DD}$. If this bias has an offset, apparent trigger level changes by that offset. Further, if offset of the bias is over the specified trigger level, the recording starts even when no voice is input.

2

5.7.2 Endless Recording Function

The TC8834 has the endless recording function. To use the function, the ENDLS terminal should be set at H level.

(1) Recording

When the ENDLS terminal is set at H level, if the address counter exceeds the maximum address of DRAMs, which is determined by the RS, M1 and M2 terminals, at the recording, it returns to 0 (HEX) and continues the recording. (When the ENDLS terminal is at L level, in the LABEL INDEX MODE at the CPU control or manual control, the recording stops)

When the stop input is given, the recording ends and the contents of the address counter at that time are transferred to the stop address register and thereafter, the address counter is added by one. Under this state, therefor, voice in the past for a loop time that is determined by maximum address and bit rate is recorded on DRAMs and corresponding address are set in the address counter and stop address register.

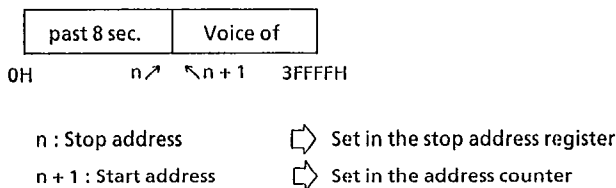


Fig.5.30 Example of endless with one 256K DRAM at 32Kbps

(2) Play-back

After changing the recording waiting state to the play-back waiting state under above mentioned state, when the start input is given, the play-back for loop time is carried out once and stopped. Since the contents of the address counter have returned to the state before the play-back, the same contents can be reproduced again. Through it is possible to stop the play-back in the middle by giving the stop input, if the start input is given again, the play-back starts from the part following the stopped part and stops at the end of the loop (the end point of the recording).

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(3) Precautions

If the recording is stopped before reaching the loop time, the not used recording part of DRAM is also reproduced.

When the ENDLS terminal is set at H level at the manual control, start address and stop address are not written into the index area. In addition, specification of phrase No. is ignored.

When the ENDLS terminal is set at H level at the CPU control, the label command cannot be used. The START command or TRIG command shall be used.

When the \overline{ACL} terminal is set at L level, reset to internal state and play-back cannot be made.

5.7.3 Pause Function

The TC8834 has the pause function at the play-back.

(1) At the manual control

When the \overline{CE} terminal is set at H level under the play-back, the play-back is paused. When an H level signal (start input) is applied to the \overline{RD} or \overline{WR} terminal, the play-back is continued. Further, when an H level signal (stop input) is given to the \overline{CE} terminal again under the play-back pause state, the system returns to the play-back waiting state.

(2) At the CPU control

When the STOP command is input during the play-back, the play-back is paused. When the START or TRIG command is issued under this state, the play-back is carried out continuously. Further when the STOP command is again issued under the play-back pause state, the system returns to the play-back waiting state.

(3) Common specification

Under the play-back pause state, the EOS terminal is kept at L level and EOS flag in the status register is kept at reset. When the state is released and it returns to the play-back waiting state, they are changed to H level and set, respectively.

5.7.4 Pop Noise Cancel Function

The TC8834 has the function to reduce pop noise which is produced at the end of recording and play-back.

(1) Recording

Once the stop input is given under the recording, the recording is stopped when a voice signal at the ADI terminal becomes smaller than the specified level. However, if the address counter overflows under the recording, the recording ends immediately irrespective of voice signal level.

(2) play-back

Once the stop input is given under the play-back, the play-back is stopped when a voice signal to be reproduced becomes smaller than the specified level. However, the system is placed in the pause status irrespective of voice level. Further, if the stop input is given under play-back pause state, the system is placed in the play-back waiting state irrespective of voice level.

(3) Precautions

A signal which is applied to the ADI terminal should be biased to $1/2V_{DD}$. If this bias has an offset over the specified level, the recording will not stop even when the stop input is given under the recording.

5.8 Maximum Address of DRAM

When the contents of the address counter reach the maximum address under the recording in the LABEL INDEX MODE at the CPU control or manual control, the TC8834 stops the recording automatically. In this case, the maximum address is stored as the stop address of a phrase. Further, the address counter is preset at address 1000 (HEX).

In the case of one phrase recording / play-back, the stop input or stop command is unnecessary.

This maximum address changes according to the settings of RS, M1 and M2 terminals. These terminals should be set according to kind and quantity of externally connected DRAMs (table 5.13).

Table 5.12 Maximum address

External DRAM	RS	M2	M1	Maximum address
256K DRAM 1pcs.	0	0	0	3FFFFH
" 2pcs.	0	0	1	7FFFFH
" 3pcs.	0	1	0	BFFFFH
" 4pcs.	0	1	1	FFFFFFH
1M DRAM 1pcs.	1	0	0	FFFFFFH
" 2pcs.	1	0	1	1FFFFFFH
" 3pcs.	1	1	0	2FFFFFFH
" 4pcs.	1	1	1	3FFFFFFH

0 = L level
1 = H level



5.9 Reset Operation

5.9.1 The Status under Reset Operation

When the \overline{ACL} terminal is set at L level, TC8834 stops all operation such as recording/play-back.

However, the refresh counter continues to operate and therefore, the contents of DRAMs remain unchanged.

Further, BUSY flag in status register becomes set during this period.

5.9.2 The Status after Reset Operation

When the \overline{ACL} terminal becomes from L to H level, the internal state of TC8834 is initialized as shown below.

- (1) Set the play-back waiting state.
- (2) Address counter and stop address register are preset to 1000 (H1EX).
- (3) ADDRESS OVERFLOW DETECTOR and ADDRESS COMPARATOR FLIP FLOP are reset.
- (4) At the CPU control, bit rate becomes 32kbps, and silence status is released.
- (5) REC and OVR flag in status register are reset.

After terminating the above completely, BUSY flag is reset.

5.9.3 Reset Processing after Power ON

When the after power on, the following items become unstable.

- (1) Recording and play-back state.
- (2) Address counter.
- (3) ADM analysis / synthesis circuit.
- (4) Other processing circuits such as start and stop processing.

Therefore, to initialize this unstable condition and assure proper operations, apply \overline{ACL} signal.

\overline{ACL} signal to be given after power ON and it's pulse width are shown in Fig. 5.32.

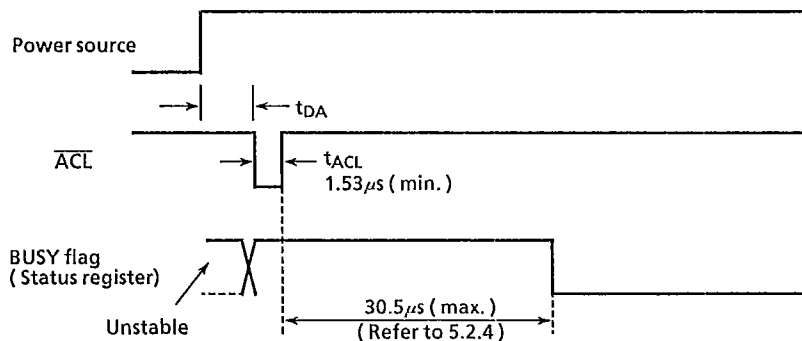


Fig 5.31 \overline{ACCL} pulse width

However, if width of t_{DA} after power ON is long, the unstable status lasts and causes malfunction (start recording / play-back, etc.) in Fig. 5.31.

So, a power on reset circuit is constructed by attaching a $1\mu\text{F}$ capacitor to the \overline{ACCL} terminal, makes the system initialization is possible immediately after power ON as illustrated in Fig. 5.32.

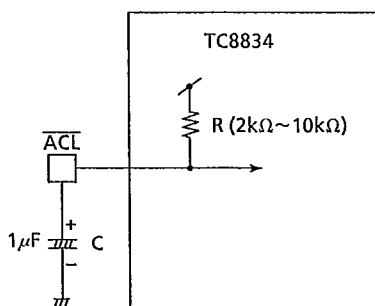


Fig.5.32 Power on reset circuit



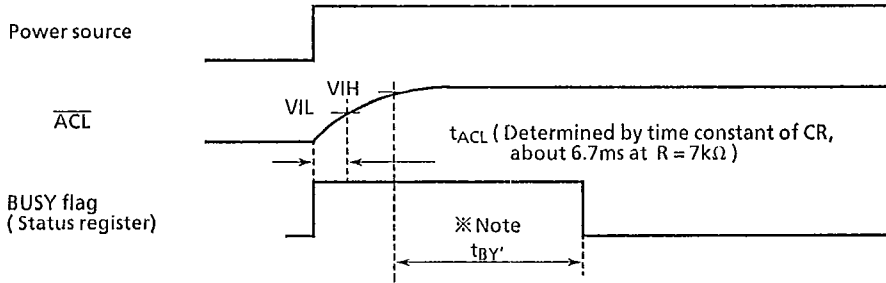
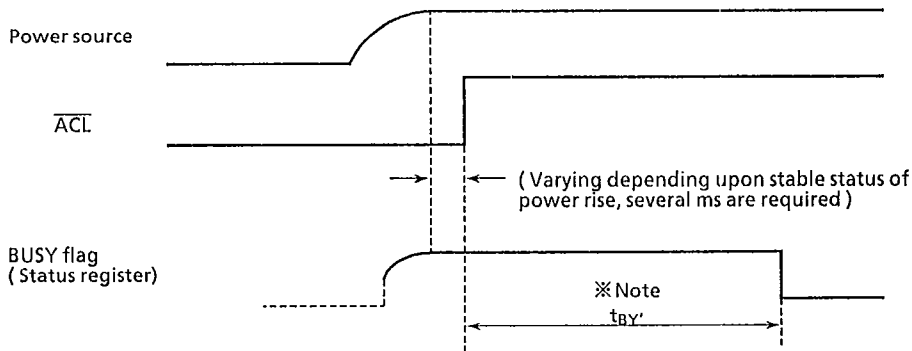


Fig 5.33 \overline{ACL} input at power on reset

However, the power on reset is effective only for a rapid step power rise and when power rise is gentle or power on / off is repeated in short cycle, no system initialization is performed.

Further, if the \overline{ACL} terminal can be controlled by a CPU regardless of power on / off at TC8834 side, the system initialization can be made as shown in Fig. 5.34



※ Note $t_{BY'}$ is a time that is required to stabilize oscillation after power on and it varies depending on an external oscillation device. (Several ms in case of CSB655)

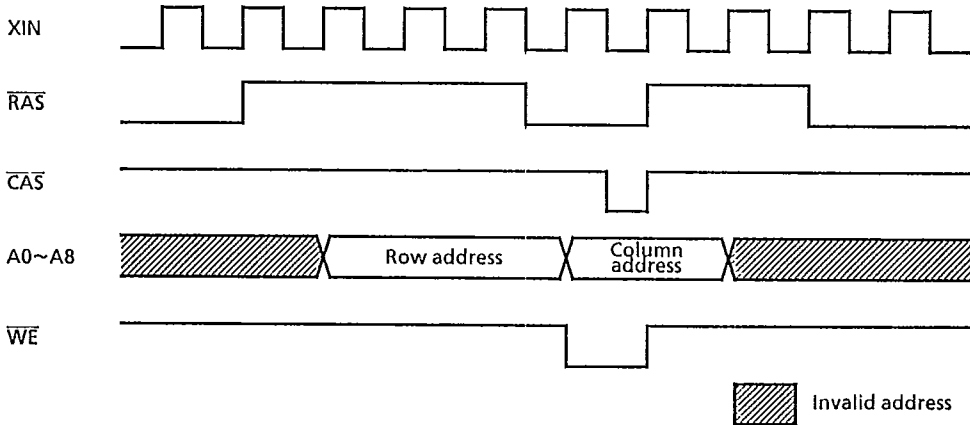
Fig.5.34 System initialization by CPU control

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5.10 Address Counter

An address counter of TC8834 is divided into row address as lower side and column one as upper side.



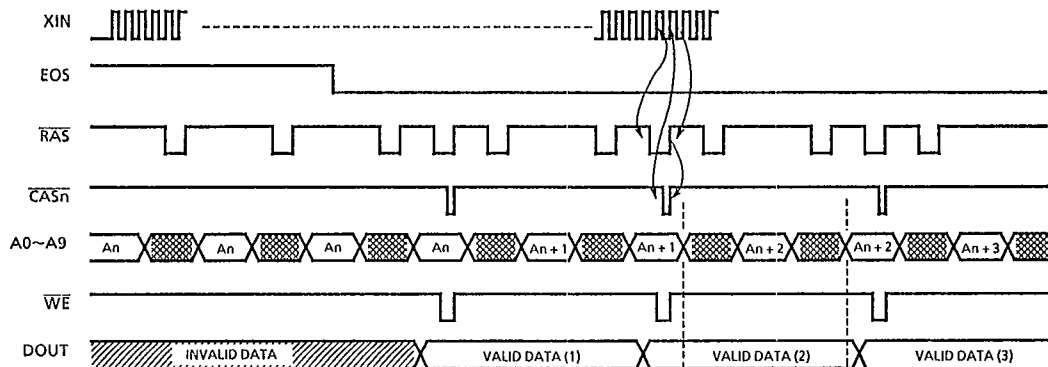
	Terminal name →	A9	A0	A9	A0
Designate address	1M	Column		Row	
		A19	A10	A9	A0
	256K	A17	A9	A8	A0

Fig.5.35 Output address

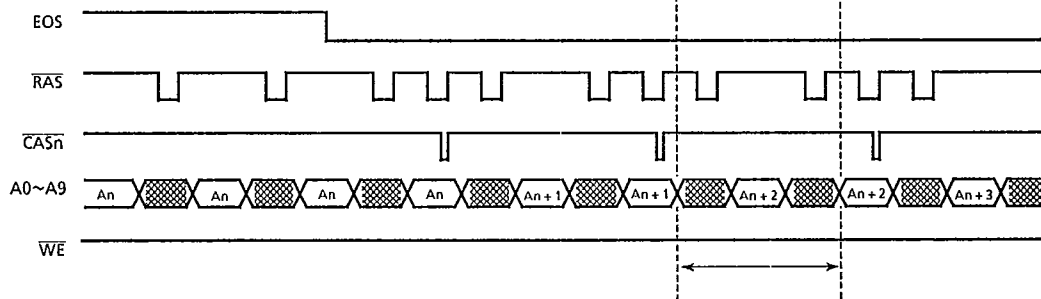
2


5.11 Access Timing at DRAM

(1) At recording (DRAMs write cycle) with 32Kbps bit rate.



(2) At play-back (DRAMs read cycle) with 32Kbps bit rate.



※ An : Output address
 VALID DATA : Voice data
 : Refresh address

Note Designates the refreshed address in above conditions
 every 6 addresses at 11 Kbps.
 every 4 addresses at 16 Kbps.
 every 3 addresses at 22 Kbps.
 par one cycle of read / write.

Fig.5.36 Access timing of DRAMs

5.12 Precautions

5.12.1 At the both CPU Control and Manual Control.

- Terminals of RS, M1, M2 and ENDLS should not be changed during the recording / play-back operation.
- During the initialization, operation such as recording / play-back stop. However, the refresh counter continues to operate so that, the contents of DRAMs can remain unchanged.
- When the DRAMs capacity is fully used, subsequent recording is not allowed to protect the data stored in DRAMs. Therefore, to make the recording newly, reset the address counter again by the \overline{ACL} terminal at the manual control or NOP and CLEAR command at the CPU control.

5.12.2 At the Manual Control.

- The selection of phrase, bit rate and recording / play-back are read by start input and not changed until next start input given. That is, TC8834 does not care those conditions (H or L level) after start operation has done.

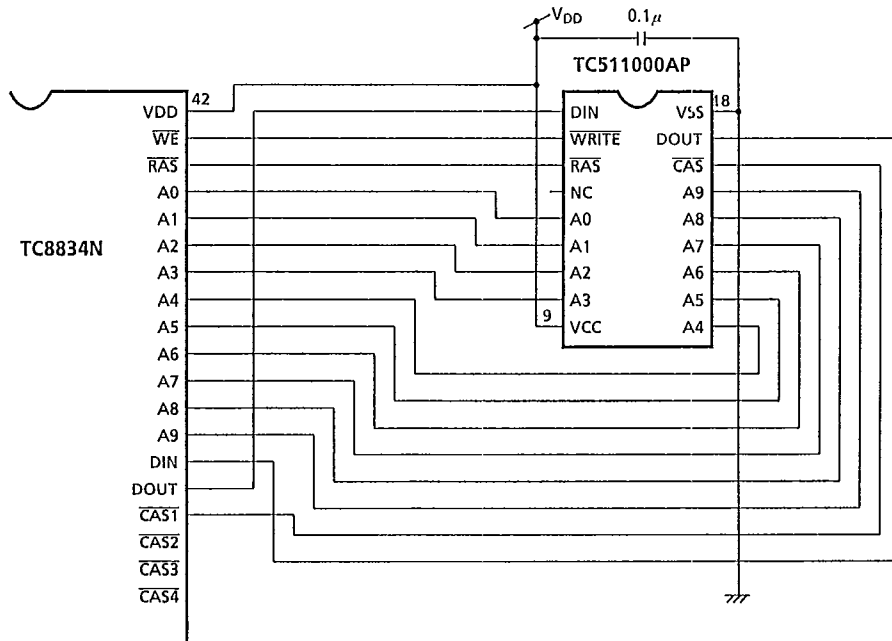
5.12.3 At the CPU Control

- Under the recording / play-back and play-back pause states, any command other than START, STOP and TRIG commands should not be given. When other commands are given to the TC8834, the operation becomes unstable.
- The recording by the LABEL command will always start by the voice trigger function.
- Do not issue any undefined command codes which are not listed on the commands list. If issue, the operation will become unstable.

5.13 Pin Description

The TC8834 uses DRAMs (Dynamic RAMs) for the storage of voice data.

Up to 4 pieces of 256K or 1M bit DRAMs are directly connected to the TC8834. But it is impossible to connect together with different capacity DRAMs in capacity.



※ A9 terminals are not used for 256K DRAM.

Fig.5.37 Connection of DRAM (In case of 1M DRAM)

Fig.5.37 shows the connection with DRAM. In case of two or more DRAMs, $\overline{CAS1}$ terminal of TC8834 must be connected to the \overline{CAS} terminal of 1'st DRAM, the $\overline{CAS2}$ to the \overline{CAS} of 2'nd DRAM and so on, That is, $\overline{CAS1} \sim \overline{CAS4}$ terminals must be connected to the \overline{CAS} terminals of each DRAM respectively. Other terminals for DRAM of TC8834 may be connected in parallel to every DRAM.

Some terminals of TC8834 must be set high or low according to the type and number of DRAM to be connected. These conditions shown in table 5.13 must not be changed during recording or reproducing operation.

Table 5.13 Terminal setting according to type and number of DRAMs

Terminal name DRAM capacity	RS1
256K bits	0
1M bits	1

Terminal name DRAM quantity	M2	M1
1 pcs.	0	0
2 pcs.	0	1
3 pcs.	1	0
4 pcs.	1	1

0 = L level
1 = H level



5.14 Clock Generator

TC8834 has two clock generators, ceramic resonator and capacitor are connected between XIN and XOUT terminals.

If using external clock, it should be fed to XIN terminal directly. (XOUT should be left open).

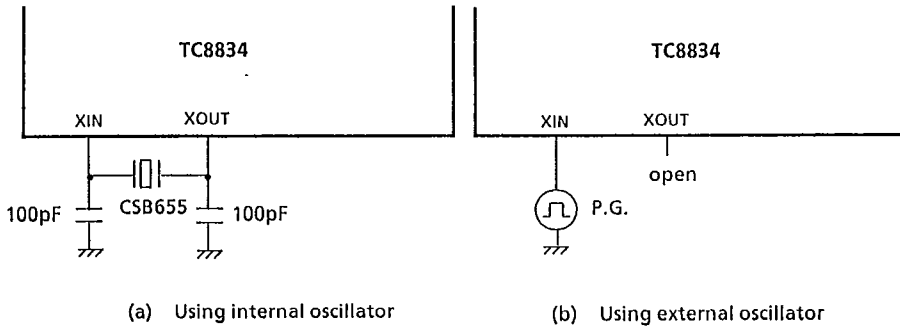


Fig.5.38 Oscillator

5.15 Analog Circuit

The TC8834, therefore voice recording / play-back system is easily composed with a microphone and an audio amplifier, filter circuit.

5.15.1 Microphone Amplifier Part

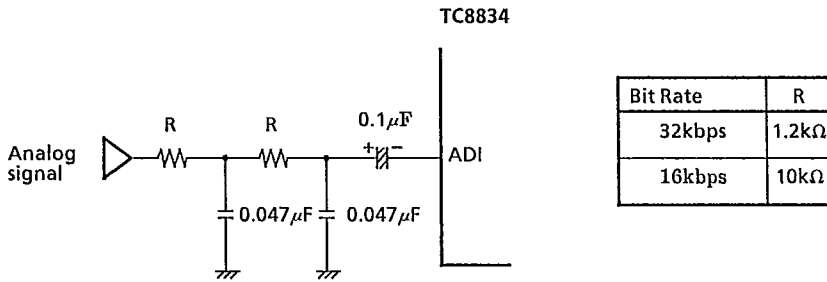


Fig 39 Example of connecting filter circuit.

5.15.2 The DAO Pin

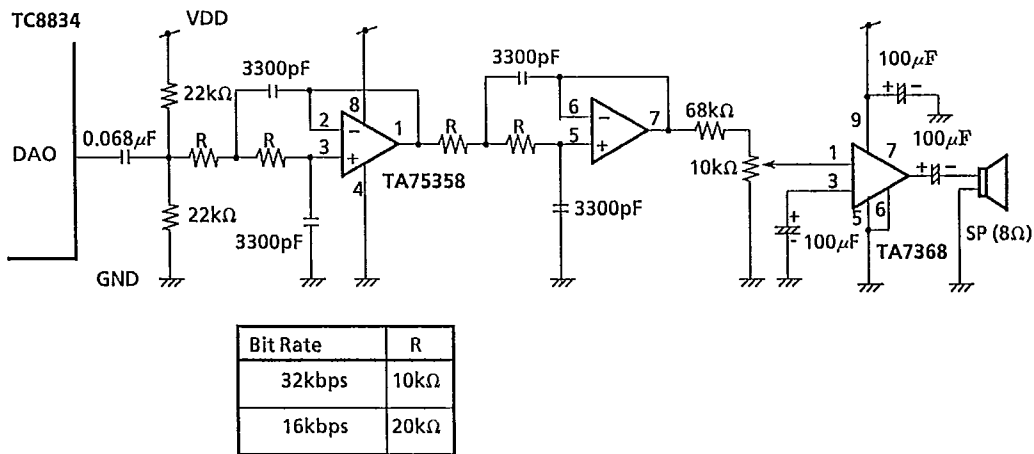


Fig 5.40 Example of connecting audio circuit.



6. ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Rating

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Supply voltage	-0.3 ~ 6.0	V
V_{IN}	Input voltage	-0.3 ~ $V_{DD} + 0.3$	V
V_{OUT}	Output voltage	-0.3 ~ $V_{DD} + 0.3$	V
T_{STG}	Storage temperature	-55 ~ 125	°C

6.2 Recommended Operating Conditions

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Supply voltage	4.5 ~ 5.5	V
V_{IN}	Input voltage	0 ~ V_{DD}	V
V_{OUT}	Output voltage	0 ~ V_{DD}	V
T_{OPR}	Operating temperature	-10 ~ 70	°C
f_{CLK}	Operating frequency (Ceramic Oscillation)	640 ~ 1000	kHz

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6.3 DC Characteristics (V_{DD} = 5V ± 10%, T_a = 25°C)

SYMBOL	ITEM	CONDITION	MIN	TYP	MAX	UNIT
I _{IH1}	Input high current (D0~D3, \overline{WR} , \overline{RD} , \overline{CE} , BP50.1, MREC, ENDS)	V _{IN} = V _{DD} , CPUM = L CHAT = L, OFF = L, STBY = L	20	100	500	μA
I _{IL1}	Input low current 1 (DIN)	V _{IN} = 0V	20	100	500	
I _{IL2}	Input low current 2 (\overline{ACL})	V _{IN} = 0V	0.4	1	1.6	mA
I _{ILK}	Input leakage current	V _{IN} = 0~V _{DD} , CPUM = H	-	-	10	μA
V _{IH1}	Input high voltage 1	DIN, D0~D3, \overline{WR} , \overline{RD} , \overline{CE}	2.4	-	-	V
V _{IH2}	Input high voltage 2	Except above	4.1	-	-	
V _{IL1}	Input low voltage 1	DIN, D0~D3, \overline{WR} , \overline{RD} , \overline{CE}	-	-	0.8	
V _{IL2}	Input low voltage 2	Except above	-	-	0.4	
I _{OH}	Output high current	V _{OUT} = 2.4 V	0.5	-	-	mA
I _{OL}	Output high current	V _{OUT} = 0.8 V	0.5	-	-	
I _{SS1}	Supply current	Under no signal I _{OUT} = 0 mA	-	-	2	mA

- Precautions :
- 1) Each TYP. value is under V_{DD} = 5.0V, T_a = 25°C
 - 2) MIN. MAX. values are defined by their absolute values.
 - 3) Supply current measured with external clock generator of 655kHz at operation mode and 46kHz at stand-by mode

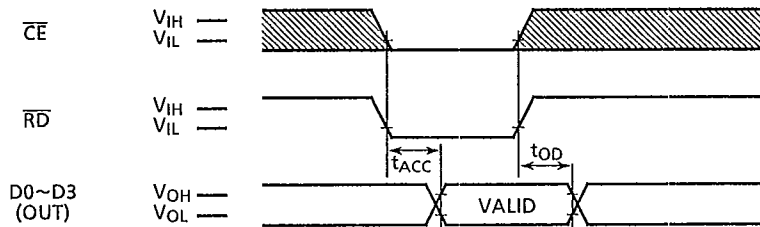


6.4 AC Characteristics ($V_{DD} = 5V \pm 10\%$, $T_a = 25^\circ C$, $f_{CLK} = 655kHz$, $C_L = 50pF$)

6.4.1 Data Read (read status register)

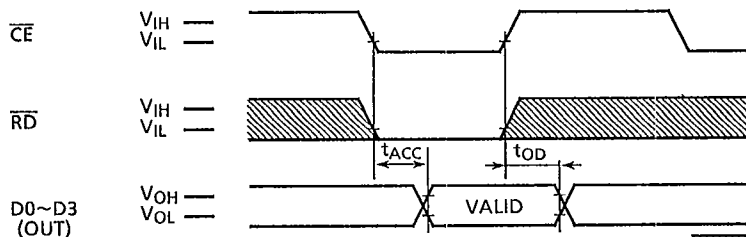
SYMBOL	ITEM	MIN	TYP	MAX	UNIT
t_{ACC}	Read access time	—	—	300	ns
t_{OD}	Output disable time	—	—	150	

Data read (1)

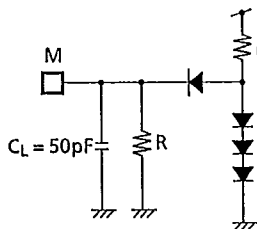


Data read (2) 9.4.6

Measurement circuit



Don't Care



Input level
 • $V_{IH} = 2.6V$
 • $V_{IL} = 0.6V$

Comparison level
 • $V_{IH} = 2.4V$
 • $V_{IL} = 0.8V$
 • $V_{OH} = 2.4V$
 • $V_{OL} = 0.8V$

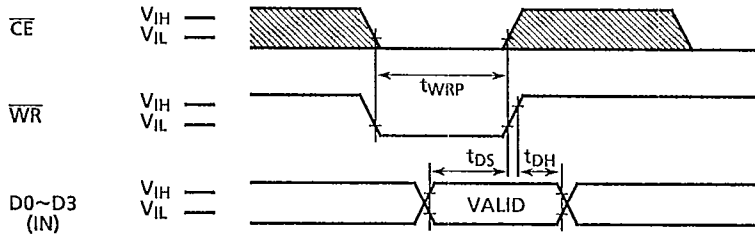
※ R =
 t_{ACC} 10kΩ
 t_{OD} 1kΩ

Diode : 1S1588

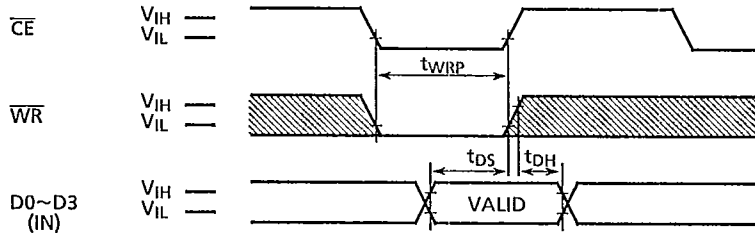
6.4.2 Data Write (write of command)


SYMBOL	ITEM	MIN	TYP	MAX	UNIT
t_{DS}	Data set up time	100	—	—	ns
t_{DH}	Data hold time	150	—	—	
t_{WRP}	\overline{WR} pulse width	300	—	—	

Data write (1)



Data write (2)



 Don't Care

Input level

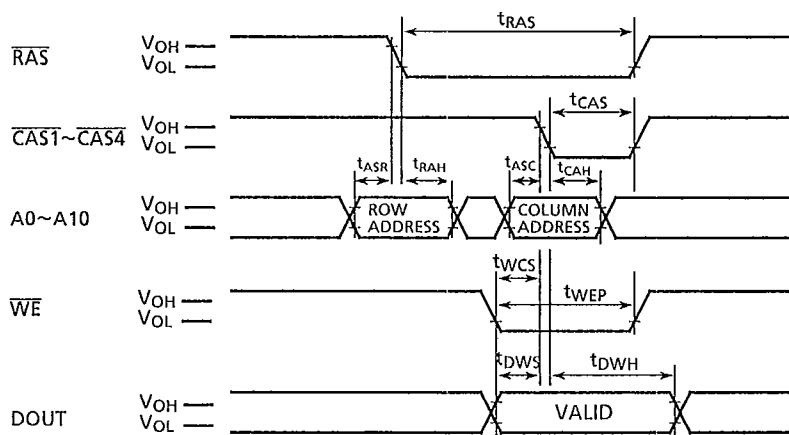
- $V_{IH} = 2.6V$
- $V_{IL} = 0.6V$

Comparison level

- $V_{IH} = 2.4V$
- $V_{IL} = 0.8V$
- $V_{OH} = 2.4V$
- $V_{OL} = 0.8V$

6.4.3 Voice Analysis (recording)

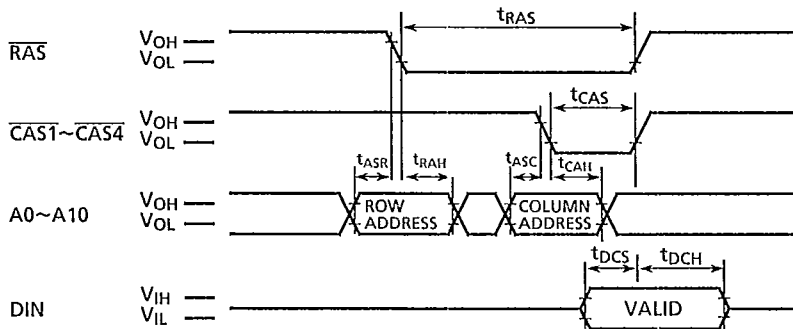
SYMBOL	ITEM	MIN	TYP	MAX	UNIT
t_{ASR}	Row address set up time	150	—	—	ns
t_{RAH}	Row address hold time	350	763	—	
t_{RAS}	\overline{RAS} pulse width	—	2.29	—	μs
t_{ASC}	Column address set up time	150	—	—	ns
t_{CAH}	Column address hold time	3.00	3.81	—	μs
t_{CAS}	\overline{CAS} pulse width	—	763	—	ns
t_{WCS}	Write command set up time	350	763	—	ns
t_{WEP}	\overline{WE} pulse width	—	1.53	—	μs
t_{DWS}	Data output set up time	4.0	—	—	μs
t_{DWH}	Data output hold time	25.0	—	—	



Comparison level
 $V_{OH} = 2.2V$
 $V_{OL} = 0.8V$

6.4.4 Voice Synthesis (Play-back)

SYMBOL	ITEM	MIN	TYP	MAX	UNIT
t_{DCS}	Data input set up time	500	—	—	ns
t_{DCH}	Data input hold time	0	—	—	



Note : Excepting t_{DCS} , t_{DCH} the values applied in the above are the same as those at voice analysis.

Input level

- $V_{IH} = 2.4V$
- $V_{IL} = 0.6V$

Comparison level

- $V_{IH} = 2.2V$
- $V_{IL} = 0.8V$
- $V_{OH} = 2.2V$
- $V_{OL} = 0.8V$



6.5 Characteristics of Analog Circuit

(Unless otherwise specified : VSS1 = VSS2 = 0V, VDD = 5V, Ta = 25 °C, fin = 1 kHz)

6.5.1 Audio In

SYMBOL	ITEM	TERMINAL	CONDITION	MIN	TYP	MAX	UNIT
V _{IN}	Input voltage range	ADI	-	-	± 1.2	± 1.6	V
R _{IN}	Input impedance	ADI	-	-	50	-	kΩ
V _{TRIG}	Voice trigger level	ADI	-	-	± 160	-	mV
V _{SLNT}	Stop recording / play-back level	ADI	-	-	± 310	-	mV

6.5.2 Audio Out

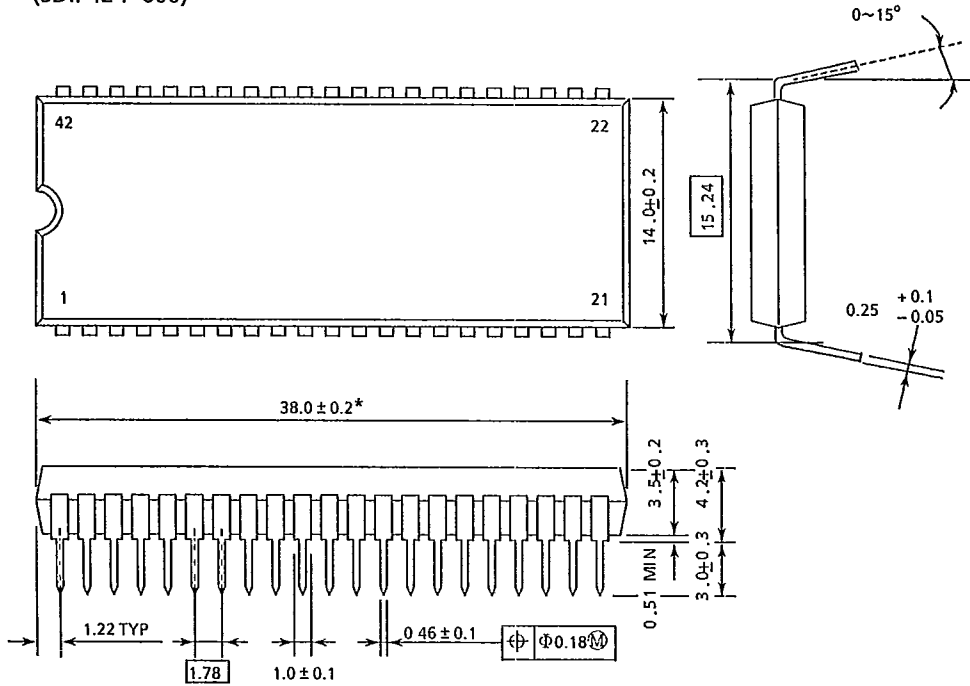
SYMBOL	ITEM	TERMINAL	CONDITION	MIN	TYP	MAX	UNIT
R _{OUT}	Output impedance	DAO	-	-	5	-	kΩ

Note Values of input voltage range, voice trigger level and stop recording / play-back level are measured as signals biased to 1/2VDD.

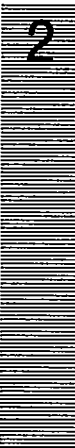
7. OUTLINE DRAWINGS

(1) 42 PIN SHRINK DUAL IN PACKAGE
(SDIP42-P-600)

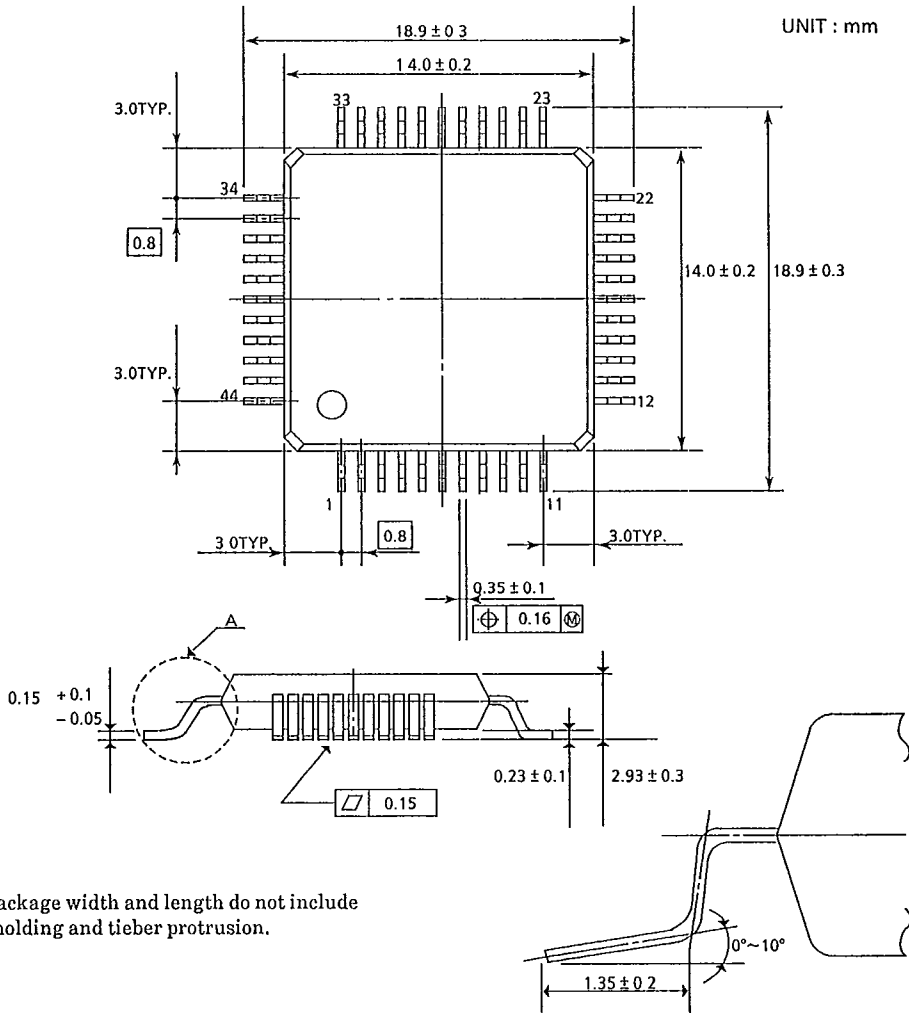
UNIT: mm



Package width and length do not include molding and tiebar protrusion.



(2) 44 PIN MINI FLAT PACKAGE
(QFP44-P-1414)



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8. APPLICATION CIRCUIT

MANUAL CONTROL TYPE

