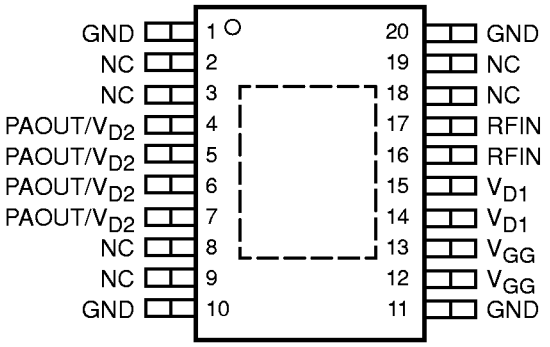
- **Power Amplifier for 1.9-GHz CDMA Applications**
- **0.5-Micron GaAs MESFET Technology**
- **Operates from 3-V to 3.6-V Supply**
- **High Output Power . . . 27.5-dBm Typical at 3-V Supply and 1.9 GHz**
- **Gain Linearity Better Than 0.5 dB Over a 37-dB Dynamic Range**
- **High Adjacent Channel Power Rejection**
- **20-Pin Plastic Surface-Mount TSSOP PWP PowerPAD™ (PWP)**

PWP PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TRF4002 personal communications system (PCS) RF power amplifier is a gallium arsenide (GaAs), integrated circuit housed in a 20-pin plastic surface-mount, thin-shrink small outline package (TSSOP). The package has a solderable pad that improves the package thermal performance by bonding the pad to an external thermal plane. The pad also acts as a low-inductance electrical path-to-ground and must be electrically connected to the printed-circuit board (PCB) ground plane as a continuation of the regular package terminals that are designated GND. The integrated circuit is suitable for 1.9-GHz code-division multiple-access (CDMA) applications.

The TRF4002 is a power amplifier that uses a two-stage topology with an on-/off-chip output inductor and impedance matching network to minimize cost. It is suitable for use in mobile systems that require high linearity. It can deliver 27.5-dBm typical output power optimized for minimum adjacent channel power.

These devices have no built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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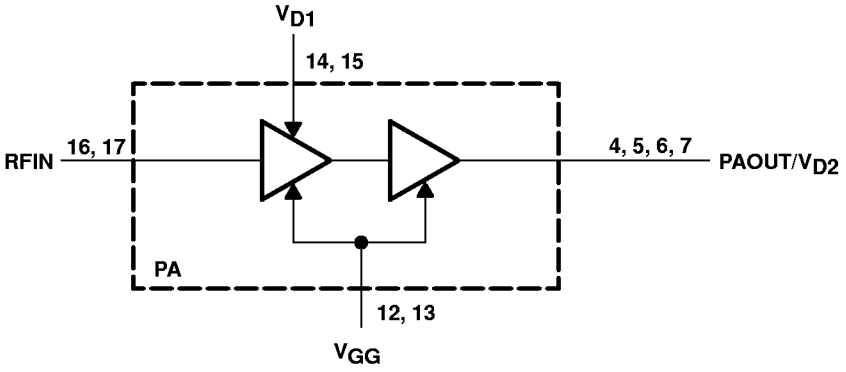
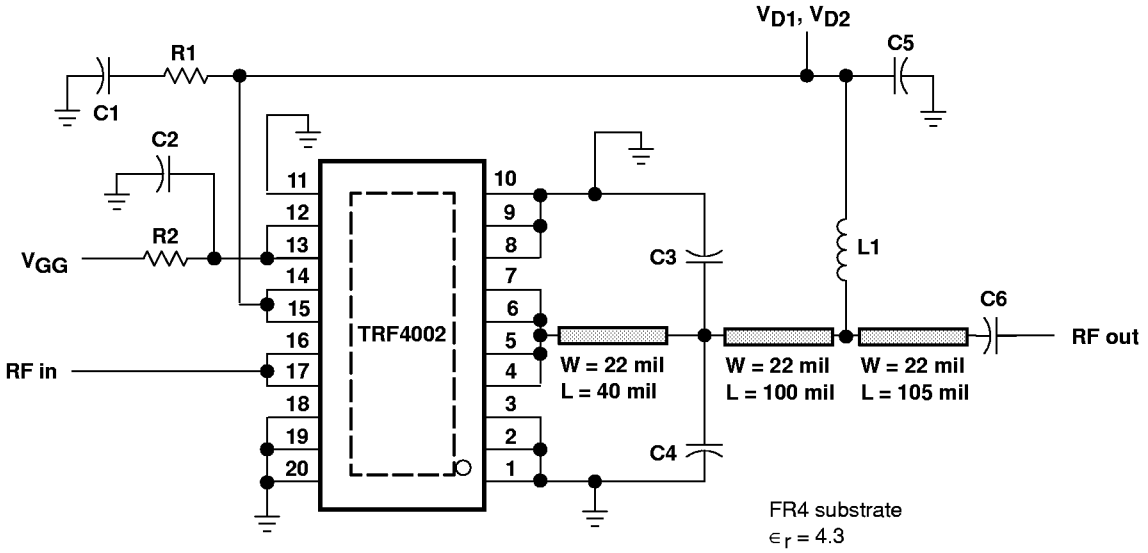
functional block diagram



application circuit



FR4 substrate
ϵ_r = 4.3
h = 12 mils
50 Ω line width = 22 mils

L1 = 12 nH
R1 = 10 Ω
R2 = 0 Ω
C1 = .01 μF
C2 = 150 pF
C3 = 1.8 pF
C4 = 1.8 pF
C5 = .01 μF
C6 = 20 pF

NOTE: Backside must be electrically grounded

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	1, 10, 11, 20		Ground
PAOUT/V_{D2}	4, 5, 6, 7	I/O	RF output and second-stage drain bias
RFIN	16, 17	I	RF input
V_{GG}	12, 13	I	Gate bias voltage
V_{D1}	14, 15	I	First-stage drain bias
NC	2, 3, 8, 9, 18, 19		No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{D1}, V_{D2} (see Note 1) . . . . . 0 V to 5 V
Bias voltage, V_{GG} (see Note 2) . . . . . – 5 to 0 V
Input power, RFIN . . . . . 15 dBm
Continuous power dissipation at or below T_A = 25°C . . . . . 4 W
Operating free-air temperature range, T_A . . . . . –30°C to 80°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. V_{GG} = –1 V
2. $V_{D1} = V_{D2}$ = 0 V

recommended operating conditions

	MIN	NOM	MAX	UNIT
Drain supply voltage, V_{D1}, V_{D2}	3		3.6	V
Gate bias voltage, V_{GG}	–0.6	–0.35	–0.2	V
Operating free-air temperature, T_A	–30		80	°C

electrical characteristics over recommended operating free-air temperature range, $V_{D1} = V_{D2} = 3$ V, $V_{GG} = -0.35$ V

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Input frequency range (RFIN)			1850		1910	MHz
$t_{d(on)}$	Turn-on time,(see Note 3)					50	µs
$t_{d(off)}$	Turn-off time, (see Note 4)					50	µs
	Gain			17	18	19	dB
	Noise figure					10	dB
	Reverse isolation			40			dB
	Input VSWR (RFIN) (see Note 5)					2:1	
	Output VSWR (PA_{OUT}/V_{D2}) (see Note 5)		Small signal conditions		2:1		
	Nominal linear output power				27.5		dBm
	Power-added efficiency		P_O = 27.7 dBm		30%		
	Gain linearity		–10 dBm < P_O < 27.7 dBm			±0.5	dB
	Adjacent channel power rejection (see Note 6)	> ±1.25-MHz offset		–44			dBc
		> ±2.25-MHz offset		–54			dBc
	Harmonics					–30	dBc
	Quiescent current				450		mA

† Typical values are at T_A = 25°C

NOTES: 3. Turn-on time is that time between the instant the power amplifier bias voltage changes from 0 V and the instant when the device output power is within ±1 dB of its rated output value.
4. Turn-off time is that time between the instant that the PA bias voltage begins to fall and the instant when the PA current consumption is less than 1 mA.
5. VSWR = voltage standing wave ratio
6. Measured at 27.5-dBM total output power with CDMA input signal.

stability

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Stability	Output VSWR < 6:1, All phase angles			–70	dBc

† Typical values are at T_A = 25°C

TYPICAL CHARACTERISTICS

GAIN
vs
INPUT POWER

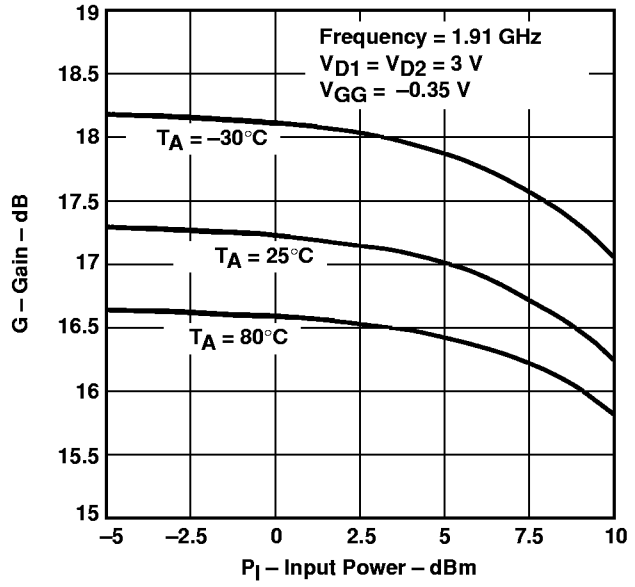


Figure 1

OUTPUT POWER
vs
INPUT POWER

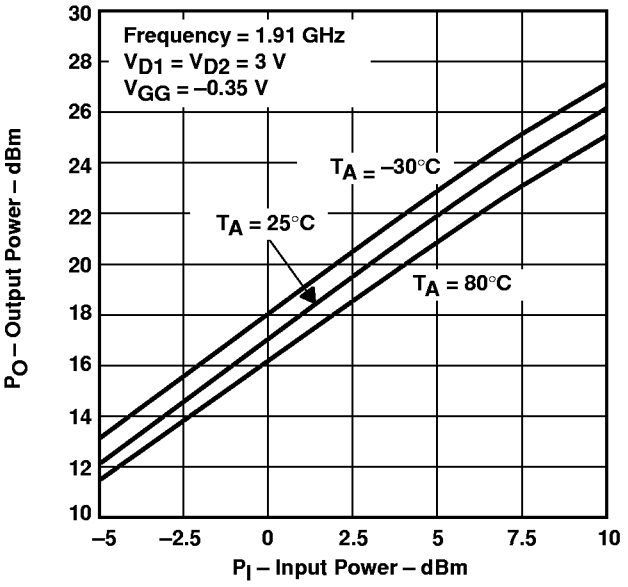


Figure 2

INPUT RETURN LOSS
vs
FREQUENCY

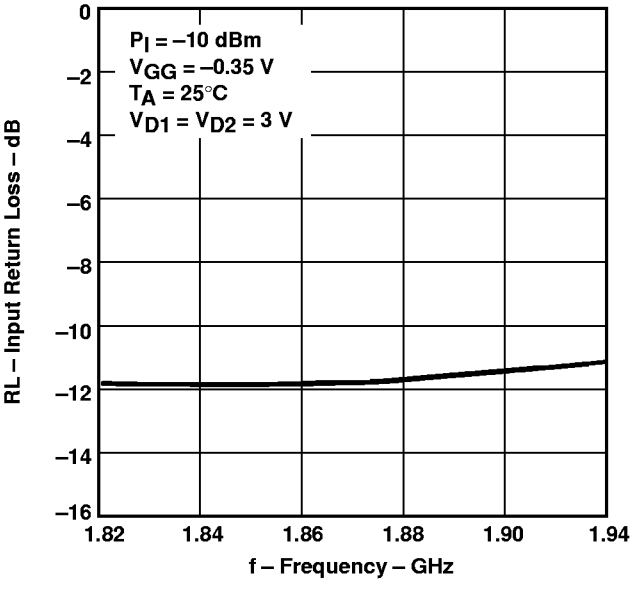


Figure 3

OUTPUT POWER
vs
FREQUENCY

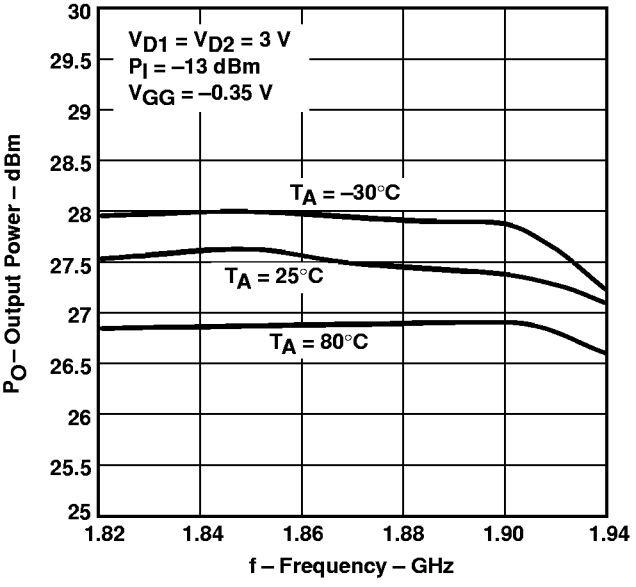


Figure 4

TYPICAL CHARACTERISTICS

GAIN
vs
FREQUENCY

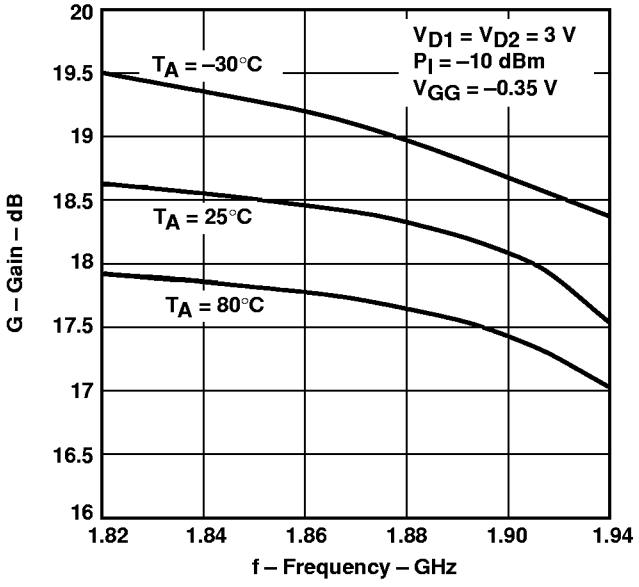


Figure 5

POWER ADDED EFFICIENCY
vs
INPUT POWER

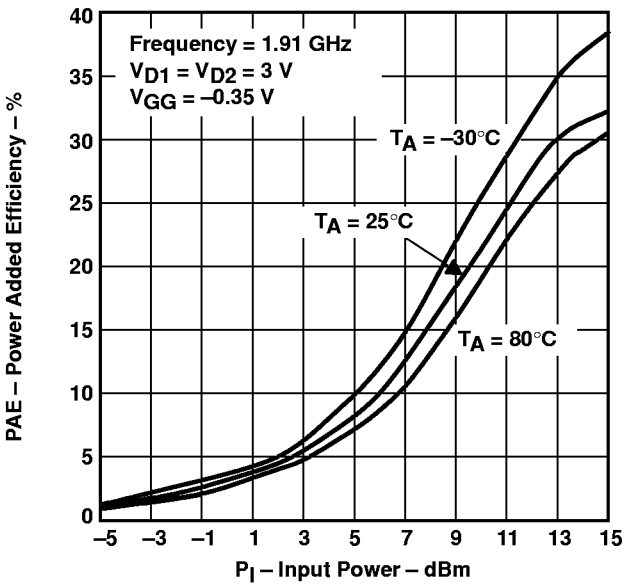


Figure 6

POWER ADDED EFFICIENCY
vs
FREQUENCY

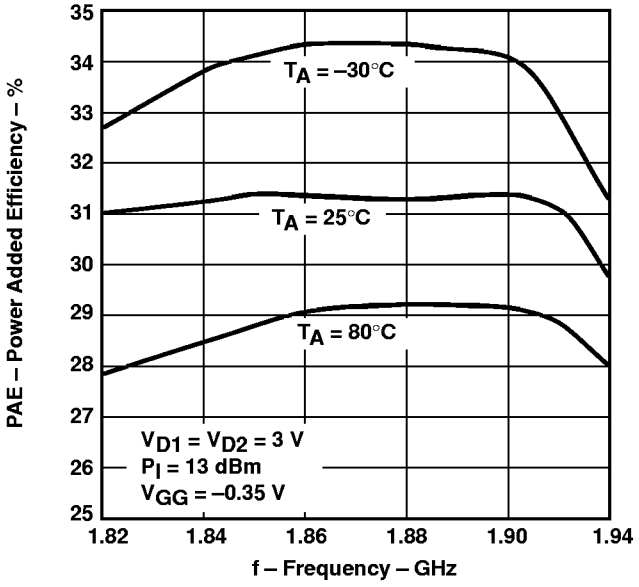


Figure 7

OUTPUT POWER
vs
DRAIN VOLTAGE

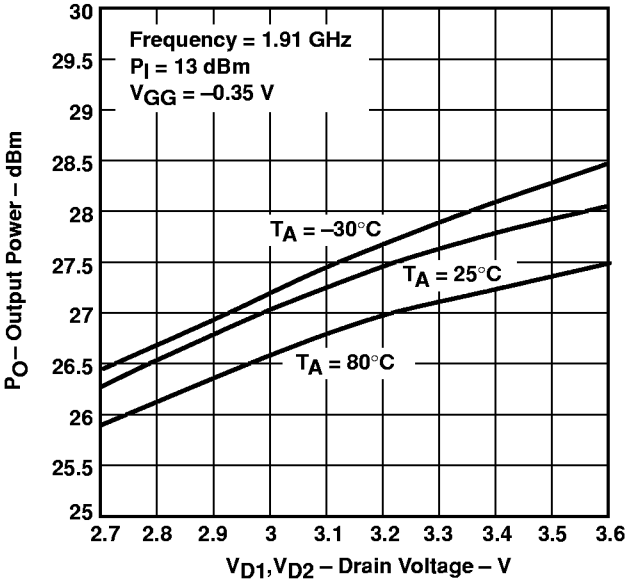
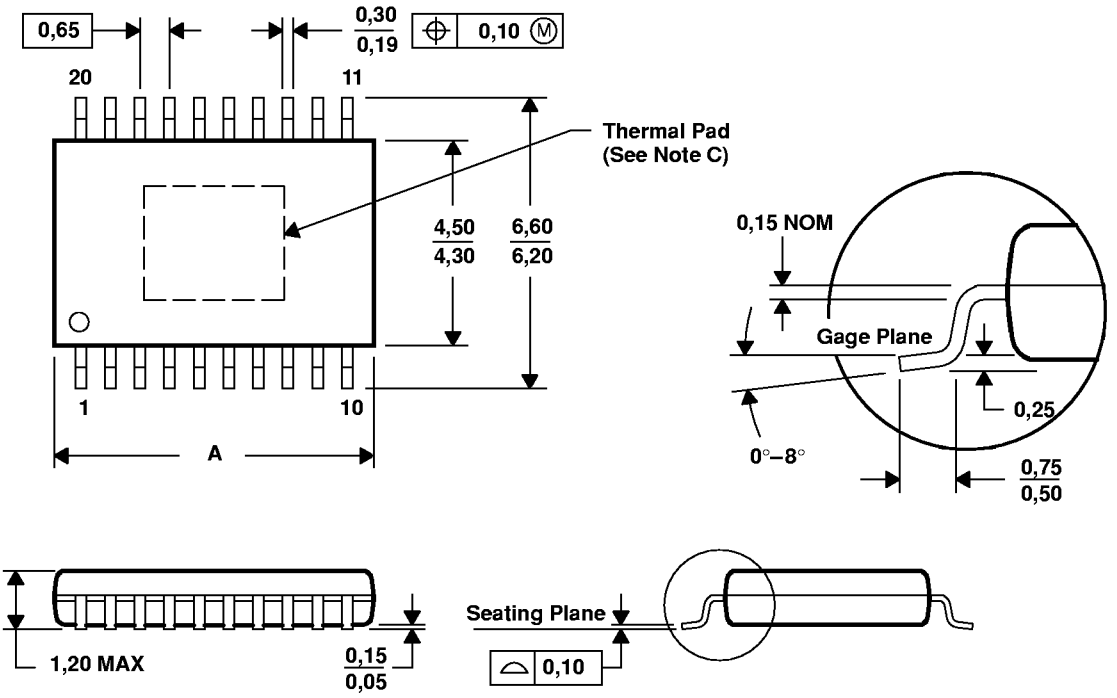


Figure 8

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**

20-PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/E 03/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This solderable pad is electrically and thermally connected to the backside of the die and possibly selected leads. The maximum pad size on the printed-circuit board should be equal to the package body size – 2,0mm.

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