DATA SHEET

NEC

MOS INTEGRATED CIRCUIT
MC-458DA72

8M-WORD BY 72-BIT SYNCHRONOUS DYNAMIC RAM MODULE REGISTERED TYPE

Description

The MC-458DA72 is a 8,388,608 words by 72 bits synchronous dynamic RAM module on which 9 pieces of 64M SDRAM : μPD4564841 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 8,388,608 words by 72 bits organization
- Clock frequency and burst cycle time

Family	/CAS latency	Clock frequency (MAX.)	Burst cycle time (MAX.)	Power consumption (MAX.)	
				Active	Standby
MC-458DA72-A10	CL = 3	100 MHz	10 ns	4,644 mW	64.8 mW (CMOS level input)
	CL = 2	67 MHz	15 ns	4,482 mW	
MC-458DA72-A12	CL = 3	83 MHz	12 ns	4,320 mW	
	CL = 2	55 MHz	18 ns	4,158 mW	
★ MC-458DA72-A10B	CL = 3	100 MHz	10 ns	4,806 mW	54 mW (CMOS level input)
	CL = 2	67 MHz	15 ns	4,482 mW	

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Quad internal banks controlled by BA0 and BA1 (Bank Select)
- Programmable burst-length : 1, 2, 4, 8 and full page
- Programmable wrap sequence (sequential / interleave)
- Programmable /CAS latency (2, 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- Single +3.3 V +0.3 / −0.15 V power supply
- LVTTL compatible
- 4,096 refresh cycles / 64 ms
- Burst termination by Burst Stop command and Precharge command
- 200-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Registered type
- Serial PD

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The mark ★ shows major revised points.

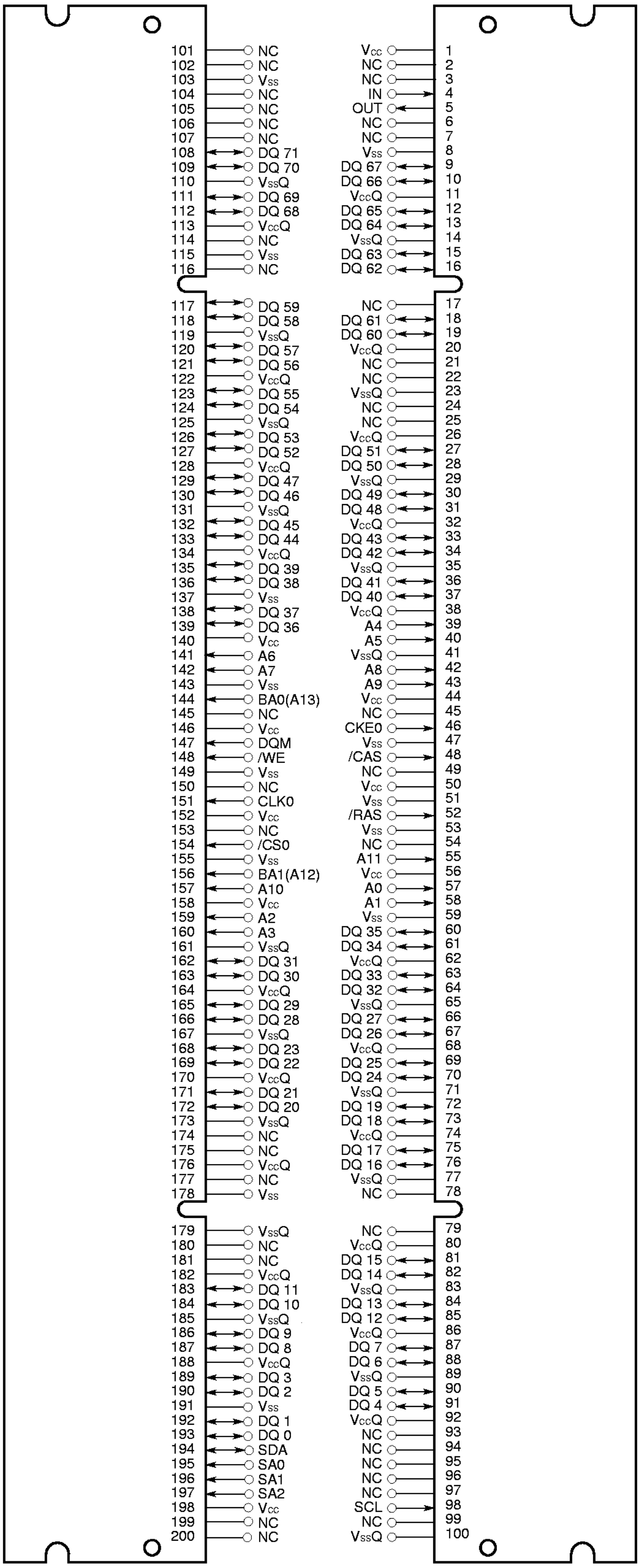
Ordering Information

Part number	Clock frequency (MAX.)	Package	Mounted devices
MC-458DA72F-A10	100 MHz	200-pin Dual In-line Memory Module (Socket Type) Edge connector : Gold plated 38.1 mm (1.5 inch) height	9 pieces of μPD4564841G5 (400 mil TSOP (II)) [Single side]
MC-458DA72F-A12	83 MHz		
★ MC-458DA72F-A10B	100 MHz		

Pin Configuration

200-pin Dual In-line Memory Module Socket Type (Edge connector: Gold plated)

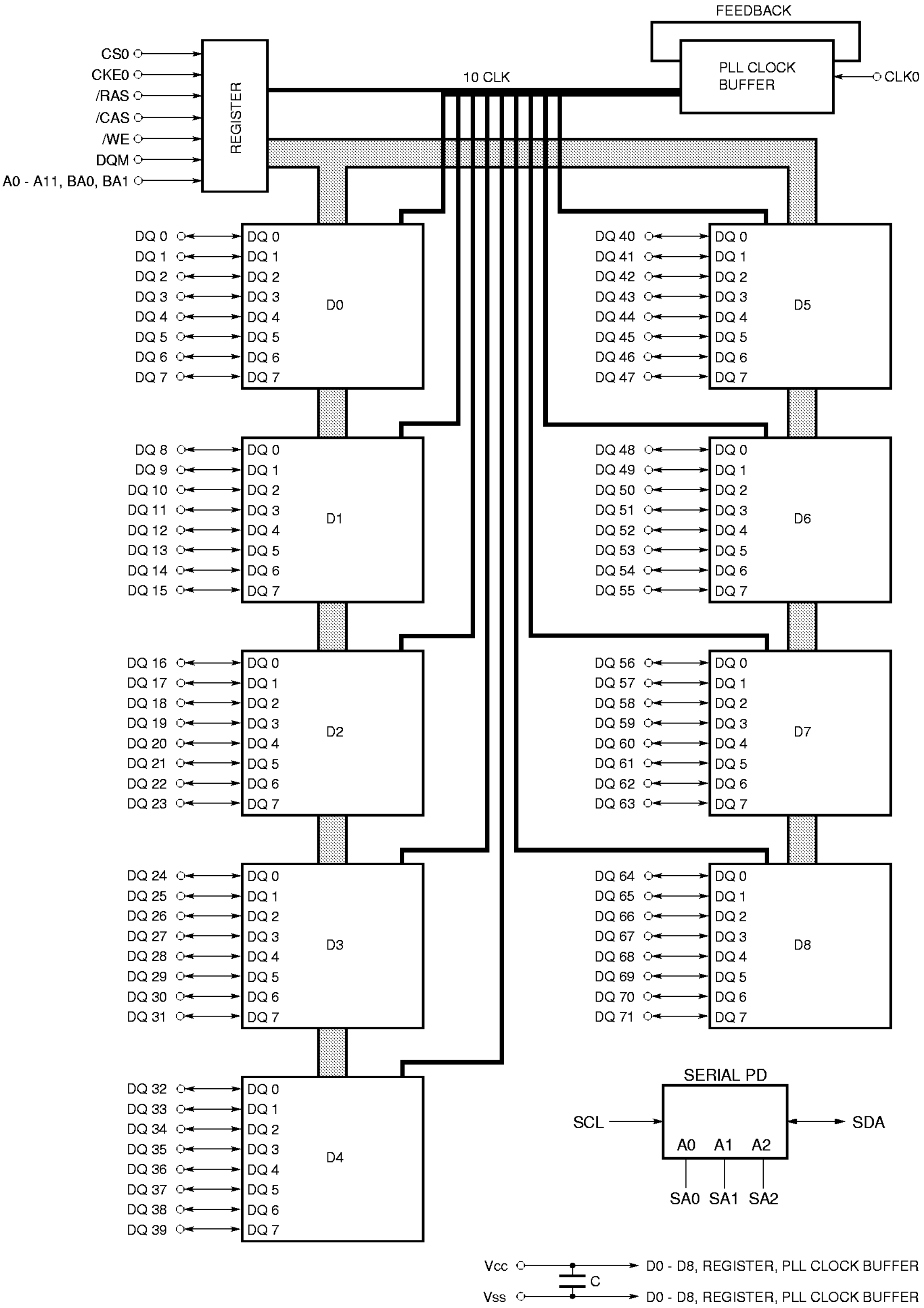
[MC-458DA72F]



/XXX indicates active low signal.

A0 - A11	: Address Inputs
[Row : A0 - A11, Column : A0 - A8]	
BA0 (A13), BA1 (A12)	: SDRAM Bank Select
DQ0 - DQ71	: Data Inputs / Outputs
CLK0	: Clock Input
CKE0	: Clock Enable Input
/CS0	: Chip Select Input
/RAS	: Row Address Strobe
/CAS	: Column Address Strobe
/WE	: Write Enable
DQM	: DQ Mask Enable
IN, OUT	: Unbuffered Physical Detect Input / Output (separate)
SA0 - SA2	: Address Input for EEPROM
SDA	: Serial Data I/O for PD
SCL	: Clock Input for PD
Vcc	: Power Supply
VccQ	: Power Supply for Input / Output
Vss	: Ground
VssQ	: Ground for Input / Output
NC	: No Connection

Block Diagram



Remarks 1. A 10 Ω ± 5% resistor shall be wired in series with DQ0 - DQ71 near the card edge connector. All clock line outputs from the PLL CLOCK BUFFER shall be equal length.

2. D0 - D8 : μPD4564841 (2M words × 8 bits × 4 banks)

Electrical Specifications

- All voltages are referenced to V_{SS} (GND).
- After power up, wait more than 100 μs and then, execute power on sequence and auto refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V_{CC}		–0.5 to +4.6	V
Voltage on input pin relative to GND	V_T		–0.5 to +4.6	V
Short circuit output current	I_O		50	mA
Power dissipation	P_D		12	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.15	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC}+0.3	V
Low level input voltage	V_{IL}		–0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A11, BA0 (A13), BA1 (A12), /RAS, /CAS, /WE, CKE0, /CS0, DQM			15	pF
	C_{I2}	CLK0			8	
Data input / output capacitance	$C_{I/O}$	DQ0 - DQ71			10	pF

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

[MC-458DA72-A10, 458DA72-A12]

Parameter	Symbol	Test condition		Grade	MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC\,(MIN.)}$, $I_O = 0$ mA	/CAS latency = 2	-A10		930	mA	1
				-A12		885		
			/CAS latency = 3	-A10		975		
				-A12		930		
Precharge standby current in power down mode	I_{CC2}P	CKE $\leq V_{IL\,(MAX.)}$, $t_{CK} = 15$ ns				27	mA	2
	I_{CC2}PS	CKE $\leq V_{IL\,(MAX.)}$, $t_{CK} = \infty$				18		
Precharge standby current in non power down mode	I_{CC2}N	CKE $\geq V_{IH\,(MIN.)}$, $t_{CK} = 15$ ns, /CS $\geq V_{IH\,(MIN.)}$, Input signals are changed one time during 30 ns.				180	mA	2
	I_{CC2}NS	CKE $\geq V_{IH\,(MIN.)}$, $t_{CK} = \infty$, Input signals are stable.				54		
Active standby current in power down mode	I_{CC3}P	CKE $\leq V_{IL\,(MAX.)}$, $t_{CK} = 15$ ns				45	mA	2
	I_{CC3}PS	CKE $\leq V_{IL\,(MAX.)}$, $t_{CK} = \infty$				36		
Active standby current in non power down mode	I_{CC3}N	CKE $\geq V_{IH\,(MIN.)}$, $t_{CK} = 15$ ns, /CS $\geq V_{IH\,(MIN.)}$, Input signals are changed one time during 30 ns.				225	mA	2
	I_{CC3}NS	CKE $\geq V_{IH\,(MIN.)}$, $t_{CK} = \infty$, Input signals are stable.				90		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK\,(MIN.)}$, $I_O = 0$ mA	/CAS latency = 2	-A10		1,020	mA	3
				-A12		930		
			/CAS latency = 3	-A10		1,245		
				-A12		1,155		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC\,(MIN.)}$	/CAS latency = 2	-A10		1,245	mA	4
				-A12		1,155		
			/CAS latency = 3	-A10		1,290		
				-A12		1,200		
Self refresh current	I_{CC6}	CKE ≤ 0.2 V				18	mA	2
Input leakage current	$I_{I\,(L)}$	$V_I = 0$ to 3.6 V, All other pins not under test = 0 V			–10	+10	μA	
Output leakage current	$I_{O\,(L)}$	D_{OUT} is disabled, $V_O = 0$ to 3.6 V			–5	+5	μA	
High level output voltage	V_{OH}	$I_O = -2.0$ mA			2.4		V	
Low level output voltage	V_{OL}	$I_O = +2.0$ mA				0.4	V	

Notes 1. I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during $t_{CK\,(MIN.)}$.

2. $V_{CC} - 0.2$ V $\leq V_{IH\,(CLK)} \leq V_{IH\,(MAX.)}$, 0 V $\leq V_{IL} \leq 0.2$ V

3. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during $t_{CK\,(MIN.)}$.

4. I_{CC5} is measured on condition that addresses are changed only one time during $t_{CK\,(MIN.)}$.

★ **[MC-458DA72-A10B]**

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	Burst length = 1	/CAS latency = 2		885	mA	**1**
		$t_{RC} \geq t_{RC\,(MIN.)}$, $I_O = 0$ mA	/CAS latency = 3		975		
Precharge standby current in power down mode	$I_{CC2}P$	CKE $\leq V_{IL\,(MAX.)}$, $t_{CK} = 15$ ns			209	mA	**2**
	$I_{CC2}PS$	CKE $\leq V_{IL\,(MAX.)}$, $t_{CK} = \infty$			15		
Precharge standby current in non power down mode	$I_{CC2}N$	CKE $\geq V_{IH\,(MIN.)}$, $t_{CK} = 15$ ns, /CS $\geq V_{IH\,(MIN.)}$, Input signals are changed one time during 30 ns.			380	mA	**2**
	$I_{CC2}NS$	CKE $\geq V_{IH\,(MIN.)}$, $t_{CK} = \infty$, Input signals are stable.			54		
Active standby current in power down mode	$I_{CC3}P$	CKE $\leq V_{IL\,(MAX.)}$, $t_{CK} = 15$ ns			245	mA	**2**
	$I_{CC3}PS$	CKE $\leq V_{IL\,(MAX.)}$, $t_{CK} = \infty$			36		
Active standby current in non power down mode	$I_{CC3}N$	CKE $\geq V_{IH\,(MIN.)}$, $t_{CK} = 15$ ns, /CS $\geq V_{IH\,(MIN.)}$, Input signals are changed one time during 30 ns.			425	mA	**2**
	$I_{CC3}NS$	CKE $\geq V_{IH\,(MIN.)}$, $t_{CK} = \infty$, Input signals are stable.			90		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK\,(MIN.)}$,	/CAS latency = 2		930	mA	**3**
		$I_O = 0$ mA	/CAS latency = 3		1,245		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC\,(MIN.)}$	/CAS latency = 2		1,245	mA	**4**
			/CAS latency = 3		1,335		
Self refresh current	I_{CC6}	CKE ≤ 0.2 V			209	mA	**2**
Input leakage current	$I_{I\,(L)}$	$V_I = 0$ to 3.6 V, All other pins not under test = 0 V		–10	+10	μA	
Output leakage current	$I_{O\,(L)}$	D_{OUT} is disabled, $V_O = 0$ to 3.6 V		–1.5	+1.5	μA	
High level output voltage	V_{OH}	$I_O = -4.0$ mA		2.4		V	
Low level output voltage	V_{OL}	$I_O = +4.0$ mA			0.4	V	

Notes 1. I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during $t_{CK\,(MIN.)}$.

2. $V_{CC} - 0.2\ V \leq V_{IH\,(CLK)} \leq V_{IH\,(MAX.)}$, $0\ V \leq V_{IL} \leq 0.2\ V$

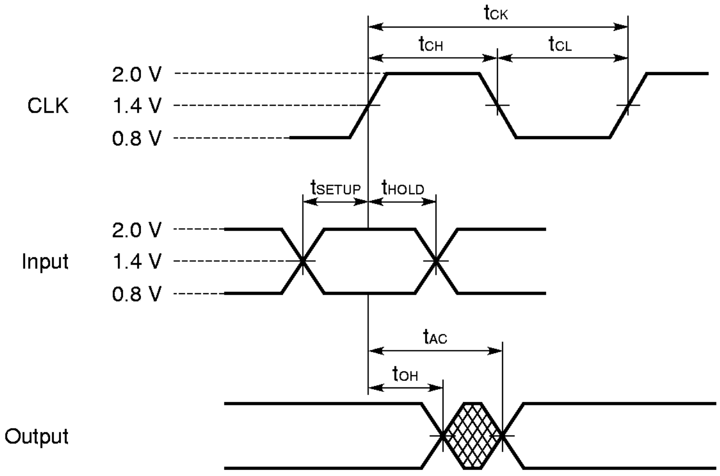
3. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during $t_{CK\,(MIN.)}$.

4. I_{CC5} is measured on condition that addresses are changed only one time during $t_{CK\,(MIN.)}$.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

AC Characteristics Test Conditions

- AC measurements assume $t_T = 1$ ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL}.
- If t_T is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH\,(MIN.)}$ and $V_{IL\,(MAX.)}$.
- An access time is measured at 1.4 V.

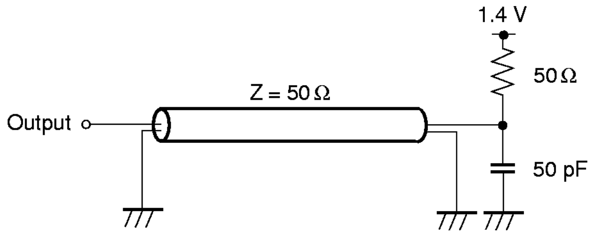


Synchronous Characteristics

[MC-458DA72-A10, 458DA72-A12]

Parameter		Symbol	-A10		-A12		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
Clock cycle time	/CAS latency = 3	t_{CK3}	10	(100 MHz)	12	(83 MHz)	ns	
	/CAS latency = 2	t_{CK2}	15	(67 MHz)	18	(55 MHz)	ns	
Access time from CLK	/CAS latency = 3	t_{AC3}		8.5		9.5	ns	1
	/CAS latency = 2	t_{AC2}		9.5		11.5	ns	1
Input CLK duty cycle		–	40	60	40	60	%	
Data-out hold time		t_{OH}	2.5		2.5		ns	1
Data-out low-impedance time		t_{LZ}	0		0		ns	
Data-out high-impedance time		t_{HZ}	3.5	8	3.5	8	ns	
Data-in setup time		t_{DS}	3.0		3.5		ns	
Data-in hold time		t_{DH}	1.5		2.0		ns	
Address setup time		t_{AS}	3.5		3.5		ns	
Address hold time		t_{AH}	0.5		0.5		ns	
CKE setup time		t_{CKS}	3.5		3.5		ns	
CKE hold time		t_{CKH}	0.5		0.5		ns	
CKE setup time (Power down exit)		t_{CKSP}	3.5		3.5		ns	
Command (/CS0, /RAS, /CAS, /WE, DQM) setup time		t_{CMS}	3.5		3.5		ns	
Command (/CS0, /RAS, /CAS, /WE, DQM) hold time		t_{CMH}	0.5		0.5		ns	

Note 1. Output load

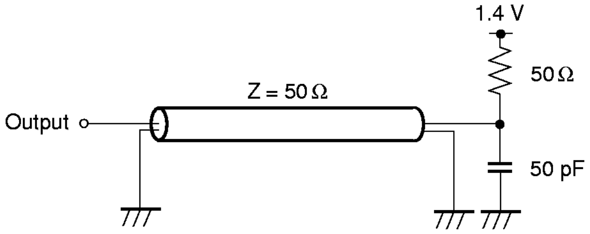


Remark These specifications are applied to the monolithic device.

★ **[MC-458DA72-A10B]**

Parameter		Symbol	-A10B		Unit	Note
			MIN.	MAX.		
Clock cycle time	/CAS latency = 3	t_{CK3}	10	(100 MHz)	ns	
	/CAS latency = 2	t_{CK2}	15	(67 MHz)	ns	
Access time from CLK	/CAS latency = 3	t_{AC3}		7.5	ns	1
	/CAS latency = 2	t_{AC2}		8.5	ns	1
Input CLK duty cycle		–	40	60	%	
Data-out hold time		t_{OH}	2.5		ns	1
Data-out low-impedance time		t_{LZ}	0		ns	
Data-out high-impedance time	/CAS latency = 3	t_{HZ3}	2.5	7.5	ns	
	/CAS latency = 2	t_{HZ2}	2.5	8.5	ns	
Data-in setup time		t_{DS}	3.0		ns	
Data-in hold time		t_{DH}	1.5		ns	
Address setup time		t_{AS}	3.5		ns	
Address hold time		t_{AH}	0.5		ns	
CKE setup time		t_{CKS}	3.5		ns	
CKE hold time		t_{CKH}	0.5		ns	
CKE setup time (Power down exit)		t_{CKSP}	3.5		ns	
Command (/CS0, /RAS, /CAS, /WE, DQM) setup time		t_{CMS}	3.5		ns	
Command (/CS0, /RAS, /CAS, /WE, DQM) hold time		t_{CMH}	0.5		ns	

Note 1. Output load



Remark These specifications are applied to the monolithic device.

Asynchronous Characteristics

[MC-458DA72-A10, 458DA72-A12]

Parameter		Symbol	-A10		-A12		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
REF to REF/ACT command period		t_{RC}	100		120		ns	
ACT to PRE command period		t_{RAS}	60	120,000	72	120,000	ns	
PRE to ACT command period		t_{RP}	30		36		ns	
Delay time ACT to READ/WRITE command		t_{RCD}	30		36		ns	
ACT (one) to ACT (another) command period		t_{RRD}	20		24		ns	
Data-in to PRE command period		t_{DPL}	−1CLK+10		−1CLK+12		ns	
Data-in to ACT (REF) command period (Auto precharge)	/CAS latency = 3	t_{DAL3}	1CLK+30		1CLK+30		ns	
	/CAS latency = 2	t_{DAL2}	30		30		ns	
Mode register set cycle time		t_{RSC}	2		2		CLK	
Transition time		t_T	1	30	1	30	ns	
Refresh time		t_{REF}		64		64	ms	

★ **[MC-458DA72-A10B]**

Parameter		Symbol	-A10B		Unit	Note
			MIN.	MAX.		
REF to REF/ACT command period		t_{RC}	90		ns	
ACT to PRE command period		t_{RAS}	60	120,000	ns	
PRE to ACT command period		t_{RP}	30		ns	
Delay time ACT to READ/WRITE command		t_{RCD}	30		ns	
ACT (one) to ACT (another) command period		t_{RRD}	20		ns	
Data-in to PRE command period		t_{DPL}	−1CLK+10		ns	
Data-in to ACT (REF) command period (Auto precharge)	/CAS latency = 3	t_{DAL3}	30		ns	
	/CAS latency = 2	t_{DAL2}	30		ns	
Mode register set cycle time		t_{RSC}	2		CLK	
Transition time		t_T	1	30	ns	
Refresh time		t_{REF}		64	ms	

Relationship Between Frequency and Latency

[MC-458DA72-A10, 458DA72-A12]

Speed version	-A10		-A12	
Clock cycle time [ns]	10	15	12	18
★ Frequency [MHz]	100	67	83	55
/CAS latency + 1 cycle	3 + 1	2 + 1	3 + 1	2 + 1
[t_{RCD}]	3	2	3	2
/RAS latency (/CAS latency + [t_{RCD}])	7	5	7	5
[t_{RC}]	10	7	9	6
[t_{RAS}]	6	4	6	4
[t_{RRD}]	2	2	2	2
[t_{RP}]	3	2	3	2
[t_{DPL}]	0	0	0	0
[t_{DAL}]	4	2	4	2

Remark All internal signals (A0 - A11, BA0, BA1, /CS0, CKE0, /RAS, /CAS, /WE, DQM) from register are delayed by one cycle. Therefore, DQ is delayed by one cycle.

★ **[MC-458DA72-A10B]**

Speed version	-A10B	
Clock cycle time [ns]	10	15
Frequency [MHz]	100	67
/CAS latency + 1 cycle	3 + 1	2 + 1
[t_{RCD}]	3	2
/RAS latency (/CAS latency + [t_{RCD}])	7	5
[t_{RC}]	9	6
[t_{RAS}]	6	4
[t_{RRD}]	2	2
[t_{RP}]	3	2
[t_{DPL}]	0	0
[t_{DAL}]	3	2

Remark All internal signals (A0 - A11, BA0, BA1, /CS0, CKE0, /RAS, /CAS, /WE, DQM) from register are delayed by one cycle. Therefore, DQ is delayed by one cycle.

Serial PD

[MC-458DA72-A10, 458DA72-A12] (1/2)

Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
0	Defines the number of bytes written into serial PD memory		80H	1	0	0	0	0	0	0	0	128 bytes
1	Total number of bytes of serial PD memory		08H	0	0	0	0	1	0	0	0	256 bytes
2	Fundamental memory type		04H	0	0	0	0	0	1	0	0	SDRAM
3	Number of rows		0CH	0	0	0	0	1	1	0	0	12 rows
4	Number of columns		09H	0	0	0	0	1	0	0	1	9 columns
5	Number of banks		01H	0	0	0	0	0	0	0	1	1 bank
6	Data width		48H	0	1	0	0	1	0	0	0	72 bits
7	Data width (continued)		00H	0	0	0	0	0	0	0	0	0
8	Voltage interface		01H	0	0	0	0	0	0	0	1	LVTTL
9	CL = 3 cycle time	-A10	A0H	1	0	1	0	0	0	0	0	10 ns
		-A12	C0H	1	1	0	0	0	0	0	0	12 ns
10	CL = 3 access time	-A10	85H	1	0	0	0	0	1	0	1	8.5 ns
		-A12	95H	1	0	0	1	0	1	0	1	9.5 ns
11	DIMM configuration type		02H	0	0	0	0	0	0	1	0	ECC
12	Refresh rate / type		80H	1	0	0	0	0	0	0	0	Normal
13	SDRAM width		08H	0	0	0	0	1	0	0	0	×8
14	Error checking SDRAM width		08H	0	0	0	0	1	0	0	0	×8
15	Minimum clock delay		01H	0	0	0	0	0	0	0	1	1 clock
16	Burst length supported		8FH	1	0	0	0	1	1	1	1	1, 2, 4, 8, F
17	Number of banks on each SDRAM		04H	0	0	0	0	0	1	0	0	4 banks
18	/CAS latency supported		06H	0	0	0	0	0	1	1	0	2, 3
19	/CS latency supported		01H	0	0	0	0	0	0	0	1	0
20	/WE latency supported		01H	0	0	0	0	0	0	0	1	0
21	SDRAM module attributes		16H	0	0	0	1	0	1	1	0	Buffered
22	SDRAM device attributes : General		1EH	0	0	0	1	1	1	1	0	
23	CL = 2 cycle time	-A10	F0H	1	1	1	1	0	0	0	0	15 ns
		-A12	30H	0	0	1	1	0	0	0	0	18 ns
24	CL = 2 access time	-A10	95H	1	0	0	1	0	1	0	1	9.5 ns
		-A12	B5H	1	0	1	1	0	1	0	1	11.5 ns
25-26			00H	0	0	0	0	0	0	0	0	
27	$t_{\text{RP (MIN.)}}$	-A10	1EH	0	0	0	1	1	1	1	0	30 ns
		-A12	24H	0	0	1	0	0	1	0	0	36 ns
28	$t_{\text{RRD (MIN.)}}$	-A10	14H	0	0	0	1	0	1	0	0	20 ns
		-A12	18H	0	0	0	1	1	0	0	0	24 ns
29	$t_{\text{RCD (MIN.)}}$	-A10	1EH	0	0	0	1	1	1	1	0	30 ns
		-A12	24H	0	0	1	0	0	1	0	0	36 ns
30	$t_{\text{RAS (MIN.)}}$	-A10	3CH	0	0	1	1	1	1	0	0	60 ns
		-A12	48H	0	1	0	0	1	0	0	0	72 ns
31	Module bank density		10H	0	0	0	1	0	0	0	0	64M bytes

[MC-458DA72-A10, 458DA72-A12] (2/2)

Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
32-61			00H	0	0	0	0	0	0	0	0	
62	SPD revision		01H	0	0	0	0	0	0	0	1	1
63	Checksum for bytes 0 - 62	-A10	94H	1	0	0	1	0	1	0	0	
		-A12	40H	0	1	0	0	0	0	0	0	
64-71	Manufacture's JEDEC ID code											
72	Manufacturing location											
73-90	Manufacture's P/N											
91-92	Revision code											
93-94	Manufacturing date											
95-98	Assembly serial number											
99-125	Mfg specific											
126			00H	0	0	0	0	0	0	0	0	
127			00H	0	0	0	0	0	0	0	0	

★ **[MC-458DA72-A10B]** (1/2)

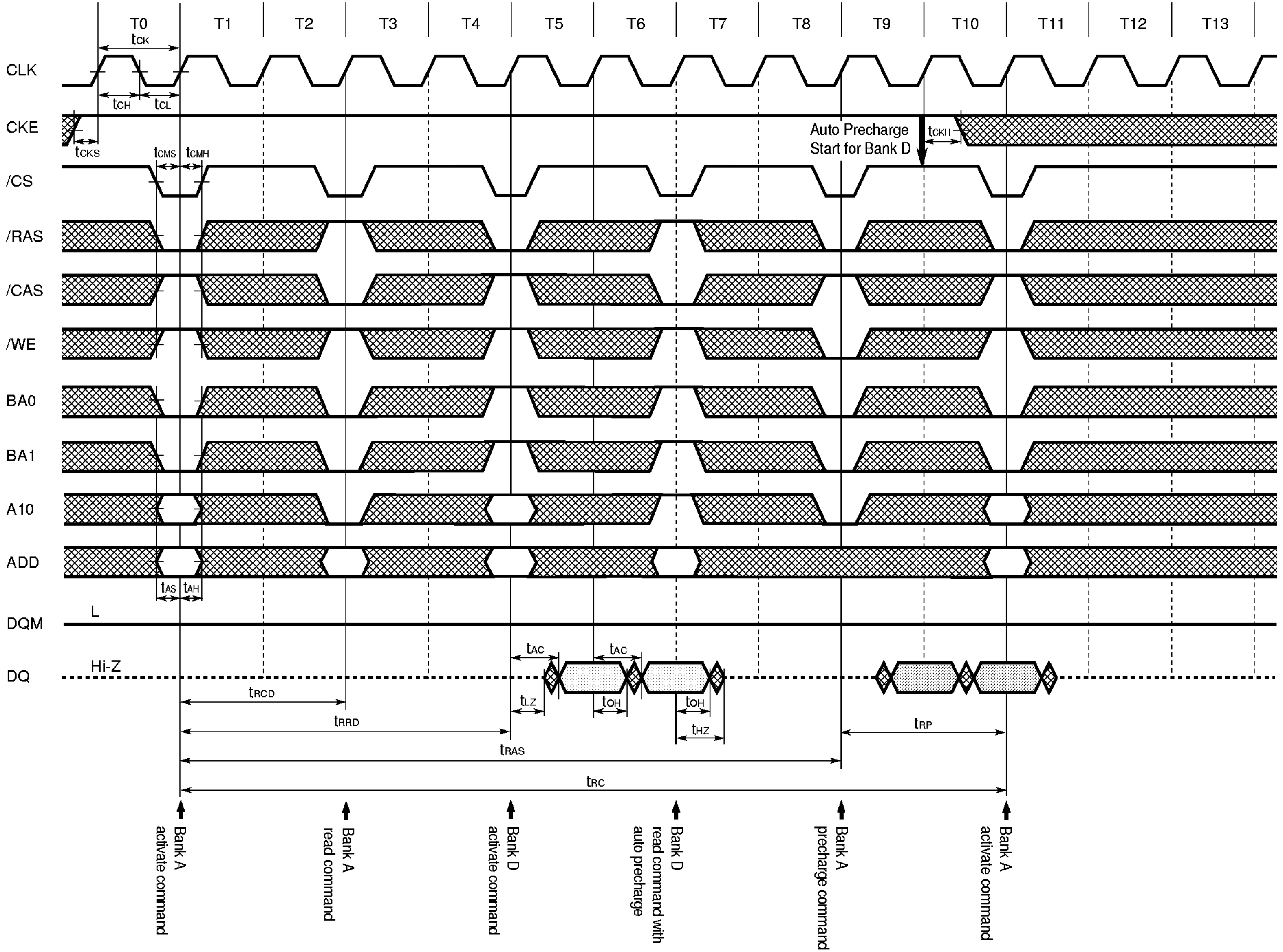
Byte No.	Function Described	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
0	Defines the number of bytes written into serial PD memory	80H	1	0	0	0	0	0	0	0	128 bytes
1	Total number of bytes of serial PD memory	08H	0	0	0	0	1	0	0	0	256 bytes
2	Fundamental memory type	04H	0	0	0	0	0	1	0	0	SDRAM
3	Number of rows	0CH	0	0	0	0	1	1	0	0	12 rows
4	Number of columns	09H	0	0	0	0	1	0	0	1	9 columns
5	Number of banks	01H	0	0	0	0	0	0	0	1	1 bank
6	Data width	48H	0	1	0	0	1	0	0	0	72 bits
7	Data width (continued)	00H	0	0	0	0	0	0	0	0	0
8	Voltage interface	01H	0	0	0	0	0	0	0	1	LVTTL
9	CL = 3 cycle time	A0H	1	0	1	0	0	0	0	0	10 ns
10	CL = 3 access time	75H	0	1	1	1	0	1	0	1	7.5 ns
11	DIMM configuration type	02H	0	0	0	0	0	0	1	0	ECC
12	Refresh rate / type	80H	1	0	0	0	0	0	0	0	Normal
13	SDRAM width	08H	0	0	0	0	1	0	0	0	×8
14	Error checking SDRAM width	08H	0	0	0	0	1	0	0	0	×8
15	Minimum clock delay	01H	0	0	0	0	0	0	0	1	1 clock
16	Burst length supported	8FH	1	0	0	0	1	1	1	1	1, 2, 4, 8, F
17	Number of banks on each SDRAM	04H	0	0	0	0	0	1	0	0	4 banks
18	/CAS latency supported	06H	0	0	0	0	0	1	1	0	2, 3
19	/CS latency supported	01H	0	0	0	0	0	0	0	1	0
20	/WE latency supported	01H	0	0	0	0	0	0	0	1	0
21	SDRAM module attributes	16H	0	0	0	1	0	1	1	0	Registered
22	SDRAM device attributes : General	1EH	0	0	0	1	1	1	1	0	
23	CL = 2 cycle time	F0H	1	1	1	1	0	0	0	0	15 ns
24	CL = 2 access time	85H	1	0	0	0	0	1	0	1	8.5 ns
25-26		00H	0	0	0	0	0	0	0	0	
27	$t_{RP\ (MIN.)}$	1EH	0	0	0	1	1	1	1	0	30 ns
28	$t_{RRD\ (MIN.)}$	14H	0	0	0	1	0	1	0	0	20 ns
29	$t_{RCD\ (MIN.)}$	1EH	0	0	0	1	1	1	1	0	30 ns
30	$t_{RAS\ (MIN.)}$	3CH	0	0	1	1	1	1	0	0	60 ns
31	Module bank density	10H	0	0	0	1	0	0	0	0	64M bytes

★ **[MC-458DA72-A10B]** (2/2)

Byte No.	Function Described	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
32-61		00H	0	0	0	0	0	0	0	0	
62	SPD revision	01H	0	0	0	0	0	0	0	1	1
63	Checksum for bytes 0 - 62	74H	0	1	1	1	0	1	0	0	
64-71	Manufacture’s JEDEC ID code										
72	Manufacturing location										
73-90	Manufacture’s P/N										
91-92	Revision code										
93-94	Manufacturing date										
95-98	Assembly serial number										
99-125	Mfg specific										
126		00H	0	0	0	0	0	0	0	0	
127		00H	0	0	0	0	0	0	0	0	

★

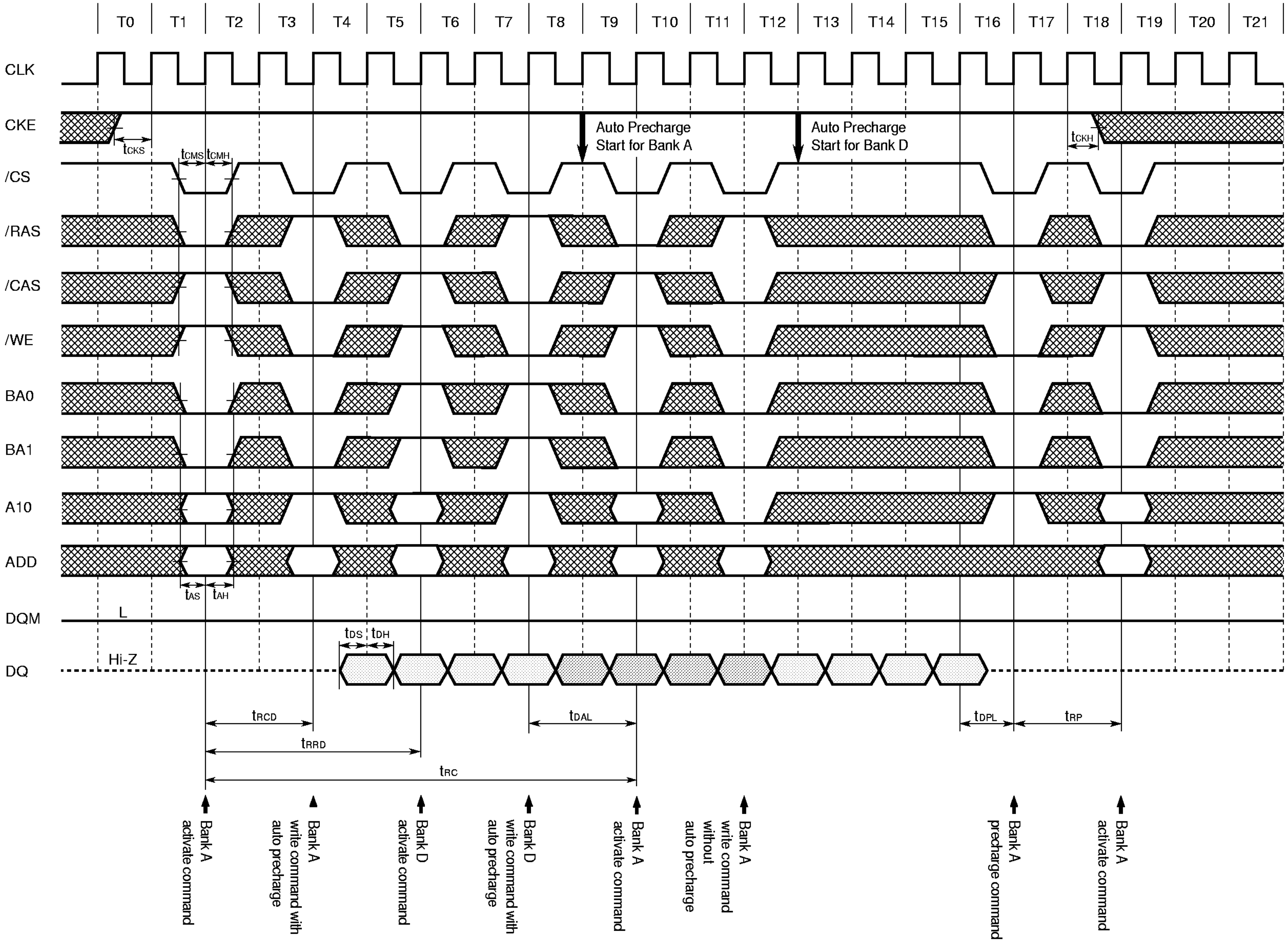
AC Parameters for Read Timing (Burst length = 2, /CAS latency = 2)



Remark All internal signals (A0 - A11, BA0, BA1, /CS0, CKE0, /RAS, /CAS, /WE, DQM) from register are delayed by one cycle. Therefore, DQ is delayed by one cycle.

★

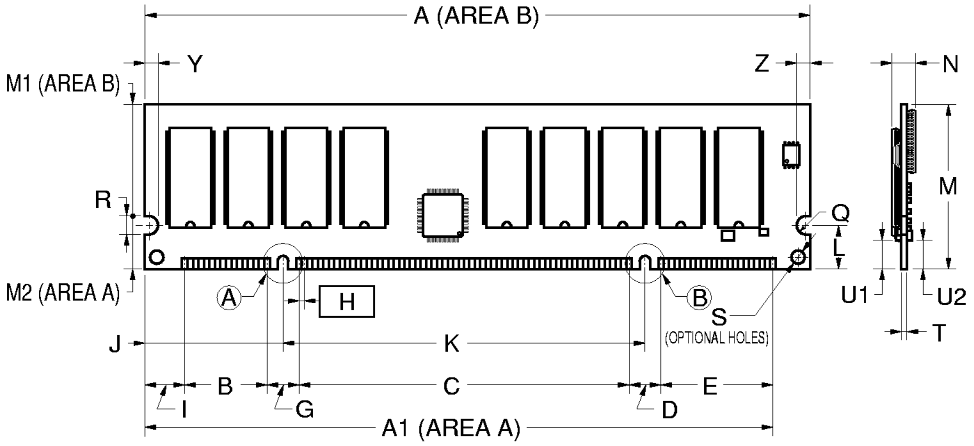
AC Parameters for Write Timing (Burst length = 4, /CAS latency = 2)

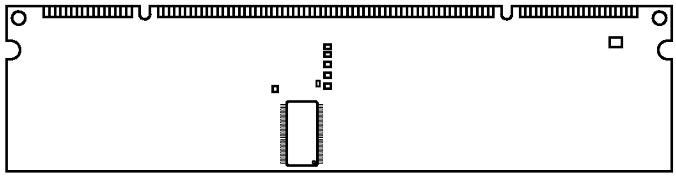


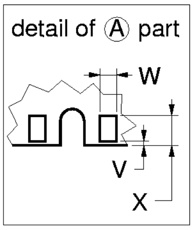
Remark All internal signals (A0 - A11, BA0, BA1, /CS0, CKE0, /RAS, /CAS, /WE, DQM) from register are delayed by one cycle. Therefore, DQ is delayed by one cycle.

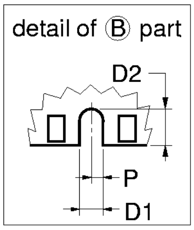
★ **Package Drawing**

200 PIN DUAL IN-LINE MODULE (SOCKET TYPE)









ITEM	MILLIMETERS	INCHES
A	153.7	6.051
A1	153.7±0.13	$6.051^{+0.006}_{-0.005}$
B	19.05	0.750
C	77.47	3.050
D	6.35	0.250
D1	2.0	0.079
D2	3.125	0.123
E	26.67	1.050
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.905	0.351
J	31.135	1.226
K	83.82	3.300
L	10.0	0.394
M	38.1±0.13	1.500±0.006
M1	26.1	1.028
M2	12.0	0.472
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.00±0.10	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.050±0.004
U1	4.0 MIN.	0.157 MIN.
U2	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54±0.10	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

M200S-50A8-1