Integrated DTMF Transceiver with Adaptive Micro Interface

Data Sheet

September 2005

Features

- Central office quality DTMF transmitter/receiver
- Low power consumption
- High speed adaptive micro interface
- Adjustable guard time
- Automatic tone burst mode
- Call progress tone detection to -30 dBm

Applications

- Credit card systems
- Paging systems
- Repeater systems/mobile radio
- Interconnect dialers
- Personal computers

Description

The MT8889C is a monolithic DTMF transceiver with call progress filter. It is fabricated in CMOS technology offering low power consumption and high reliability.

Ordering Information

MT8889CE	20 Pin PDIP	Tubes
MT8889CS	20 Pin SOIC	Tubes
MT8889CN	24 Pin SSOP	Tubes
MT8889CE1	20 Pin PDIP*	Tubes
MT8889CS1	20 Pin SOIC*	Tubes
MT8889CN1	24 Pin SSOP*	Tubes
MT8889CPR	28 Pin PLCC	Tape & Reel
MT8889CSR	20 Pin SOIC	Tape & Reel
MT8889CSR1	20 Pin SOIC*	Tape & Reel

*Pb Free Matte Tin

-40°C to +85°C

The receiver section is based upon the industry standard MT8870 DTMF receiver while the transmitter utilizes a switched capacitor D/A converter for low distortion, high accuracy DTMF signalling. Internal counters provide a burst mode such that tone bursts can be transmitted with precise timing. A call progress filter can be selected allowing a microprocessor to analyze call progress tones.

The MT8889C utilizes an adaptive micro interface, which allows the device to be connected to a number of popular microcontrollers with minimal external logic.

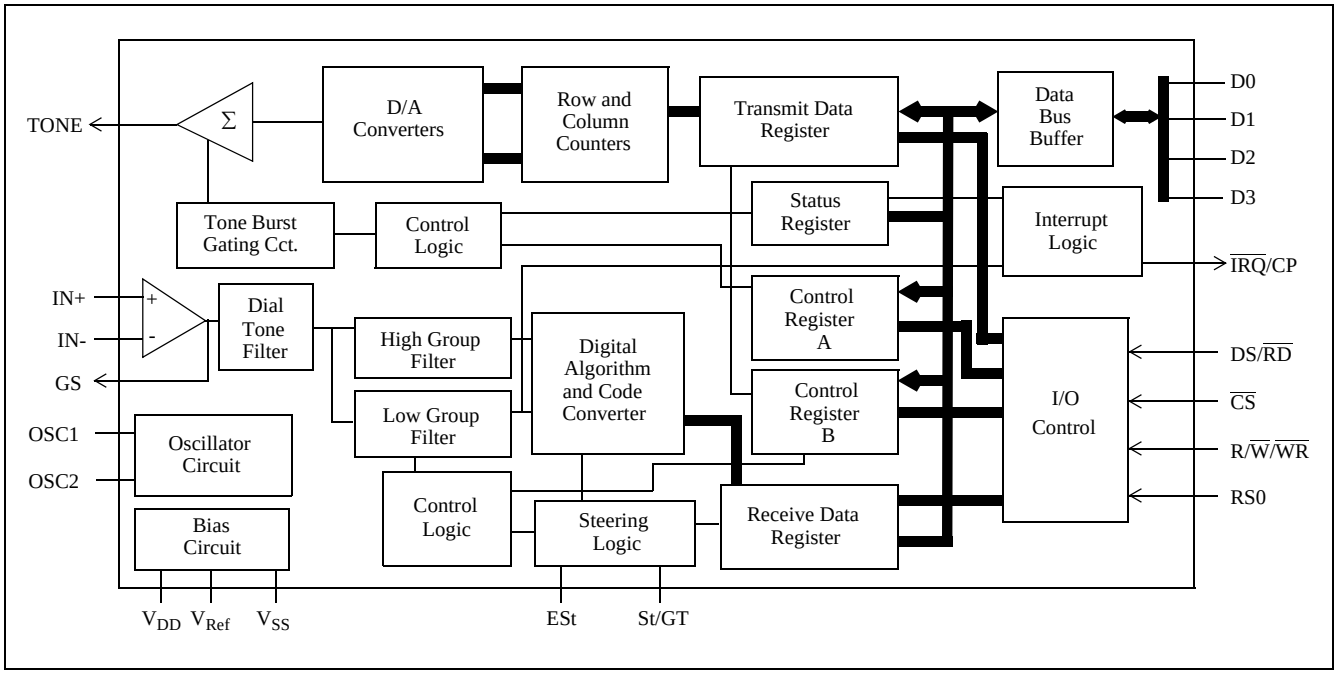


Figure 1 - Functional Block Diagram

Functional Description

The MT8889C Integrated DTMF Transceiver consists of a high performance DTMF receiver with an internal gain setting amplifier and a DTMF generator, which employs a burst counter to synthesize precise tone bursts and pauses. A call progress mode can be selected so that frequencies within the specified passband can be detected. The adaptive micro interface allows microcontrollers, such as the 68HC11, 80C51 and TMS370C50, to access the MT8889C internal registers.

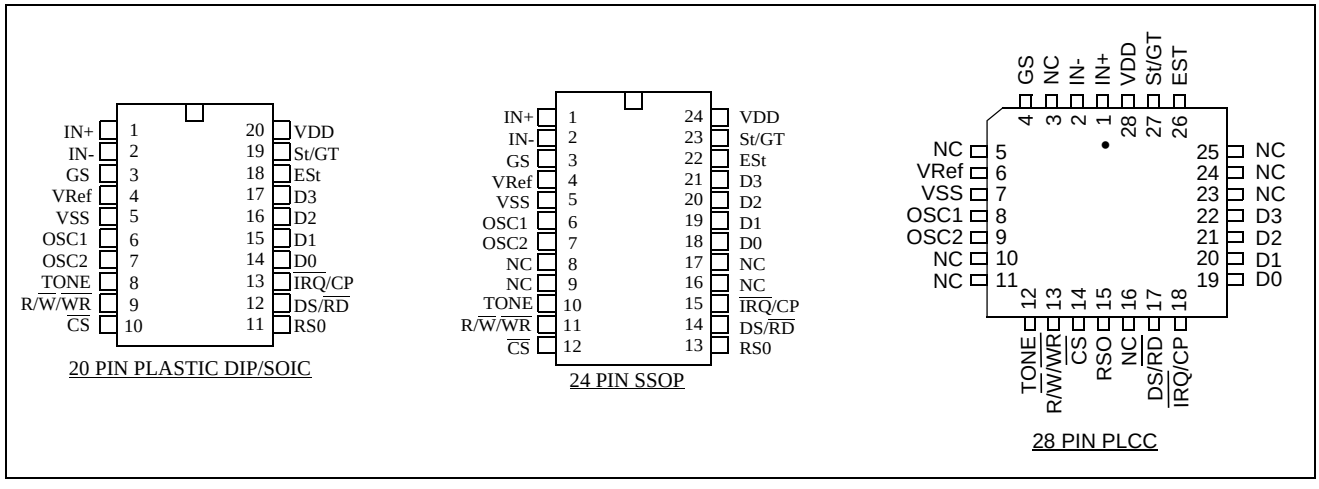


Figure 2 - Pin Connections

Pin Description

Pin #			Name	Description
20	24	28		
1	1	1	IN+	**Non-inverting** op-amp input.
2	2	2	IN-	**Inverting** op-amp input.
3	3	4	GS	**Gain Select**. Gives access to output of front end differential amplifier for connection of feedback resistor.
4	4	6	V_{Ref}	**Reference Voltage** output ($V_{DD}/2$).
5	5	7	V_{SS}	Ground (0V).
6	6	8	OSC1	DTMF clock/oscillator input. Connect a 4.7 MΩ resistor to VSS if crystal oscillator is used.
7	7	9	OSC2	**Oscillator** output. A 3.579545 MHz crystal connected between OSC1 and OSC2 completes the internal oscillator circuit. Leave open circuit when OSC1 is driven externally.
8	10	12	TONE	Output from internal DTMF transmitter.
9	11	13	R/$\overline{W}$ ($\overline{WR}$)	(Motorola) **Read/$\overline{\text{Write}}$** or (Intel) **$\overline{\text{Write}}$** microprocessor input. TTL compatible.
10	12	14	$\overline{CS}$	**Chip Select** input. This signal must be qualified externally by either address strobe (AS), valid memory address (VMA) or address latch enable (ALE) signal, see Figure 14.
11	13	15	RS0	**Register Select** input. Refer to Table 3 for bit interpretation. TTL compatible.
12	14	17	DS ($\overline{RD}$)	(Motorola) **Data Strobe** or (Intel) **$\overline{\text{Read}}$** microprocessor input. Activity on this input is only required when the device is being accessed. TTL compatible.

Pin Description (continued)

Pin #			Name	Description
20	24	28		
13	15	18	$\overline{IRQ}$/CP	**Interrupt Request/Call Progress** (open drain) output. In interrupt mode, this output goes low when a valid DTMF tone burst has been transmitted or received. In call progress mode, this pin will output a rectangular signal representative of the input signal applied at the input op-amp. The input signal must be within the bandwidth limits of the call progress filter, see Figure 8.
14-17	18-21	19-22	D0-D3	Microprocessor data bus. High impedance when $\overline{CS}$ = 1 or DS =0 (Motorola) or $\overline{RD}$ = 1 (Intel). TTL compatible.
18	22	26	ESt	**Early Steering** output. Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
19	23	27	St/GT	**Steering Input/Guard Time** output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
20	24	28	V_{DD}	Positive power supply (5 V typical).
	8, 9, 16,17	3,5,10, 11,16, 23-25	NC	No Connection.

1.0 Input Configuration

The input arrangement of the MT8889C provides a differential-input operational amplifier as well as a bias source (V_{Ref}), which is used to bias the inputs at $V_{DD}/2$. Provision is made for connection of a feedback resistor to the op-amp output (GS) for gain adjustment. In a single-ended configuration, the input pins are connected as shown in Figure 3.

Figure 4 shows the necessary connections for a differential input configuration.

2.0 Receiver Section

Separation of the low and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies (see Table 1). The filters also incorporate notches at 350 Hz and 440 Hz for exceptional dial tone rejection. Each filter output is followed by a single order switched capacitor filter section, which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

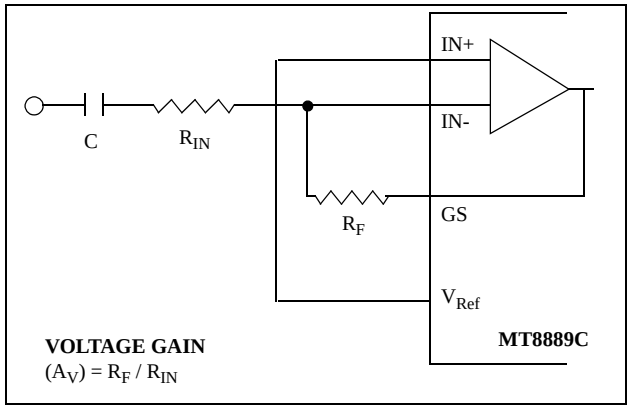


Figure 3 - Single-Ended Input Configuration

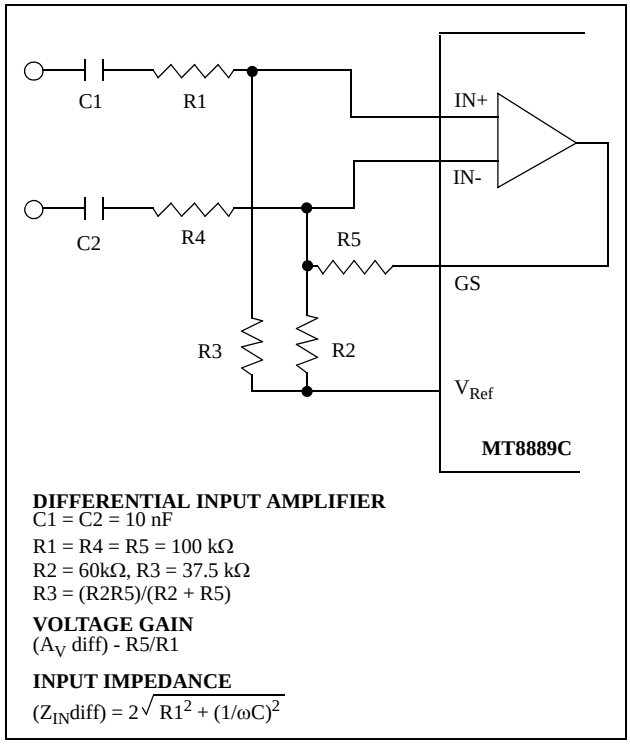


Figure 4 - Differential Input Configuration

F_{LOW}	F_{HIGH}	DIGIT	D_3	D_2	D_1	D_0
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0

Table 1 - Functional Encode/Decode Table

F_{LOW}	F_{HIGH}	DIGIT	D_3	D_2	D_1	D_0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

Table 1 - Functional Encode/Decode Table (continued)

0= LOGIC LOW, 1= LOGIC HIGH

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the “signal condition” in some industry specifications) the “Early Steering” (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state.

3.0 Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes v_c (see Figure 5) to rise as the capacitor discharges. Provided that the signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), v_c reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Table 1) into the Receive Data Register. At this point the GT output is activated and drives v_c to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag goes high, signalling that a received tone pair has been registered. The status of the delayed steering flag can be monitored by checking the appropriate bit in the status register. If Interrupt mode has been selected, the $\overline{IRQ}$/CP pin will pull low when the delayed steering flag is active.

The contents of the output latch are updated on an active delayed steering transition. This data is presented to the four bit bidirectional data bus when the Receive Data Register is read. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

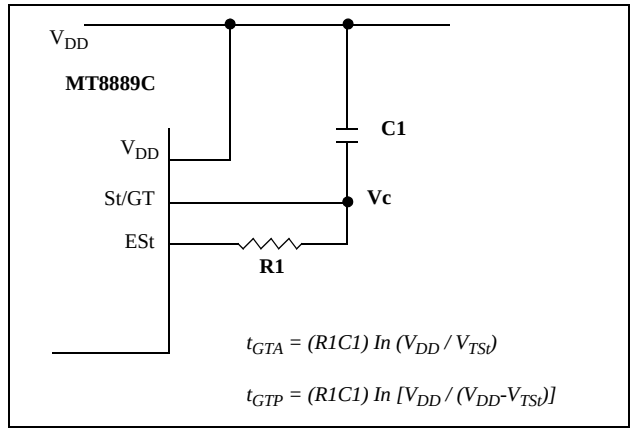


Figure 5 - Basic Steering Circuit

Guard Time Adjustment

The simple steering circuit shown in Figure 5 is adequate for most applications. Component values are chosen according to the following inequalities (see Figure 7):

$$t_{REC} \geq t_{DPmax} + t_{GTPmax} - t_{DAmin}$$

$$t_{\overline{REC}} \leq t_{DPmin} + t_{GTPmin} - t_{DAmax}$$

$$t_{ID} \geq t_{DAmax} + t_{GTAmax} - t_{DPmin}$$

$$t_{DO} \leq t_{DAmin} + t_{GTAmin} - t_{DPmax}$$

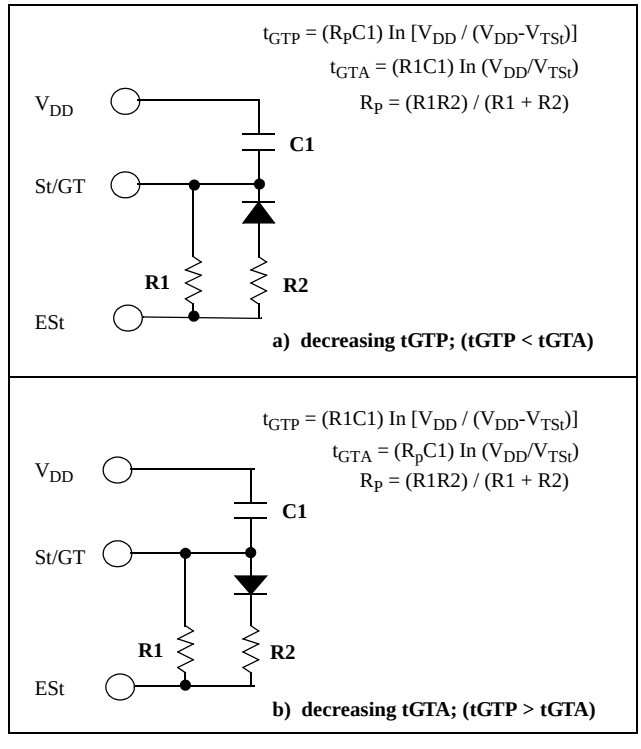


Figure 6 - Guard Time Adjustment

The value of t_{DP} is a device parameter (see AC Electrical Characteristics) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C1 of 0.1 μF is recommended for most applications, leaving R1 to be selected by the designer. Different steering arrangements may be used to select independent tone present (t_{GTP}) and tone absent (t_{GTA}) guard times. This may be necessary to meet system specifications which place both accept and reject limits on tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity.

Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain a valid signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 6. The receiver timing is shown in Figure 7 with a description of the events in Figure 9.

4.0 Call Progress Filter

A call progress mode, using the MT8889C, can be selected allowing the detection of various tones, which identify the progress of a telephone call on the network. The call progress tone input and DTMF input are common, however, call progress tones can only be detected when CP mode has been selected. DTMF signals cannot be detected if CP mode has been selected (see Table 7). Figure 8 indicates the useful detect bandwidth of the call progress filter. Frequencies presented to the input, which are within the 'accept' bandwidth limits of the filter, are hard-limited by a high gain comparator with the IRQ/CP pin serving as the output. The squarewave output obtained from the schmitt trigger can be analyzed by a microprocessor or counter arrangement to determine the nature of the call progress tone being detected. Frequencies which are in the 'reject' area will not be detected and consequently the IRQ/CP pin will remain low.

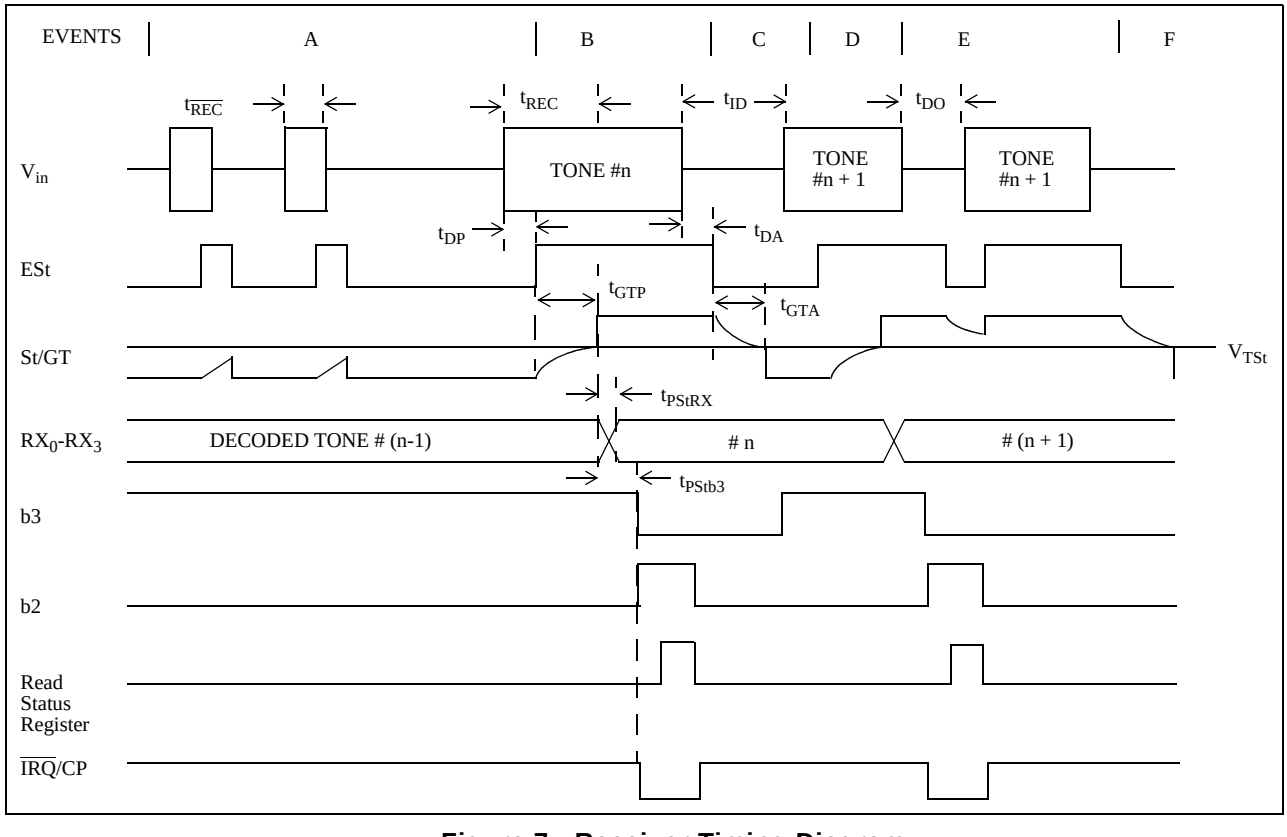


Figure 7 - Receiver Timing Diagram

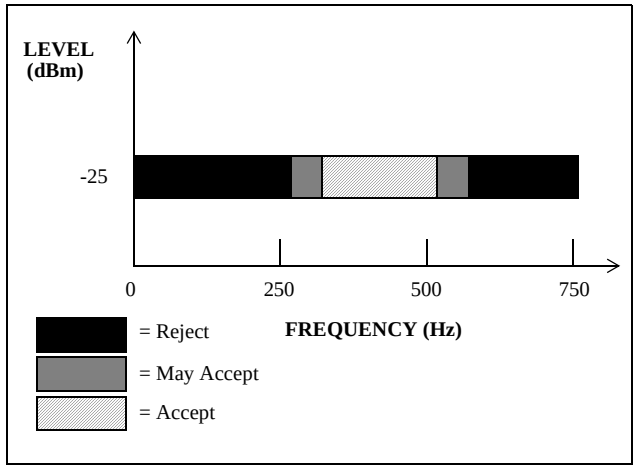


Figure 8 - Call Progress Response

EXPLANATION OF EVENTS

A)	TONE BURSTS DETECTED, TONE DURATION INVALID, RX DATA REGISTER NOT UPDATED.
B)	TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN RX DATA REGISTER.
C)	END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, INFORMATION IN RX DATA REGISTER RETAINED UNTIL NEXT VALID TONE PAIR.
D)	TONE #n+1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN RX DATA REGISTER.
E)	ACCEPTABLE DROPOUT OF TONE #n+1, TONE ABSENT DURATION INVALID, DATA REMAINS UNCHANGED.
F)	END OF TONE #n+1 DETECTED, TONE ABSENT DURATION VALID, INFORMATION IN RX DATA REGISTER RETAINED UNTIL NEXT VALID TONE PAIR.

EXPLANATION OF SYMBOLS

V_{in}	DTMF COMPOSITE INPUT SIGNAL.
ESt	EARLY STEERING OUTPUT. INDICATES DETECTION OF VALID TONE FREQUENCIES.
St/GT	STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.
RX_0-RX_3	4-BIT DECODED DATA IN RECEIVE DATA REGISTER
b3	DELAYED STEERING. INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSTITUTING A VALID SIGNAL. ACTIVE LOW FOR THE DURATION OF A VALID DTMF SIGNAL.
b2	INDICATES THAT VALID DATA IS IN THE RECEIVE DATA REGISTER. THE BIT IS CLEARED AFTER THE STATUS REGISTER IS READ.
$\overline{IRQ}$/CP	INTERRUPT IS ACTIVE INDICATING THAT NEW DATA IS IN THE RX DATA REGISTER. THE INTERRUPT IS CLEARED AFTER THE STATUS REGISTER IS READ.
$t_{\overline{REC}}$	MAXIMUM DTMF SIGNAL DURATION NOT DETECTED AS VALID.
t_{REC}	MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION.
t_{ID}	MINIMUM TIME BETWEEN VALID SEQUENTIAL DTMF SIGNALS.
t_{DO}	MAXIMUM ALLOWABLE DROPOUT DURING VALID DTMF SIGNAL.
t_{DP}	TIME TO DETECT VALID FREQUENCIES PRESENT.
t_{DA}	TIME TO DETECT VALID FREQUENCIES ABSENT.
t_{GTP}	GUARD TIME, TONE PRESENT.
t_{GTA}	GUARD TIME, TONE ABSENT.

Figure 9 - Description of Timing Events

5.0 DTMF Generator

The DTMF transmitter employed in the MT8889C is capable of generating all sixteen standard DTMF tone pairs with low distortion and high accuracy. All frequencies are derived from an external 3.579545 MHz crystal. The sinusoidal waveforms for the individual tones are digitally synthesized using row and column programmable dividers and switched capacitor D/A converters. The row and column tones are mixed and filtered providing a DTMF signal with low total harmonic distortion and high accuracy. To specify a DTMF signal, data conforming to the encoding format shown in Table 1 must be written to the transmit Data Register. Note that this is the same as the receiver output code. The individual tones which are generated (f_{LOW} and f_{HIGH}) are referred to as Low Group and High Group tones. As seen from the table, the low group frequencies are 697, 770, 852 and 941 Hz. The high group frequencies are 1209, 1336, 1477 and 1633 Hz. Typically, the high group to low group amplitude ratio (twist) is 2 dB to compensate for high group attenuation on long loops.

The period of each tone consists of 32 equal time segments. The period of a tone is controlled by varying the length of these time segments. During write operations to the Transmit Data Register the 4 bit data on the bus is latched and converted to 2 of 8 coding for use by the programmable divider circuitry. This code is used to specify a time segment length, which will ultimately determine the frequency of the tone. When the divider reaches the appropriate count, as determined by the input code, a reset pulse is issued and the counter starts again. The number of time segments is fixed at 32, however, by varying the segment length as described above the frequency can also be varied. The divider output clocks another counter, which addresses the sinewave lookup ROM.

The lookup table contains codes which are used by the switched capacitor D/A converter to obtain discrete and highly accurate DC voltage levels. Two identical circuits are employed to produce row and column tones, which are then mixed using a low noise summing amplifier. The oscillator described needs no “start-up” time as in other DTMF generators since the crystal oscillator is running continuously thus providing a high degree of tone burst accuracy. A bandwidth limiting filter is incorporated and serves to attenuate distortion products above 8 kHz. It can be seen from Figure 6 that the distortion products are very low in amplitude.

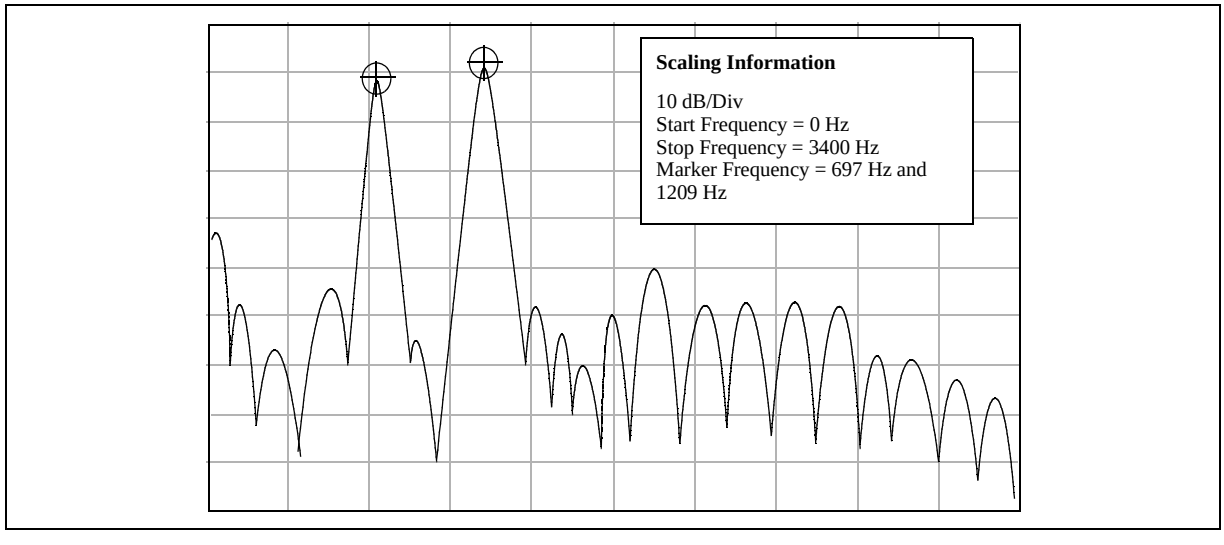


Figure 10 - Spectrum Plot

6.0 Burst Mode

In certain telephony applications it is required that DTMF signals being generated are of a specific duration determined either by the particular application or by any one of the exchange transmitter specifications currently existing. Standard DTMF signal timing can be accomplished by making use of the Burst Mode. The transmitter is capable of issuing symmetric bursts/pauses of predetermined duration. This burst/pause duration is 51 ms±1 ms which is a standard interval for autodialer and central office applications. After the burst/pause has been issued, the appropriate bit is set in the Status Register indicating that the transmitter is ready for more data. The timing described above is available when DTMF mode has been selected. However, when CP mode (Call Progress mode) is selected, the burst/pause duration is doubled to 102 ms ±2 ms. Note that when CP mode and Burst mode have been selected, DTMF tones may be transmitted only and *not* received. In applications where a non-standard burst/pause time is desirable, a software timing loop or external timer can be used to provide the timing pulses when the burst mode is disabled by enabling and disabling the transmitter.

7.0 Single Tone Generation

A single tone mode is available whereby individual tones from the low group or high group can be generated. This mode can be used for DTMF test equipment applications, acknowledgment tone generation and distortion measurements. Refer to Control Register B description for details.

ACTIVE INPUT	OUTPUT FREQUENCY (Hz)		%ERROR
	SPECIFIED	ACTUAL	
L1	697	699.1	+0.30
L2	770	766.2	-0.49
L3	852	847.4	-0.54
L4	941	948.0	+0.74
H1	1209	1215.9	+0.57
H2	1336	1331.7	-0.32
H3	1477	1471.9	-0.35
H4	1633	1645.0	+0.73

Table 2 - Actual Frequencies Versus Standard Requirements

8.0 Distortion Calculations

The MT8889C is capable of producing precise tone bursts with minimal error in frequency (see Table 2). The internal summing amplifier is followed by a first-order lowpass switched capacitor filter to minimize harmonic components and intermodulation products. The total harmonic distortion for a *single tone* can be calculated using Equation 1, which is the ratio of the total power of all the extraneous frequencies to the power of the fundamental frequency expressed as a percentage.

$$THD\ (\%) = 100 \frac{\left(\sqrt{V^2_{2f} + V^2_{3f} + V^2_{4f} + ... V^2_{nf}}\right)}{V_{fundamental}}$$

Figure 11 - Equation 1. THD (%) For a Single Tone

The Fourier components of the tone output correspond to V_{2f}.... V_{nf} as measured on the output waveform. The total harmonic distortion for a *dual tone* can be calculated using Equation 2. V_L and V_H correspond to the low group amplitude and high group amplitude, respectively and V^2_{IMD} is the sum of all the intermodulation components. The internal switched-capacitor filter following the D/A converter keeps distortion products down to a very low level as shown in Figure 10.

$$THD\ (\%) = 100 \frac{\left(\sqrt{V^2_{2L} + V^2_{3L} + ... V^2_{nL} + V^2_{2H} + V^2_{3H} + .. V^2_{nH} + V^2_{IMD}}\right)}{\sqrt{V^2_L + V^2_H}}$$

Figure 12 - Equation 2. THD (%) For a Dual Tone

9.0 DTMF Clock Circuit

The internal clock circuit is completed with the addition of a standard television colour burst crystal. The crystal specification is as follows:

Frequency:	3.579545 MHz
Frequency Tolerance:	±0.1%
Resonance Mode:	Parallel
Load Capacitance:	18 pF
Maximum Series Resistance:	150 ohms
Maximum Drive Level:	2 mW

e.g. CTS Knights MP036S

Toyocom TQC-203-A-9S

A number of MT8889C devices can be connected as shown in Figure 13 such that only one crystal is required. Alternatively, the OSC1 inputs on all devices can be driven from a TTL buffer with the OSC2 outputs left unconnected.

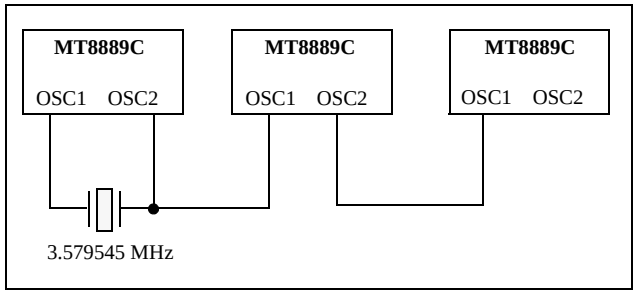


Figure 13 - Common Crystal Connection

10.0 Microprocessor Interface

The MT8889C design incorporates an adaptive interface, which allows it to be connected to various kinds of microprocessors. Key functions of this interface include the following:

- Continuous activity on DS/$\overline{RD}$ is not necessary to update the internal status registers.
- senses whether input timing is that of an Intel or Motorola controller by monitoring the DS ($\overline{RD}$), R/$\overline{W}$ ($\overline{WR}$) and $\overline{CS}$ inputs.
- generates equivalent $\overline{CS}$ signal for internal operation for all processors.
- differentiates between multiplexed and non-multiplexed microprocessor buses. Address and data are latched in accordingly.
- compatible with Motorola and Intel processors.

Figure 19 shows the timing diagram for Motorola microprocessors with separate address and data buses. Members of this microprocessor family include 2 MHz versions of the MC6800, MC6802 and MC6809. For the MC6809, the chip select ($\overline{CS}$) input signal is formed by NANDing the (E+Q) clocks and address decode output. For the MC6800 and MC6802, $\overline{CS}$ is formed by NANDing VMA and address decode output. On the falling edge of $\overline{CS}$, the internal logic senses the state of data strobe (DS). When DS is low, Motorola processor operation is selected.

Figure 20 shows the timing diagram for the Motorola MC68HC11 (1 MHz) microcontroller. The chip select ($\overline{CS}$) input is formed by NANDing address strobe ($\overline{AS}$) and address decode output. Again, the MT8889C examines the state of DS on the falling edge of $\overline{CS}$ to determine if the micro has a Motorola bus (when DS is low). Additionally, the Texas Instruments TMS370CX5X is qualified to have a Motorola interface. Figure 14(a) summarizes connection of these Motorola processors to the MT8889C DTMF transceiver.

Figures 21 and 22 are the timing diagrams for the Intel 8031/8051 (12 MHz) and 8085 (5 MHz) micro-controllers with multiplexed address and data buses. The MT8889C latches in the state of $\overline{RD}$ on the falling edge of $\overline{CS}$. When $\overline{RD}$ is high, Intel processor operation is selected. By NANDing the address latch enable (ALE) output with the high-byte address (P2) decode output, $\overline{CS}$ can be generated. Figure 14(b) summarizes the connection of these Intel processors to the MT8889C transceiver.

NOTE: The adaptive micro interface relies on high-to-low transition on $\overline{CS}$ to recognize the microcontroller interface and this pin must not be tied permanently low.

The adaptive micro interface provides access to five internal registers. The read-only Receive Data Register contains the decoded output of the last valid DTMF digit received. Data entered into the write-only Transmit Data Register will determine which tone pair is to be generated (see Table 1 for coding details). Transceiver control is accomplished with two control registers (see Tables 6 and 7), CRA and CRB, which have the same address. A write operation to CRB is executed by first setting the most significant bit (b3) in CRA. The following write operation to the same address will then be directed to CRB, and subsequent write cycles will be directed back to CRA. The read-only status register indicates the current transceiver state (see Table 8).

A software reset must be included at the beginning of all programs to initialize the control registers upon power-up or power reset (see Figure 17). Refer to Tables 4-7 for bit descriptions of the two control registers.

The multiplexed $\overline{IRQ}$/CP pin can be programmed to generate an interrupt upon validation of DTMF signals or when the transmitter is ready for more data (burst mode only). Alternatively, this pin can be configured to provide a square-wave output of the call progress signal. The $\overline{IRQ}$/CP pin is an open drain output and requires an external pull-up resistor (see Figure 15).

	Motorola	Intel		
RS0	**R/$\overline{W}$**	**$\overline{WR}$**	**$\overline{RD}$**	**FUNCTION**
0	0	0	1	Write to Transmit Data Register
0	1	1	0	Read from Receive Data Register
1	0	0	1	Write to Control Register
1	1	1	0	Read from Status Register

Table 3 - Internal Register Functions

b3	b2	b1	b0
RSEL	IRQ	CP/$\overline{DTMF}$	TOUT

Table 4 - CRA Bit Positions

b3	b2	b1	b0
C/$\overline{R}$	S/$\overline{D}$	TEST	$\overline{BURST}$ $\overline{ENABLE}$

Table 5 - CRB Bit Positions

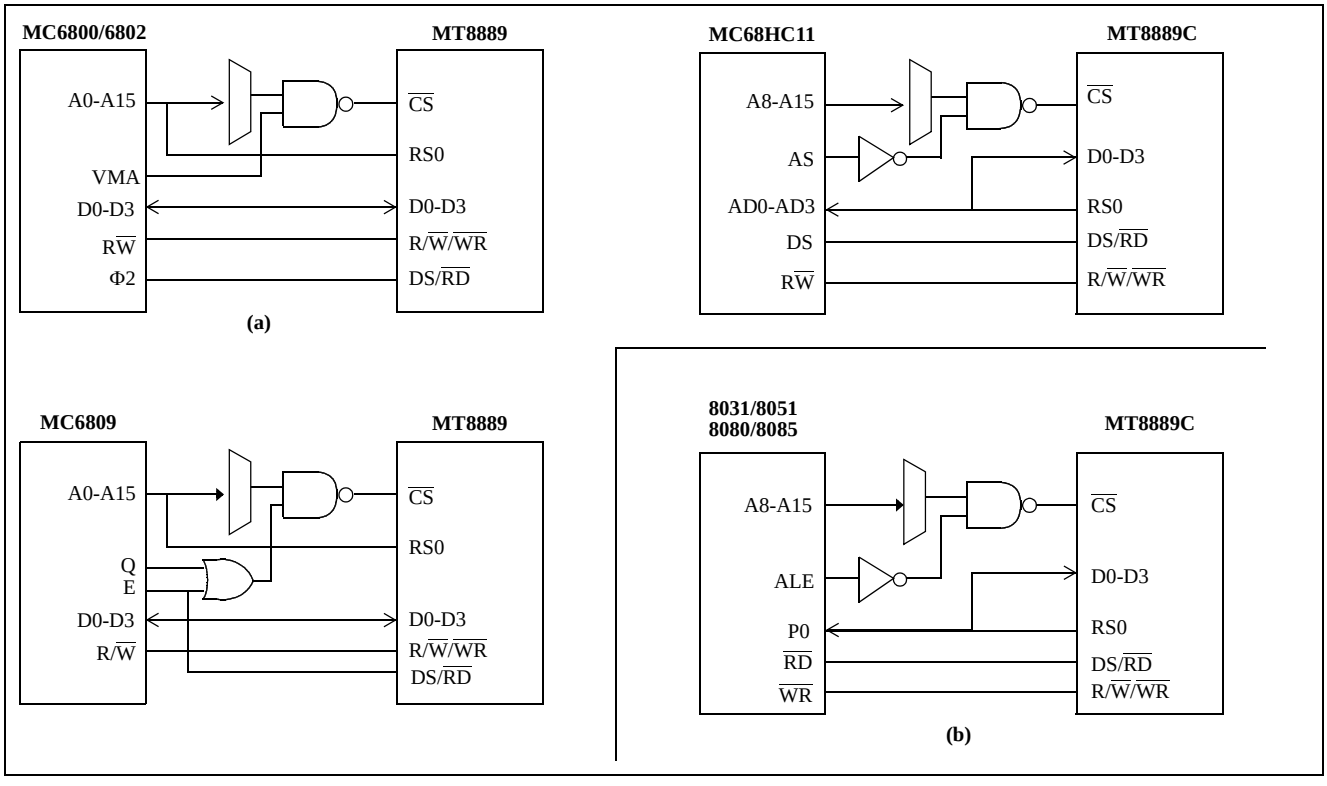


Figure 14 - a) & b) - MT8889 Interface Connections for Various Intel and Motorola Micros

BIT	NAME	DESCRIPTION
b0	TOUT	**Tone Output Control**. A logic high enables the tone output; a logic low turns the tone output off. This bit controls all transmit tone functions.
b1	CP/$\overline{\text{DTMF}}$	**Call Progress or DTMF Mode Select**. A logic high enables the receive call progress mode; a logic low enables DTMF mode. In DTMF mode the device is capable of receiving and transmitting DTMF signals. In CP mode a rectangular wave representation of the received tone signal will be present on the $\overline{\text{IRQ}}$/CP output pin if IRQ has been enabled (control register A, b2=1). In order to be detected, CP signals must be within the bandwidth specified in the AC Electrical Characteristics for Call Progress. Note: DTMF signals cannot be detected when CP mode is selected.
b2	IRQ	**Interrupt Enable**. A logic high enables the interrupt function; a logic low de-activates the interrupt function. When IRQ is enabled and DTMF mode is selected (control register A, b1=0), the $\overline{\text{IRQ}}$/CP output pin will go low when either 1) a valid DTMF signal has been received for a valid guard time duration, or 2) the transmitter is ready for more data (burst mode only).
b3	RSEL	**Register Select**. A logic high selects control register B for the next write cycle to the control register address. After writing to control register B, the following control register write cycle will be directed to control register A.

Table 6 - Control Register A Description

BIT	NAME	DESCRIPTION
b0	$\overline{\text{BURST}}$	**Burst Mode Select**. A logic high de-activates burst mode; a logic low enables burst mode. When activated, the digital code representing a DTMF signal (see Table 1) can be written to the transmit register, which will result in a transmit DTMF tone burst and pause of equal durations (typically 51 msec). Following the pause, the status register will be updated (b1 - Transmit Data Register Empty), and an interrupt will occur if the interrupt mode has been enabled. When CP mode (control register A, b1) is enabled the normal tone burst and pause durations are extended from a typical duration of 51 msec to 102 msec. When $\overline{\text{BURST}}$ is high (de-activated) the transmit tone burst duration is determined by the TOUT bit (control register A, b0).
b1	TEST	**Test Mode Control**. A logic high enables the test mode; a logic low de-activates the test mode. When TEST is enabled and DTMF mode is selected (control register A, b1=0), the signal present on the $\overline{\text{IRQ}}$/CP pin will be analogous to the state of the DELAYED STEERING bit of the status register (see Figure 7, signal b3).
b2	S/$\overline{\text{D}}$	**Single or Dual Tone Generation**. A logic high selects the single tone output; a logic low selects the dual tone (DTMF) output. The single tone generation function requires further selection of either the row or column tones (low or high group) through the C/$\overline{\text{R}}$ bit (control register B, b3).
b3	C/$\overline{\text{R}}$	**Column or Row Tone Select**. A logic high selects a column tone output; a logic low selects a row tone output. This function is used in conjunction with the S/$\overline{\text{D}}$ bit (control register B, b2).

Table 7 - Control Register B Description

BIT	NAME	STATUS FLAG SET	STATUS FLAG CLEARED
b0	IRQ	Interrupt has occurred. Bit one (b1) or bit two (b2) is set.	Interrupt is inactive. Cleared after Status Register is read.
b1	TRANSMIT DATA REGISTER EMPTY (BURST MODE ONLY)	Pause duration has terminated and transmitter is ready for new data.	Cleared after Status Register is read or when in non-burst mode.
b2	RECEIVE DATA REGISTER FULL	Valid data is in the Receive Data Register.	Cleared after Status Register is read.
b3	$\overline{\text{DELAYED}}$ $\overline{\text{STEERING}}$	Set upon the valid detection of the absence of a DTMF signal.	Cleared upon the detection of a valid DTMF signal.

Table 8 - Status Register Description

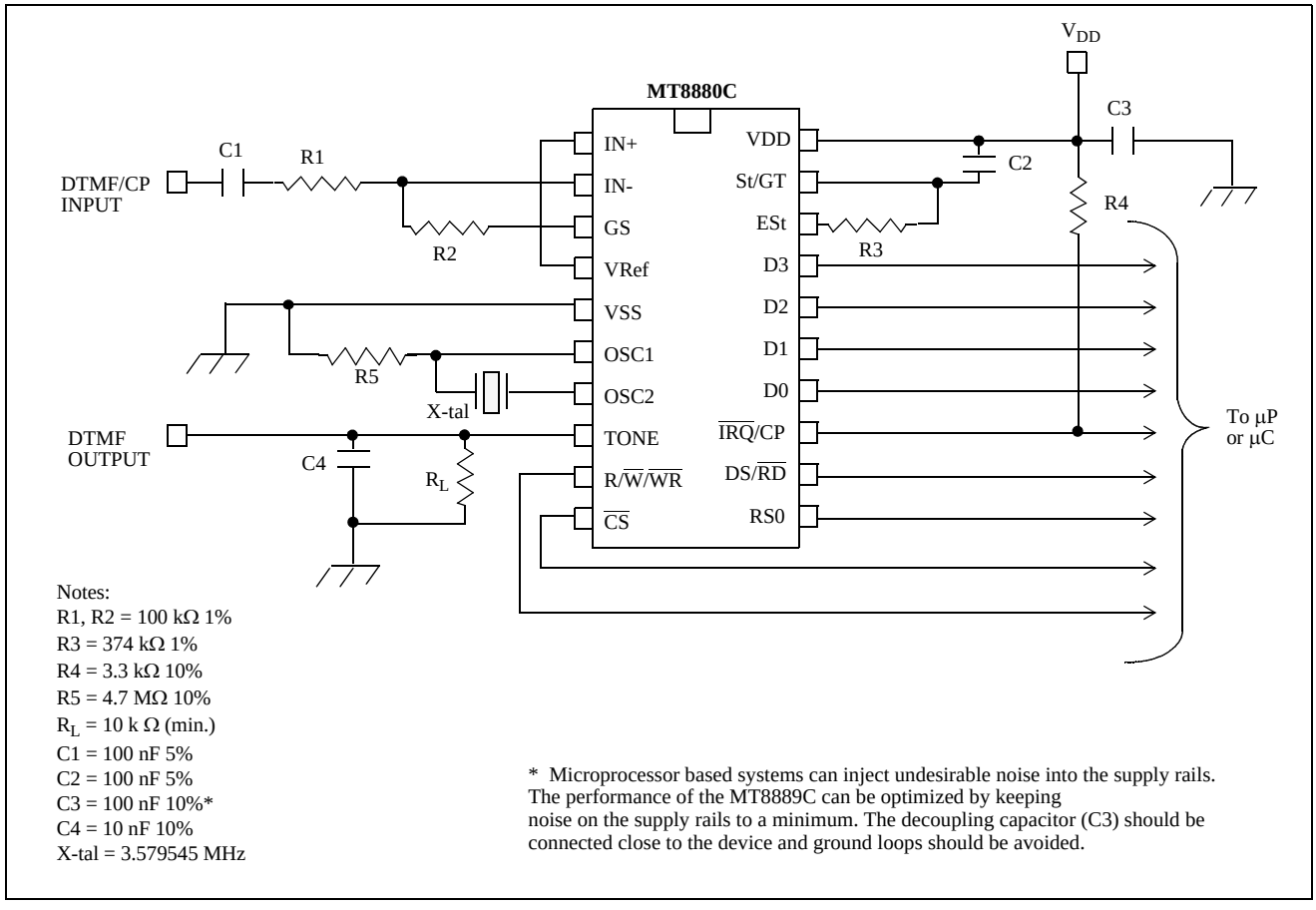


Figure 15 - Application Circuit (Single-Ended Input)

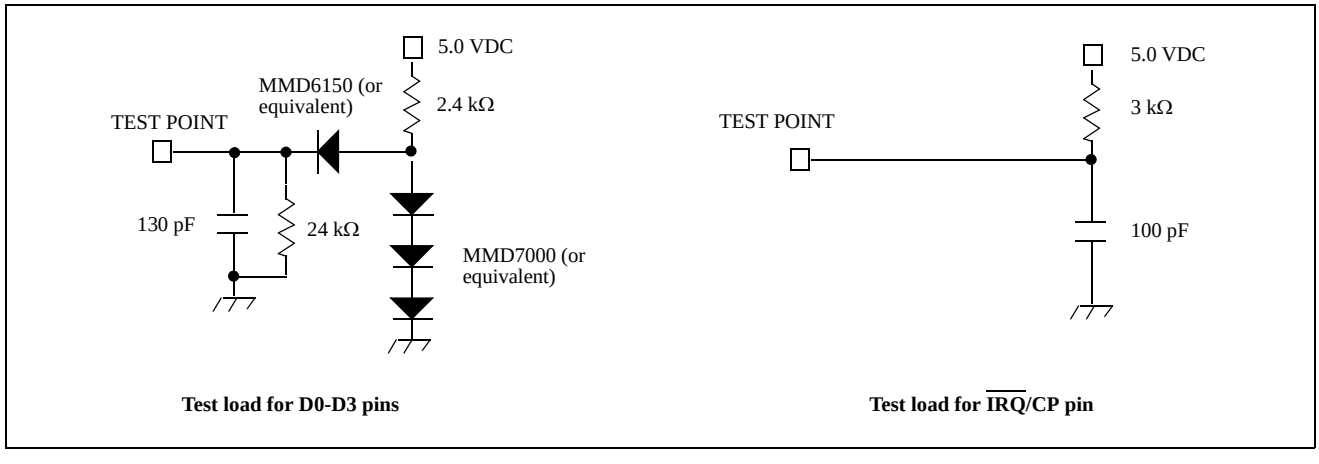


Figure 16 - Test Circuits

INITIALIZATION PROCEDURE

A software reset must be included at the beginning of all programs to initialize the control registers after power up. The initialization procedure should be implemented 100ms after power up.

Description:	**Motorola**		**Intel**		**Data**			
	RS0	**R/$\overline{W}$**	**$\overline{WR}$**	**RD**	**b3**	**b2**	**b1**	**b0**
1) Read Status Register	1	1	1	0	X	X	X	X
2) Write to Control Register	1	0	0	1	0	0	0	0
3) Write to Control Register	1	0	0	1	0	0	0	0
4) Write to Control Register	1	0	0	1	1	0	0	0
5) Write to Control Register	1	0	0	1	0	0	0	0
6) Read Status Register	1	1	1	0	X	X	X	X

TYPICAL CONTROL SEQUENCE FOR BURST MODE APPLICATIONS

Transmit DTMF tones of 50 ms burst/50 ms pause and Receive DTMF Tones.

Sequence:

	RS0	R/$\overline{W}$	$\overline{WR}$	$\overline{RD}$	b3	b2	b1	b0
1) Write to Control Register A (tone out, DTMF, $\overline{IRQ}$, Select Control Register B)	1	0	0	1	1	1	0	1
2) Write to Control Register B (burst mode)	1	0	0	1	0	0	0	0
3) Write to Transmit Data Register (send a digit 7)	0	0	0	1	0	1	1	1
4) Wait for an Interrupt or Poll Status Register								
5) Read the Status Register	1	1	1	0	X	X	X	X
-if bit 1 is set, the Tx is ready for the next tone, in which case...								
Write to Transmit Register (send a digit 5)	0	0	0	1	0	1	0	1
-if bit 2 is set, a DTMF tone has been received, in which case....								
Read the Receive Data Register	0	1	1	0	X	X	X	X
-if both bits are set...								
Read the Receive Data Register	0	1	1	0	X	X	X	X
Write to Transmit Data Register	0	0	0	1	0	1	0	1

NOTE: IN THE TX BURST MODE, STATUS REGISTER BIT 1 WILL NOT BE SET UNTIL 100 ms (±2 ms) AFTER THE DATA IS WRITTEN TO THE TX DATA REGISTER. IN EXTENDED BURST MODE THIS TIME WILL BE DOUBLED TO 200 ms (± 4 ms)

Figure 17 - Application Notes

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Power supply voltage V_{DD}-V_{SS}	V_{DD}		6	V
2	Voltage on any pin	V_I	V_{SS}-0.3	V_{DD}+0.3	V
3	Current at any pin (Except V_{DD} and V_{SS})			10	mA
4	Storage temperature	T_{ST}	-65	+150	°C
5	Package power dissipation	P_D		1000	mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Positive power supply	V_{DD}	4.75	5.00	5.25	V	
2	Operating temperature	T_O	-40		+85	°C	
3	Crystal clock frequency	f_{CLK}	3.575965	3.579545	3.583124	MHz	

‡ Typical figures are at 25 °C and for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - V_{SS}=0 V.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	SUP	Operating supply voltage	V_{DD}	4.75	5.0	5.25	V	
2		Operating supply current	I_{DD}		7.0	11	mA	
3		Power consumption	P_C			57.8	mW	
4	INPUTS	High level input voltage (OSC1)	V_{IHO}	3.5			V	Note 9*
5		Low level input voltage (OSC1)	V_{ILO}			1.5	V	Note 9*
6		Steering threshold voltage	V_{TSt}	2.2	2.3	2.5	V	V_{DD}=5V
7	OUTPUTS	Low level output voltage (OSC2)	V_{OLO}			0.1	V	No load Note 9*
8		High level output voltage (OSC2)	V_{OHO}	4.9			V	No load Note 9*
9		Output leakage current (IRQ)	I_{OZ}		1	10	µA	V_{OH}=2.4 V
10		V_{Ref} output voltage	V_{Ref}	2.4	2.5	2.6	V	No load, V_{DD}=5V
11		V_{Ref} output resistance	R_{OR}		1.3		kΩ	
12	Digital	Low level input voltage	V_{IL}			0.8	V	
13		High level input voltage	V_{IH}	2.0			V	
14		Input leakage current	I_{IZ}			10	µA	V_{IN}=V_{SS} to V_{DD}
15	Data Bus	Source current	I_{OH}	-1.4	-6.6		mA	V_{OH}=2.4V
16		Sink current	I_{OL}	2.0	4.0		mA	V_{OL}=0.4V
17	ESt and St/GT	Source current	I_{OH}	-0.5	-3.0		mA	V_{OH}=4.6V
18		Sink current	I_{OL}	2	4		mA	V_{OL}=0.4V

DC Electrical Characteristics† (continued)- V_{SS}=0 V.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
19	$\overline{IRQ}$/ CP	Sink current	I_{OL}	4	16		mA	V_{OL}=0.4V

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25 °C, V_{DD} =5V and for design aid only: not guaranteed and not subject to production testing.
* See "Notes" following AC Electrical Characteristics Tables.

Electrical Characteristics Gain Setting Amplifier - Voltages are with respect to ground (V_{SS}) unless otherwise stated, V_{SS}= 0V.

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Input leakage current	I_{IN}			100	nA	$V_{SS} \le V_{IN} \le V_{DD}$
2	Input resistance	R_{IN}	10			MΩ	
3	Input offset voltage	V_{OS}			25	mV	
4	Power supply rejection	PSRR	50			dB	1 kHz
5	Common mode rejection	CMRR	40			dB	
6	DC open loop voltage gain	A_{VOL}	40			dB	C_L = 20p
7	Unity gain bandwidth	BW	1.0			MHz	C_L = 20p
8	Output voltage swing	V_O	0.5		V_{DD}-0.5	V	$R_L \ge 100$ kΩ to V_{SS}
9	Allowable capacitive load (GS)	C_L			100	pF	PM>40°
10	Allowable resistive load (GS)	R_L	50			kΩ	V_O = 4Vpp
11	Common mode range	V_{CM}	1.0		V_{DD}-1.0	V	R_L = 50kΩ

Figures are for design aid only: not guaranteed and not subject to production testing.
Characteristics are over recommended operating conditions unless otherwise stated.

MT8889C AC Electrical Characteristics†- Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes*
1	RX	Valid input signal levels (each tone of composite signal)		-29		+1	dBm	1,2,3,5,6
				27.5		869	mV_{RMS}	1,2,3,5,6

† Characteristics are over recommended operating conditions (unless otherwise stated) using the test circuit shown in Figure 15.

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated. f_C=3.579545 MHz

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Notes*
1	RX	Positive twist accept				8	dB	2,3,6,9
2		Negative twist accept				8	dB	2,3,6,9
3		Freq. deviation accept		±1.5%± 2Hz				2,3,5
4		Freq. deviation reject		±3.5%				2,3,5
5		Third tone tolerance			-16		dB	2,3,4,5,9,10
6		Noise tolerance			-12		dB	2,3,4,5,7,9,10
7		Dial tone tolerance			22		dB	2,3,4,5,8,9

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C, V_{DD} = 5V, and for design aid only: not guaranteed and not subject to production testing.
* *See "Notes" following AC Electrical Characteristics Tables.

AC Electrical Characteristics† - Call Progress - Voltages are with respect to ground (V_{SS}), unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Conditions
1	Accept Bandwidth	f_A	310		500	Hz	@ -25 dBm, Note 9
2	Lower freq. (REJECT)	f_{LR}		290		Hz	@ -25 dBm
3	Upper freq. (REJECT)	f_{HR}		540		Hz	@ -25 dBm
4	Call progress tone detect level (total power)		-30			dBm	

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD}=5V, and for design aid only: not guaranteed and not subject to production testing

AC Electrical Characteristics† - DTMF Reception - Typical DTMF tone accept and reject requirements. Actual values are user selectable as per Figures 5, 6 and 7.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Conditions
1	Minimum tone accept duration	t_{REC}		40		ms	
2	Maximum tone reject duration	$t_{\overline{REC}}$		20		ms	
3	Minimum interdigit pause duration	t_{ID}		40		ms	
4	Maximum tone drop-out duration	t_{DO}		20		ms	

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD}=5V, and for design aid only: not guaranteed and not subject to production testing

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}), unless otherwise stated.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Conditions
1	TONE IN	Tone present detect time	t_{DP}	3	11	14	ms	Note 11
2		Tone absent detect time	t_{DA}	0.5	4	8.5	ms	Note 11
3		Delay St to b3	t_{PStb3}		13		µs	See Figure 7
4		Delay St to RX_0-RX_3	t_{PStRX}		8		µs	See Figure 7
5	TONE OUT	Tone burst duration	t_{BST}	50		52	ms	DTMF mode
6		Tone pause duration	t_{PS}	50		52	ms	DTMF mode
7		Tone burst duration (extended)	t_{BSTE}	100		104	ms	Call Progress mode
8		Tone pause duration (extended)	t_{PSE}	100		104	ms	Call Progress mode
9		High group output level	V_{HOUT}	-6.1		-2.1	dBm	R_L=10kΩ
10		Low group output level	V_{LOUT}	-8.1		-4.1	dBm	R_L=10kΩ
11		Pre-emphasis	dB_P	0	2	3	dB	R_L=10kΩ
12		Output distortion (Single Tone)	THD		-35		dB	25 kHz Bandwidth
13								R_L=10kΩ
14		Frequency deviation	f_D		±0.7	±1.5	%	f_C=3.579545 MHz
15		Output load resistance	R_{LT}	10		50	kΩ	

AC Electrical Characteristics† (continued) - Voltages are with respect to ground (V_{SS}), unless otherwise stated.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Conditions
16	XTAL	Crystal/clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
17	XTAL	Clock input rise and fall time	t_{CLRF}			110	ns	Ext. clock
18	XTAL	Clock input duty cycle	DC_{CL}	40	50	60	%	Ext. clock
19	XTAL	Capacitive load (OSC2)	C_{LO}			30	pF	

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics†- MPU Interface - Voltages are with respect to ground (V_{SS}), unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Conditions
1	DS/$\overline{RD}$/$\overline{WR}$ clock frequency	f_{CYC}		4.0		MHz	Figure 18
2	DS/$\overline{RD}$/$\overline{WR}$ cycle period	t_{CYC}		250		ns	Figure 18
3	DS/$\overline{RD}$/$\overline{WR}$ low pulse width	t_{CL}	150			ns	Figure 18
4	DS/$\overline{RD}$/$\overline{WR}$ high pulse width	t_{CH}		100		ns	Figure 18
5	DS/$\overline{RD}$/$\overline{WR}$ rise and fall time	$t_{R,}t_F$			20	ns	Figure 18
6	R/$\overline{W}$ setup time	t_{RWS}	23			ns	Figures 19 & 20
7	R/$\overline{W}$ hold time	t_{RWH}	20			ns	Figures 19 & 20
8	Address setup time (RS0)	t_{AS}	0			ns	Figures 19 - 22
9	Address hold time (RS0)	t_{AH}	40	20		ns	Figures 19 - 22
10	Data hold time (read)	t_{DHR}	22			ns	Figures 19 - 22
11	DS/$\overline{RD}$ to valid data delay (read)	t_{DDR}			100	ns	Figures 19 - 22
12	Data setup time (write)	t_{DSW}	45			ns	Figures 19 - 22
13	Data hold time (write)	t_{DHW}	10			ns	Figures 19 - 22
14	Chip select setup time	t_{CSS}	45	35		ns	Figures 19 - 22
15	Chip select hold time	t_{CSH}	40			ns	Figures 19 - 22
16	Input Capacitance (data bus)	C_{IN}		5		pF	
17	Output Capacitance ($\overline{IRQ}$/CP)	C_{OUT}		5		pF	

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD}=5V, and for design aid only: not guaranteed and not subject to production testing

NOTES:

1. dBm=decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration=40 ms. Tone pause=40 ms.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. The tone pair is deviated by ± 1.5%±2 Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are 350 and 440 Hz (±2%).
9. Guaranteed by design and characterization. Not subject to production testing.
10. Referenced to the lowest amplitude tone in the DTMF signal.
11. For guard time calculation purposes.

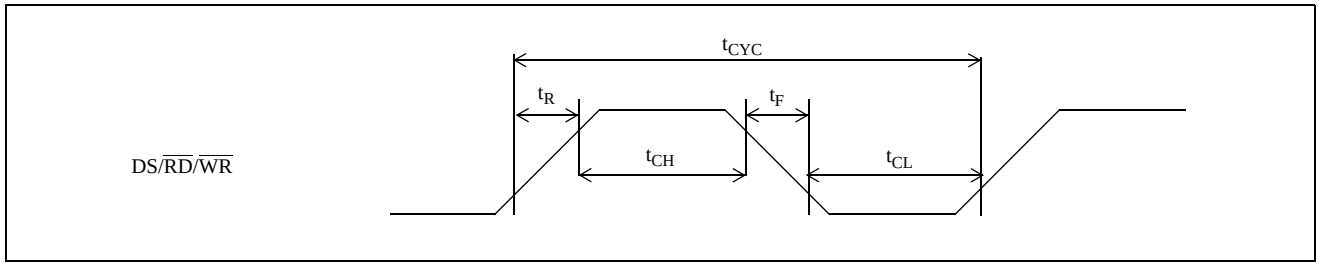


Figure 18 - DS/RD/WR Clock Pulse

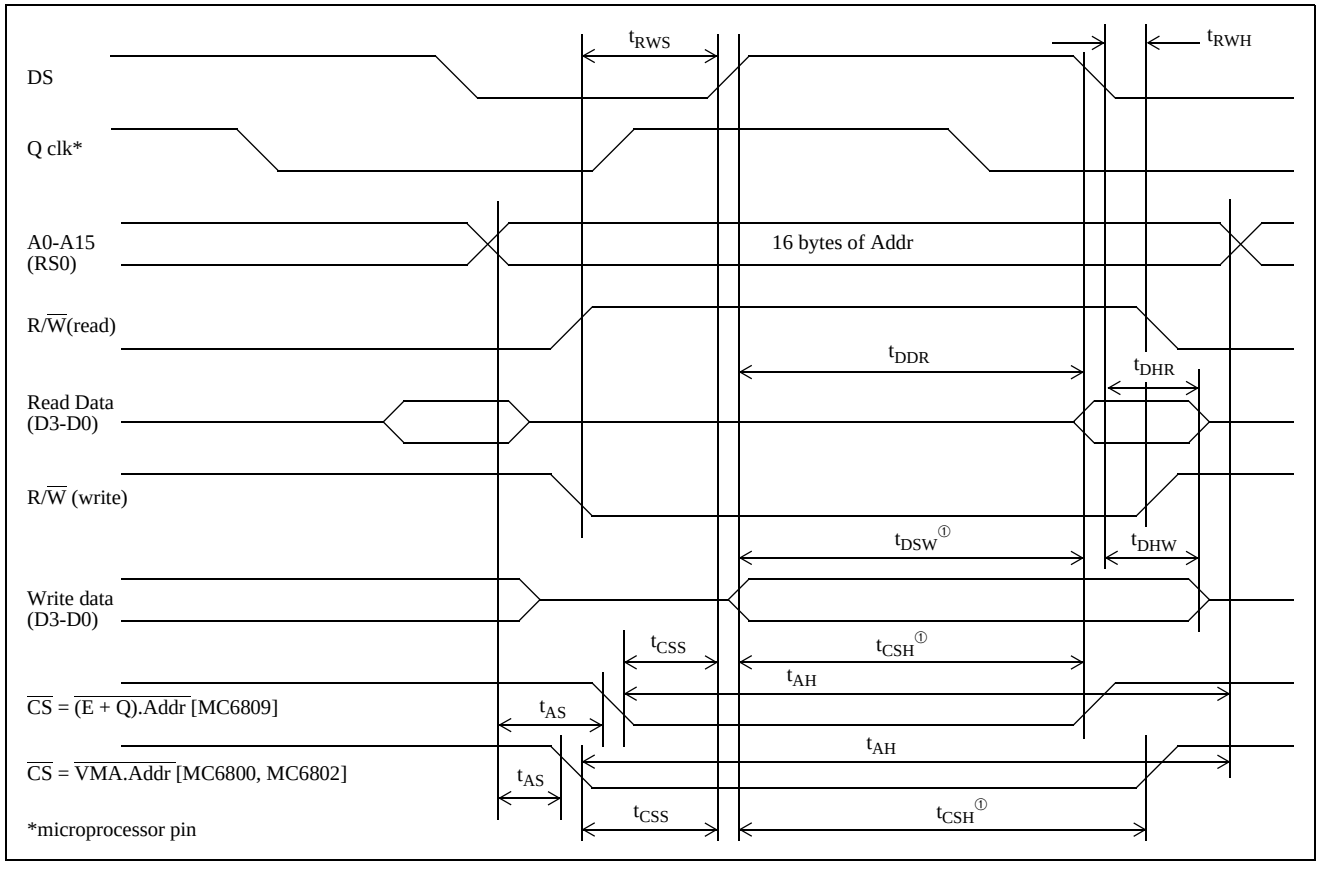


Figure 19 - MC6800/MC6802/MC6809 Timing Diagram

Note: ① t_{DSW} is from data to DS falling edge; t_{CSH} is from DS rising edge to $\overline{CS}$ rising edge

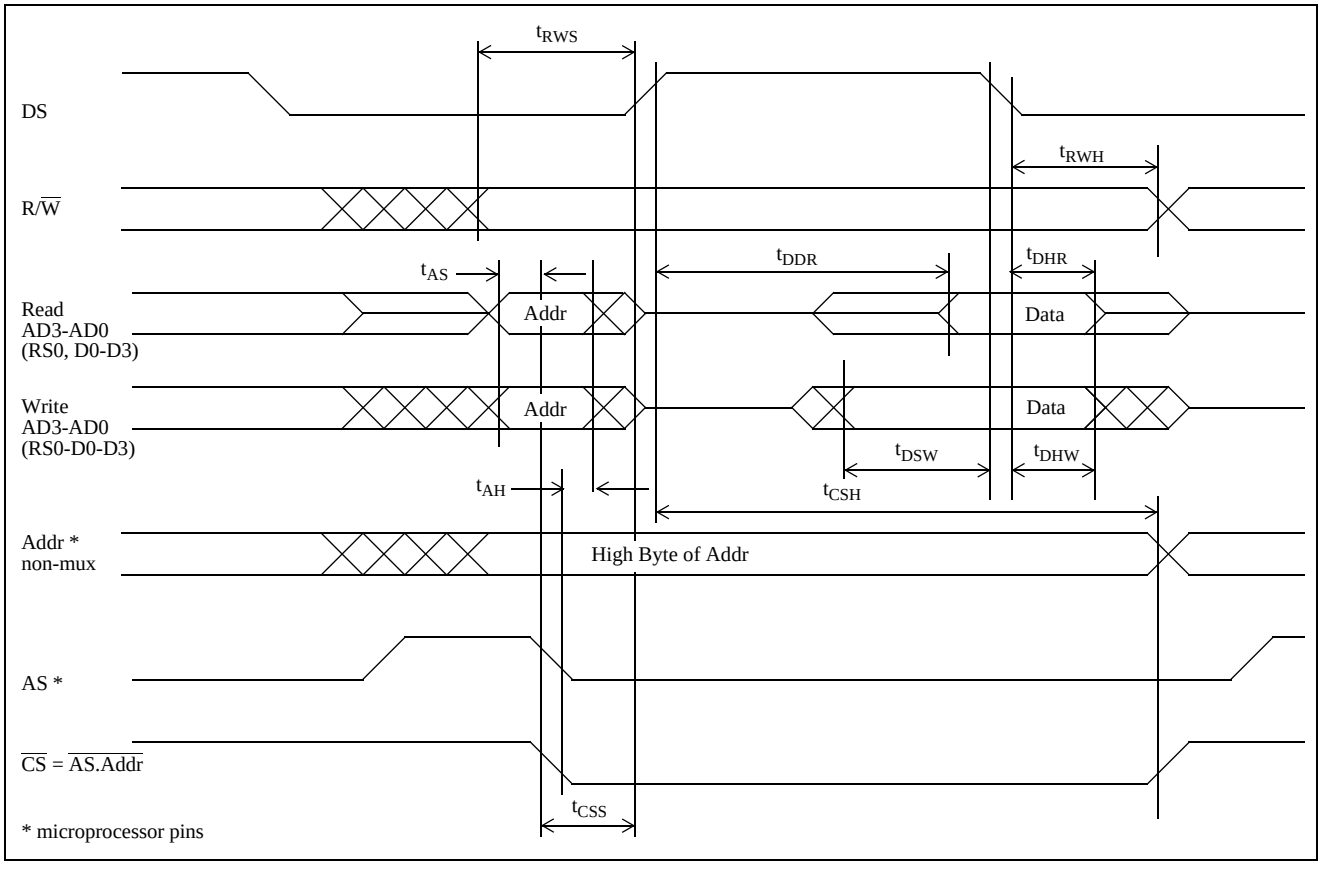


Figure 20 - MC68HC11 Bus Timing (with multiplexed address and data buses)

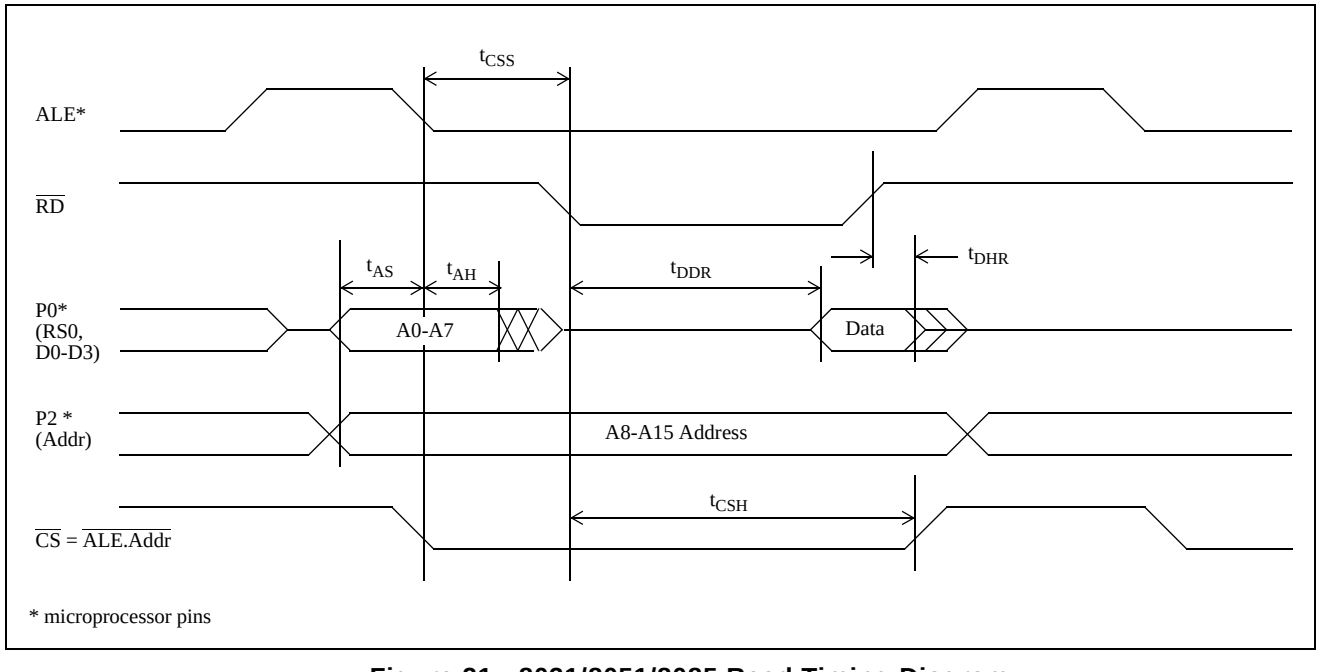


Figure 21 - 8031/8051/8085 Read Timing Diagram

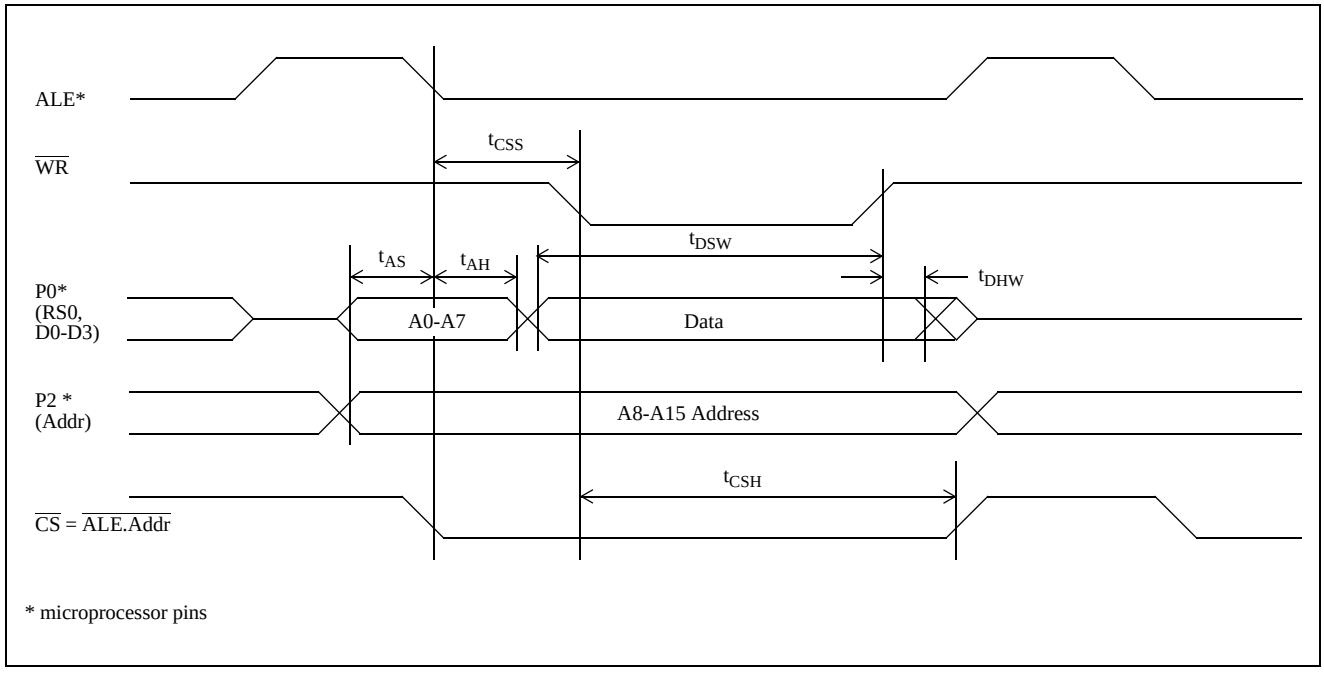
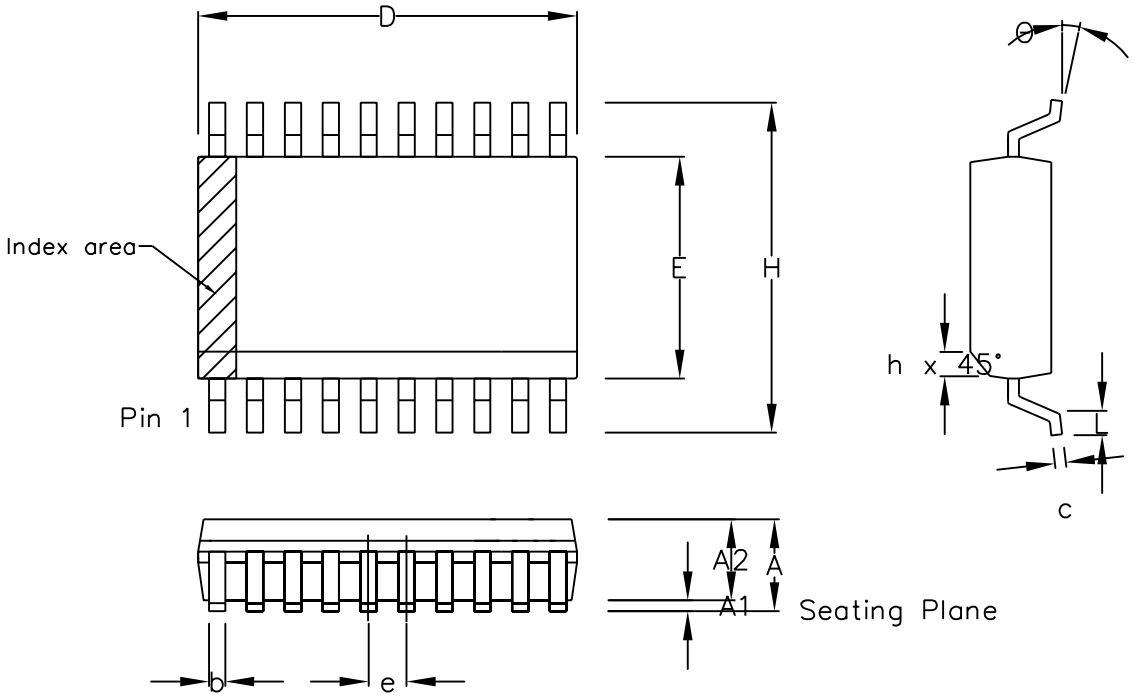


Figure 22 - 8031/8051/8085 Write Timing Diagram



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.35		2.65		0.093		0.104
A1	0.10		0.30		0.004		0.012
A2	2.25		2.35		0.089		0.092
D	12.60		13.00		0.496		0.512
H	10.00		10.65		0.394		0.419
E	7.40		7.60		0.291		0.299
L	0.40		1.27		0.016		0.050
e	1.27 BSC.				0.050 BSC.		
b	0.33		0.51		0.013		0.020
c	0.23		0.32		0.009		0.013
θ	0°		8°		0°		8°
h	0.25		0.75		0.010		0.029
	Pin features						
N	20						
Conforms to JEDEC MS-013AC Iss. C							

Notes:
1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	
ACN	6746	201941	213098	
DATE	7Apr95	27Feb97	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

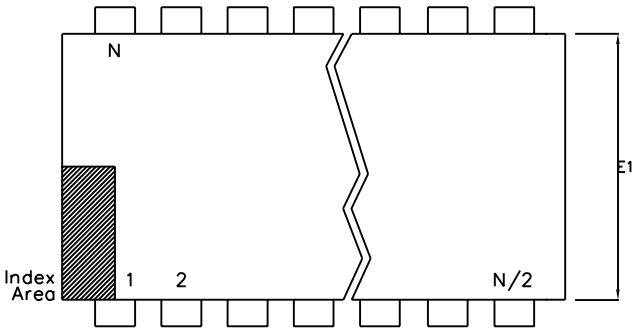
Previous package codes

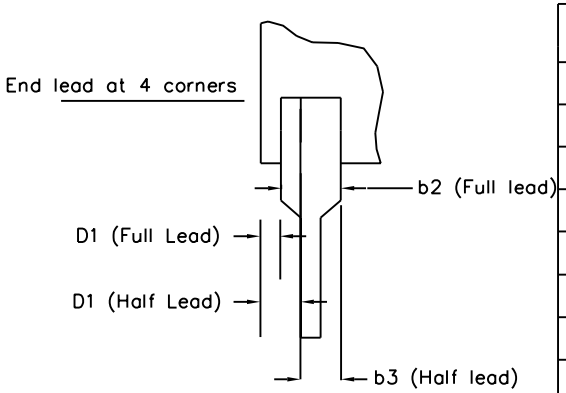
MP / S

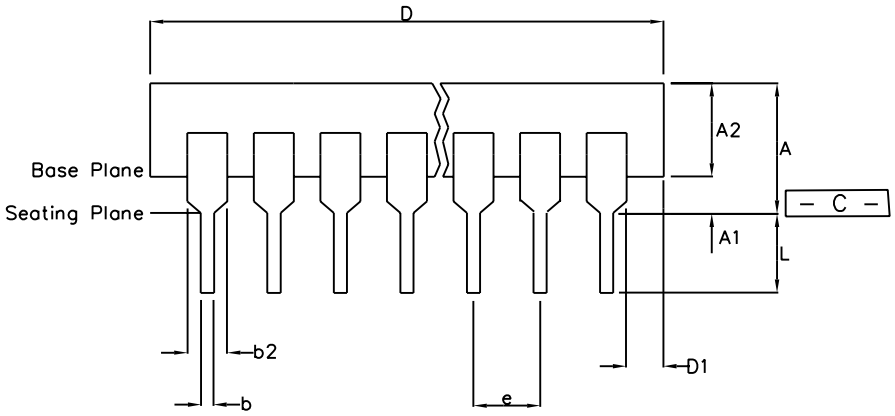
Package Code DC

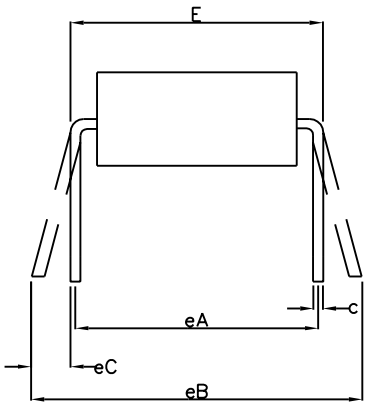
Package Outline for 20 lead SOIC (0.300" Body Width)

GPD00015









	Min mm	Max mm	Min Inches	Max Inches
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	4.95	0.115	0.195
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
b3	n/a	n/a	n/a	n/a
c	0.20	0.36	0.008	0.014
D	24.89	26.92	0.980	1.060
D1	0.13		0.005	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
e	2.54 BSC		0.100 BSC	
eA	7.62 BSC		0.300 BSC	
eB		10.92		0.430
eC	0.00	1.52	0.000	0.060
L	2.92	3.81	0.115	0.150
N	20		20	
Conforms to Jedec MS-001AD Issue D				

Notes:
1. Dimensions D, D1 & E1 do not include mould flash or protrusions.
2. Dimensions E & eA are measured with leads constrained to be perpendicular to datum – C –
3. Dimensions eB & eC are measured with the leads unconstrained
4. Controlling dimensions are Inches. Millimeter conversions are not necessarily exact.
5. N is the maximum of terminal positions.

This drawing supersedes: –
UK drawing # 418/ED/39502/005

ISSUE	1	2		
ACN	202562	213107		
DATE	9Jun97	15Jul02		
APPRD.				

ZARLINK SEMICONDUCTOR

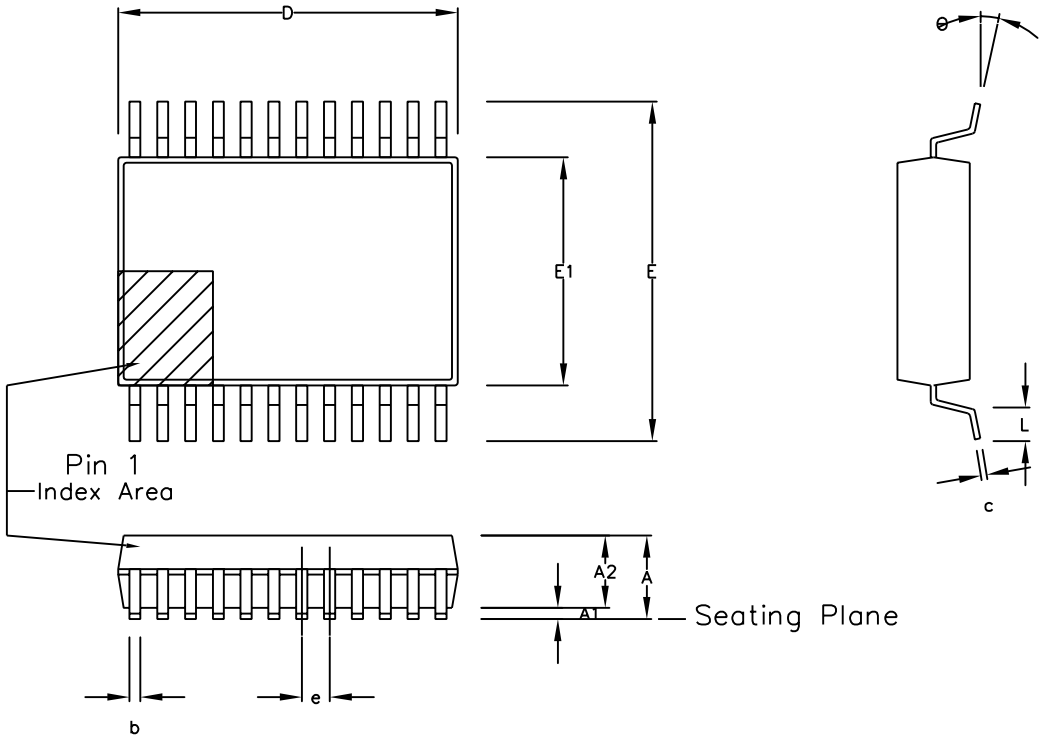
Previous package codes

DP / E

Package Code DA

Package Outline for 20 lead PDIP

GPD00347



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	1.70		2.00		0.067		0.079
A1	0.05		0.20		0.002		0.008
A2	1.65		1.85		0.065		0.073
D	7.90		8.50		0.311		0.335
E	7.40		8.20		0.291		0.323
E1	5.00		5.60		0.197		0.220
L	0.55		0.95		0.022		0.037
e	0.65 BSC.				0.026 BSC.		
b	0.22		0.38		0.009		0.015
c	0.09		0.25		0.004		0.010
θ	0°		8°		0°		8°
	Pin features						
N	24						
Conforms to JEDEC MO-150 AG Iss. B							

This drawing supersedes:-
418/ED/51481/003 (UK)

Notes:
1. A visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimensions D and E1 do not include mould flash or protrusion. Mould flash or protrusion shall not exceed 0.20 mm per side. D and E1 are maximum plastic body size dimensions including mould mismatch.
4. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of b dimension. Dambar intrusion shall not reduce dimension b by more than 0.07 mm.

ISSUE	1	2	3	
ACN	201934	205233	213104	
DATE	27Feb97	25Sep98	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes
NP / N

Package Code DD

Package Outline for
24 lead SSOP
(5.3mm Body Width)

GPD00295

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