HD49420FS

PIP Controller (for NTSC) with On-Chip A/D and D/A Converters

Description

The HD49420FS is a memory controller for NTSC-type picture-in-picture (PIP) systems. The chip integrates one 6-bit A/D converter, two 7-bit D/A converters, a three-channel multiplexer, a $4f_{SC}$ phase-locked loop (PLL), and oscillators for memory read and write operations.

A three-chip PIP system can be configured by combining the HD49420FS with two additional ICs (the HA11579 and HM53461). This chipset requires far fewer external components than its predecessor (the HD49412FS, HA11569, and HM53461).

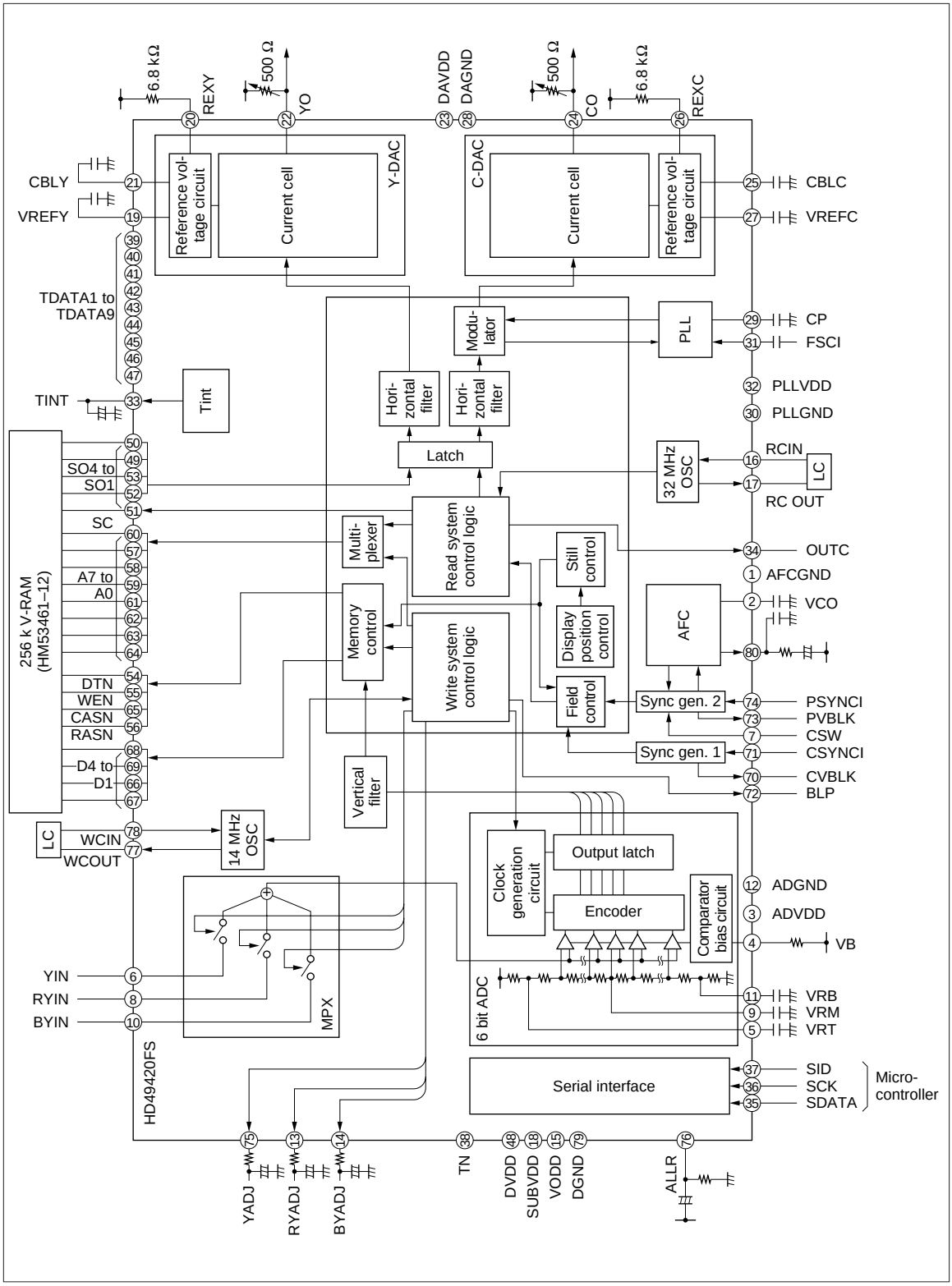
Functions

- PIP memory controller
- Three-channel multiplexer with clamping function
- One 6-bit A/D converter (3.5-Msps)
- Two 7-bit D/A converters (32 Msps and 14 Msps)
- $4f_{SC}$ (14 MHz) PLL
- Memory read oscillator and memory write oscillator
- Bus interface (3 lines)

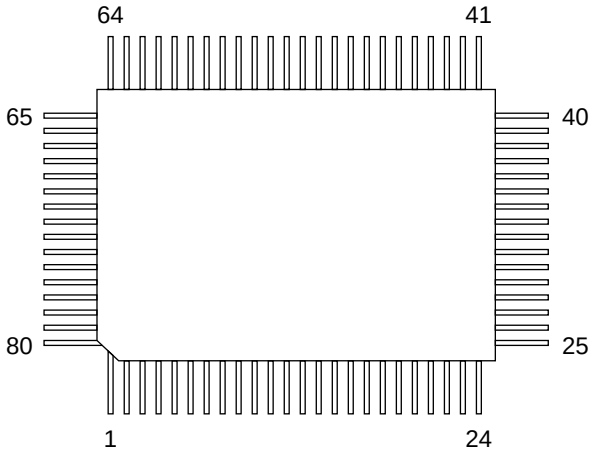
Features

- Requires only two other ICs (HA11579 and HM53461) to form an NTSC-type PIP system
- Sub-picture freeze (still mode)
- On-chip vertical and horizontal filters

Block Diagram



Pin Arrangement



(Top view)

Pin Description

Pin No.	Pin Name	Pin Function	I/O
1	AFCGND	AFC ground	—
2	VCO	VCO	Analog I
3	ADVDD	Analog power supply	—
4	VB	ADC comparator bias voltage	DC I
5	VRT	ADC reference voltage (high)	DC
6	YIN	Y signal input	Analog I
7	CSW	Main signal judgement	Schmitt I
8	RYIN	R-Y signal input	Analog I
9	VRM	ADC reference voltage (center level)	DC
10	BYIN	B-Y signal input	Analog I
11	VRB	ADC reference voltage (low)	DC
12	ADGND	Analog ground	—
13	RYADJ	R-Y signal DC level adjustment output	CMOS O
14	BYADJ	B-Y signal DC level adjustment output	CMOS O
15	VODD	Oscillator power supply	—
16	RCIN	Read-oscillator input	CMOS I
17	RCOUT	Read-oscillator output	CMOS O
18	SUBVDD	Substrate power supply	—
19	VREFY	Y-DAC reference voltage	DC
20	REXY	Y-DAC bias current input	DC I
21	CBLY	Y-DAC bias voltage	DC O
22	YO	Sub-picture Y signal output	Analog O
23	DAVDD	DAC power supply	—
24	CO	Sub-picture C signal output	Analog O
25	CBLC	C-DAC bias voltage	DC O

Pin Description (cont)

Pin No.	Pin Name	Pin Function	I/O
26	REXC	C-DAC bias current input	DC I
27	VREFC	C-DAC reference voltage	DC
28	DAGND	DAC ground	—
29	CP	PLL filter	Analog
30	PLLGND	PLL ground	—
31	FSCI	Main picture burst-lock f_{SC} input	Analog I
32	PLLVDD	PLL power supply	—
33	TINT	Tint control signal output	CMOS O
34	OUTC	Sub-picture output timing signal	CMOS O
35	SDATA	Serial data input	Schmitt I
36	SCK	Serial clock input	Schmitt I
37	SID	Serial ID input	Schmitt I
38	TN	Test mode control	CMOS I
39	TDATA1	Test pin	CMOS I
40	TDATA2	Test pin	CMOS I
41	TDATA3	Test pin/write-oscillator monitor output	CMOS I/O
42	TDATA4	Test pin	CMOS I
43	TDATA5	Test pin	CMOS I
44	TDATA6	Test pin	CMOS I
45	TDATA7	Test pin/read-oscillator monitor output	CMOS I/O
46	TDATA8	Test pin	CMOS I
47	TDATA9	Test pin	CMOS I

Pin Description (cont)

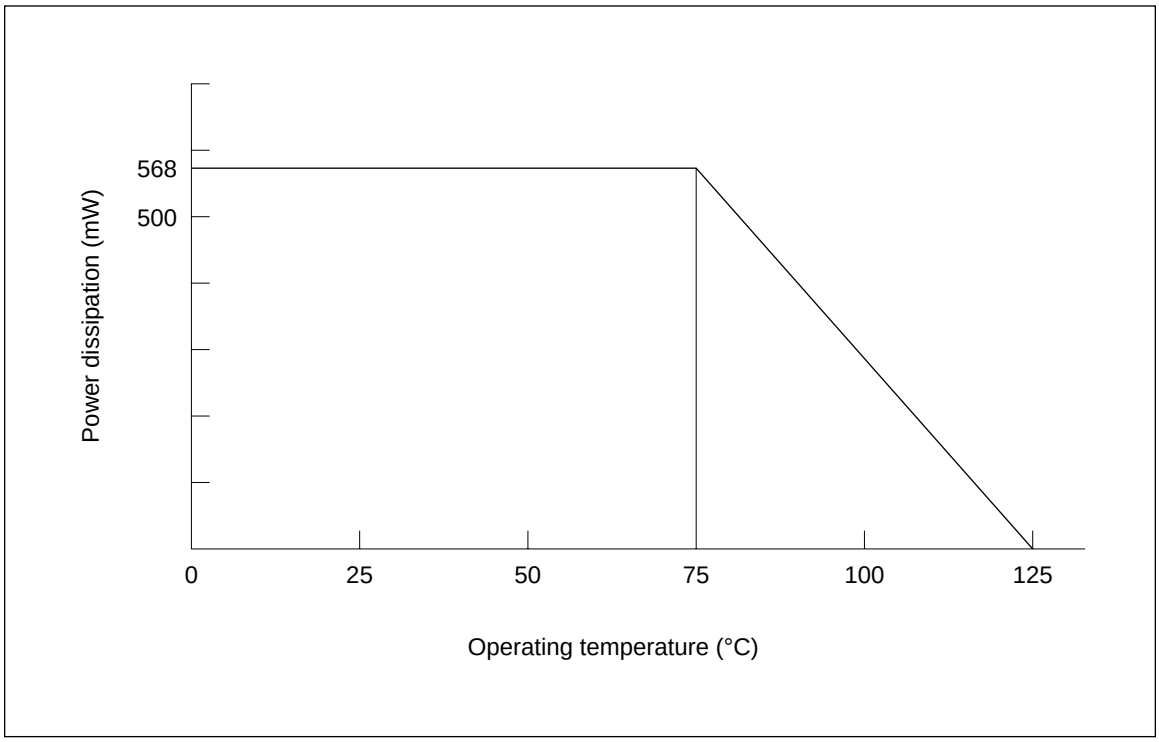
Pin No.	Pin Name	Pin Function	I/O
48	DVDD	Digital power supply	—
49	SO3	V-RAM read data input	TTL I
50	SO4	V-RAM read data input	TTL I
51	SC	V-RAM serial read clock output	CMOS O
52	SO1	V-RAM read data input	TTL I
53	SO2	V-RAM read data input	TTL I
54	DTN	V-RAM data transfer mode/read mode control output	CMOS O
55	WEN	V-RAM write control output	CMOS O
56	RASN	V-RAM row address assigned output	CMOS O
57	A6	V-RAM address output	CMOS O
58	A5	V-RAM address output	CMOS O
59	A4	V-RAM address output	CMOS O
60	A7	V-RAM address output (MSB)	CMOS O
61	A3	V-RAM address output	CMOS O
62	A2	V-RAM address output	CMOS O
63	A1	V-RAM address output	CMOS O
64	A0	V-RAM address output (LSB)	CMOS O
65	CASN	V-RAM column address assigned output	CMOS O
66	D2	V-RAM data output	CMOS O
67	D1	V-RAM data output	CMOS O
68	D4	V-RAM data output	CMOS O

Pin Description (cont)

Pin No.	Pin Name	Pin Function	I/O
69	D3	V-RAM data output	CMOS O
70	CVBLK	Sub-picture vertical mask signal output	3 level O
71	CSYNCI	Sub-picture C-SYNC signal input	Schmitt I
72	BLP	Sub-picture blanking signal output	CMOS O
73	PVBLK	Main-picture vertical mask signal output	3 level O
74	PSYNCI	Main-picture C-SYNC signal input	Schmitt I
75	YADJ	Y signal DC adjustment output	CMOS O
76	ALLR	Power-ON reset signal input	CMOS I
77	WCOUT	Write-oscillator output	CMOS O
78	WCIN	Write-oscillator input	CMOS I
79	DGND	Digital ground	—
80	AFCFIL	AFC filter	Analog I/O

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage	V_{DD}	7	V	
Power dissipation	P_T	568	mW	T_a = 25°C
Analog input voltage	Via	–0.3 to V_{DD} + 0.3	V	
Digital input voltage	Vid	–0.3 to V_{DD} + 0.3	V	
Operating temperature	T_{opr}	–10 to 75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	



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Electrical Characteristics (T_a = 25°C, V_{DD} = 5 V)

Item	Symbol	Specifications Min	Typ	Max	Unit	Test Conditions	Pin Nos.
Operating supply voltage	V_{DD}	4.75	5.00	5.25	V		
Current drawn	I_{DD}	—	60	—	mA		
Input current	I_{ID}	–10	—	10	µA		7, 16, 35, 36, 37, 49, 50, 52, 53, 71, 74, 76, 78
Input VTH1	V_{THC}	1.5	—	3.5	V	C-MOS input	38, 76
Input VTH2	V_{THT}	0.8	—	2.4	V	TTL input	49, 50, 52, 53
Input VTH3(+)		2.5	—	3.5	V	Schmitt input (rising)	7, 71, 74
Input VTH3(–)		1.5	—	2.5	V	Schmitt input (falling)	7, 71, 74
Input VTH4(+)		1.6	—	2.4	V	Schmitt input (rising)	35, 36, 37
Input VTH4(–)		0.8	—	1.6	V	Schmitt input (falling)	35, 36, 37
Output voltage (high)		3.5	—	V_{DD}	V		13, 14, 17, 33, 34, 51, 54, 55, 56 to 70, 72, 75, 77
Output voltage (low)		0	—	1.5	V		13, 14, 17, 33, 34, 51, 54, 55, 56 to 70, 72, 75, 77
ADC resolution		6	6	6	bit		
ADC reference voltage (high)		3.20	3.25	3.30	V		5
ADC reference voltage (low)		1.70	1.75	1.80	V		11
DAC resolution		7	7	7	bit		22, 24
DAC output voltage (full scale)		4.97	—	5.0	V		22, 24
DAC output voltage (zero scale)		3.9	4.0	4.1	V		22, 24
PLL pull-in (+)		3.92	—	—	MHz		31
PLL pull-in (–)		—	—	3.23	MHz		31
Write-oscillator frequency		—	13.9	—	MHz		
Read-oscillator frequency		—	31.3	—	MHz		
Sync. process output voltage levels (high)	V_{OUTH}	4.5	4.9	5.0	V	Load current: –10 µA	70, 73
Sync. process output voltage levels (medium)	V_{OUTM}	2.0	2.5	3.0	V	Load current: ±10 µA	70, 73
Sync. process output voltage levels (low)	V_{OUTL}	0.0	0.1	0.5	V	Load current: +10 µA	70, 73
AFC pull-in range (+)		500	600	—	Hz	f_H (center) = 15.734 kHz	71, 74
AFC pull-in range (–)		—	–600	–500	Hz	f_H (center) = 15.734 kHz	71, 74

Serial Interface
(timing waveforms and functional description)

Description

1. SID, SCK, and SDATA are high in the non-operative state.
2. The start of a new transaction is initiated when SID and SCK are low. Thereafter, 8 address bits are transferred, beginning with the LSB (A0).
3. The address is latched at the rising edge of SCK.
4. Setting SID high initiates the address comparison in the siave circuits.
5. The data is latched at the rising edge of SCK. Eight data bits are transferred, beginning with the LSB (D0).
6. The completion of a bus transaction is signalled by a short SID pulse.
7. The minimum values of TCK and TID are both 6 µs.
8. This transaction is not related to the horizontal and vertical synchronizing signal timing

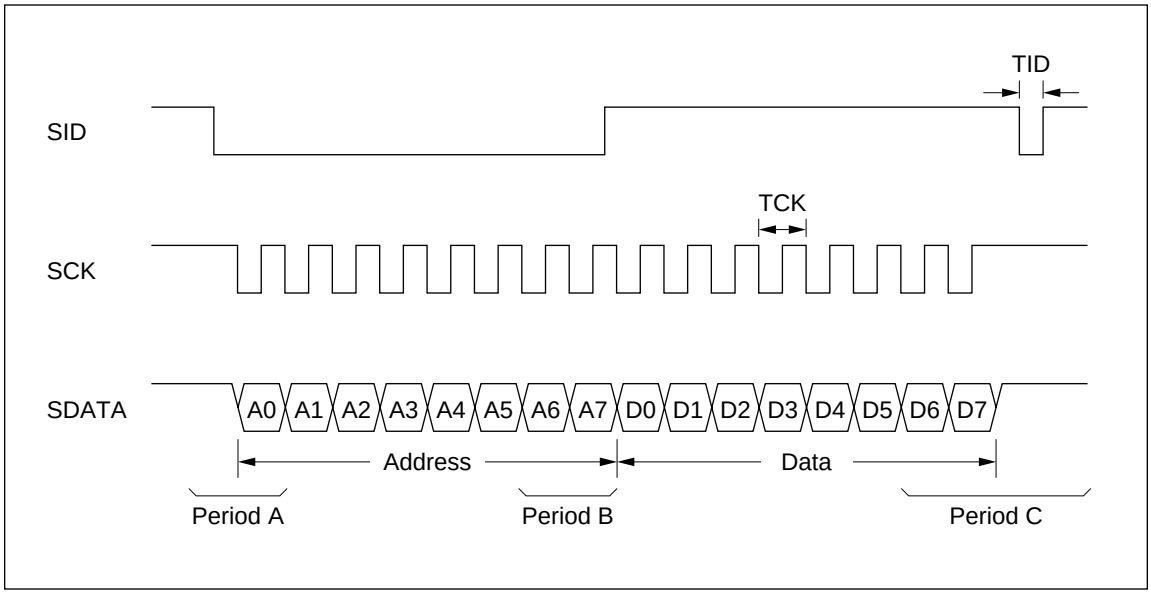

Table 1 Timing Specifications

		Value (µs)	
Period	**Symbol**	**Min**	**Max**
A	T1	1	—
	T2	3	—
	T3	0	—
	T4	1	—
	T5	3	—
B	T6	1	—
	T7	1	—
C	T8	6	—
	T9	1	—

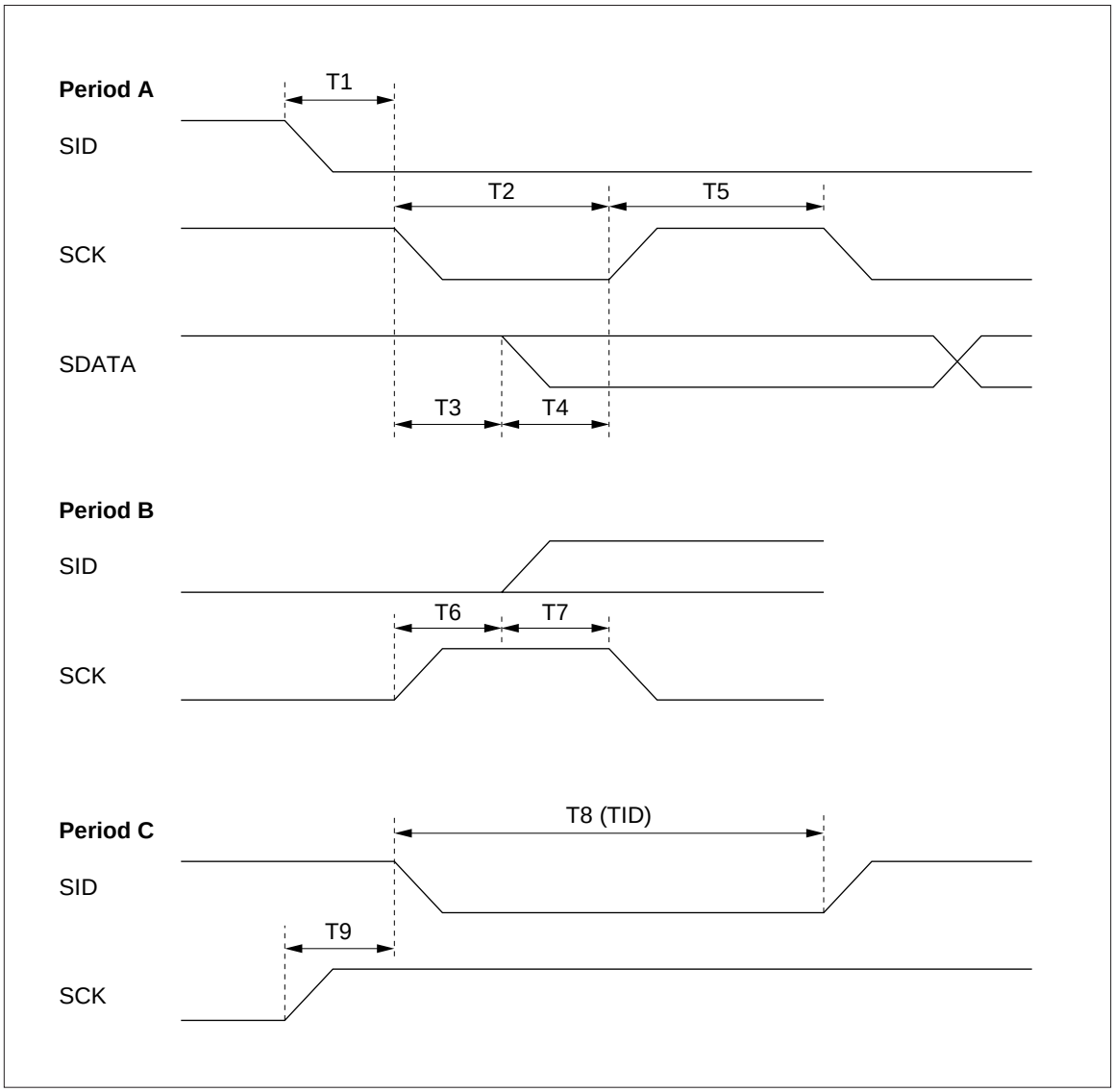

Table 2 Bus Control Data Format

Address (A7 to A0)	Data Name	Function	Data Format (initialized data) D7	D6	D5	D4	D3	D2	D1	D0
$(00)_H$	Set-up mode	Refer to table 3			WAKU	MUTE	STILL	LEFT	UP	PIP
$(02)_H$	Test mode	Refer to table 3						SYNCA	SYNC	TRIM
$(04)_H$	Tint adjustment	Total ±40° 2°/step	← Data (1000000) →							
$(05)_H$	Horizontal position adjustment	380 ns (L) to 380 ns (R) 190 ns/step						← Data (100) →		
$(06)_H$	Y-out amplitude adjustment	Total ±14% 2%/step					← Data (1000) →			
$(07)_H$	C-out amplitude adjustment	Total ±21% 3%/step					← Data (1000) →			
$(08)_H$	Y signal delay adjustment (write)	–1400 ns to 560 ns 280 ns/step					← Data (1000) →			
$(09)_H$	Y signal delay adjustment (read)	–100 ns to 150 ns 50 ns/step						← Data (100) →		
$(0A)_H$	Frame Y level adjustment	Input data = Y level	← Data (1000000) →							
$(0B)_H$	Gray-back-ground Y level adjustment	Input data = Y level	← Data (1000000) →							
$(0C)_H$	Sub-picture output timing	62 ns (L) to 186 (R) 62 ns/step					← Data (1000) →			

Table 3 Mode Format

Name	Function	Setting Format Data: 0	Data: 1	Initial Function (ALLR)
PIP	PIP mode on/off	Off	On	Off
UP	Sub-picture location up/down	Down	Up	Down
LEFT	Sub-picture location left/right	Right	Left	Right
STILL	Sub-picture motion/still mode	Motion	Still	Motion
MUTE	Sub-picture mute on/off	Off	On	Off
WAKU	Sub-picture frame on/off	Off	On	On
TRIM	Read/write-oscillator monitor on/off	Off	On	Off
SYNC	Main sync signal input mode	Refer to table 4		0
SYNCA				0

Note: TRIM is used for testing. This function is not used in normal operation.

Table 4 Sync Mode

Main H/V	SYNCA	SYNC	AFC Application
Internal	0	0	Main H (When CSW is low,AFC do not work.)
External	0	1	———

Adjustment Data

$(04)_H$ Tint Adjustment:

Data									
D7	D6	D5	D4	D3	D2	D1	D0	Pin 33 Voltage (V)*	Note
	1	1	1	1	1	1	1	4.96	
	1	1	1	1	1	1	0	4.92	
	1	1	1	1	1	0	1	4.88	
				⋮				⋮	
	1	0	0	0	0	0	1	2.54	
	1	0	0	0	0	0	0	2.50	Initial data
	0	1	1	1	1	1	1	2.46	
				⋮				⋮	
	0	0	0	0	0	1	0	0.08	
	0	0	0	0	0	0	1	0.04	
	0	0	0	0	0	0	0	0	

Note: * V_{DD} = 5 V

$(05)_H$ Horizontal Position Adjustment:

Data									
D7	D6	D5	D4	D3	D2	D1	D0	Position Shift (ns)	Note
					1	1	1	Right 380	
					1	1	0	Right 380	
					1	0	1	Right 190	
					1	0	0	Center	Initial data
					0	1	1	Left 190	
					0	1	0	Left 380	
					0	0	1	Left 380	
					0	0	0	Left 380	

$(06)_H$ Y-OUT Amplitude Adjustment:

Data									
D7	D6	D5	D4	D3	D2	D1	D0	Amplitude (Vp-p)	Note
				1	1	1	1	1.14	
	1	1	1	0	1.12				
				1	1	0	1	1.10	
				1	1	0	0	1.08	
				1	0	1	1	1.06	
				1	0	1	0	1.04	
				1	0	0	1	1.02	
				1	0	0	0	1.00	Initial data
				0	1	1	1	0.98	
				0	1	1	0	0.96	
				0	1	0	1	0.94	
				0	1	0	0	0.92	
				0	0	1	1	0.90	
				0	0	1	0	0.88	
				0	0	0	1	0.86	
				0	0	0	0	0.84	

$(07)_H$ C-OUT Amplitude Adjustment:

Data									
D7	D6	D5	D4	D3	D2	D1	D0	Amplitude (Vp-p)	Note
				1	1	1	1	1.21	
				1	1	1	0	1.18	
				1	1	0	1	1.15	
				1	1	0	0	1.12	
				1	0	1	1	1.09	
				1	0	1	0	1.06	
				1	0	0	1	1.03	
				1	0	0	0	1.00	Initial data
				0	1	1	1	0.97	
				0	1	1	0	0.94	
				0	1	0	1	0.91	
				0	1	0	0	0.88	
				0	0	1	1	0.85	
				0	0	1	0	0.82	
				0	0	0	1	0.79	
				0	0	0	0	0.76	

$(08)_H$ Y Signal Delay Adjustment (write):

Data									
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Delay (ns)**	**Note**
				1	1	1	1	560	
				1	1	1	0	560	
				1	1	0	1	560	
				1	1	0	0	560	
				1	0	1	1	560	
				1	0	1	0	560	
				1	0	0	1	280	
				1	0	0	0	Center	Initial data
				0	1	1	1	–280	
				0	1	1	0	–560	
				0	1	0	1	–840	
				0	1	0	0	–1120	
				0	0	1	1	–1400	
				0	0	1	0	–1400	
				0	0	0	1	–1400	
				0	0	0	0	–1400	

$(09)_H$ Y Signal Delay Adjustment (read):

Data									
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Delay (ns)**	**Note**
					1	1	1	150	
					1	1	0	100	
					1	0	1	50	
					1	0	0	Center	Initial data
					0	1	1	–50	
					0	1	0	–100	
					0	0	1	–100	
					0	0	0	–100	

$(0A)_H$ Frame Y Level Adjustment:

Data									
D7	D6	D5	D4	D3	D2	D1	D0	Level (IRE)	Note
	1	1	1	1	1	1	1	100	
	1	1	1	1	1	1	0	99.2	
	1	1	1	1	1	0	1	98.4	
	⋮	⋮							
	1	0	0	0	0	0	1	50.8	
	1	0	0	0	0	0	0	50	Initial data
	0	1	1	1	1	1	1	49.2	
	⋮	⋮							
	0	0	0	0	0	1	0	1.6	
	0	0	0	0	0	0	1	0.8	
	0	0	0	0	0	0	0	0	

$(0B)_H$ Gray Background Y Level Adjustment:

Data									
D7	D6	D5	D4	D3	D2	D1	D0	Level (IRE)	Note
	1	1	1	1	1	1	1	100	
	1	1	1	1	1	1	0	99.2	
	1	1	1	1	1	0	1	98.4	
	⋮	⋮							
	1	0	0	0	0	0	1	50.8	
	1	0	0	0	0	0	0	50	Initial data
	0	1	1	1	1	1	1	49.2	
	⋮	⋮							
	0	0	0	0	0	1	0	1.6	
	0	0	0	0	0	0	1	0.8	
	0	0	0	0	0	0	0	0	

$(0C)_H$ Sub-Picture Output Timing:

Data									
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Timing Shift (ns)**	**Note**
				1	1	1	1	Right 186	
				1	1	1	0	Right 186	
				1	1	0	1	Right 186	
				1	1	0	0	Right 186	
				1	0	1	1	Right 186	
				1	0	1	0	Right 124	
				1	0	0	1	Right 62	
				1	0	0	0	Center	Initial data
				0	1	1	1	Left 62	
				0	1	1	0	Left 62	
				0	1	0	1	Left 62	
				0	1	0	0	Left 62	
				0	0	1	1	Left 62	
				0	0	1	0	Left 62	
				0	0	0	1	Left 62	
				0	0	0	0	Left 62	