MC-422000A32
2,097,152 x 32-Bit
Dynamic CMOS RAM Module

Description

The MC-422000A32 is a fast-page dynamic RAM module organized as 2,097,152 words by 32 bits and designed to operate from a single +5-volt power supply. Advanced CMOS circuitry ensures minimum power dissipation and excellent operating margins.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. Data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$. Refreshing is accomplished by $\overline{RAS}$-only refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, hidden refresh cycles, or by the 1024 address combinations of A_0 - A_9 during a 16-ms period.

The MC-422000A36 is packaged in a variety of Single Inline Memory Modules (SIMM™). Each SIMM contains sixteen 1,048,576 x 4-bit μPD424400 DRAMs, and 16 power supply decoupling capacitors for noise reduction. DQ_0 - DQ_{31} are common input/output pins.

Features

- 2,097,152-word by 32-bit organization
- Single +5-volt power supply
- Fast-page cycles
- Low power dissipation
- $\overline{RAS}$-only refresh cycles
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Hidden refresh cycles
- 1024 refresh cycles every 16 ms
- TTL-compatible inputs and outputs
- 72-pin SIMM packaging

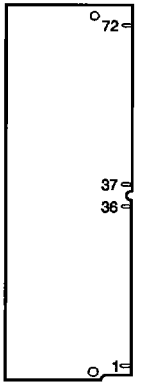
Pin Identification

Name	Function
A_0 - A_9	Address inputs
$\overline{CAS}_0$ - $\overline{CAS}_3$	Column address strobes
DQ_0 - DQ_{31}	Common data inputs/outputs
$\overline{RAS}_0$ - $\overline{RAS}_3$	Row address strobes
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

SIMM is a trademark of Wang Laboratories.

Pin Configuration

72-Pin Socket-Mountable SIMM



Pin	Symbol
1	GND
2	DQ_0
3	DQ_{16}
4	DQ_1
5	DQ_{17}
6	DQ_2
7	DQ_{18}
8	DQ_3
9	DQ_{19}
10	V_{CC}
11	NC
12	A_0
13	A_1
14	A_2
15	A_3
16	A_4
17	A_5
18	A_6
19	NC
20	DQ_4
21	DQ_{20}
22	DQ_5
23	DQ_{21}
24	DQ_6
25	DQ_{22}
26	DQ_7
27	DQ_{23}
28	A_7
29	NC
30	V_{CC}
31	A_8
32	A_9
33	$\overline{RAS}_3$
34	$\overline{RAS}_2$
35	NC
36	NC
37	NC
38	NC
39	GND
40	$\overline{CAS}_0$
41	$\overline{CAS}_2$
42	$\overline{CAS}_3$
43	$\overline{CAS}_1$
44	$\overline{RAS}_0$
45	$\overline{RAS}_1$
46	NC
47	$\overline{WE}$
48	NC
49	DQ_8
50	DQ_{24}
51	DQ_9
52	DQ_{25}
53	DQ_{10}
54	DQ_{26}
55	DQ_{11}
56	DQ_{27}
57	DQ_{12}
58	DQ_{28}
59	V_{CC}
60	DQ_{29}
61	DQ_{13}
62	DQ_{30}
63	DQ_{14}
64	DQ_{31}
65	DQ_{15}
66	NC
67	[Note 1]
68	[Note 1]
69	[Note 1]
70	[Note 1]
71	NC
72	GND

Notes:

[1] Pins 67-70 are defined by access time:

Pin	60 ns	70 ns	80 ns	100 ns
67	NC	NC	NC	NC
68	NC	NC	NC	NC
69	NC	GND	NC	GND
70	NC	NC	GND	GND

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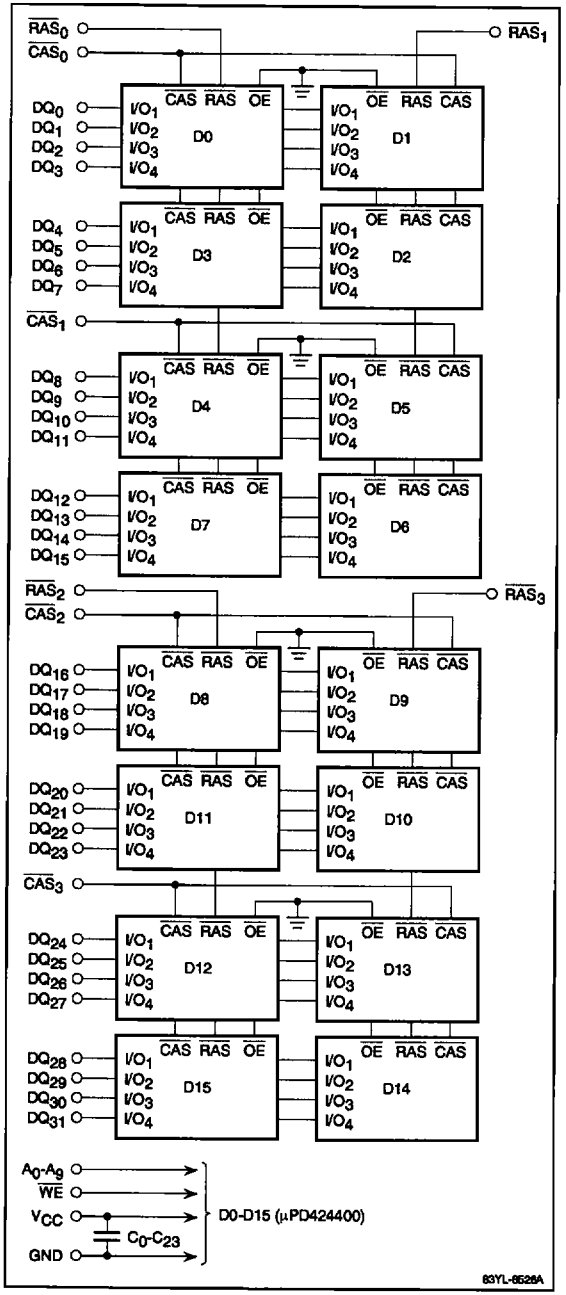
Ordering Information

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-422000A32B-60	60 ns	72-pin socket-mountable SIMM (solder plating)	25.4 mm (1.0 inch)	9.3 mm (0.366 inch)	Sixteen μPD424400LA
B-70	70 ns				
B-80	80 ns				
B-10	100 ns				
MC-422000A32F-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
F-70	70 ns				
F-80	80 ns				
F-10	100 ns				
MC-422000A32BJ-60	60 ns	72-pin socket-mountable SIMM (solder plating)	31.75 mm (1.250 inch)	9.3 mm (0.366 inch)	Sixteen μPD424400LA
BJ-70	70 ns				
BJ-80	80 ns				
BJ-10	100 ns				
MC-422000A32FJ-60	60 ns	72-pin socket-mountable SIMM (gold plating)			
FJ-70	70 ns				
FJ-80	80 ns				
FJ-10	100 ns				

Connection Diagram



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Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	16 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	121	pF	A_0 - A_9
	C_{I2}	137	pF	$\overline{WE}$
	C_{I3}	48	pF	$\overline{RAS}$
	C_{I4}	48	pF	$\overline{CAS}$
Input/output capacitance	C_{I1}/C_{O1}	29	pF	DQ_0 - DQ_{31}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		32	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			16	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current	$I_{I(L)}$	−160	160	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	μA	DQ_0 to DQ_{31} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±5%

		-60		-70		-80		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating current, average	I_{CC1}		1020		860		780		700	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		1020		860		780		700	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		780		700		620		540	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		1020		860		780		700	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		30		35		40		50	ns	(Notes 7, 9)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45		55	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0	20	0	20	0	20	0	25	ns	
Row address setup time	t_{ASR}	0		0		0		0		ns	
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		15		20		20		25	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	17		17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
Data setup time	t_{CLZ}	0		0		0		0		ns	
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		10		10		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
Data-in hold time	t_{DH}	15		15		15		20		ns	(Note 15)
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 10)

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AC Characteristics (cont)

		-60		-70		-80		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Fast-page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	50	ns	(Note 9)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	60	100,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		140		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 13)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		16		16		16		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		15		15		20		ns	
$\overline{WE}$ setup time	t_{WSR}	10		10		10		10		ns	
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 14)

AC Characteristics (cont)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

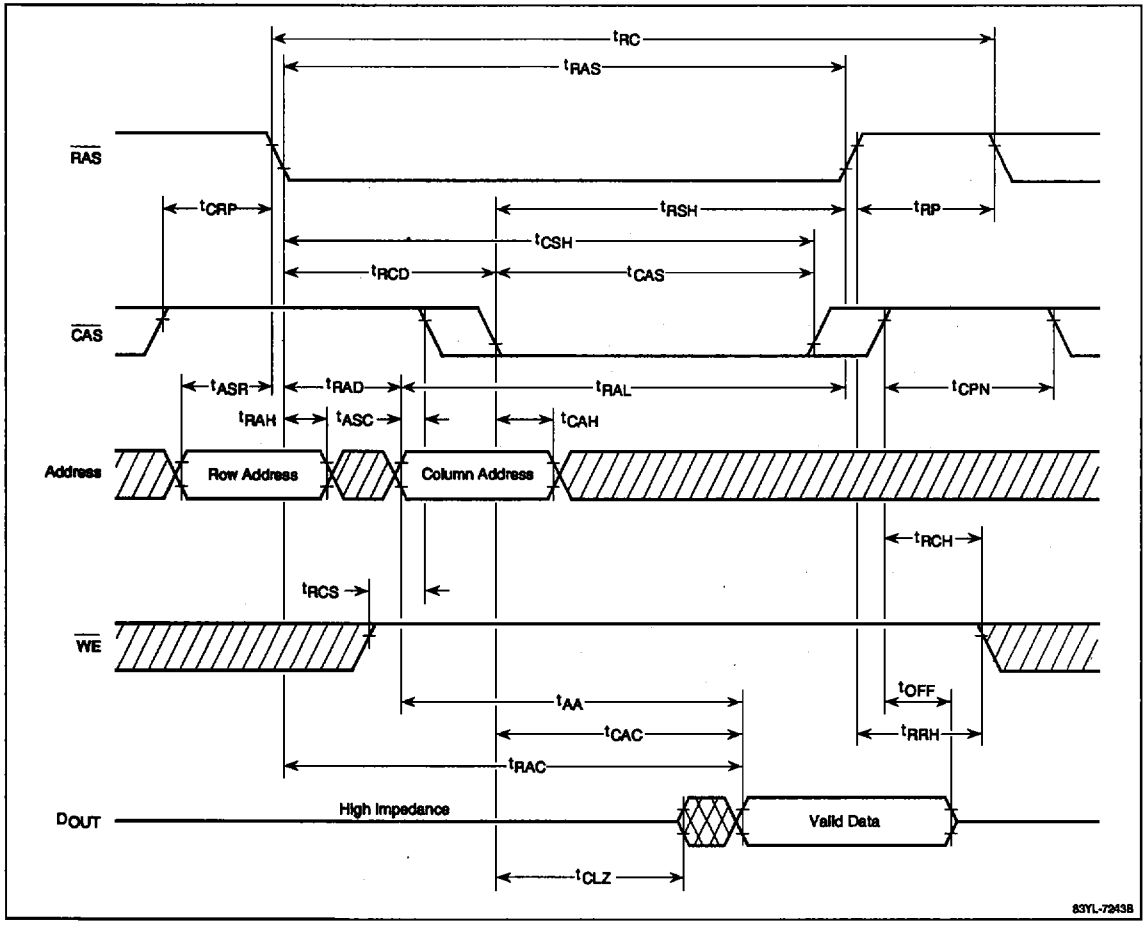
(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

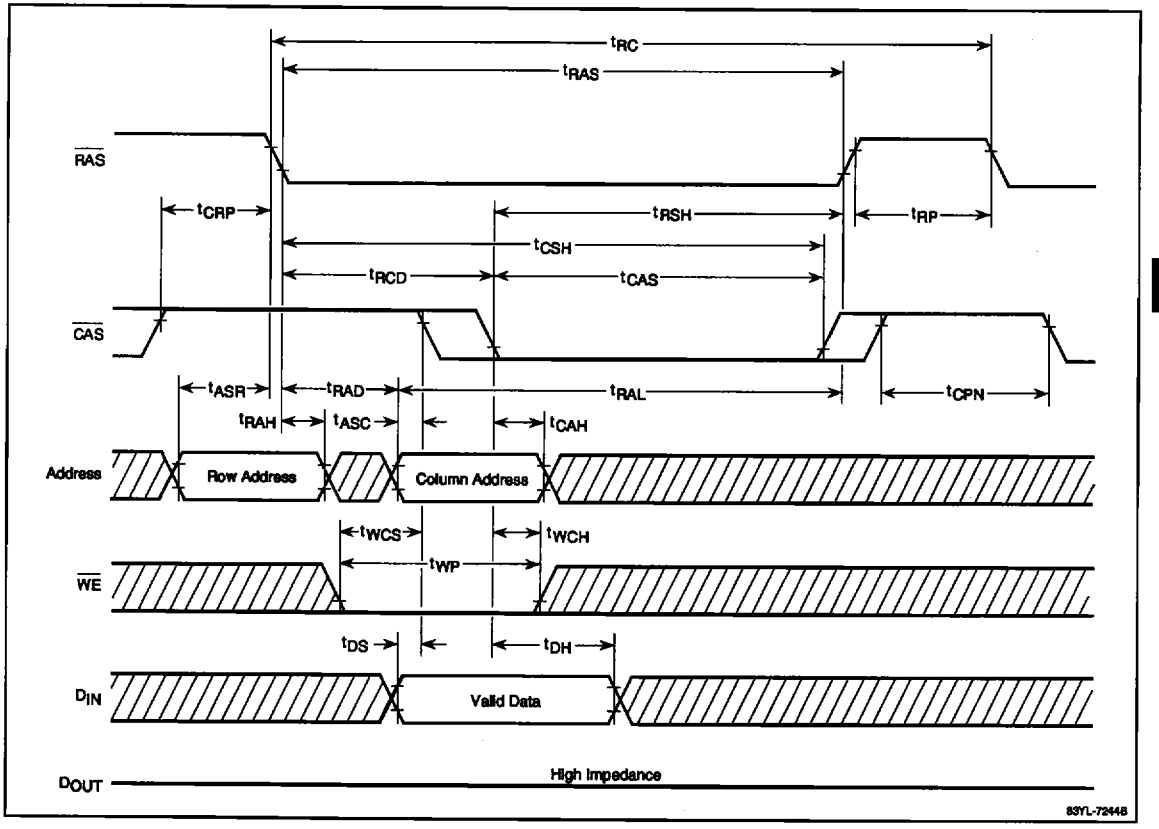
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle



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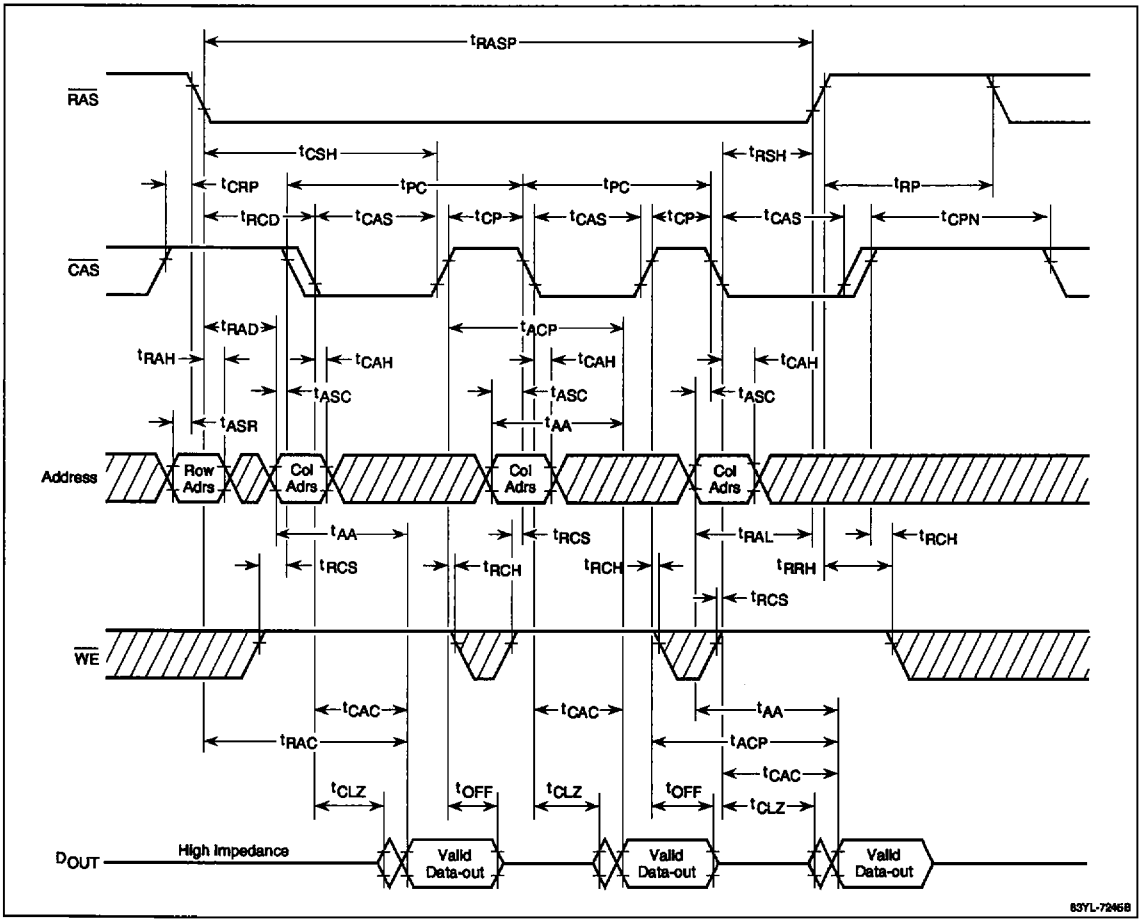
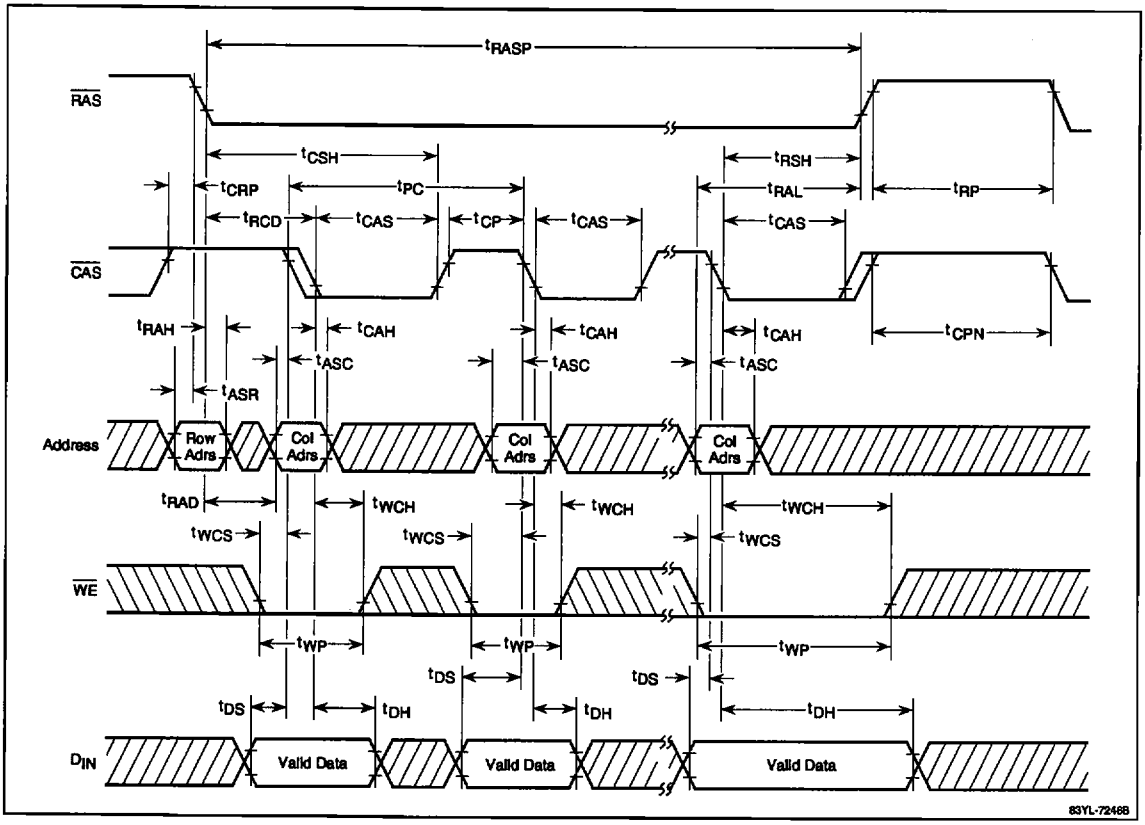
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Early Write Cycle



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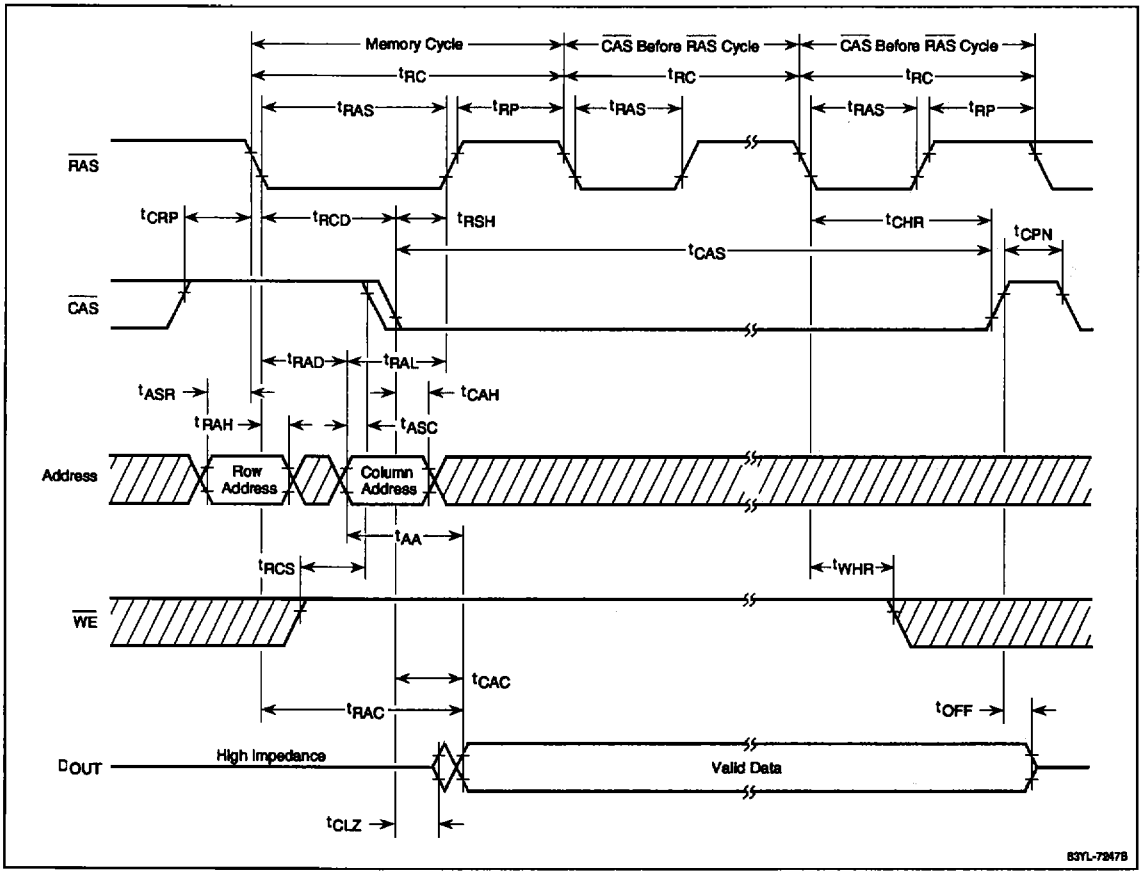
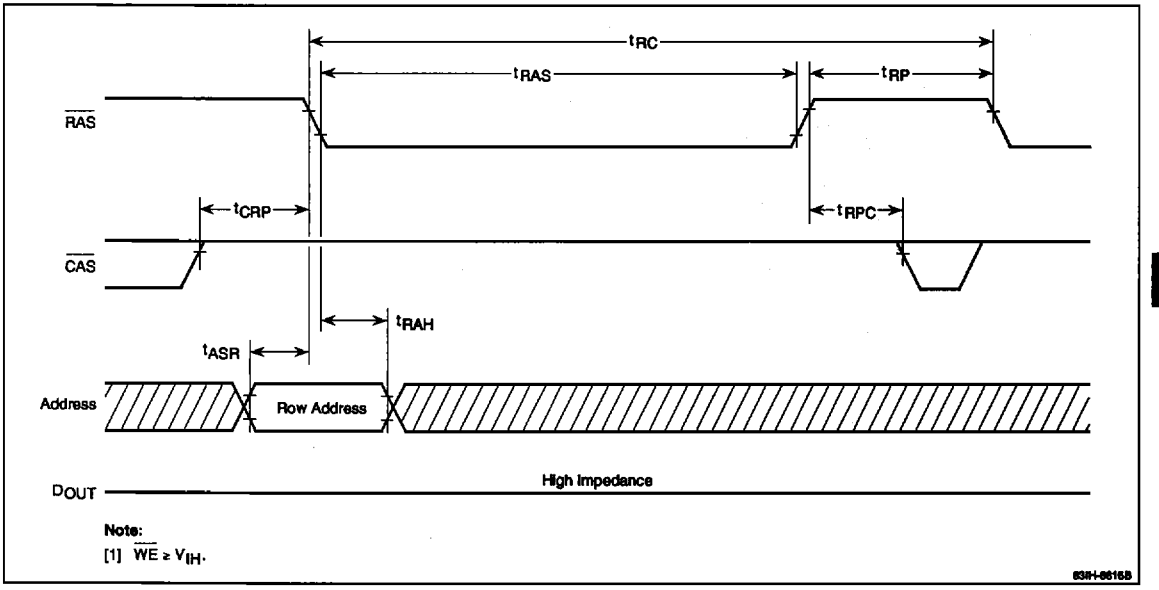
Timing Waveforms (cont)

Hidden Refresh Cycle



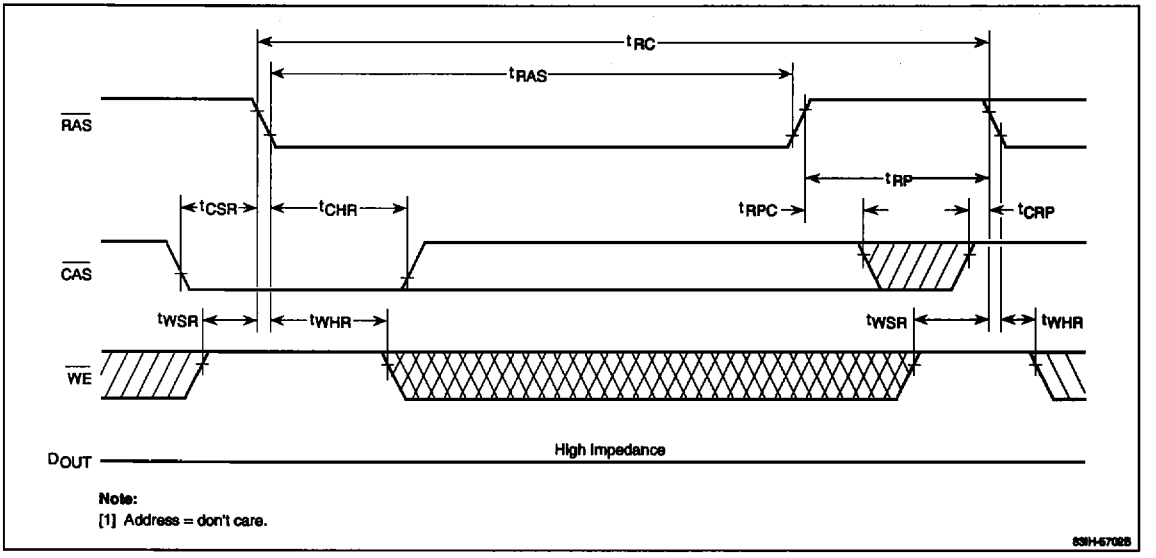
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] Address = don't care.

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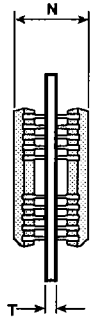
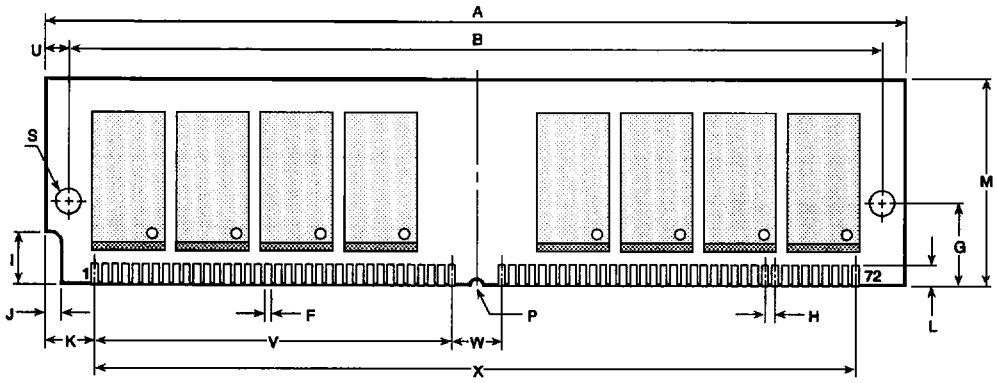
Package Drawings

72-Pin Socket Mountable SIMM (MC-422000A32B/F)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	1.04	.041
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.54 min	.100 min

Item	Millimeters	Inches
M	25.4	1.000
N	9.3	.366
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004





MC-422000A32B/F

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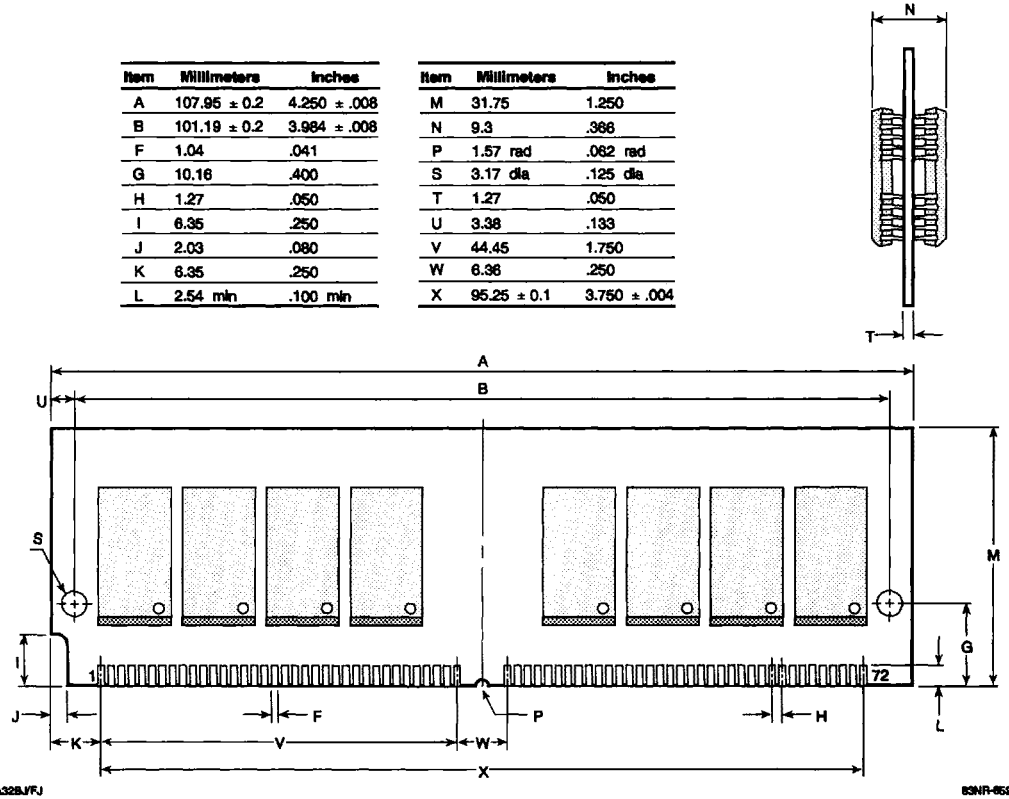
Package Drawings (cont)

72-Pin Socket Mountable SIMM (MC-422000A32/BJ/FJ)

Item	Millimeters	Inches
A	107.95 ± 0.2	4.250 ± .008
B	101.19 ± 0.2	3.984 ± .008
F	1.04	.041
G	10.16	.400
H	1.27	.050
I	6.35	.250
J	2.03	.080
K	6.35	.250
L	2.54 min	.100 min

Item	Millimeters	Inches
M	31.75	1.250
N	9.3	.366
P	1.57 rad	.062 rad
S	3.17 dia	.125 dia
T	1.27	.050
U	3.38	.133
V	44.45	1.750
W	6.36	.250
X	95.25 ± 0.1	3.750 ± .004



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