

Features

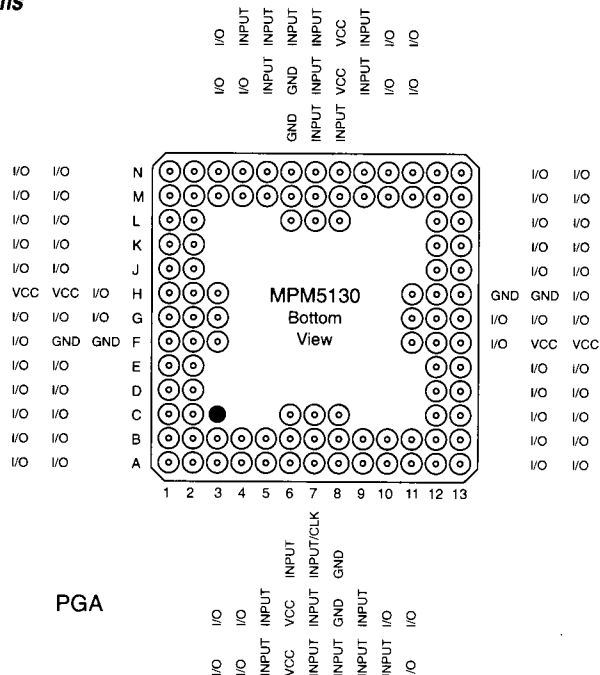
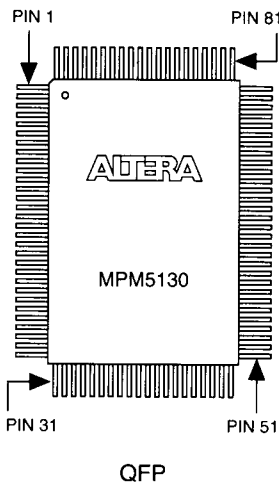
- ❑ CMOS, Mask-Programmed Logic Device (MPLD) capable of implementing high-density custom logic functions
- ❑ High-volume replacement for EPM5130 EPLD designs
- ❑ Zero-power operation (typically 25 μ A standby)
- ❑ Active power of 30 mA at 20 MHz
- ❑ High speed ($t_{PD} = 25$ ns) with 62.5-MHz clock rates
- ❑ TTL I/O compatibility
- ❑ MAX+PLUS and MAX+PLUS II development system support, featuring schematic capture, Altera Hardware Description Language (AHDL), and waveform design entry; logic minimization and synthesis; and full timing simulation
- ❑ Available in 100-pin plastic quad flat pack (QFP) and pin-grid array (PGA) packages

General Description

Altera's MPM5130 MPLD provides a high-volume replacement for EPM5130 designs. It is pin-, function-, and timing-compatible with existing EPM5130 designs. MPM5130 designs are created with Altera's MAX+PLUS or MAX+PLUS II development system and prototyped with EPM5130 EPLDs. The source files are then converted to produce the MPLD. The MPM5130 MPLD is available in 100-pin QFP and PGA packages. See Figure 11.

Figure 11. MPM5130 Package Pin-Out Diagrams

See Table 1 in this data sheet for QFP pin-outs.
Package outlines not drawn to scale.



This data sheet provides minimum and maximum AC and DC parametric values for the MPM5130 MPLD. For additional information, refer to the *EPM5016 to EPM5192 EPLDs: High-Speed, High-Density MAX 5000 Devices Data Sheet* in this data book.

Absolute Maximum Ratings Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	-2.0	7.0	V
V_I	DC input voltage	See Note (1)	-2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	mA
I_{OUT}	DC output current, per pin		-25	25	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	-65	150	°C
T_{AMB}	Ambient temperature	Under bias	-65	135	°C
T_J	Junction temperature	Under bias		150	°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	°C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions See Notes (2), (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		$V_{CC} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3		0.8	V
V_{OH}	High-level TTL output voltage	$I_{OH} = -4$ mA DC	2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	-10		10	μA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	-40		40	μA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, No load		25		μA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, $f = 1.0$ MHz, See Note (4)		1.5		mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	$V_{IN} = 0\text{ V}, f = 1.0\text{ MHz}$		10	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0\text{ V}, f = 1.0\text{ MHz}$		20	pF

AC Operating Conditions See Note (3)

External Timing Parameters			MPM5130-1 Note (5)		MPM5130-2		MPM5130		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
t_{PD1}	Input to non-registered output	$C1 = 35\text{ pF}$		25		30		35	ns
t_{PD2}	I/O input to non-registered output			40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_H	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	$C1 = 35\text{ pF}$		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		8		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	$C1 = 35\text{ pF}$		25		30		35	ns
t_{ACH}	Array clock high time	See Note (6)	11		14		16		ns
t_{ACL}	Array clock low time		9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	See Note (4)	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	See Note (4)	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	See Note (7)	62.5		50		40		MHz

Notes to tables:

- Minimum DC input is -0.3 V . During transitions, the inputs may undershoot to -2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
- Typical values are for $T_A = 25^\circ\text{ C}$ and $V_{CC} = 5\text{ V}$.
- Operating conditions: $V_{CC} = 5\text{ V} \pm 5\%$, $T_A = 0^\circ\text{ C}$ to 70° C for commercial use.
- Measured with a device programmed as eight 16-bit counters.
- This version is under development. Contact Altera Marketing at (408) 984-2800 for information on availability.
- This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
- The f_{MAX} values represent the highest frequency for pipelined data.

Figure 12 shows typical supply current versus frequency for MPM5130 MPLDs. Table 1 shows the pin-outs for the MPM5130 QFP package.

Figure 12. MPM5130 I_{CC} vs. Frequency

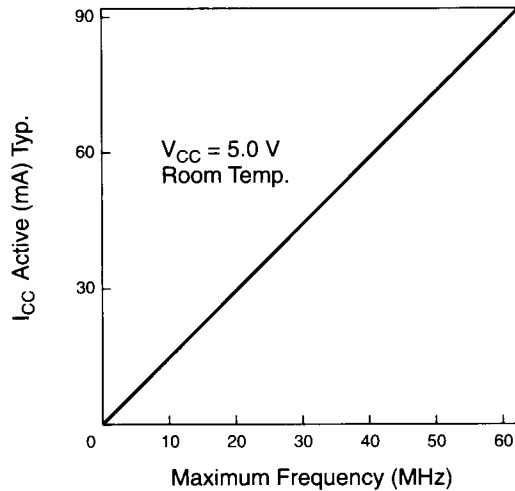


Table 1. MPM5130 QFP Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	I/O	21	INPUT	41	I/O	61	INPUT	81	I/O
2	I/O	22	INPUT	42	I/O	62	GND	82	I/O
3	I/O	23	I/O	43	VCC	63	GND	83	I/O
4	I/O	24	I/O	44	VCC	64	INPUT	84	I/O
5	I/O	25	I/O	45	I/O	65	INPUT	85	I/O
6	I/O	26	I/O	46	I/O	66	INPUT	86	I/O
7	I/O	27	I/O	47	I/O	67	INPUT	87	GND
8	I/O	28	I/O	48	I/O	68	VCC	88	GND
9	INPUT	29	I/O	49	I/O	69	VCC	89	I/O
10	INPUT	30	I/O	50	I/O	70	INPUT	90	I/O
11	INPUT	31	I/O	51	I/O	71	INPUT	91	I/O
12	GND	32	I/O	52	I/O	72	INPUT	92	I/O
13	GND	33	I/O	53	I/O	73	I/O	93	VCC
14	INPUT	34	I/O	54	I/O	74	I/O	94	VCC
15	INPUT	35	I/O	55	I/O	75	I/O	95	I/O
16	INPUT/CLK	36	I/O	56	I/O	76	I/O	96	I/O
17	INPUT	37	GND	57	I/O	77	I/O	97	I/O
18	VCC	38	GND	58	I/O	78	I/O	98	I/O
19	VCC	39	I/O	59	INPUT	79	I/O	99	I/O
20	INPUT	40	I/O	60	INPUT	80	I/O	100	I/O