Signetics

FAST 74F384
Multiplier

8-Bit Serial/Parallel Two's Complement Multiplier
Preliminary Specification

FAST Products

FEATURES

- **8-bit by 1-bit sequential logic element**
- **Multiplies two numbers represented in Two's Complement**
- **Parallel inputs accept and store an 8-bit multiplicand ($X_0 - X_7$)**
- **K input is used for expansion to longer words**
- **Mode Control (M) is used to establish the most significant device**
- **Asynchronous Parallel Load (PL) input clears the internal flip-flop to the start condition and enables the X latches to accept new multiplicand data**

DESCRIPTION

The 'F384 is an 8-bit sequential logic element that multiplies two numbers represented in Two's Complement notation. The device implements Booth's algorithm internally to produce a Two's Complement product that needs no subsequent correction. Parallel inputs accept and store an 8-bit multiplicand ($X_0 - X_7$). The multiplier word is applied to the Y input in a serial bit stream, least significant bit first. The product is clocked out at the SP output, least significant bit first.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F384	100MHz	60mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F384N
16-Pin Plastic SOL	N74F384D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$X_0 - X_7$	Multiplicand data inputs	1.0/1.0	20μA/0.6mA
CP	Clock input (active rising edge)	1.0/1.0	20μA/0.6mA
K	Serial expansion input	1.0/1.0	20μA/0.6mA
M	Mode control input	1.0/1.0	20μA/0.6mA
$\overline{PL}$	Asynchronous Parallel Load input	1.0/1.0	20μA/0.6mA
Y	Serial multiplier inputs	1.0/1.0	20μA/0.6mA
SP	Serial X,Y product output	50/33.3	1mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

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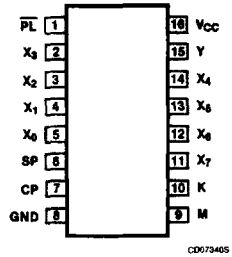
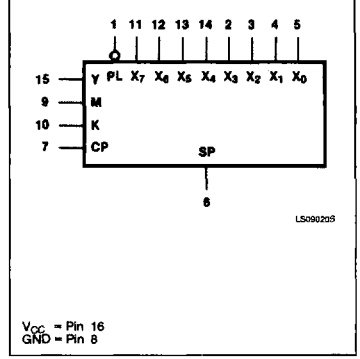
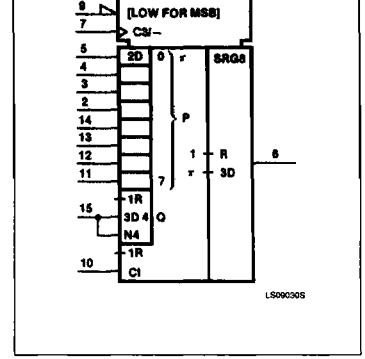
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



The K input is used for expansion to longer X words, using two or more 'F384 devices. The Mode Control (M) input is used to establish the most significant device. An asynchronous Parallel Load (PL) input clears the internal flip-flops to the start condition and enables the X latches to accept new multiplicand data.

Referring to the Logic Diagram, the multiplicand ($X_0 - X_7$) latches are enabled to receive new data when $\overline{PL}$ is Low. Data that meets the setup time requirements is latched and stored when $\overline{PL}$ goes High. The Low signal on $\overline{PL}$ also clears the Y_{a-1} flip-flop as well as the Carry-save flip-flops and the partial product register in the arithmetic section. Figure 1 is a conceptual logic diagram of a typical cell in the arithmetic section, except for the first (X_7) cell, in which K is the B_i input and M is incorporated into the Carry logic. The cells use the Carry-save technique to avoid the complexity and delays inherent in look-ahead Carry schemes for longer words.

Figure 2 is a timing diagram for an 8 × 8 multiplication process. New multiplicand data enters the X latches during bit time T_0. It is assumed that $\overline{PL}$ goes Low shortly after the CP rising edge that marks the beginning of T_0 and goes High again shortly after the beginning of T_1. The LSB (Y_0) of the multiplier is applied to the Y input during T_1 and combines with X_0 in the least significant cell to form the appropriate D input (X_0Y_0) to the sum flip-flop. This is clocked into the sum flip-flop by the CP rising edge at the beginning of T_2 and this LSB (S_0) of the product is available shortly thereafter at the SP output of the package.

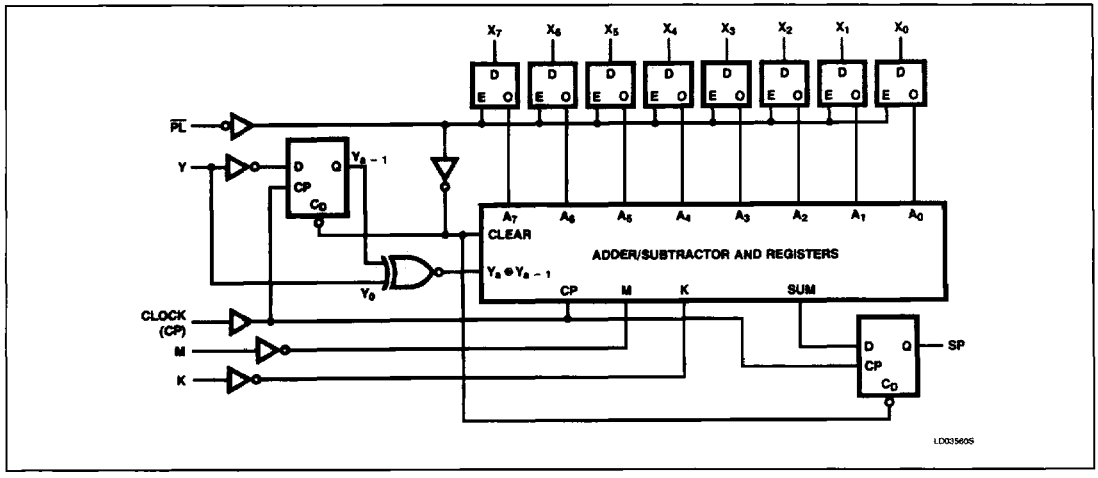
FUNCTION TABLE

INPUTS						INTERNAL	OUTPUT	FUNCTION
$\overline{PL}$	CP	K	M	X_1	Y	Y_{a-1}	SP	
X	X	L	L	X	X	X	X	Most significant multiplier device
X	X	CS	H	X	X	X	X	Device cascaded in multiplier string
L	X	X	X	OP	X	L	L	Load new multiplicand and clear internal sum and carry registers
H	X	X	X	X	X	X	X	Device enabled
H	↑	X	X	X	L	L	AR	Shift sum register
H	↑	X	X	X	L	H	AR	Add multiplicand to sum register and shift
H	↑	X	X	X	H	L	AR	Subtract multiplicand from sum register and shift
H	↑	X	X	X	H	H	AR	Shift sum register

H = High voltage level
L = Low voltage level
↑ = Low-to-High Transition
CS = Connected to SP output of high-order device
OP = X_1 latches open for new data (I = 0 – 7)
AR = Output as required per Booth's algorithm
X = Don't care

The next-least bit (Y_1) of the multiplier is also applied during T_2. The detailed logic design of the cell is such that during T_2 the D input to the sum flip-flop of the least significant cell contains not only X_0Y_1 but also, the X_1Y_0 product. Thus the term ($X_1Y_0 + X_0Y_1$) is formed at the D input of the least significant sum flip-flop during T_2 and this next-least term S_1 of the product is available at the SP output shortly after the CP rising edge at the beginning of T_3. Due to storage in the two preceding cells and in its own Carry flip-flop, the D input to the least significant sum flip-flop during T_3 will contain the products X_2Y_0 and X_1Y_1 as well as X_0Y_2. During each succeeding bit time the SP output contains information formed one stage further upstream. For example, the SP output during T_9 contains X_7Y_0, which was actually formed during T_1.

LOGIC DIAGRAM



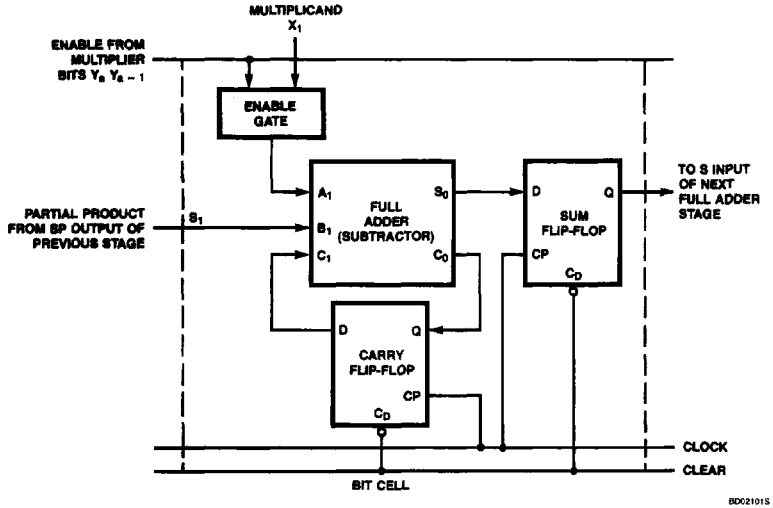


Figure 1. Conceptual Carry Save Adder Cell

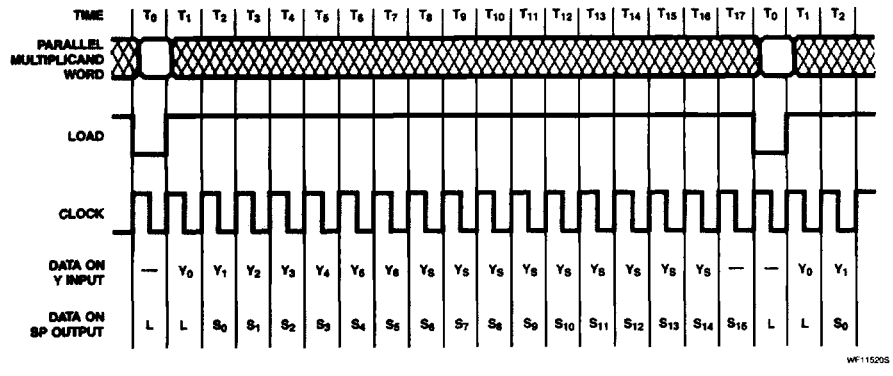


Figure 2. Timing Diagram Showing 18 Clock Cycle Operation of 8 × 8 Multiplication

The MSB Y_7 (the sign bit Y_S) of the multiplier is first applied to the Y input during T_8 and must also be applied during bit times T_9 through T_{16}. This extension of the sign bit is a necessary adjunct to the implementation of Booth's algorithm and is a built-in feature of the 'F322 Shift Register. Figure 3 shows the method of using two 'F384s to perform a 12 × n bit multiplication. Notice that the sign of X is effectively extended by connecting X_{11} to $X_4 - X_7$ of the most significant package. Whereas the 8 × 8 multiplication required 18 clock periods (m + n to form the product terms plus T_0 to clear the multiplier plus T_{17} to recognize and store S_{15}), the arrangement of Figure 3 requires 12 + n bits to form the product terms plus the bit times to clear the multiplier and to recognize and store SP_{n+11}.

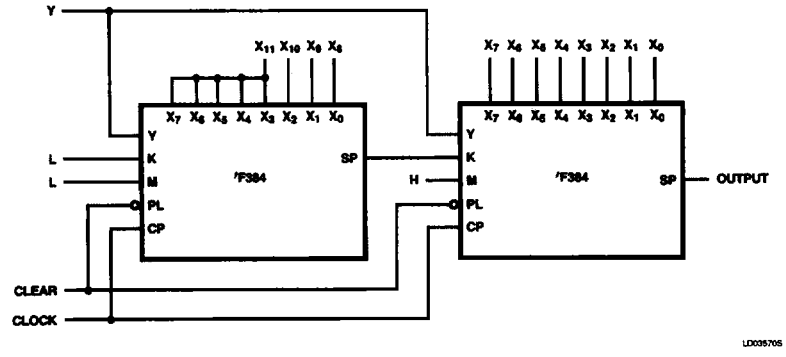


Figure 3. 12-Bit by n-Bit Two's Complement Multiplier

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		74F384			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V			−0.4	−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−75		−250	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			60	90	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F384					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	100		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to SP	Waveform 1	3.5 3.5	4.5 4.5	5.5 5.5	3.5 3.5	10.0 10.0	ns
t_{PHL}	Propagation delay $\overline{PL}$ to SP	Waveform 2	6.0	10.0	13.0	6.0	14.0	ns

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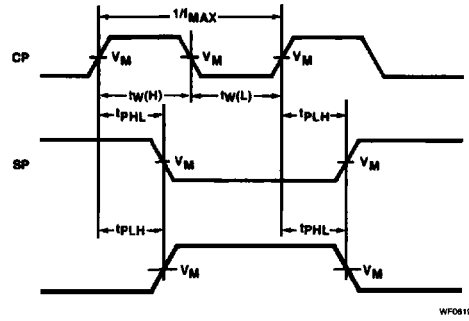
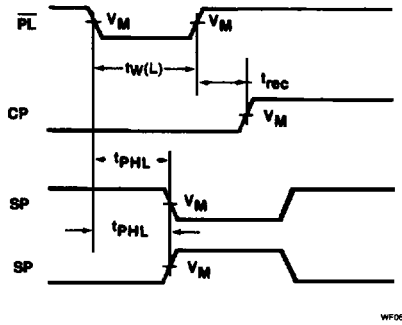
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	74F384					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low K to CP	Waveform 3	13.5 13.5			15.0 15.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low K to CP	Waveform 3	2.0 2.0			2.0 2.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low Y to CP	Waveform 3	15.0 15.0			15.0 15.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Y to CP	Waveform 3	2.0 2.0			2.0 2.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low X_n to $\overline{PL}$	Waveform 3	5.5 5.5			6.5 6.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low X_n to $\overline{PL}$	Waveform 3	2.0 2.0			2.0 2.0		ns
$t_w(H)$ $t_w(L)$	CP pulse width High or Low	Waveform 1	7.0 5.5			7.5 6.0		ns
$t_w(L)$	$\overline{PL}$ pulse width Low	Waveform 2	6.5			7.0		ns
t_{rec}	Recovery time $\overline{PL}$ to CP	Waveform 2	5.5			6.0		ns

AC WAVEFORMS



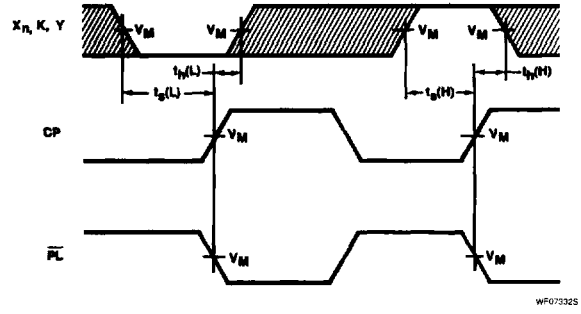
Waveform 1. Clock to Output Delays, Clock Pulse Width and Maximum Clock Frequency



Waveform 2. Master Reset Pulse Width, Master to Output Delay and Master Reset to Clock Recovery Time

NOTE: For all waveforms, $V_M = 1.5V$.

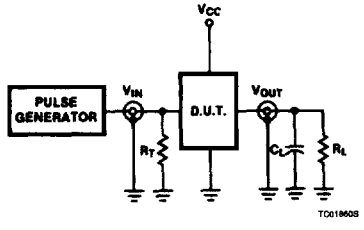
AC WAVEFORMS (Continued)



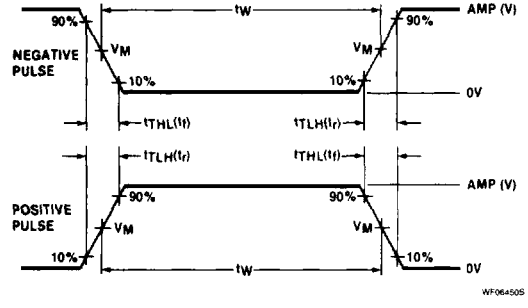
Waveform 3. Data and Select Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS
R_L = Load resistor to GND; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

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